THE DATASHEET OF

LM34919CQTL/NOPB

LM34919C-Q1 Ultra Small 50V, 600 mA Constant On-Time Buck Switching Regulator

Check for Samples: LM34919C-Q1

FEATURES

- **AEC-Q100 qualified (T_j = -40°C to 125°C)**
- **Maximum Switching Frequency: 2.6 MHz**
- **Input Voltage Range: 4.5 V to 50 V**
- **Integrated N-Channel buck switch**
- **Integrated Start-Up Regulator**
- **No Loop Compensation Required**
- **Ultra-Fast Transient Response**
- **Operating Frequency Remains Constant with Load Current and Input Voltage**
- **Adjustable Output Voltage**
- **Power Good Output**
- **Enable Input**
- **Valley Current Limit at 0.64 A Typical**
- **Precision Internal Voltage Reference**
- **Low I_Q Shutdown (<10 µA)**
- **Highly Efficient Operation**
- **Thermal Shutdown**
- **12-Bump 2 mm x 2 mm DSBGA and 12-pin 4 mm x 4 mm WSON Packages**

APPLICATIONS

- **Automotive Safety and Infotainment**
- **High Efficiency Point-of-Load (POL) Regulator**
- **Telecommunication Buck Regulator**
- **Secondary Side Post Regulator**

DESCRIPTION

The LM34919C Step Down Switching Regulator features all of the functions needed to implement a low-cost, efficient, buck bias regulator capable of supplying 0.6 A to the load. This buck regulator contains an N-Channel Buck Switch and is available in DSBGA and WSON packages. The constant on-time feedback regulation scheme requires no loop compensation, results in fast load transient response, and simplifies circuit implementation. The operating frequency remains constant with line and load variations due to the inverse relationship between the input voltage and the on-time. The valley current limit results in a smooth transition from constant voltage to constant current mode when current limit is detected, reducing the frequency and output voltage, without the use of foldback. Additional features include: Power Good, enable, VCC undervoltage lockout, thermal shutdown, gate drive undervoltage lockout, and maximum duty cycle limiter.

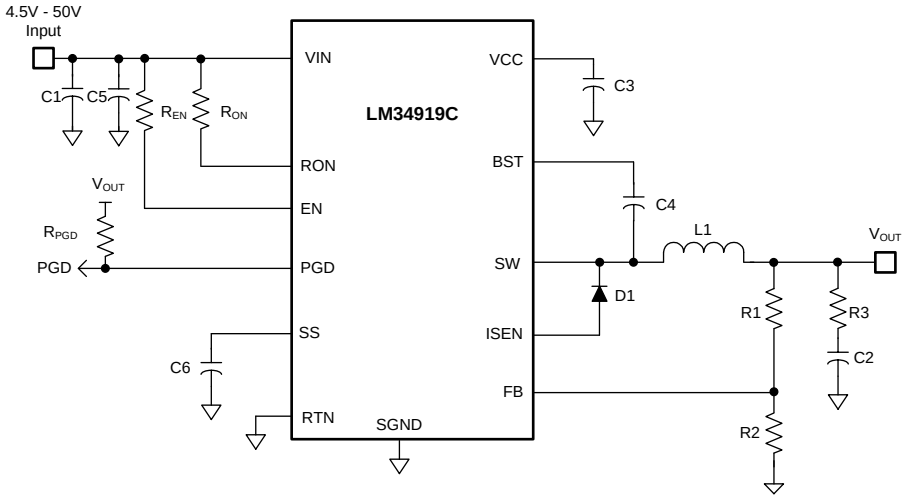


Figure 1. Basic Step Down Regulator

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)

	VALUE	UNIT
V_{IN}, EN , RON to RTN	65	V
BST to RTN	79	V
SW to RTN (Steady State)	–1.5 to 65	V
SW to V_{IN}	+0.3	V
BST to VCC	65	V
BST to SW	14	V
VCC to RTN	14	V
PGD	14	V
SGND to RTN	–0.3 to 0.3	V
SS to RTN	–0.3 to 4	V
FB to RTN	–0.3 to 7	V
Storage Temperature Range	–65 to 150	ºC
ESD Rating HBM	2	kV
Junction Temperature	150	ºC

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the devices at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Recommended Operating Conditions (1)

	VALUE	UNIT
V_{IN}	4.5 to 50	V
Junction Temperature	−40 to 125	°C

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which the device is intended to be fully functional. For verified specifications and test conditions, see Electrical Characteristics.

Electrical Characteristics

Unless otherwise specified, these specifications apply for –40°C ≤ T_J ≤ +125°C, V_{IN} = 12 V, R_{ON} = 100 kΩ. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
EN Power Up Feature (EN Pin)						
EN	EN Threshold	EN rising		2.1	3.0	V
	EN Disable Threshold	EN falling	0.5	1.3		V
	EN Input Current	EN = V_{IN} = 12 V		10	50	µA
I_{SD}	VIN Shutdown Current	EN = 0 V		1	8	µA
Start-Up Regulator, VCC						
V_{CC}Reg	V_{CC} Regulated Output	V_{IN} = 12 V	6.1	7	7.6	V
		V_{IN} =4.5 V, I_{CC} = 3 mA		4.43		V
	V_{IN} – V_{CC} Dropout Voltage	I_{CC} = 0 mA, Non-Switching V_{CC} = $UVLO_{VCC}$ + 250 mV		20		mV
	V_{CC} Output Impedance	0 mA ≤ I_{CC} ≤ 5 mA, V_{IN} = 4.5 V		16		Ω
		0 mA ≤ I_{CC} ≤ 5 mA, V_{IN} = 8 V		8		
	V_{CC} Current Limit	V_{CC} = 0 V		27		mA
$UVLO_{VCC}$	V_{CC} Under-Voltage Lockout Threshold Measured at V_{CC}	V_{CC} Increasing	3.4	3.75	4.1	V
		V_{CC} Decreasing	3.25	3.6	3.95	
	$UVLO_{VCC}$ Hysteresis, at VCC			150		mV
	V_{CC} Under-Voltage Lock-Out Threshold Measured at V_{IN}	V_{IN} Increasing, I_{CC} = 3 mA		3.90	4.50	V
	V_{CC} Under-Voltage Lock-Out Threshold Measured at V_{IN}	V_{IN} Decreasing, I_{CC} = 3 mA		3.80	4.25	
	$UVLO_{VCC}$ Filter Delay	100 mV Overdrive		3		µs
I_Q	I_{IN} Operating Current	Non-Switching, FB = 3 V, SW = Open		2.2	3.8	mA
Switch Characteristics						
$R_{ds(on)}$	Buck Switch Rds(on) (DSBGA)	I_{TEST} = 200 mA		0.35	0.9	Ω
	Buck Switch Rds(on) (WSON-12)	I_{TEST} = 200 mA		0.45	1	
$UVLO_{GD}$	Gate Drive UVLO	V_{BST} - V_{SW} Increasing	2.40	2.95	3.60	V
		V_{BST} - V_{SW} Decreasing		2.82		
	UVLOGD Hysteresis			130		mV
Soft-start Pin						
V_{SS}	Pull-Up Voltage			2.52		V
	Internal Current Source	V_{SS} = 1V		10.5		µA
Current Limit						
I_{LIM}	Threshold	Current out of I_{SEN}	0.52	0.64	0.76	A
	Resistance from ISEN to SGND			190		mΩ
	Response Time			50		ns
On Timer						
$t_{ON - 1}$	On-Time	V_{IN} = 12 V, R_{ON} = 100 kΩ		300		ns
$t_{ON - 2}$	On-Time	V_{IN} = 24 V, R_{ON} = 100 kΩ		175		
$t_{ON - 3}$	On-Time	V_{IN} = 4.5 V, R_{ON} = 100 kΩ		760		
Off Timer						
t_{OFF}	Minimum Off-time		100	120	150	ns

Electrical Characteristics (continued)

Unless otherwise specified, these specifications apply for –40°C ≤ T_J ≤ +125°C, V_{IN} = 12 V, R_{ON} = 100 kΩ. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Regulation and Over-Voltage Comparators (FB Pin)						
V_{REF}	FB Regulation Threshold	SS pin = Steady State	2.47	2.52	2.57	V
	FB Over-Voltage Threshold			3.0		
	FB Bias Current	FB = 3 V		1		nA
Power Good Feature (PGD Pin)						
PGD_{UV}	PGD UV Threshold Rising, With Respect to V_{REF}	FB Increasing	87	92	97	%
	PGD UV Threshold Falling	FB Decreasing		90		
PGD_{OV}	PGD OV Threshold Rising	FB Increasing		120		
	PGD OV Threshold Falling	FB Decreasing		110		
$T_{d,\ PGD}$	PGD Delay	Falling Edge		10		us
I_{PGD}	PGD Pulldown	Vin = 4.5 V, FB = 3 V, Vpg = 0.1 V	1			mA
Thermal Shutdown						
T_{SD}	Thermal Shutdown Temperature			175		°C
	Thermal Shutdown Hysteresis			20		
Thermal Resistance						
θ_{JA}	Junction to Ambient 0 LFPM Air Flow (DSBGA Packages)			61		°C/W
	For WSON Package (Exposed Pad)			50		

PIN DESCRIPTIONS

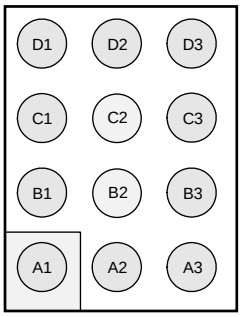


Figure 2. DSBGA Package Bump View

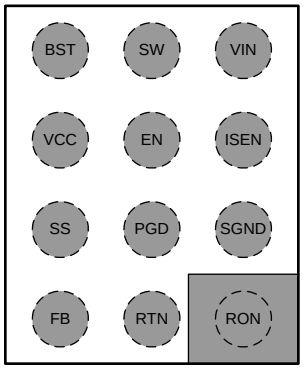


Figure 3. DSBGA Package Top View

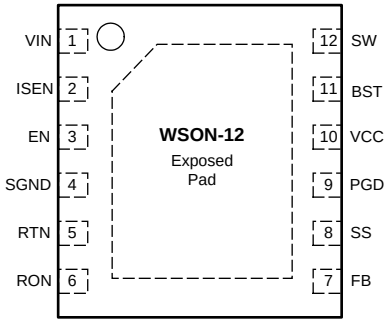


Figure 4. WSON Top View

Pin Descriptions

PIN NUMBER	PIN NUMBER (WSON-12)	NAME	DESCRIPTION	APPLICATION INFORMATION
A1	6	RON	On-time control and shutdown	An external resistor from VIN to this pin sets the buck switch on-time.
A2	5	RTN	Circuit Ground	Ground for all internal circuitry other than the current limit detection.
A3	7	FB	Feedback input from the regulated output	Internally connected to the regulation and overvoltage comparators. The regulation level is 2.52 V (typ.).
B1	4	SGND	Sense Ground	Re-circulating current flows into this pin to the current sense resistor.

Pin Descriptions (continued)

PIN NUMBER	PIN NUMBER (WSON-12)	NAME	DESCRIPTION	APPLICATION INFORMATION
B2	9	PGD	Power Good	Open drain. Logic output indicates when the voltage at the FB pin has increased above 92% of the internal reference. The falling threshold for PGD is 90% of the internal reference. An external pull-up resistor connecting PGD pin to a voltage less than 14 V is required.
B3	8	SS	Soft-start	An internal current source charges an external capacitor to 2.52 V, providing the soft-start function.
C1	2	ISEN	Current sense	The re-circulating current flows through the internal sense resistor and out of this pin to the free-wheeling diode. Valley current limit is nominally set at 0.64 A.
C2	3	EN	Enable Pin	Pull low to disable the part for low shutdown current. Shutdown threshold is 1.3 V (typ).
C3	10	VCC	Output from the startup regulator	Nominally regulated at 7.0 V. An external voltage (7 V - 14 V) can be applied to this pin to reduce internal dissipation. An internal diode connects V_{CC} to VIN.
D1	1	VIN	Input supply voltage	Nominal input range is 4.5 V to 50 V.
D2	12	SW	Switching Node	Internally connected to the buck switch source. Connects to the inductor, free-wheeling diode, and bootstrap capacitor.
D3	11	BST	Boost pin for bootstrap capacitor	Connect a 0.022 µF capacitor from SW to this pin. The capacitor is charged from V_{CC} via an internal diode during each off-time.
	EP (WSON Only)			Exposed pad should be connected to RTN pin and system ground for proper cooling.

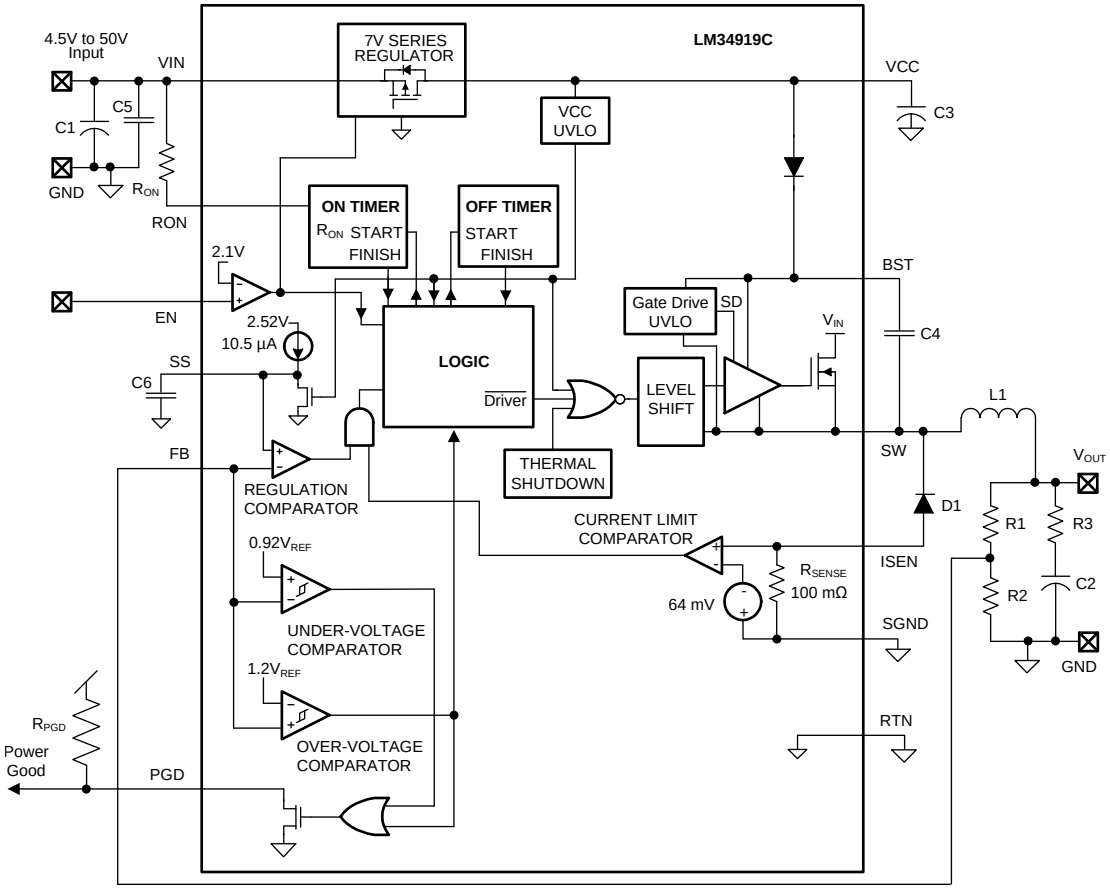
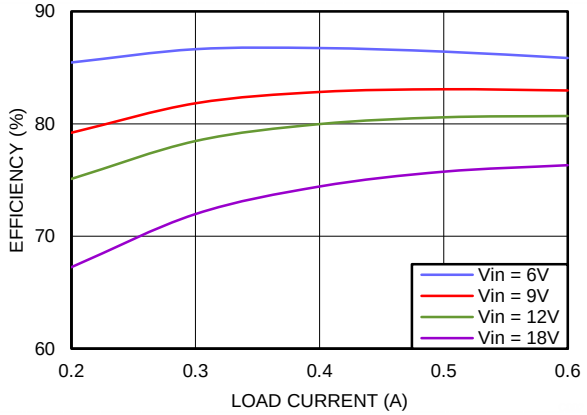


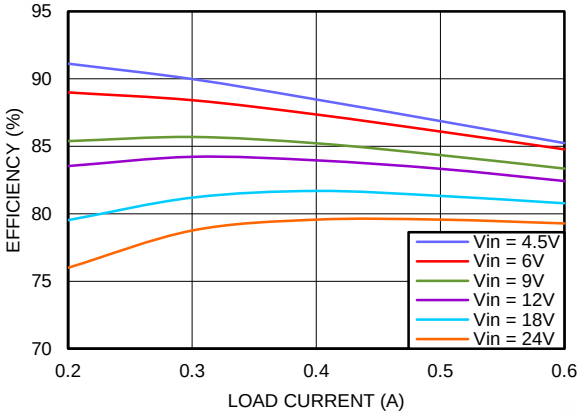
Figure 5. Functional Block Diagram

Typical Performance Characteristics

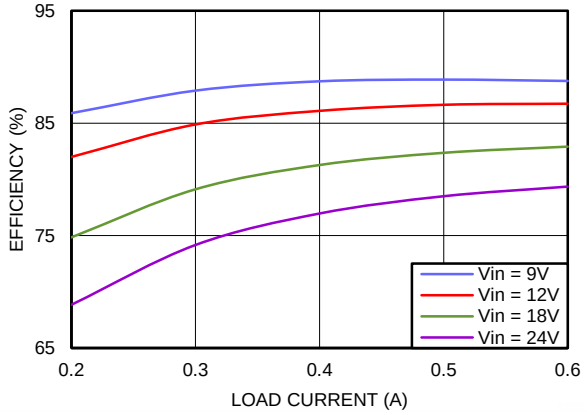
Efficiency at 2.1 MHz, V_{OUT} = 3.3 V



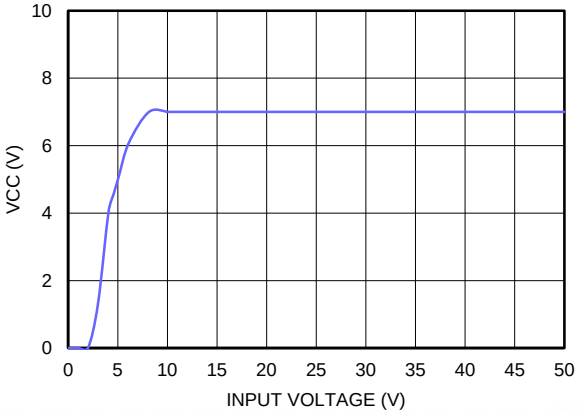
Efficiency at 250 kHz, V_{OUT} = 3.3 V



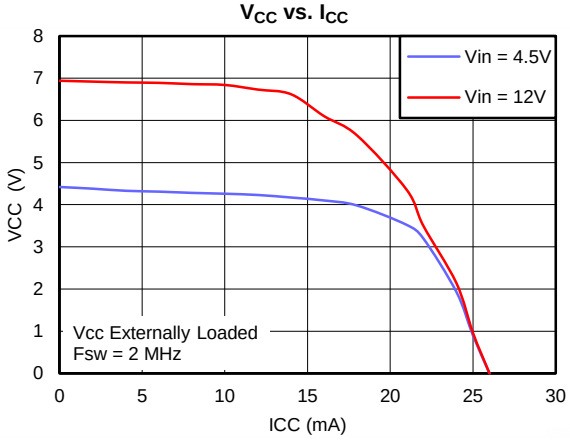
Efficiency at 2.1 MHz, V_{OUT} = 5 V



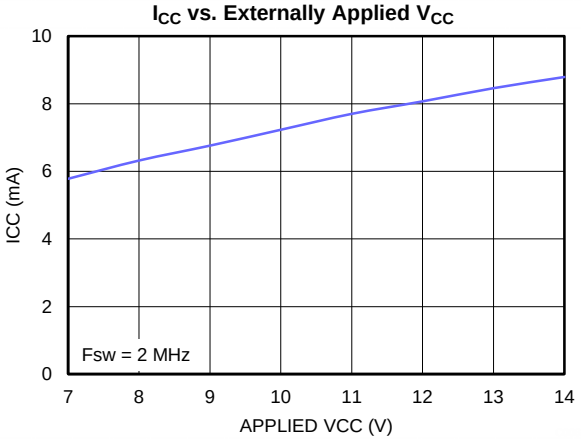
V_{CC} vs. V_{IN}



V_{CC} vs. I_{CC}

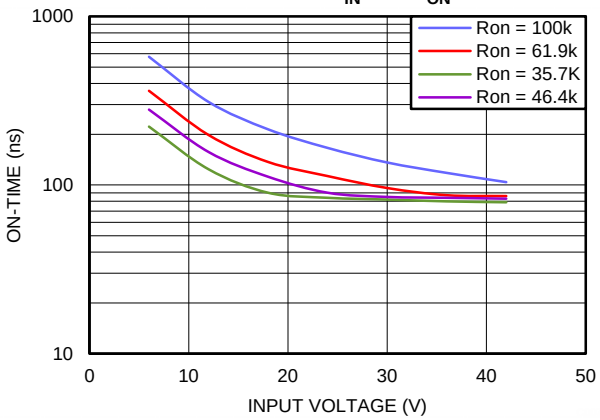


I_{CC} vs. Externally Applied V_{CC}

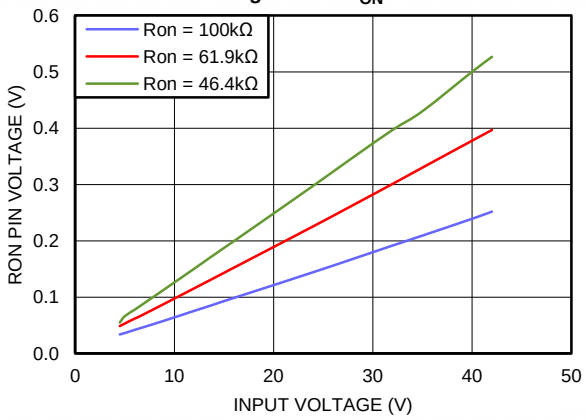


Typical Performance Characteristics (continued)

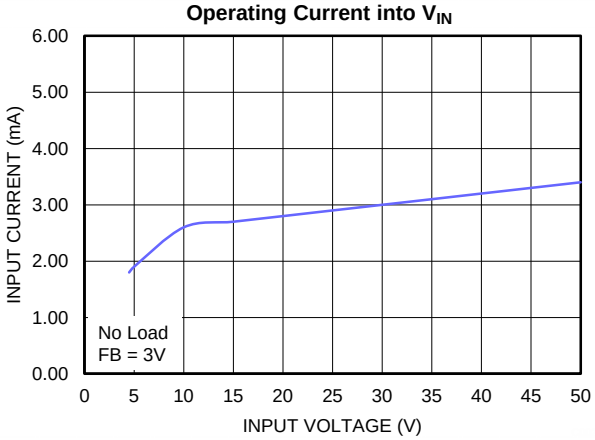
ON-TIME vs. V_{IN} and R_{ON}



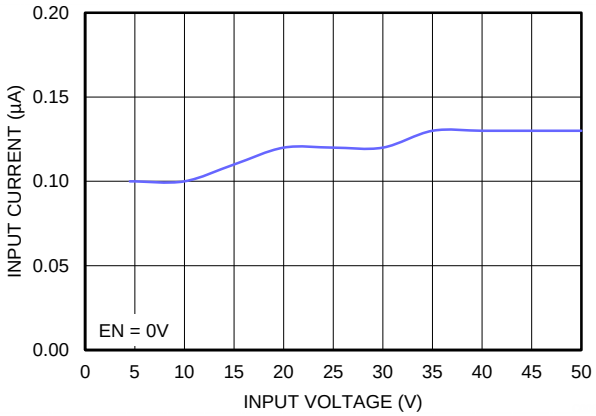
Voltage at the R_{ON} Pin



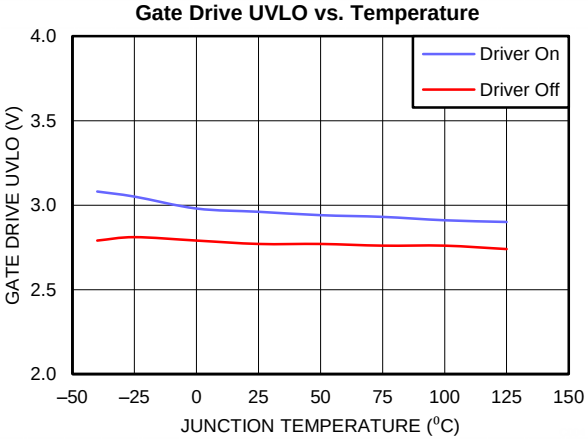
Operating Current into V_{IN}



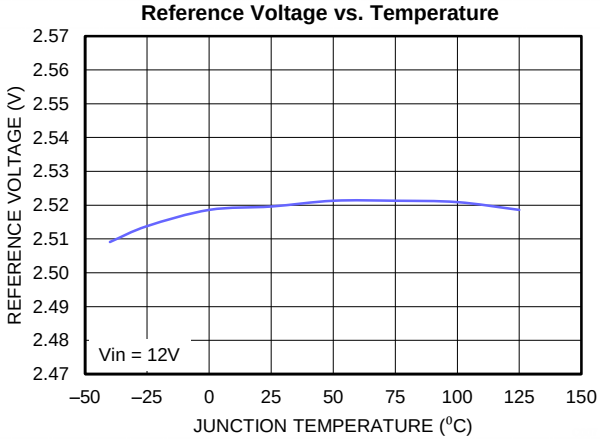
Shutdown Current into V_{IN}



Gate Drive UVLO vs. Temperature

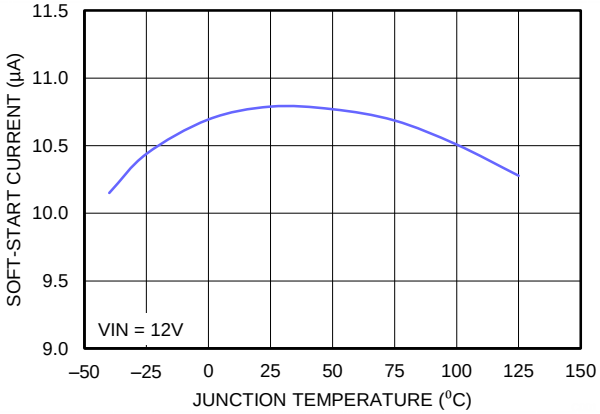


Reference Voltage vs. Temperature

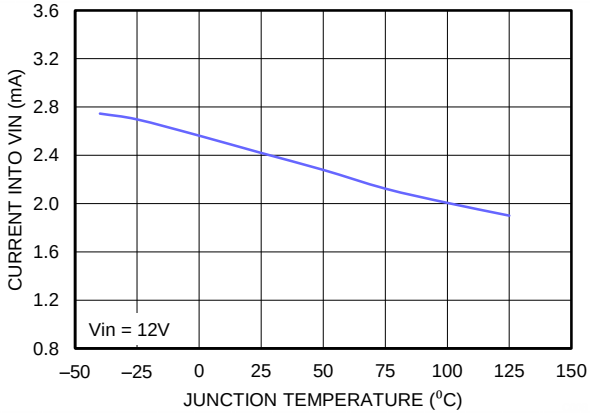


Typical Performance Characteristics (continued)

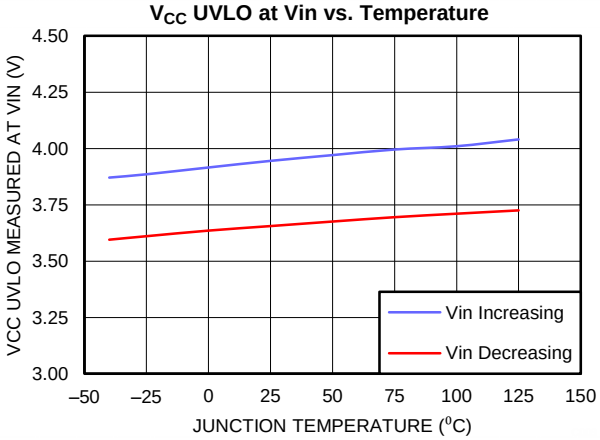
Soft-Start Current vs. Temperature



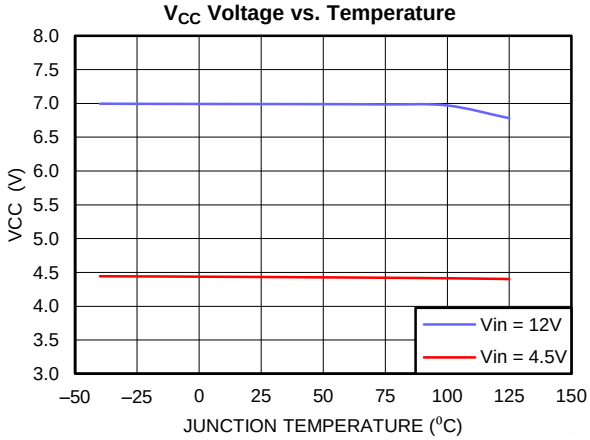
Operating Current vs. Temperature



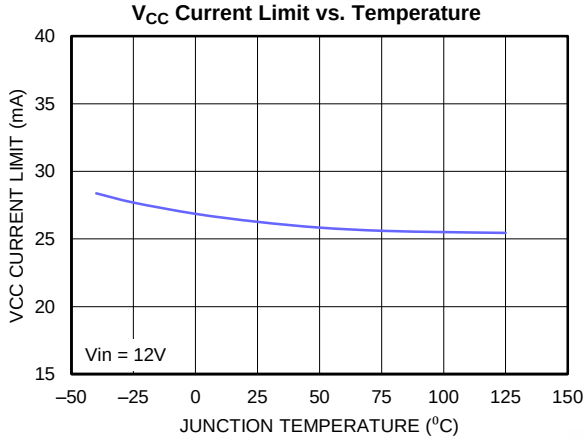
V_{CC} UVLO at Vin vs. Temperature



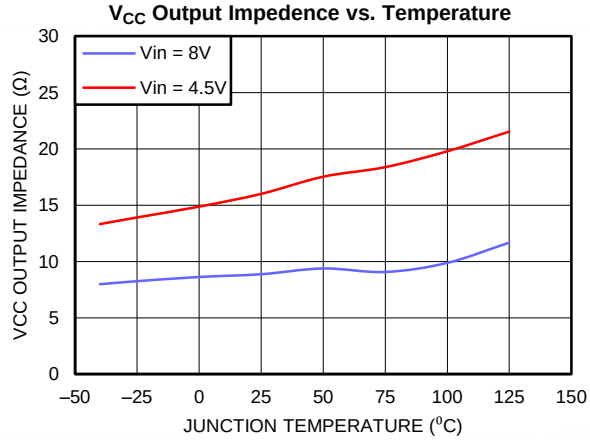
V_{CC} Voltage vs. Temperature



V_{CC} Current Limit vs. Temperature

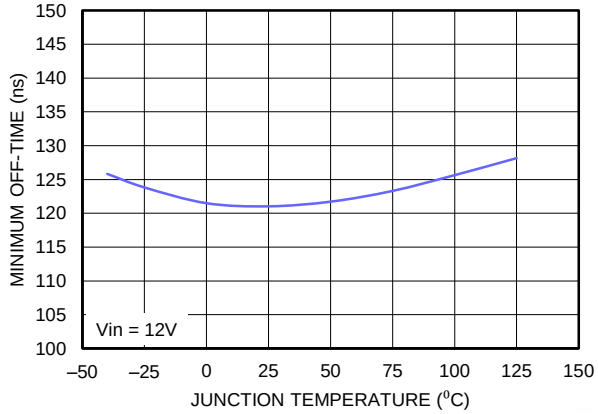


V_{CC} Output Impedence vs. Temperature

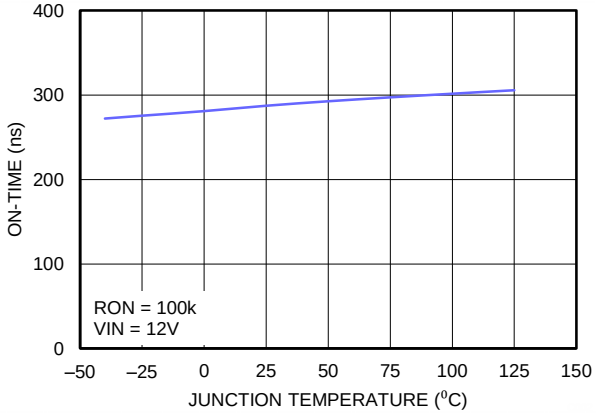


Typical Performance Characteristics (continued)

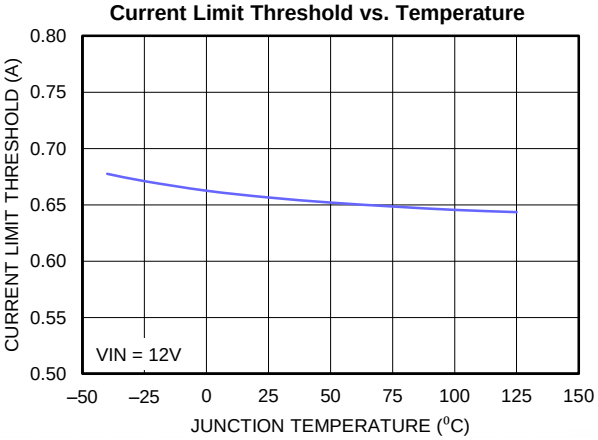
Minimum Off-Time vs. Temperature



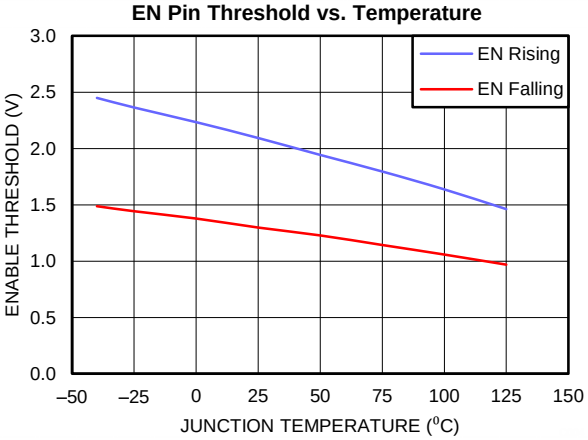
On-Time vs. Temperature



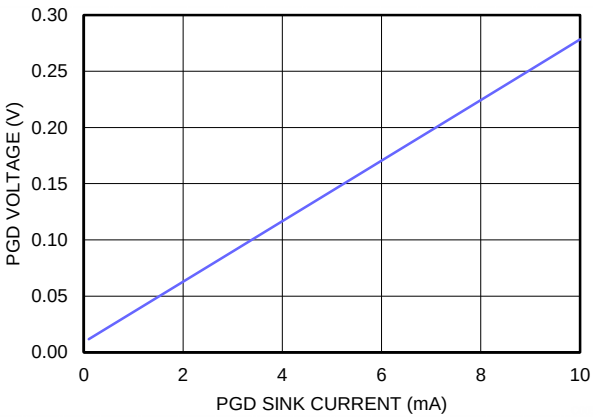
Current Limit Threshold vs. Temperature



EN Pin Threshold vs. Temperature



PGD vs. Sink Current



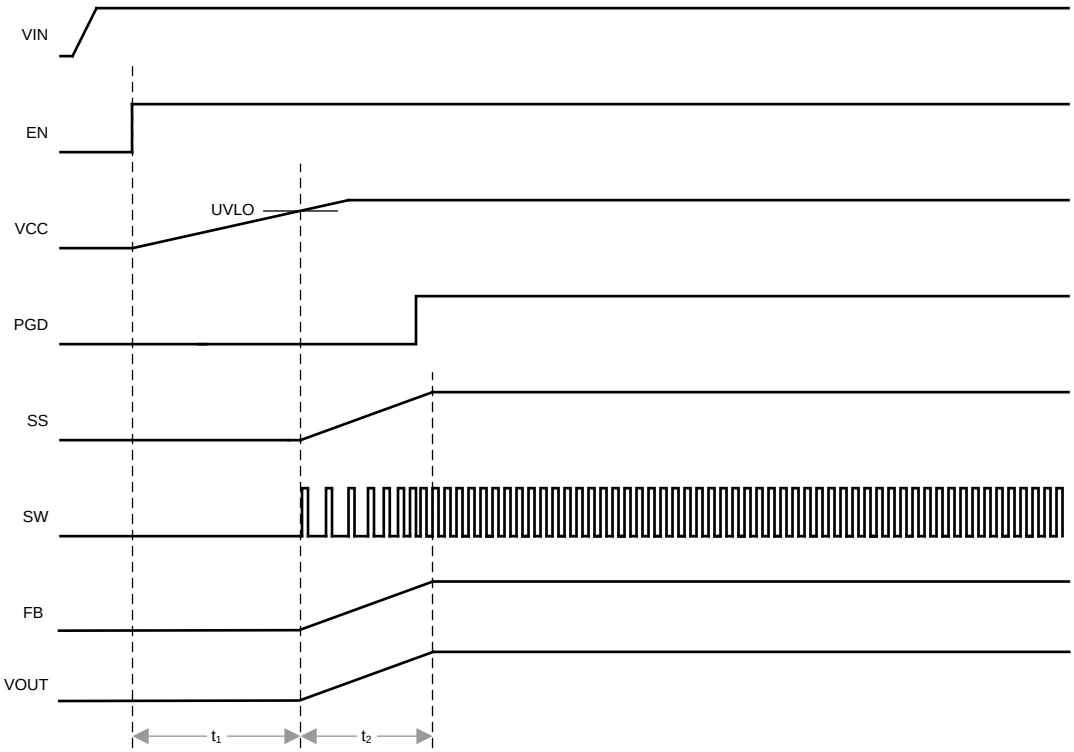


Figure 6. Start-Up Sequence

Functional Description

Device Information

The LM34919C Step Down Switching Regulator features all the functions needed to implement a low cost, efficient buck bias power converter capable of supplying 600 mA to the load. This high voltage regulator is easy to implement and is available in DSBGA and WSON packages. The regulator's operation is based on a constant on-time control scheme, where the on-time is determined by V_{IN}. This feature allows the operating frequency to remain relatively constant with load and input voltage variations. The feedback control requires no loop compensation resulting in fast load transient response. The valley current limit detection circuit, internally set at 0.64 A, holds the buck switch off until the high current level subsides. This scheme protects against excessively high current if the output is short-circuited when V_{IN} is high.

The LM34919C can be applied in numerous applications to efficiently step down higher voltages. Additional features include: Thermal shutdown, V_{CC} undervoltage lockout, gate drive undervoltage lockout, maximum duty cycle limiter, power good, and enable.

Control Circuit Overview

The LM34919C buck DC-DC regulator employs a control scheme based on a comparator and a one-shot on-timer, with the output voltage feedback (FB) compared to an internal reference (2.52 V). If the FB voltage is below the reference the N-channel buck switch is turned on for a time period determined by the input voltage and a programming resistor R_{ON}. Following the on-time the switch remains off until the FB voltage falls below the reference but not less than the minimum off-time. The buck switch then turns on for another on-time period. Typically, during start-up, or when the load current increases suddenly, the off-times are at the minimum. Once regulation is established, in steady state operations, the off-times are longer and automatically adjust to produce the SW pin duty cycle required for output regulation.

When in regulation, the LM34919C operates in continuous conduction mode at heavy load currents and discontinuous conduction mode at light load currents. In continuous conduction mode current always flows through the inductor, never reaching zero during the off-time. In this mode the operating frequency remains relatively constant with load and line variations. The minimum load current for continuous conduction mode is one-half the inductor's ripple current amplitude. The operating frequency is approximately:

$$F_S = \frac{V_{OUT}}{R_{ON} \times 35.5 \times 10^{-12}} \text{ Hz} \quad (1)$$

The buck switch duty cycle is approximately equal to:

$$DC = \frac{t_{ON}}{t_{ON} + t_{OFF}} = \frac{V_{OUT}}{V_{IN}} \quad (2)$$

In discontinuous conduction mode, current through the inductor ramps up from zero to a peak during the on-time, then ramps back to zero before the end of the off-time. The next on-time period starts when the voltage at FB falls below the reference. Until then the inductor current remains zero, and the load current is supplied by the output capacitor. In this mode the operating frequency is lower than in continuous conduction mode, and varies with load current. Conversion efficiency is maintained at light loads since the switching losses decrease with the reduction in load and frequency.

The output voltage is set by two external resistors (R1, R2). The regulated output voltage is calculated as follows:

$$\mathbf{V_{OUT} = 2.52 \text{ x } (R1 + R2) / R2} \quad (3)$$

Output voltage regulation is based on ripple voltage at the feedback input, normally obtained from the output voltage ripple through the feedback resistors. The LM34919C requires a minimum of 25 mV of ripple voltage at the FB pin. In cases where the output capacitor's ESR is insufficient additional series resistance may be required (R3).

Start-Up Regulator, V_{CC}

The start-up regulator is integral to the LM34919C. The input pin (VIN) can be connected directly to line voltage up to 50 V with transient capability to 65 V. The V_{CC} output regulates at 7.0 V and is current limited at 27 mA. Upon power up, the regulator sources current into the external capacitor at VCC (C3). When the voltage on the VCC pin reaches the undervoltage lockout rising threshold of 3.75 V, the buck switch is enabled and the soft-start pin is released to allow the soft-start capacitor (C6) to charge up.

The minimum input voltage is determined by the V_{CC} UVLO falling threshold (≅3.6 V). When V_{CC} falls below the falling threshold the V_{CC} UVLO activates to shut off the output. If V_{CC} is externally loaded, the minimum input voltage increases.

To reduce power dissipation in the start-up regulator, an auxiliary bias voltage can be diode connected to the V_{CC} pin (see Figure 7). Setting the auxiliary bias voltage between 7.6 V and 14 V shuts off the internal regulator reducing internal power dissipation. The sum of the auxiliary voltage and the input voltage (V_{CC} + V_{IN}) cannot exceed 79 V. An internal diode connects VCC to VIN. (See Figure 5).

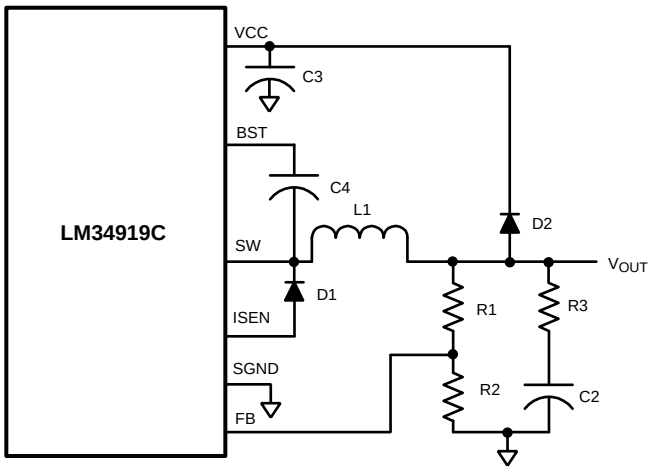


Figure 7. Self Biased Configuration

Regulation Comparator

The feedback voltage at FB is compared to the voltage at the soft-start pin. In normal operation (the output voltage is regulated), an on-time period is initiated when the voltage at FB falls below 2.52 V. The buck switch stays on for the programmed on-time causing the FB voltage to rise above 2.52 V. After the on-time period, the buck switch stays off until the FB voltage falls below 2.52 V. Input bias current at the FB pin is less than 100 nA over temperature.

Overvoltage Comparator and Undervoltage Comparator

The voltage at FB is compared to an internal overvoltage comparator reference (120% of internal reference voltage). If the voltage at FB rises above this reference, the on-time pulse is immediately terminated. This condition can occur if the input voltage or the output load changes suddenly, or if the inductor (L1) saturates. The buck switch remains off until the voltage at FB falls below 2.52 V.

When the FB pin voltage rises above the undervoltage comparator voltage reference (92% of the internal reference voltage), the PGD pin is released and is pulled high by the external pull-up resistor. When the FB pin voltage measures less than 90% of the internal reference voltage, the PGD pin switches low.

ON-Time Timer

The on-time is determined by the R_{ON} resistor and the input voltage (V_{IN}), and is calculated from:

$$T_{ON} = \frac{R_{ON} \times 35.5 \times 10^{-12}}{V_{IN}} \text{ s} \quad (4)$$

The inverse relationship with V_{IN} results in a nearly constant frequency as V_{IN} is varied. To set a specific continuous conduction mode switching frequency (f_S), the R_{ON} resistor is determined from the following:

$$R_{ON} = \frac{V_{OUT}}{F_S \times 35.5 \times 10^{-12}} \ \Omega \quad (5)$$

The minimum off-time limits the maximum duty cycle achievable with a low voltage at V_{IN}. The minimum on-time is limited to ≅ 90 ns.

Enable

The LM34919C can be remotely shut down by forcing the Enable (EN) pin low. The bias and control circuits are turned off when EN is pulled below the enable shutdown falling threshold of 1.3 V (typ). In the shutdown mode the input current falls below 10 µA. If remote shutdown feature is not needed the EN pin can be connected to the input voltage or any voltage greater than 3 V. In this case the device is enabled and disabled based on the VCC UVLO threshold.

Current Limit

Current limit detection occurs during the off-time by monitoring the recirculating current through the free-wheeling diode (D1). Referring to Figure 5, when the buck switch is turned off the inductor current flows out of ISEN and through D1. If the valley point of that current exceeds 0.64 A the current limit comparator output switches to delay the start of the next on-time period. The next on-time starts when the valley point of the current out of ISEN is below 0.64 A and the voltage at FB is below 2.52 V. If the overload condition persists causing the inductor current valley point to exceed 0.64 A during each cycle the operating frequency is lower due to longer-than-normal off-times.

Figure 8 illustrates the inductor current waveform. During normal operation the load current is Io, the average of the ripple waveform. When the load resistance decreases the current ratchets up until the lower peak reaches 0.64 A. During the Current Limited portion of Figure 8, the current ramps down to 0.64 A during each off-time, initiating the next on-time (assuming the voltage at FB is <2.52 V). During each on-time the current ramps up an amount equal to:

$$\Delta I = (V_{IN} - V_{OUT}) \times t_{ON} / L1 \quad (6)$$

During this time the LM34919C operates in a constant current mode with an average load current (I_{OCL}) equal to 0.64 A + ΔI/2.

Generally, in applications where the switching frequency is higher than ≅300 kHz and a relatively small value inductor is used, the higher dI/dt of the inductor's ripple current results in an effectively lower valley current limit threshold due to the response time of the current limit detection circuit. However, since the small value inductor results in a relatively high ripple current amplitude (ΔI in Figure 8), the load current (I_{OCL}) at current limit typically exceeds 640 mA.

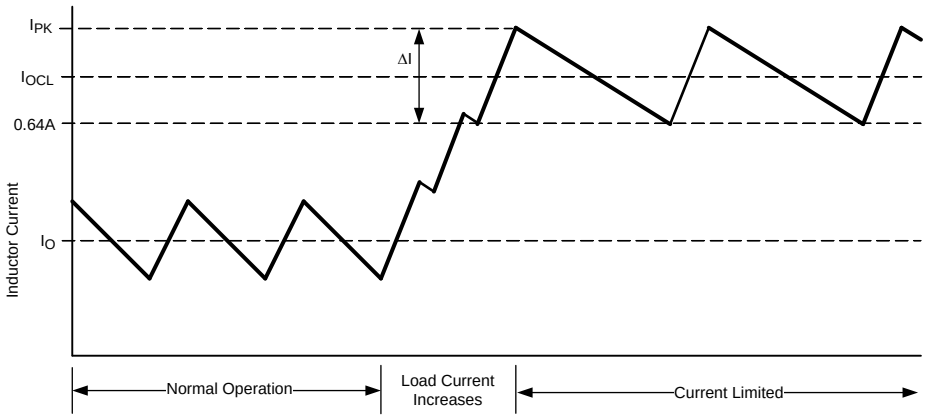


Figure 8. Inductor Current - Current Limit Operation

N - Channel Buck Switch and Driver

The LM34919C integrates an N-Channel buck switch and associated floating high side gate driver. The peak current allowed through the buck switch is 1.5 A, and the maximum allowed average current is 1 A. The gate driver circuit works in conjunction with an external bootstrap capacitor and an internal high voltage diode. A 0.022 µF capacitor (C4) connected between BST and SW provides the voltage to the driver during the on-time. During each off-time, the SW pin is at approximately -1 V, and C4 charges from V_{CC} through the internal diode. The minimum off-time of LM34919C ensures sufficient time each cycle to recharge the bootstrap capacitor.

Soft-Start

The soft-start feature allows the converter to gradually reach a steady state operating point, thereby reducing start-up stresses and current surges. Upon turn-on, after V_{CC} reaches the undervoltage threshold, an internal 10.5 µA current source charges up the external capacitor at the SS pin to 2.52 V. The ramping voltage at SS (and the inverting input of the regulation comparator) ramps up the output voltage in a controlled manner.

An internal switch grounds the SS pin if V_{CC} is below the undervoltage lockout threshold, or if the EN pin is grounded.

Power Good Output

The Power Good Output (PGD) indicates when the voltage at the FB pin is close to the internal 2.52 V reference voltage. The PGD pin remains low inside the device when the FB pin voltage is outside the range set by the PGDUV and PGDOV thresholds (see Electrical Characteristics). The PGD pin is internally connected to the drain of an N-channel MOSFET switch. An external pull-up resistor (RPGD), connected to an appropriate voltage not exceeding 14 V, is required at PGD to indicate the status of LM34919C to other circuitry. For best results, pull up the PGD pin to the output voltage. When PGD is low, the voltage at the pin is determined by the current into the pin. See the graph "PGD Low Voltage vs. Sink Current." Upon powering, as VIN is increased, PGD stays low until the output voltage takes the voltage at the FB pin above 92% of the internal reference voltage, at which time PGD switches high. As VIN is decreased (e.g., during shutdown), PGD remains high until the voltage at the FB pin falls below 90% (typ.) of the internal reference. PGD then switches low and remains low.

Thermal Shutdown

The LM34919C should be operated such that the junction temperature does not exceed 125°C. If the junction temperature increases to 175°C (typical), an internal Thermal Shutdown circuit forces the controller to a low-power reset state by disabling the buck switch. This feature helps prevent catastrophic failures from accidental device overheating. When the junction temperature reduces below 155°C (hysteresis = 20°C) normal operation resumes.

APPLICATION INFORMATION

External Components

The procedure for calculating the external components is illustrated with the following design example. Referring to Figure 5, the circuit is to be configured for the following specifications:

- V_{OUT} = 3.3 V
- V_{IN} = 4.5 V to 24 V
- Minimum load current = 200 mA
- Maximum load current = 600 mA
- Switching Frequency = 1.5 MHz
- Soft-start time = 5 ms

R1 and R2: These resistors set the output voltage. The ratio of the feedback resistors is calculated from:

$$R1/R2 = (V_{OUT}/2.52\ V) - 1 \quad (7)$$

For this example, R1/R2 = 0.32. R1 and R2 should be chosen from standard value resistors in the range of 1.0 kΩ - 10 kΩ which satisfy the above ratio. For this example, 2.49 kΩ is chosen for R2 and 787 Ω for R1.

R_{ON}: This resistor sets the on-time and the switching frequency. The switching frequency must be less than 1.53 MHz to ensure the minimum forced on-time does not cause cycle skipping when operating at the maximum input voltage. The R_{ON} resistor is calculated from Equation 8:

$$R_{ON} = \frac{V_{OUT}}{F_{SW} \times 35.5 \times 10^{-12}} = 61.9k\Omega \quad (8)$$

Check that this value resistor does not set an on-time less than 90 ns at maximum V_{IN}.

A standard value 61.9 kΩ resistor is used, resulting in a nominal frequency of 1.50 MHz. The minimum on-time is calculated ≅92 ns at Vin = 24 V, and the maximum on-time is ≅488 ns at Vin = 4.5 V. Alternately, R_{ON} can be determined using Equation 4 if a specific on-time is required.

L1: The main parameter affected by the inductor is the inductor current ripple amplitude (I_{OR}). The minimum load current is used to determine the maximum allowable ripple in order to maintain continuous conduction mode, where the lower peak does not reach 0 mA. This is not a requirement of the LM34919C, but serves as a guideline for selecting L1. For this case the maximum ripple current is:

$$I_{OR(MAX)} = 2 \times I_{OUT(min)} = 400\ mA \quad (9)$$

If the minimum load current is zero, use 20% of $I_{OUT(max)}$ for $I_{OUT(min)}$ in Equation 9. The ripple calculated in Equation 9 is then used in Equation 10:

$$L1 = \frac{(V_{IN(max)} - V_{OUT}) \times t_{on(min)}}{I_{OR(MAX)}} = 4.76\ \mu H \quad (10)$$

A standard value 8.2 µH inductor is selected. The maximum ripple amplitude, which occurs at maximum V_{IN}, calculates to 232 mA p-p, and the peak current is 716 mA at maximum load current. Ensure the selected inductor is rated for this peak current.

C2 and R3: Since the LM34919C requires a minimum of 25 mVp-p ripple at the FB pin for proper operation, the required ripple at V_{OUT} is increased by R1 and R2. This necessary ripple is created by the inductor ripple current flowing through R3, and to a lesser extent by the ESR of C2. The minimum inductor ripple current is calculated using Equation 6, rearranged to solve for I_{OR} at minimum V_{IN}.

$$I_{OR(MIN)} = \frac{(V_{IN(min)} - V_{OUT}) \times t_{on(max)}}{L1} = 71.4\ mA \quad (11)$$

The minimum value for R3 is equal to:

$$R3_{(min)} = \frac{25mV \times (R1 + R2)}{R2 \times I_{OR(MIN)}} = 0.47\ \Omega \quad (12)$$

A standard value 0.47 Ω resistor is used for R3 to allow for tolerances. C2 should generally be no smaller than 3.3 µF, although that is dependent on the frequency and the desired output characteristics. C2 should be a low ESR, good quality ceramic capacitor. Experimentation is usually necessary to determine the minimum value for C2, as the nature of the load may require a larger value. A load which creates significant transients requires a larger value for C2 than a non-varying load.

C1 and C5: C1's purpose is to supply most of the switch current during the on-time and limit the voltage ripple at V_{IN}.

At maximum load current, when the buck switch turns on, the current into V_{IN} suddenly increases to the lower peak of the inductor's ripple current, ramps up to the upper peak, then drops to zero at turn-off. The average current during the on-time is the load current. For a worst case calculation, C1 must supply this average load current during the maximum on-time, without letting the voltage at V_{IN} drop more than 0.5 V. The minimum value for C1 is calculated from:

$$C1 = \frac{I_{OUT\ (max)} \times t_{ON}}{\Delta V} = 0.5\ \mu F \tag{13}$$

where t_{ON} is the maximum on-time, and ΔV is the allowable ripple voltage. Input ripple of 0.5 V is acceptable in typical applications. C5's purpose is to minimize transients and ringing due to long lead inductance leading to the VIN pin. A low ESR, 0.1 µF ceramic chip capacitor must be located close to the VIN and RTN pins.

C3: The capacitor at the VCC pin provides noise filtering and stability for the Vcc regulator. C3 should be no smaller than 0.1 µF, and should be a good quality, low ESR, ceramic capacitor. C3's value, and the V_{CC} current limit, determine a portion of the turn-on-time (t_1 in (Figure 6).

C4: The recommended value for C4 is 0.022 µF. A high quality ceramic capacitor with low ESR is recommended as C4 supplies a surge current to charge the buck switch gate at each turn-on. A low ESR also helps ensure a complete recharge during each off-time.

C6: The capacitor at the SS pin determines the soft-start time, i.e. the time for the output voltage to reach its final value (t_2 in Figure 6). The capacitor value is determined from the following:

$$C6 = \frac{t_2 \times 10.5\ \mu A}{2.5V} = 0.021\ \mu F \tag{14}$$

D1: A Schottky diode is recommended. Ultra-fast recovery diodes are not recommended as the high speed transitions at the SW pin may inadvertently affect the device's operation through external or internal EMI. The diode should be rated for the maximum input voltage, the maximum load current, and the peak current which occurs in current limiting. The diode's average power dissipation is calculated from:

$$P_{D1} = V_F \times I_{OUT} \times (1\text{-}D) \tag{15}$$

where V_F is the diode forward voltage drop, and D is the duty cycle at the SW pin.

Final Circuit

The final circuit is shown in Figure 9, and its performance is shown in Figure 10 and Figure 11.

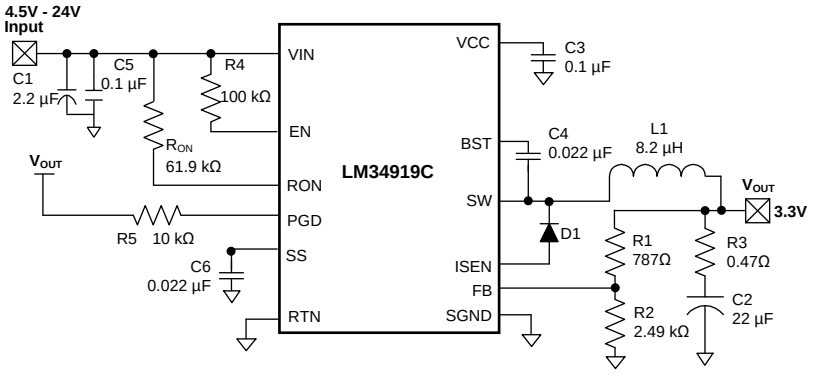


Figure 9. Example Circuit

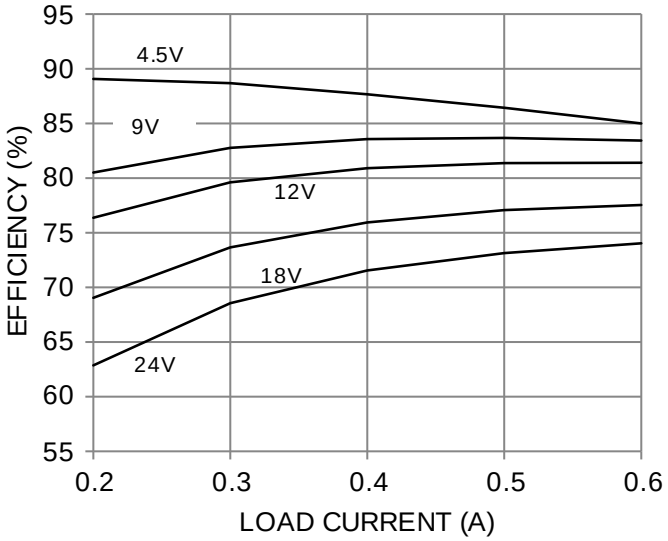


Figure 10. Efficiency (1.5 MHz, V_{OUT} = 3.3 V)

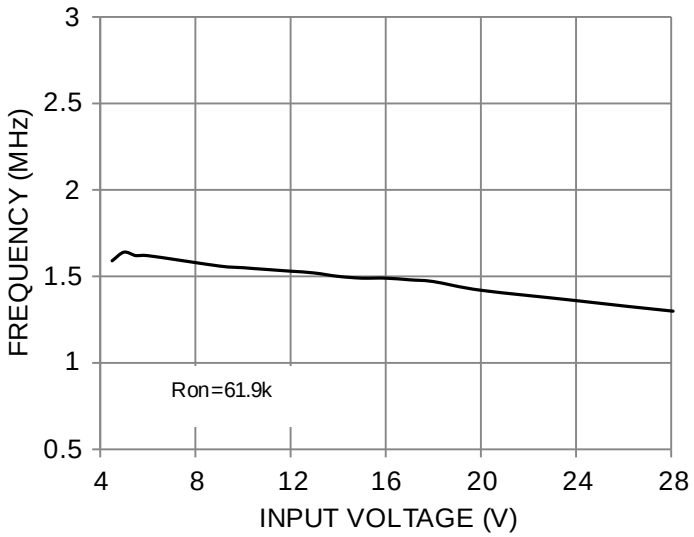


Figure 11. Frequency vs. V_{IN} (V_{OUT} = 3.3 V)

Low Output Ripple Configurations

For applications where lower ripple at V_{OUT} is required, the following options can be used to reduce or nearly eliminate the ripple.

a) Reduced ripple configuration: In Figure 12, Cff is added across R1 to AC-couple the ripple at V_{OUT} directly to the FB pin. This allows the ripple at V_{OUT} to be reduced to a minimum of 25 mVp-p by reducing R3, since the ripple at V_{OUT} is not attenuated by the feedback resistors. The minimum value for Cff is determined from:

$$Cff = \frac{t_{ON\,(max)} \times 3}{(R1//R2)} \tag{16}$$

where $t_{ON(max)}$ is the maximum on-time, which occurs at $V_{IN(min)}$. The next larger standard value capacitor should be used for Cff. R1 and R2 should each be towards the upper end of the 2 kΩ to 10 kΩ range.

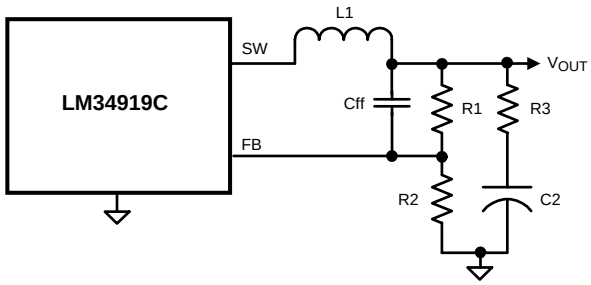


Figure 12. Reduced Ripple Configuration

b) Minimum ripple configuration: The circuit of Figure 13 provides minimum ripple at V_{OUT}, determined primarily by characteristics of C2 and the inductor's ripple current since R3 is removed. RA and CA are chosen to generate a sawtooth waveform at their junction and that voltage is AC-coupled to the FB pin via CB. To determine the values for RA, CA and CB, use the following procedure:

Calculate $V_A = V_{OUT} - (V_{SW} \times (1 - (V_{OUT}/V_{IN(min)})))$ (17)

where V_{SW} is the absolute value of the voltage at the SW pin during the off-time (typically 1 V). V_A is the DC voltage at the RA/CA junction. Calculate the RA-CA product in Equation 18.

$$RA \times CA = \frac{(V_{IN(min)} - V_A) \times t_{ON}}{\Delta V} \quad (18)$$

where t_{ON} is the maximum on-time (at minimum input voltage), and ΔV is the desired ripple amplitude at the RA/CA junction, typically 50 mV. RA and CA are then chosen from standard value components to achieve the above product. Typically CA is 3000 pF to 5000 pF and RA is 10 kΩ to 300 kΩ. CB is then chosen large compared to CA, typically 0.1 µF. R1 and R2 should each be towards the upper end of the 2 kΩ to 10 kΩ range.

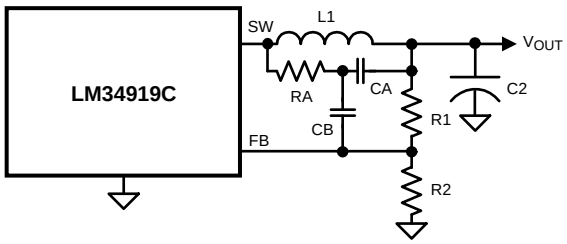


Figure 13. Minimum Output Ripple Using Ripple Injection

c) Alternate minimum ripple configuration: The circuit in Figure 14 is the same as that in Figure 9, except the output voltage is taken from the junction of R3 and C2. The ripple at V_{OUT} is determined by the inductor ripple current and C2's characteristics. R3 slightly degrades the load regulation because the feedback resistors are not directly connected to V_{OUT}. This circuit may be suitable if the load current is fairly constant.

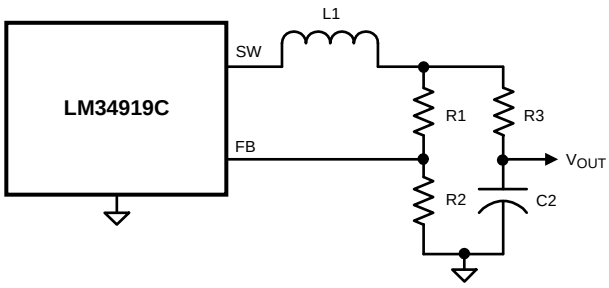


Figure 14. Alternate Minimum Output Ripple Configuration

Minimum Load Current

The LM34919C requires a minimum load current of 1 mA. If the load current falls below that level, the bootstrap capacitor (C4) may discharge during the long off-time, and the circuit will either shutdown or cycle on and off at a low frequency. If the load current is expected to drop below 1 mA in the application, R1 and R2 should be chosen low enough in value so they provide the minimum required current at nominal V_{OUT}.

PC Board Layout

Refer to application note AN-1112 for PC board guidelines for the DSBGA package.

The LM34919C regulation, overvoltage, and current limit comparators are very fast, and respond to short duration noise pulses. Layout considerations are therefore critical for optimum performance. The layout should be as compact as possible, and all of the components must be as close as possible to their associated pins. The two major current loops have currents which switch very fast, and so these loops should be as small as possible to minimize conducted and radiated EMI. The first loop is that formed by C1, through the VIN to SW pins, L1, C2, and back to C1.The second current loop is formed by D1, L1, C2 and the SGND and ISEN pins.

The power dissipation within the LM34919C can be approximated by determining the total conversion loss (P_{IN} - P_{OUT}), and then subtracting the power losses in the free-wheeling diode and the inductor. The power loss in the diode is approximately:

$$P_{D1} = I_{OUT} \times V_F \times (1-D) \quad (19)$$

where I_{OUT} is the load current, V_F is the diode's forward voltage drop, and D is the on-time duty cycle. The power loss in the inductor is approximately:

$$P_{L1} = I_{OUT}^2 \times R_L \times 1.1 \quad (20)$$

where R_L is the inductor's DC resistance, and the 1.1 factor is an approximation for the AC losses. If it is expected that the internal dissipation of the LM34919C will produce excessive junction temperatures during normal operation, good use of the PC board ground plane can help to dissipate heat. Additionally the use of wide PC board traces, where possible, can help conduct heat away from the device. Judicious positioning of the PC board within the end product, along with the use of any available air flow (forced or natural convection) will help reduce the junction temperatures.

Changes from Revision splat (September 2013) to Revision A **Page**

- Added value of the integrated high side switch for WSON package 3

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM34919CQSD/NOPB	ACTIVE	WSON	DNT	12	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L34919C	Samples
LM34919CQSDX/NOPB	ACTIVE	WSON	DNT	12	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L34919C	Samples
LM34919CQTL/NOPB	ACTIVE	DSBGA	YZR	12	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	SL9C	Samples
LM34919CQTLX/NOPB	ACTIVE	DSBGA	YZR	12	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	SL9C	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

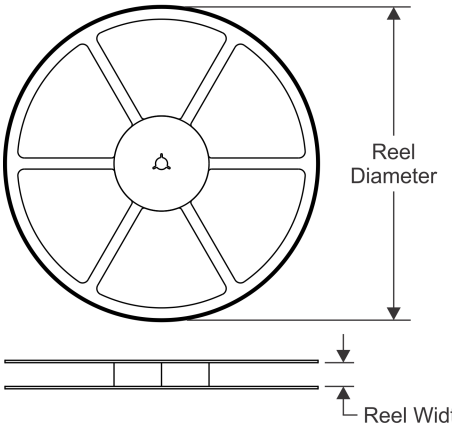
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

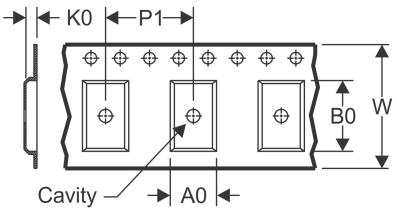
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

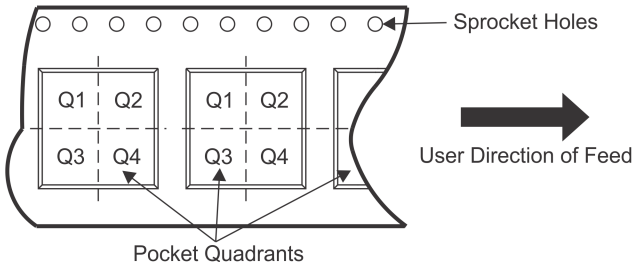


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

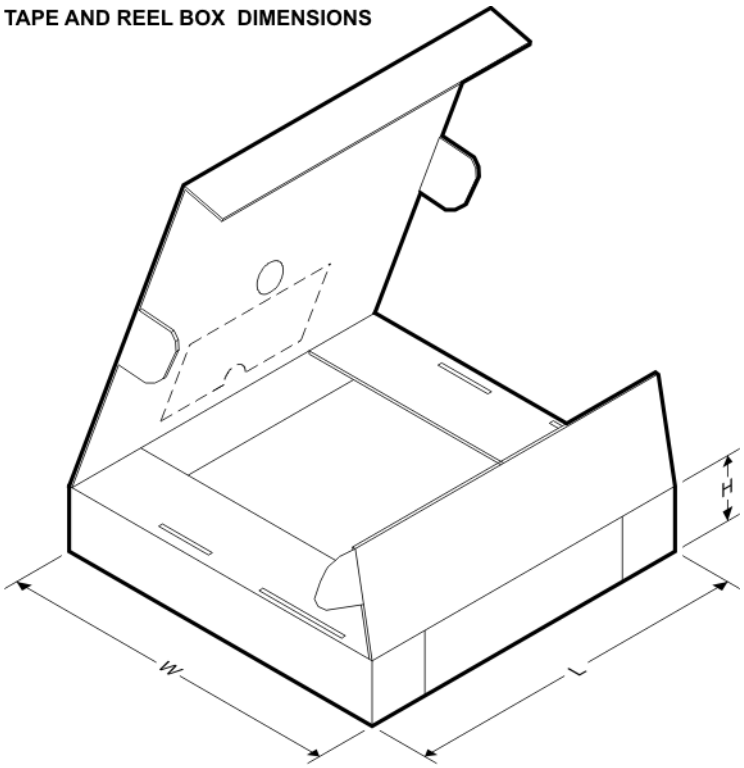
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM34919CQSD/NOPB	WSON	DNT	12	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LM34919CQSDX/NOPB	WSON	DNT	12	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LM34919CQTL/NOPB	DSBGA	YZR	12	250	178.0	8.4	2.03	2.21	0.76	4.0	8.0	Q1
LM34919CQTLX/NOPB	DSBGA	YZR	12	3000	178.0	8.4	2.03	2.21	0.76	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

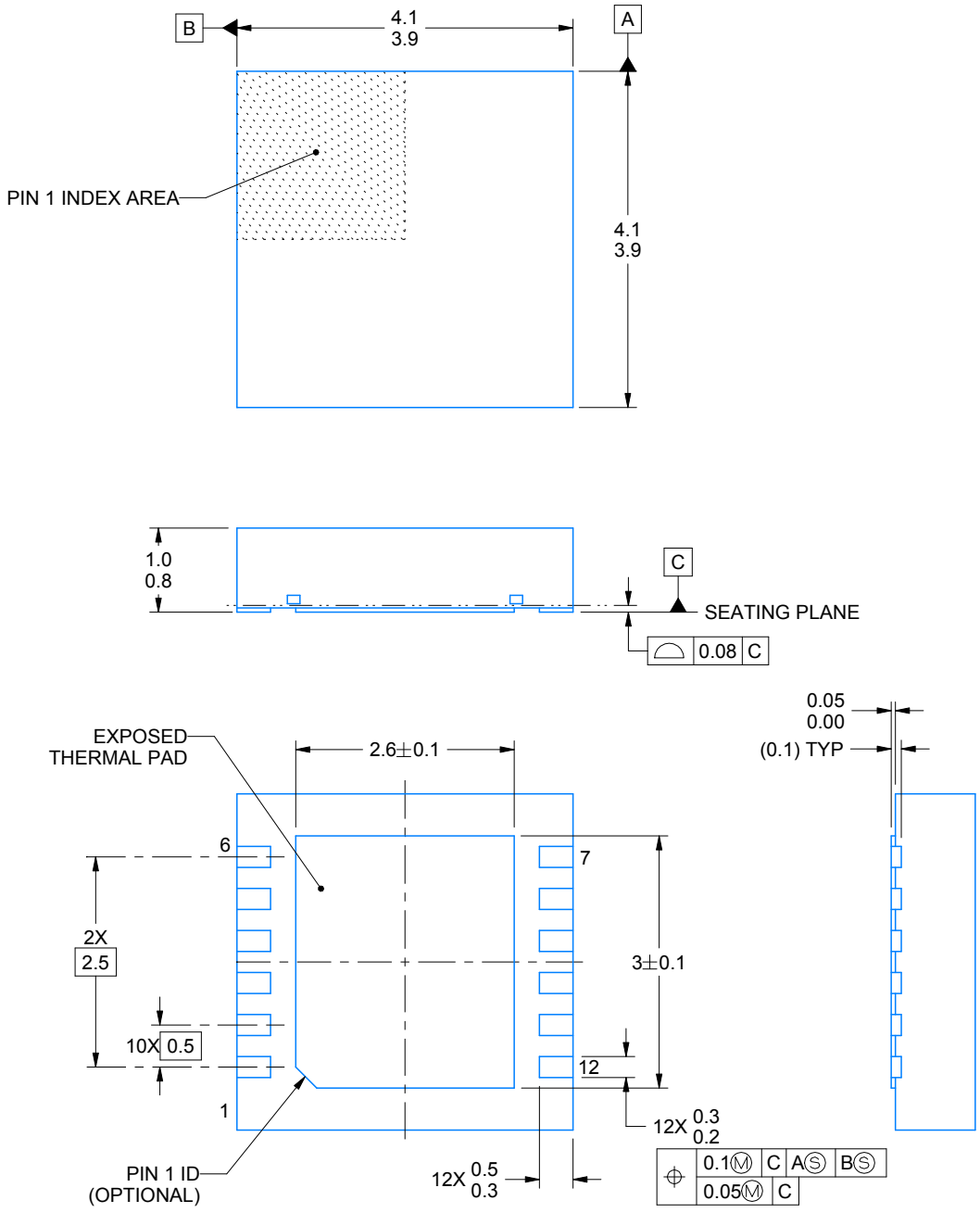
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM34919CQSD/NOPB	WSON	DNT	12	1000	210.0	185.0	35.0
LM34919CQSDX/NOPB	WSON	DNT	12	4500	367.0	367.0	35.0
LM34919CQTL/NOPB	DSBGA	YZR	12	250	210.0	185.0	35.0
LM34919CQTLX/NOPB	DSBGA	YZR	12	3000	210.0	185.0	35.0

DNT0012B

PACKAGE OUTLINE

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



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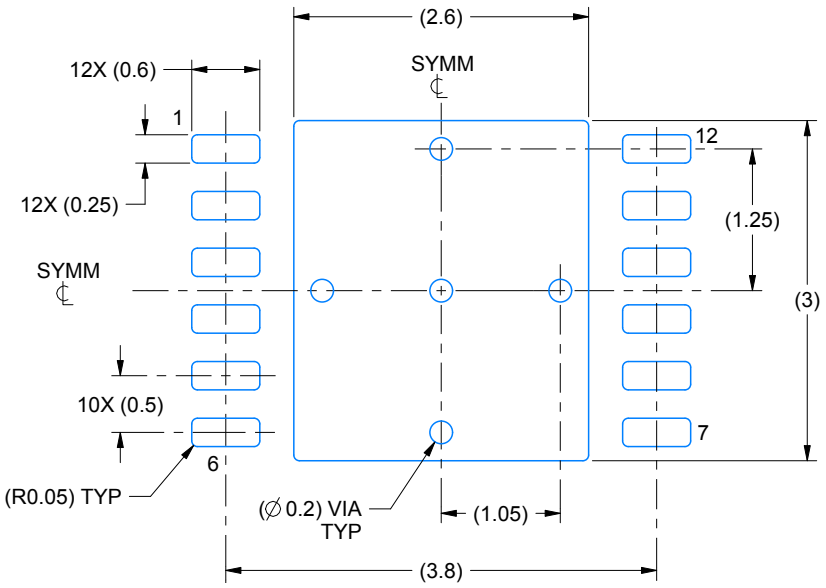
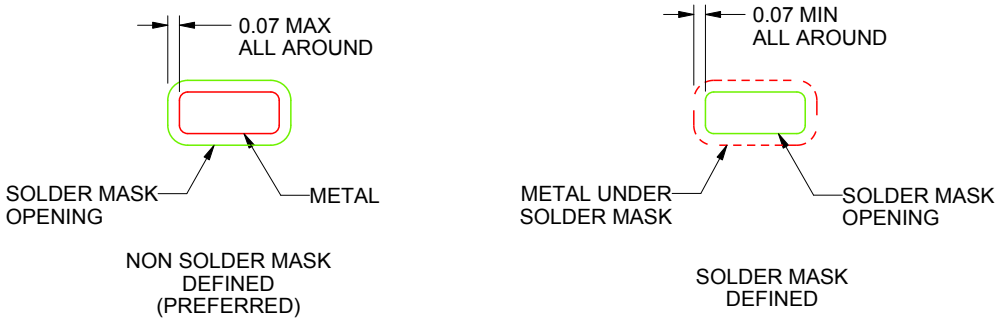
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:15X



SOLDER MASK DETAILS

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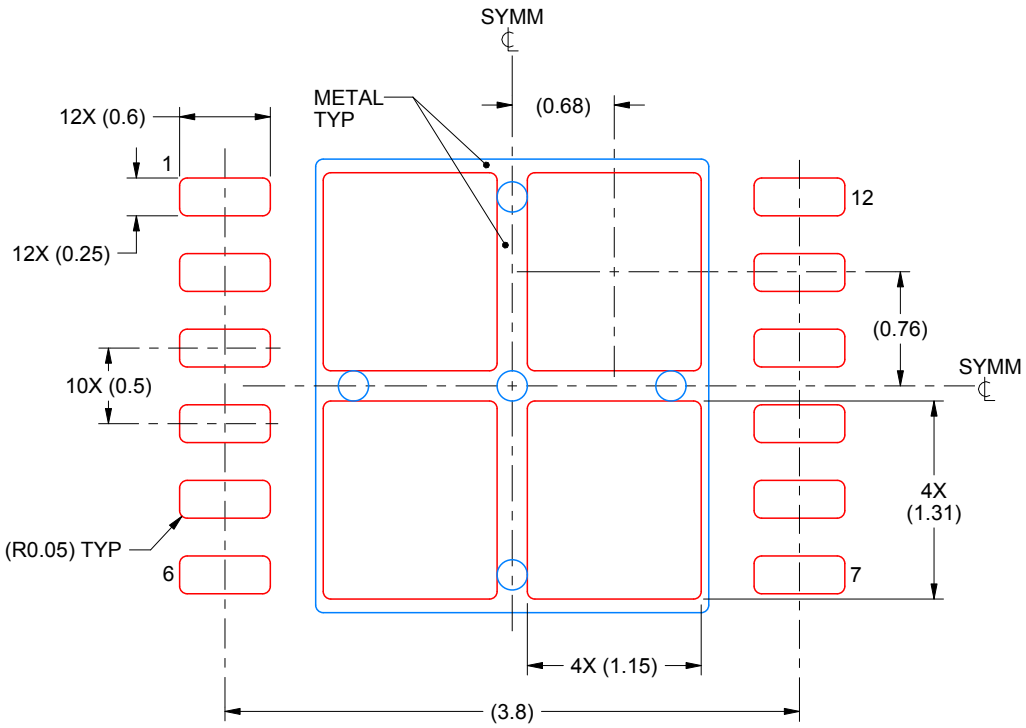
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
77% PRINTED SOLDER COVERAGE BY AREA
SCALE:20X

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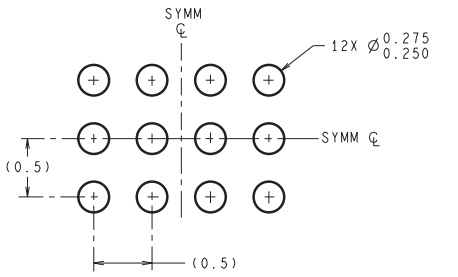
NOTES: (continued)

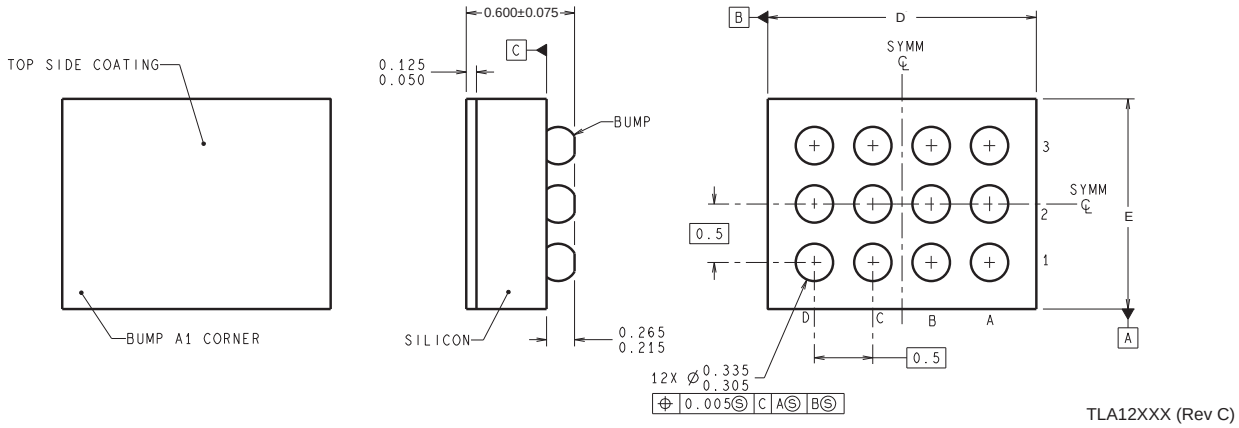
5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

YZR0012



DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY

LAND PATTERN RECOMMENDATION



TLA12XXX (Rev C)

D: Max = 2.055 mm, Min =1.995 mm

E: Max = 1.844 mm, Min =1.784 mm

4215049/A 12/12

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

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