THE DATASHEET OF

LM5037MT/NOPB

LM5037 Dual-Mode PWM Controller With Alternating Outputs

1 Features

- High-Voltage (100-V) Start-up Regulator
- Alternating Outputs for Double-Ended Topologies
- Current-mode or Feed-forward Voltage-mode Control
- Programmable Maximum Duty Cycle Limit
- 2% Feedback Reference Accuracy
- High Gain-bandwidth Error Amplifier
- Programmable Line Undervoltage Lockout (UVLO) with Adjustable Hysteresis
- Versatile Dual Mode Overcurrent Protection with Hiccup Delay Timer
- Programmable Soft-start Time
- Precision 5-V Reference Output
- Current Sense Leading Edge Blanking
- Resistor Programmed 2-MHz Capable Oscillator
- Oscillator Synchronization Capability with Low-Frequency Lockout Protection

2 Applications

- Telecom Power Converters
- Industrial Power Converters

3 Description

The LM5037 PWM controller contains all the features necessary to implement balanced double-ended power converter topologies, such as push-pull, half-bridge and full-bridge. These double-ended topologies allow for higher efficiencies and greater power densities compared to common single-ended topologies such as the flyback and forward. The device can be configured for either voltage mode or current mode control with minimum external components. Two alternating gate drive outputs are provided, each capable of 1.2-A peak output current. The device can be configured to operate directly from the input voltage rail over a wide range of 13 V to 100 V.

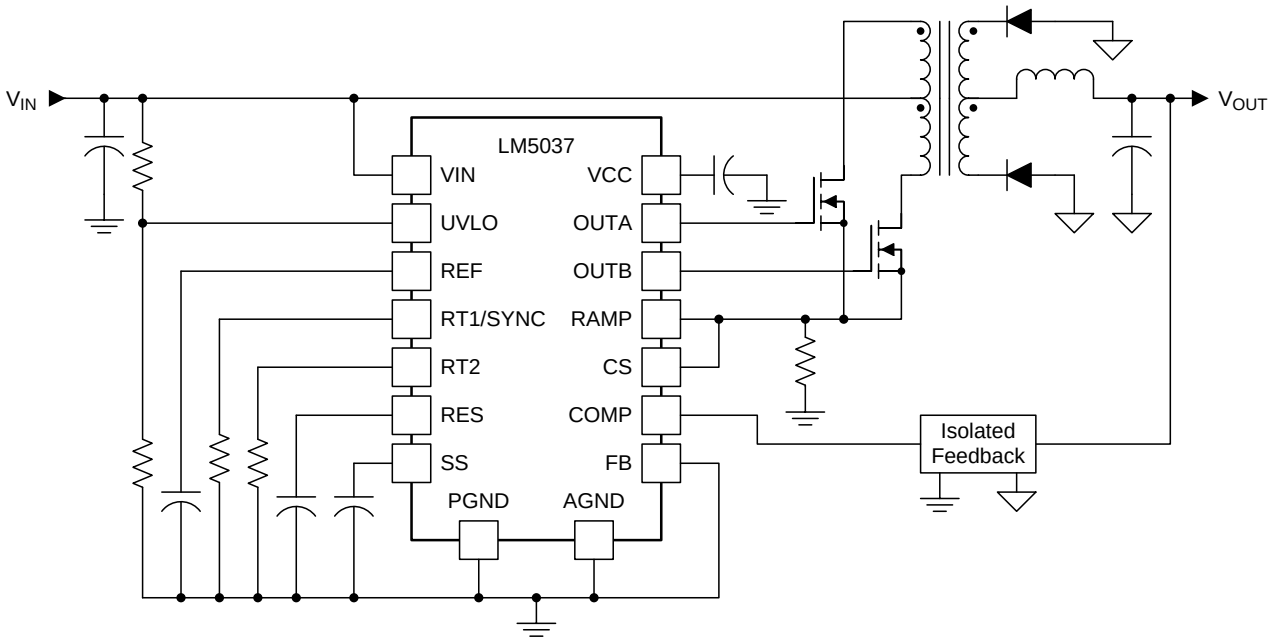
Additional features include programmable maximum duty cycle limit, line undervoltage lockout, cycle-by-cycle current limit and a hiccup mode fault protection with adjustable timeout delay, soft-start and a 2 MHz capable oscillator with synchronization capability, precision reference and thermal shutdown.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM5037	TSSOP (16)	5.00 mm × 4.4 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Application



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (March 2013) to Revision D **Page**

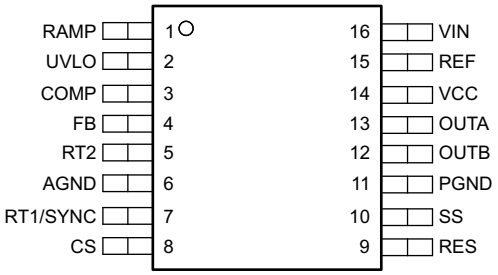
- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

Changes from Revision B (March 2013) to Revision C **Page**

- Changed layout of National Data Sheet to TI format ... 26

5 Pin Configuration and Functions

PW PACKAGE
16 PIN TSSOP
(TOP VIEW)



Pin Functions

PIN		I/O(1)	DESCRIPTION
NAME	NO.		
AGND	6	—	Analog ground. Connect directly to power ground
COMP	3	I/O	Input to the pulse width modulator. Output of the error amplifier and input to the PWM comparator.
CS	8	I	Current sense input. If the CS pin exceeds 250 mV the output pulse terminates, entering cycle-by-cycle current limit. An internal switch holds the CS pin low for a period of 65 ns after either output switches high to blank leading edge transients.
FB	4	I	Feedback. Connected to inverting input of the error amplifier. An internal 1.25-V reference is connected to the non-inverting input of the error amplifier. In isolated applications using an external error amplifier, this pin should be connected to the analog ground pin (AGND).
OUTA	13	O	Output driver. Alternating gate-drive output of the pulse width modulator. These pins are capable of 1.2-A peak source and sink current.
OUTB	12		
PGND	11	—	Power ground. Connect directly to the analog ground pin (AGND).
RAMP	1	I	Pulse width modulator ramp. Modulation ramp for the PWM comparator. This ramp can be a representative of the primary current (current mode) or proportional to input voltage (feed-forward voltage mode). This pin is reset to ground at the conclusion of every cycle by an internal FET.
REF	15	O	Output of a 5V reference. Locally decouple with a capacitor with a value of 0.1-µF or greater. Maximum output current is 10 mA (typ).
RES	9	I	Restart timer. If cycle-by-cycle current limit is reached during any cycle, the device sources 18 µA of current to the external RES pin capacitor. If the RES capacitor voltage reaches 2.0 V, the soft-start capacitor is discharged and then released with a pull-up current of 1 µA. After the first output pulse (when SS = 1 V), the SS pin charging current increases to the normal level of 100 µA.
RT1/SYNC	7	I	Oscillator dead-time control. The resistance connected between this pin (RT1/SYNC) and the AGND pin sets the oscillator maximum on-time. The sum of this maximum on-time and the forced dead-time (set by the RT2 pin) sets the oscillator period.
RT2	5	I	Oscillator dead-time control. The resistance connected between this pin (RT2) and the AGND pin sets the forced dead-time between switching periods of the alternating outputs.
SS	10	I	Soft-start. An external capacitor and an internal 100-µA current source set the soft-start ramp. The SS current source is reduced to 1 µA following a restart event (RES pin high).
UVLO	2	I	Line undervoltage lockout. An external voltage divider from the power source sets the shutdown and standby comparator threshold levels. When the UVLO pin exceeds the 0.45-V shutdown threshold, the VCC pin and REF pin regulators are enabled. When the UVLO pin exceeds the 1.25-V standby threshold, the SS pin is released and the device enters the active mode.
VCC	14	I/O	Output of the high voltage start-up regulator. The VCC pin voltage is regulated to 7.7 V. If an auxiliary winding raises the voltage on this pin above the regulation set point, the internal start-up regulator shuts down thus reducing the power dissipation of the device. Locally decouple the VCC pin with a capacitor with a value of 0.47 µF or greater.
VIN	16	I	Input voltage source. Input to the VCC start-up regulator. Operating input range is 13 V to 100 V. For power sources outside of this range, the LM5037device can be biased directly at the VCC pin by an external regulator.

(1) I = Input, O = Output, G = Ground

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Input voltage (2)	VIN	–0.3	105	V
	VCC, OUTA, OUTB	–0.3	16	
	CS	–0.3	1.0	
	UVLO, FB, RT2, RT1/SYNC, RAMP, SS, REF	–0.3	7	
Output voltage		–0.3	7	V
Storage temperature, T_{stg}		−65	50	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All input voltage ratings apply w/r/t GND.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VIN	Supply input voltage range	13		100	V
VCC	External voltage applied to VCC	8		15	V
T_J	Operating junction temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC (1)		LM5037 PW (TSSOP) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	99.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	32.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	45.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.0	°C/W
ψ_{JB}	Junction-to-board characterization parameter	45.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

over operating free-air temperature range, V_{VIN} = 48 V, V_{VCC} = 10 V, $R_{RT1/SYNC}$ = 30.1 kΩ, R_{RT2} = 30.1 kΩ, V_{UVLO} = 3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STARTUP REGULATOR (VCC PIN)						
V_{VCC}	VCC voltage	I_{VCC} = 10 mA	7.4		8	V
		I_{VCC} = 10 mA, T_A = 25°C		7.7		
$I_{VCC(lim)}$	VCC current limit	V_{VCC} = 7 V	45			mA
		V_{VCC} = 7 V, T_A = 25°C		60		
$V_{VCC(UV)}$	VCC undervoltage threshold	V_{VIN} = V_{VCC}	VCC Reg-0.2			V
		V_{VIN} = V_{VCC}, T_A = 25°C		VCC Reg-0.1		
	Hysteresis			1.5		
I_{VIN}	Startup regulator current	V_{VIN} = 100 V, V_{UVLO} = 0 V			430	µA
		V_{VIN} = 100 V, V_{UVLO} = 0 V, T_A = 25°C		350		
		V_{VIN} = 48 V, V_{UVLO} = 0 V			370	
		V_{VIN} = 48 V, V_{UVLO} = 0 V, T_A = 25°C		325		
I_{VCC}	Supply current into VCC from external source	Output pins and COMP = Open			5.5	mA
		Output pins and COMP = Open, T_A = 25°C		3		
VOLTAGE REFERENCE REGULATOR (REF PIN)						
V_{REF}	REF pin voltage	I_{REF} = 0 mA	4.75		5.15	V
		I_{REF} = 0 mA, T_A = 25°C		5		
	REF voltage regulation	0 A ≤ I_{REF} ≤ 2.5 mA			25	mV
		0 A ≤ I_{REF} ≤ 2.5 mA, T_A = 25°C		7		
$I_{REF(lim)}$	REF current limit	V_{REF} = 4.5 V	5			mA
		V_{REF} = 4.5 V, T_A = 25°C		10		
	V_{REF} undervoltage threshold		3.7		4.3	V
		T_A = 25°C		4		
$V_{REF(UV)}$	Hysteresis			0.35		V
UNDERVOLTAGE LOCKOUT AND SHUTDOWN (UVLO PIN)						
V_{UVLO}	Undervoltage lockout threshold		1.20		1.295	V
		T_A = 25°C		1.25		
		UVLO voltage rising	0.37		0.47	
		UVLO voltage rising, T_A = 25°C		0.42		
	Hysteresis voltage			0.1		V
I_{UVLO}	Hysteresis current	UVLO pin sinking	18		25	µA
		UVLO pin sinking, T_A = 25°C		22		
CURRENT SENSE INPUT (CS PIN)						
V_{CS}	Current limit threshold		0.22		0.29	V
		T_A = 25°C		0.25		
$t_{DLY(CS)}$	CS delay to output(1)	V_{CS} rising from zero to 1 V. No load.		27		ns
$t_{BLK(CS)}$	Leading edge blanking time at CS			66		ns
$R_{CS(sink)}$	CS sink impedance (clocked)(2)				45	Ω
		T_A = 25°C		21		

(1) Time for OUTA pin and OUTB pin to fall to 90% of VCC.
(2) Internal FET sink impedance.

Electrical Characteristics (continued)

over operating free-air temperature range, V_{VIN} = 48 V, V_{VCC} = 10 V, $R_{RT1/SYNC}$ = 30.1 kΩ, R_{RT2} = 30.1 kΩ, V_{UVLO} = 3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CURRENT LIMIT RESTART (RES PIN)						
V_{RES}	RES voltage threshold		1.9		2.2	V
		T_A = 25°C		2		
$I_{CHG(src)}$	Charge source current	V_{RES} = 1.5 V	14		22	µA
		V_{RES} = 1.5 V, T_A = 25°C		18		
$I_{DSCHG(snk)}$	Discharge sink current	V_{RES} = 1 V	5		11	µA
		V_{RES} = 1 V, T_A = 25°C		8		
SOFT-START (SS PIN)						
I_{SS}	Charging current	V_{SS} = 0, Normal operation	70		130	µA
		V_{SS} = 0, Normal operation, T_A = 25°C		100		
		V_{SS} = 0, Hiccup mode restart	0.6		1.5	
		V_{SS} = 0, Hiccup mode restart, T_A = 25°C		1		
$I_{SS(sink)}$	Soft-stop current sink	V_{SS} = 2.0 V	70		130	µA
		V_{SS} = 2.0 V, T_A = 25°C		100		
OSCILLATOR (RT1/SYNC AND RT2 PINS)						
t_{DEAD}	Dead time	R_{RT2} = 15 kΩ	40		105	ns
		R_{RT2} = 15 kΩ, T_A = 25°C		75		
		R_{RT2} = 75 kΩ		250		
f_{SW1}	Switching frequency 1 (3)	$R_{RT1/SYNC}$ = 30.1 kΩ, R_{RT2} = 30.1 kΩ	176		223	kHz
		$R_{RT1/SYNC}$ = 30.1 kΩ, R_{RT2} = 30.1 kΩ, T_A = 25°C		200		
f_{SW2}	Switching frequency 2 (3)	$R_{RT1/SYNC}$ = 11 kΩ, R_{RT2} = 30.1 kΩ	441		571	kHz
		$R_{RT1/SYNC}$ = 11 kΩ, R_{RT2} = 30.1 kΩ, T_A = 25°C		508		
	DC voltage level			2		V
	Input synchronization threshold voltage		2.5		3.4	V
		T_A = 25°C		3		
PWM CONTROLLER (COMP PIN)						
$t_{DLY(pwm)}$	Delay-to-output time			65		ns
V_{PWM-OS}	SS to RAMP offset voltage		0.7		1.2	V
		T_A = 25°C		1		
D_{MIN}	Mimumum duty cycle	V_{SS} = 0 V			0%	
	COMP open circuit voltage	V_{FB} = 0 V	4.5		5	V
		V_{FB} = 0 V, T_A = 25°C		4.75		
	COMP short circuit current	V_{FB} = 0 V, V_{COMP} = 0 V	0.5		1.5	mA
		V_{FB} = 0 V, V_{COMP} = 0 V, T_A = 25°C		1		
VOLTAGE FEED-FORWARD (RAMP PIN)						
$R_{RAMP(sink)}$	RAMP sink impedance (clocked)				20	Ω
		T_A = 25°C		5		

(3) Measured at OUTA, half oscillator frequency

Electrical Characteristics (continued)

over operating free-air temperature range, V_{VIN} = 48 V, V_{VCC} = 10 V, $R_{RT1/SYNC}$ = 30.1 kΩ, R_{RT2} = 30.1 kΩ, V_{UVLO} = 3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ERROR AMPLIFIER						
GBW	Gain bandwidth			4		MHz
	DC gain					
	Input voltage	$V_{FB} = V_{COMP}$	1.22		1.27	V
		$V_{FB} = V_{COMP}$, T_A = 25°C		1.245		
	COMP pin sink capability	V_{FB} = 1.5 V, V_{COMP} = 1 V	5	13		mA
	FB pin bias current			10		nA
MAIN OUTPUT DRIVERS (OUTA AND OUTB PINS)						
V_{OH}	High-level output voltage	I_{OUT} = 50 mA, (Source)	V_{VCC}–0.5			V
		I_{OUT} = 50 mA, (Source), T_A = 25°C		V_{VCC}–0.25		
V_{OL}	Low-level output voltage	I_{OUT} = 100 mA (Sink)			0.5	V
		I_{OUT} = 100 mA (Sink), T_A = 25°C		0.2		
t_{RISE}	Rise time	C_{LOAD} = 1 nF		15		ns
t_{FALL}	Fall time	C_{LOAD} = 1 nF		13		ns
$I_{PEAK(src)}$	Peak source current	V_{VCC} = 10 V		1.2		A
$I_{PEAK(snk)}$	Peak source current	V_{VCC} = 10V		1.2		A
THERMAL SHUTDOWN						
T_{SD}	Thermal shutdown threshold			165		°C
	Thermal shutdown hysteresis			25		°C

6.6 Typical Characteristics

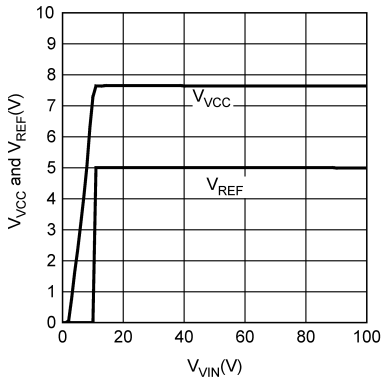


Figure 1. Reference Voltage vs. Input Voltage

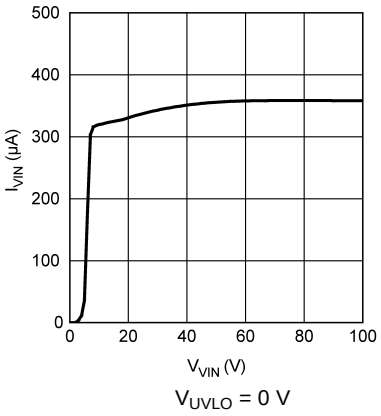


Figure 2. Start-Up Regulator Current vs Input Voltage

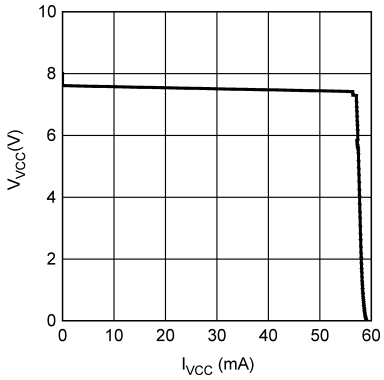


Figure 3. Input Voltage vs Input Current

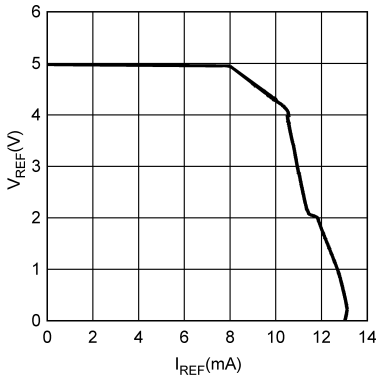


Figure 4. Reference Voltage vs. Reference Current

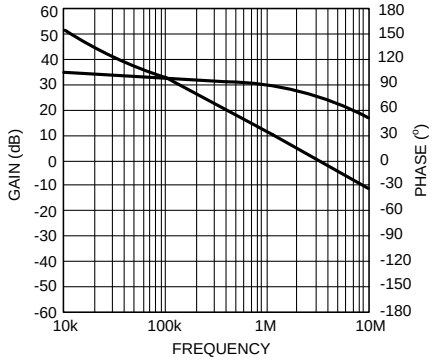


Figure 5. Feedback Amplifier Bode Plot

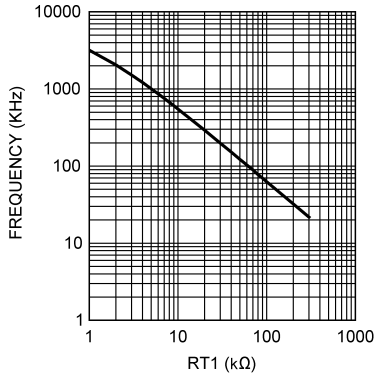


Figure 6. Oscillator Frequency vs Timing Resistance ($R_{RT1/SYNC}$)

Typical Characteristics (continued)

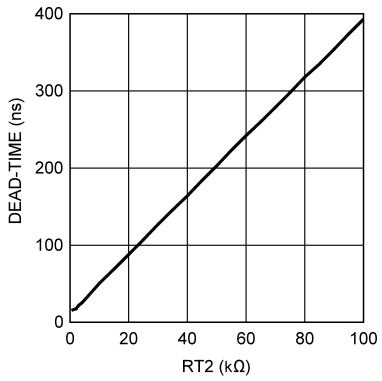


Figure 7. Dead Time vs. Timing Resistance (R_{RT2})

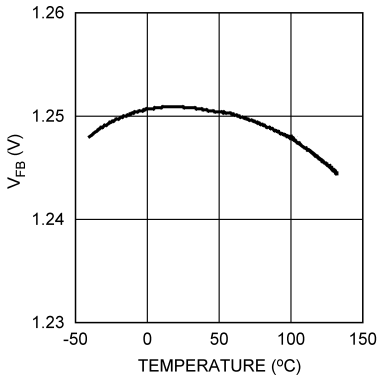


Figure 8. Feedback Voltage vs. Temperature

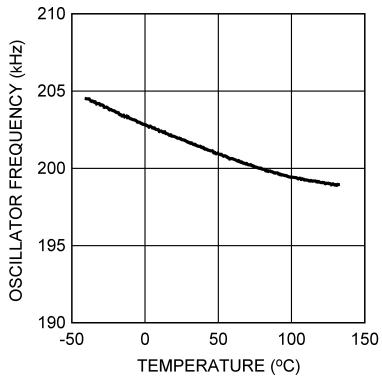


Figure 9. Oscillator Frequency vs. Temperature

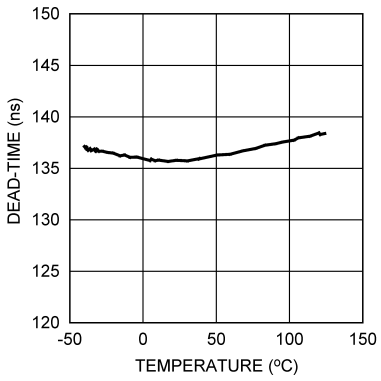


Figure 10. Dead-Time vs. Temperature

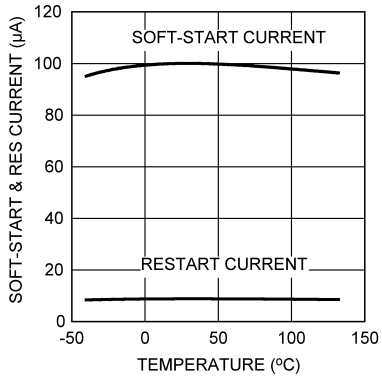


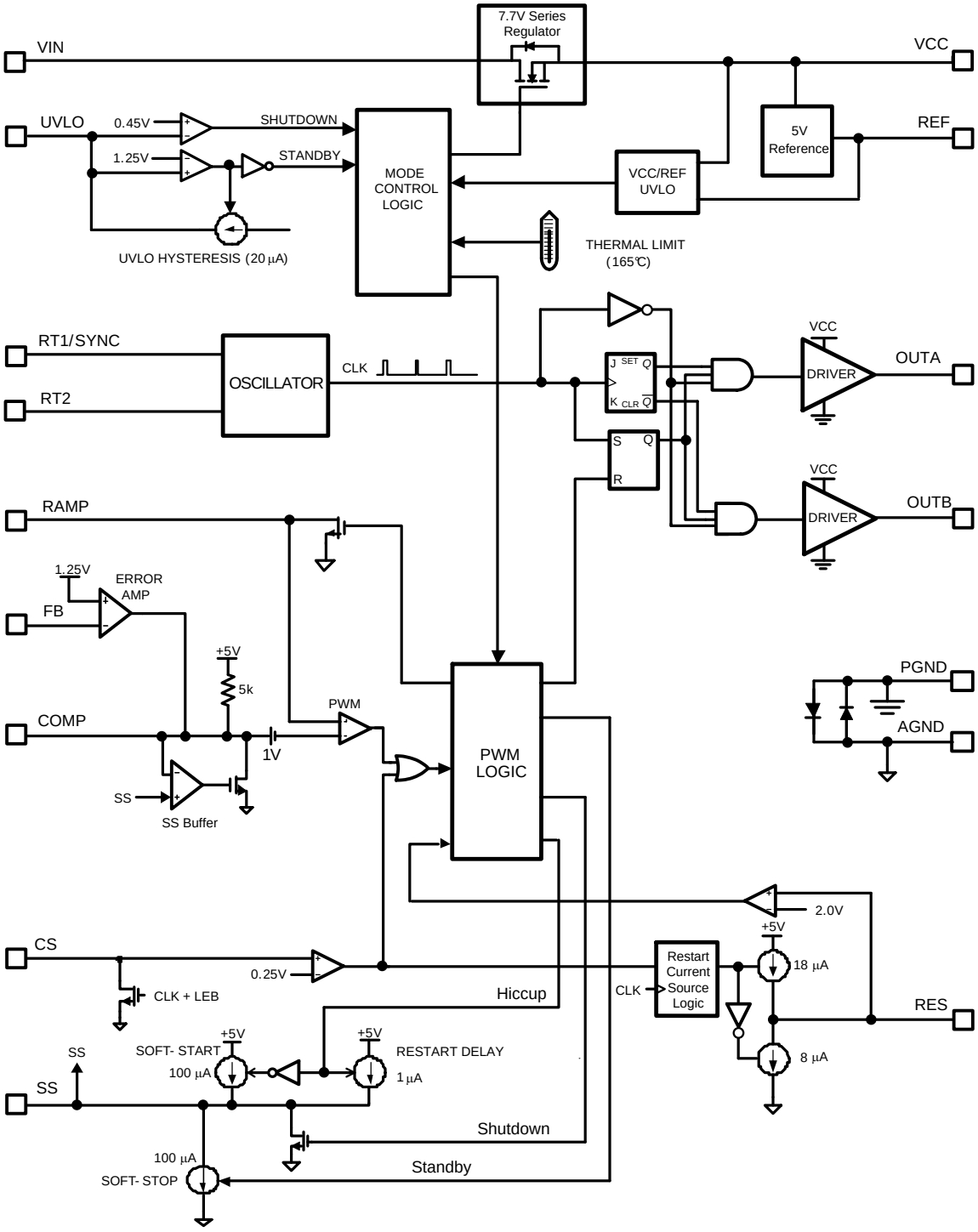
Figure 11. Soft-Start and Restart Current vs. Temperature

7 Detailed Description

7.1 Overview

The LM5037 PWM controller contains all the features necessary to implement double-ended power converter topologies such as push-pull, half-bridge and full-bridge. The unique architecture allows the modulator to be configured for either voltage-mode or current-mode control. The device provides two alternating gate driver outputs to drive the primary-side power MOSFETs with programmable forced dead-time. The device can be configured to operate with bias voltages ranging from 13 V to 100 V. Additional features include line undervoltage lockout, cycle-by-cycle current limit, voltage feed-forward compensation, hiccup mode fault protection with adjustable delays, soft-start, a 2-MHz capable oscillator with synchronization capability, precision reference and thermal shutdown. These features simplify the design of double ended topologies. The *Functional Block Diagram* section shows the functional block diagram.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 High-Voltage Start-Up Regulator

The LM5037 device contains an internal high voltage, start-up regulator that allows the input pin (VIN) to be connected directly to the supply voltage over a range of 13V to a maximum of 100 V. The regulator input can withstand transients up to 105 V. The regulator output at VCC (7.7 V) is internally current limited with a minimum of 45 mA. When the UVLO pin potential is greater than 0.45 V, the VCC regulator is enabled to charge an external capacitor connected to the VCC pin. The VCC regulator provides power to the voltage reference (REF) and the gate drivers (OUTA and OUTB). When the voltage on the VCC pin exceeds its undervoltage (VCC UV) threshold, the internal voltage reference (REF) reaches its regulation set point of 5 V and the UVLO voltage is greater than 1.25 V, the controller outputs are enabled. The value selected for the VCC capacitor depends on the total system design, and its start-up characteristics. The recommended range of values for the VCC capacitor between 0.47 µF and 10 µF.

Powering VCC from an external supply can reduce the internal power dissipation of the device. In typical applications, an auxiliary transformer winding is connected through a diode to the VCC pin. This winding must raise the VCC voltage above 8.1 V to shut off the internal start-up regulator. Powering VCC from an auxiliary winding improves efficiency while reducing the controller's power dissipation. The VCC UV circuit function remains in this mode, requiring that VCC never falls below its nominal threshold during the start-up sequence. The VCC regulator series pass transistor includes a diode between VCC and VIN that should not be forward biased in normal operation. Therefore the auxiliary VCC voltage should never exceed the VIN voltage.

An external DC bias voltage can be used instead of the internal regulator by connecting the external bias voltage to both the VCC and the VIN pins. In this particular case, the external bias must be greater than maximum VCC pin regulation of 8 V and less than the VCC maximum operating voltage rating (15 V).

7.3.2 Reference

The REF pin is the output of a 5-V linear regulator that can be used to bias an opto-coupler transistor and external housekeeping circuits. The regulator output is internally current limited to 10 mA (typical).

7.3.3 Error Amplifier

An internal high gain error amplifier is provided within the LM5037. The non-inverting amplifier reference is tied to a 1.25 V reference. In non-isolated applications the power converter output is connected to the FB pin via the voltage setting resistors and loop compensation is connected between the COMP and FB pins. A typical gain/phase plot is shown in the *Typical Characteristics* section.

For most isolated applications the error amplifier function is implemented on the secondary side. Since the internal error amplifier is configured as an open drain output, it can be disabled by connecting FB to ground. The internal, 5-kΩ pull-up resistor connected between the COMP pin and the 5-V reference can be used as the pull-up for an opto-coupler or other isolation device .

7.3.4 Cycle-By-Cycle Current Limit

The CS pin is to be driven by a signal representative of the transformer primary current. The current sense signal can be generated by using a sense resistor or a current sense transformer. If the voltage sensed at the CS pin exceeds 0.25 V, the current sense comparator terminates the output driver pulse. If the high current condition persists, the controller operates in a cycle-by-cycle current limit mode with duty cycle determined by the current sense comparator instead of the PWM comparator. Cycle-by-cycle current limiting may eventually trigger the hiccup mode restart cycle; depending on the configuration of the RES pin (see *Overload Protection Timer* section). To suppress noise, a small R-C filter connected to the CS pin and located near the controller is recommended. An internal, 21-Ω MOSFET discharges the external current sense filter capacitor at the conclusion of every cycle. The discharge MOSFET remains on for an additional 65 ns after either OUTA or OUTB driver switches high to blank leading edge transients in the current sensing circuit. Discharging the CS pin filter each cycle and blanking leading edge spikes reduces the filtering requirements and improves the current sense response time. The current sense comparator is very fast and may respond to short duration noise pulses. Layout considerations are critical for the current sense filter and sense resistor. The capacitor associated with the

Feature Description (continued)

CS filter must be placed very close to the device and connected directly to the CS and AGND pins. If a sense resistor located in the source of the main MOSFET switch is used for current sensing, a low inductance type of resistor is required. When designing with a current sense resistor, all the noise sensitive, low power ground connections should be connected together near the AGND pin, and a single connection should be made to the power ground (sense resistor ground point).

7.3.5 Soft-Start Sequence

The soft-start circuit allows the regulator to gradually reach a steady state operating point, thereby reducing start-up stresses and current surges. When bias is supplied to the LM5037, the SS pin capacitor is discharged by an internal MOSFET. When the UVLO, VCC and REF pins reach their operating thresholds, the SS capacitor is released and charged with a 100 µA current source. The PWM comparator control voltage at the COMP pin is clamped to the SS pin voltage by an internal amplifier. When the PWM comparator input reaches 1 V, output pulses commence with slowly increasing duty cycle. The voltage at the SS pin eventually increases to 5 V, while the voltage at the PWM comparator increases to the value required for regulation as determined by the voltage feedback loop.

One method to disable the regulator is to ground the SS pin. This forces the internal PWM control signal to ground, reducing the output duty cycle quickly to zero. Releasing the SS pin initiates a soft-start sequence and normal operation resumes. A second shutdown method is discussed in the *Thermal Protection* section.

7.3.6 PWM Comparator

The pulse width modulation (PWM) comparator compares the voltage ramp signal at the RAMP pin to the loop error signal. The loop error signal is derived from the internal error amplifier (COMP pin). The resulting control voltage passes through a 1-V level shift before being applied to the PWM comparator. This comparator is optimized for speed in order to achieve minimum controllable duty cycles. The common mode input voltage range of the PWM comparator is from 0 V to 4.3 V.

7.3.7 Modulation Ramp

The voltage at the RAMP pin provides the modulation ramp for the PWM comparator. The PWM comparator compares the modulation ramp signal at the RAMP pin to the loop error signal to control the output duty cycle. The modulation ramp can be implemented either as a ramp proportional to input voltage, known as feed-forward voltage mode control, or as a ramp proportional to the primary current, known as current mode control. The RAMP pin is reset by an internal FET with an $R_{DS(on)}$ of 5 Ω (typical) at the end of every cycle. The ability to configure the RAMP pin for either voltage mode or current mode allows the controller to be implemented for the optimum control method for the selected power stage topology. Configuring RAMP pin is explained below and the differences between voltage mode control and current mode control in various double-ended topologies is explained in *Application Information* section.

7.3.8 Feed-Forward Voltage Mode

An external resistor (R_{FF}) and capacitor (C_{FF}) connected to VIN, AGND, and the RAMP pins is required to create the PWM ramp signal as shown in Figure 12. It can be seen that the slope of the signal at RAMP varies in proportion to the input line voltage. This varying slope provides line feed-forward information necessary to improve line transient response with voltage mode control. The RAMP signal is compared to the error signal by the pulse width modulator comparator to control the duty cycle of the outputs. With a constant error signal, the on-time (t_{ON}) varies inversely with the input voltage (VIN) to stabilize the Volt-Second product of the transformer primary. At the end of clock period, an internal FET engages to reset the C_{FF} capacitor. The formulae for R_{FF} and C_{FF} and component selection criteria are explained in *Application and Implementation* section. The amplitude of the signal driving RAMP pin must not exceed the common mode input voltage range of the PWM comparator (3.3 V) while in normal operation.

Feature Description (continued)

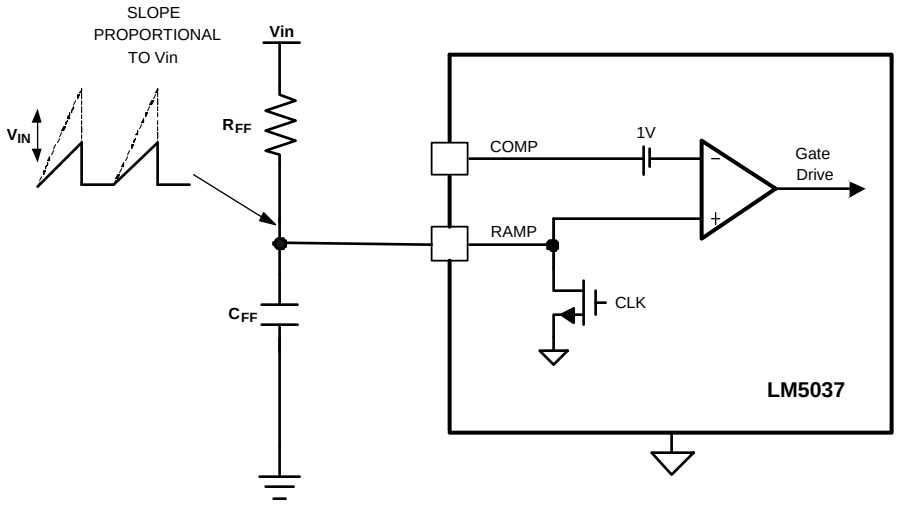


Figure 12. Feed-Forward Voltage Mode Configuration

7.3.9 Current Mode

The LM5037 device can be configured for current mode control by injecting a signal representative of primary current into the RAMP pin. One way to achieve this is shown in Figure 13. Filter components R_{filter} and C_{filter} are used to filter leading edge noise spikes. The signal at the CS pin is thus a ramp on a pedestal. The pedestal corresponds to the continuous conduction current in the transformer at the beginning of an OUTA or OUTB conduction cycle. The R-C circuit (R_{Slope} and C_{Slope}), shown in Figure 13, tied to V_{REF} adds an additional ramp to the current sense signal. This additional ramp signal, known as slope compensation, is required to avoid instabilities at duty cycles above 50% (25% per phase). The compensated RAMP signal consists of two parts, the primary current signal and the slope compensation. The compensated RAMP signal is compared to the error signal by the PWM comparator to control the duty cycle of the outputs. The RAMP capacitor and CS capacitor are reset through internal discharge FETs. The on-resistance ($R_{DS(on)}$) of RAMP discharge FET is 5 Ω (typical); this ensures fast discharge of the RAMP reset capacitor. Any dc voltage source can be used in place of V_{REF} to generate the slope compensation ramp.

The timing diagram shown in Figure 14 depicts the current mode waveforms and relative timing. When OUTA or OUTB is enabled, the signal at the RAMP pin consists of the CS pin signal (current ramp on a pedestal) plus the slope compensation ramp (dotted lines). When OUTA or OUTB is turned off, the primary current component is absent but the voltage at the RAMP pin continues to rise due to slope compensation component until the end of the clock period, after which it is reset by the RAMP discharge FET. A component selection example is explained in detail in the *Application and Implementation* section.

Feature Description (continued)

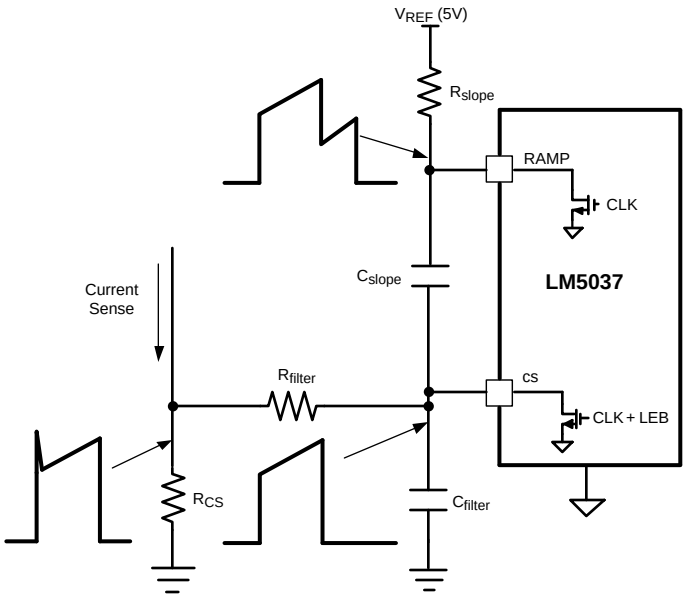


Figure 13. Current Mode Configuration with Slope Compensation

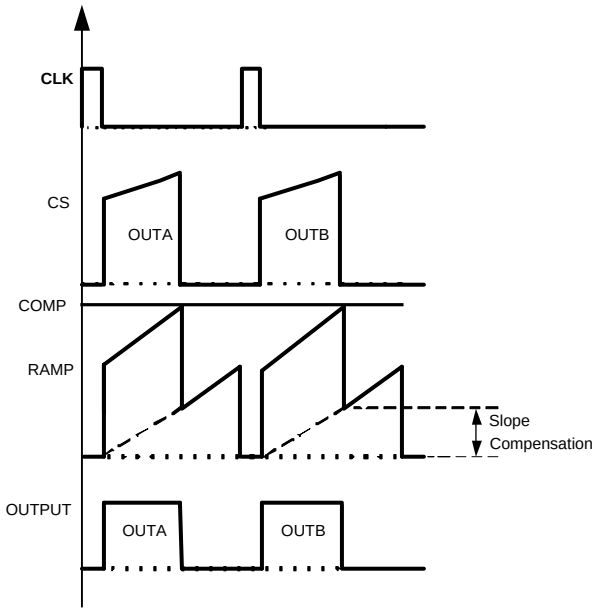


Figure 14. Timing Diagram for Current Mode Configuration

7.3.10 Oscillator

The LM5037 device oscillator frequency and the maximum duty cycle are set by two external resistors connected between the RT1/SYNC and RT2 pins to AGND. The minimum dead-time between OUTA and OUTB pulses is proportional to the RT2 resistor value and the overall oscillator frequency is inversely proportional to $R_{RT1/SYNC}$ and R_{RT2} resistor values. Each output switches at half the oscillator frequency. Use Equation 1 to calculate a value of R_{RT2} that supports a required dead-time. Use Equation 2 to calculate a value of R_{RT2} that supports a maximum duty cycle (D_{MAX}).

Feature Description (continued)

$$R_{RT2} = \left(\frac{t_{DEAD}}{5 \times 10^{-12}} \right) \quad (1)$$

$$50\ ns \leq t_{DEAD} \leq 250\ ns \quad (2)$$

$$R_{RT2} = \left(\frac{\left(\frac{(1 - D_{MAX})}{f_{OSC}} \right)}{5 \times 10^{-12}} \right) \quad (3)$$

The recommended dead-time range is between 50 ns and 250 ns. Beyond 250 ns, the R_{RT2} resistance becomes excessively large, and is prone to noise pickup. Fixed internal delays limit the dead-time to greater than 50 ns. After the dead-time has been programmed by RT2, the overall oscillator frequency can be set by selecting the resistor $R_{RT1/SYNC}$ using Equation 4.

$$R_{RT1/SYNC} = \left(\frac{\left(\frac{1}{f_{OSC}} \right) - t_{DEAD}}{0.162 \times 10^{-9}} \right) \quad (4)$$

For example, if the desired oscillator frequency is 400 kHz (OUTA and OUTB each switching at 200 kHz) and desired dead-time is 100 ns, the maximum duty cycle for each output is 96%. The value of $R_{RT1/SYNC}$ is 15 kΩ and R_{RT2} is 20 kΩ.

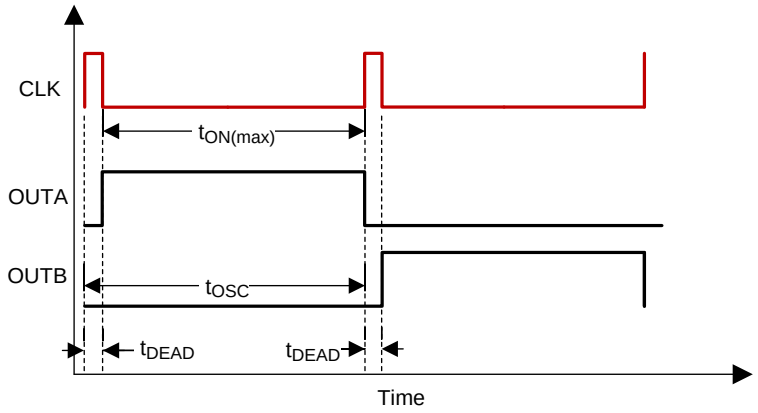


Figure 15. Timing Diagram of OUTA, OUTB and Dead-Time Set by RT2

As shown in Figure 15, the internal clock pulse width is the same as the dead-time set by the RT2 pin. This dead-time pulse is used to limit the maximum duty cycle for each of the outputs. Also, the discharge FET connected to the RAMP pin is enabled during the dead-time every clock period. The voltages at both the RT1/SYNC and RT2 pins are internally regulated to a nominal 2 V. Both the $R_{RT1/SYNC}$ and R_{RT2} resistors should be located as close as possible to the device, and connected directly to the pins. Consider the tolerance of the external resistors and the frequency tolerance indicated in the *Electrical Characteristics* table when determining the worst case frequency range.

7.3.11 Synchronization Capability

The LM5037 device can be synchronized to an external clock by applying a narrow ac pulse to the RT1/SYNC pin. The external clock must be at least 10% higher than the free-running oscillator frequency set by the $R_{RT1/SYNC}$ and R_{RT2} resistors. If the external clock frequency is less than the programmed frequency, the device ignores the synchronizing pulses. The synchronization pulse width at the RT1/SYNC pin must be a minimum of 15 ns wide. The synchronization signal should be coupled into the RT1/SYNC pin through a 100 pF capacitor or

Feature Description (continued)

another value small enough to ensure the sync pulse width at RT1/SYNC is less than 60% of the clock period under all conditions. When the synchronizing pulse transitions from low-to-high (rising edge), the voltage at the RT1/SYNC pin must be driven to exceed 3.0 V from its nominal 2.0 Vdc level. During the synchronization clock signal low time, the voltage at the RT1/SYNC pin clamps at 2 V by an internal regulator. The $R_{RT1/SYNC}$ and R_{RT2} resistors are always required, whether the oscillator is free running or externally synchronized.

7.3.12 Gate Driver Outputs (OUTA and OUTB Pins)

The LM5037 device provides two alternating gate driver outputs, OUTA and OUTB. The internal gate drivers can each source and sink 1.2-A peak each. The maximum duty cycle is inherently limited to less than 50% and is based on the value of R_{RT2} resistor. As an example, if the COMP pin is in a high state, $R_{RT1/SYNC}$ = 15 kΩ and R_{RT2} = 20 kΩ then the outputs operate at a maximum duty cycle of 96%.

7.3.13 Thermal Protection

Internal thermal shutdown circuitry is provided to protect the integrated circuit in the event the maximum rated junction temperature is exceeded. When activated, typically at 165°C, the controller is forced into a low power standby state with the output drivers (OUTA and OUTB) and the bias regulators (VCC and REF) disabled. This helps to prevent catastrophic failures from accidental device overheating. During thermal shutdown, the soft-start capacitor is fully discharged and the controller follows a normal start-up sequence after the junction temperature falls to the operating level (140°C).

7.4 Device Functional Modes

7.4.1 Overload Protection Timer

The LM5037 device provides a current limit restart timer to disable the outputs and force a delayed restart (hiccup mode) if a current limit condition is repeatedly sensed. The number of cycle-by-cycle current limit events required to trigger the restart is programmed by the external capacitor at the RES pin. During each PWM cycle, the device either sources to or sinks current from the RES pin capacitor. If no current limit is detected during a cycle, a 8-µA discharge current sink is enabled to pull the RES pin towards ground. If a current limit is detected, the 8-µA sink current is disabled and a 18-µA current source causes the voltage at the RES pin to gradually increase. The device protects the converter with cycle-by-cycle current limiting while the voltage at RES pin increases. If the RES voltage reaches the 2.0 V threshold, the following restart sequence occurs (also see Figure 16):

- The RES capacitor and SS capacitors are fully discharged.
- The soft-start current source is reduced from 100 µA to 1 µA.
- The SS capacitor voltage slowly increases. When the SS voltage reaches approximately 1 V, the PWM comparator produces the first narrow output pulse. After the first pulse occurs, the SS source current reverts to the normal 100 µA level. The SS voltage increases at its normal rate, gradually increasing the duty cycle of the output drivers.
- If the overload condition persists after restart, cycle-by-cycle current limiting begins to increase the voltage on the RES capacitor again, repeating the hiccup mode sequence.
- If the overload condition no longer exists after restart, the RES pin remains at ground by the 8-µA current sink and normal operation resumes.

7.4.1.1 Overload Timer Function

This section lists the modes of protection available by configuring the overload timer function.

7.4.1.1.1 Cycle-by-cycle Only

The hiccup mode can be completely disabled by connecting a zero to 50 kΩ resistor from the RES pin to AGND. In this configuration, the cycle-by-cycle protection limits the output current indefinitely and no hiccup sequences occurs.

Device Functional Modes (continued)

7.4.1.1.2 Hiccup Only

The timer can be configured for immediate activation of a hiccup sequence upon detection of an overload by leaving the RES pin open circuit. In this configuration, the first detection of current limit condition by the CS pin comparator initiates a hiccup cycle with SS capacitor fully discharged and a delayed restart.

7.4.1.1.3 Delayed Hiccup

Connecting a capacitor to the RES pin provides a programmed interval of cycle-by-cycle limiting before initiating a hiccup mode restart, as previously described. The dual advantages of this configuration are that a short term overload does not cause a hiccup mode restart but during extended overload conditions, the average dissipation of the power converter remains very low.

7.4.1.2 Externally Controlled Hiccup

The RES pin can also be used as an input. The RES pin forces the device into a delayed restart sequence when the pin rises to a level greater than the 2.0 V hiccup threshold. For example, an external trigger for a delayed restart sequence may come from an over-temperature protection circuit or an output over-voltage sensor.

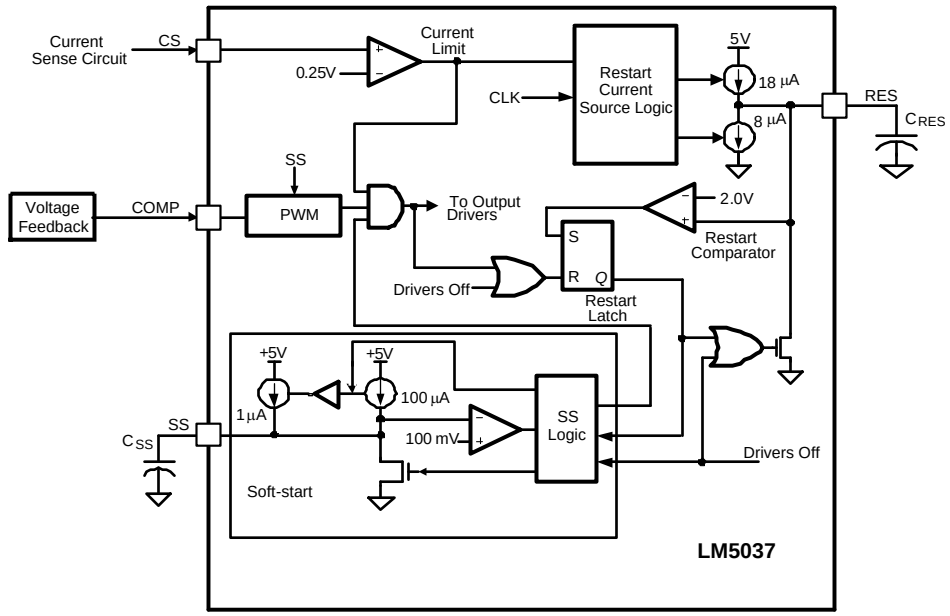


Figure 16. Current Limit Restart Circuit

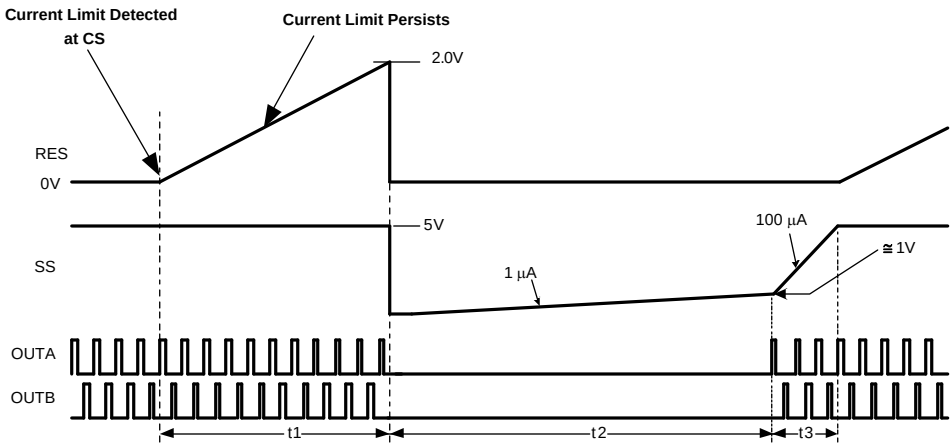


Figure 17. Current Limit Restart Timing

Device Functional Modes (continued)

7.4.2 Topology and Control Algorithm Choice

The LM5037 device has all the features required to implement double-ended power converter topologies such as push-pull, half-bridge and full-bridge with minimum external components. One key feature is the flexibility in control algorithm selection. For example, the device can be used to implement either voltage mode control or current mode control. Designers familiar with these topologies recognize that conventionally, current mode control is used for push-pull and full-bridge topologies while voltage mode control is required for the half-bridge topology. In limited applications, voltage mode control can be used for push-pull and full-bridge topologies as well, with special care to maintain flux balance, such as using a dc-blocking capacitor in the primary (full-bridge). The goal of this section is to illustrate implementation of both current mode control and voltage mode control using the LM5037 device and aid the designer in the design process.

7.4.3 Voltage Mode Control

An external resistor (R_{FF}) and capacitor (C_{FF}) connected to VIN, AGND, and the RAMP pins is required to create a saw-tooth modulation ramp signal shown in Figure 18. The slope of the signal at RAMP varies in proportion to the input line voltage. The varying slope provides line feed-forward information necessary to improve line transient response with voltage mode control. With a constant error signal, the on-time (t_{ON}) varies inversely with the input voltage (VIN) to stabilize the Volt • Second product of the transformer primary. Using a line feed-forward ramp for PWM control requires very little change in the voltage regulation loop to compensate for changes in input voltage, as compared to a fixed slope oscillator ramp. Furthermore, voltage mode control is less susceptible to noise and does not require leading edge filtering, and is therefore a good choice for wide input range power converters. Voltage mode control requires a more complicated compensation network, due to the complex-conjugate poles of the L-C output filter.

In push-pull and full-bridge topologies, any asymmetry in the volt-second product applied to primary in one phase may not be cancelled by subsequent phase, possibly resulting in a dc current build-up in the transformer, which pushes the transformer core towards saturation. Special care in the transformer design, such as gapping the core, or adding ballasting resistance in the primary is required to rectify this imbalance when using voltage mode control with these topologies. Current mode control naturally corrects for any volt-second asymmetry in the primary.

The recommended capacitor value range for C_{FF} is 100 pF to 1500 pF. Referring to Figure 18, it can be seen that value C_{FF} must be small enough such that the capacitor can be discharged within the clock (CLK) pulse width each cycle. The CLK pulse width is same as the dead-time set by RT2. The minimum possible dead-time for the device is 50 ns and the internal discharge FET $R_{DS(on)}$ is 5 Ω (typical),

The value of R_{FF} required can be calculated from

$$R_{FF} = \frac{-1}{f_{OSC} \times C_{FF} \times \ln\left(1 - \frac{V_{RAMP}}{V_{IN(min)}}\right)} \quad (5)$$

For example, assuming a V_{RAMP} of 1 V at $V_{IN(min)}$ (a good compromise of signal range and noise immunity), oscillator frequency, f_{OSC} of 250 kHz, $V_{IN(min)}$ of 24 V, and C_{FF} = 270 pF results in a value for R_{FF} of 348 kΩ.

Device Functional Modes (continued)

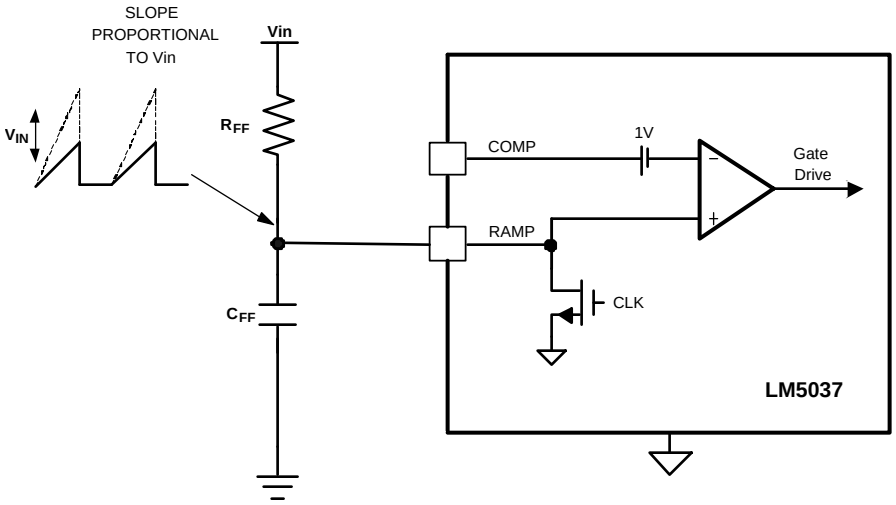


Figure 18. Feed-Forward Voltage Mode Configuration

7.4.4 Current Mode Control

The LM5037 device can be configured in current mode control by applying the primary current signal into the RAMP pin. One way to achieve this is shown in Figure 19, which depicts a simplified push-pull converter. The primary current is sensed using a sense resistor and the current information is then filtered and applied to the RAMP pin through capacitor C_{slope}, for use as the modulation ramp. It can be seen that the signal applied to the RAMP pin consists of the primary current information from the CS pin plus an additional ramp for slope compensation, added by R_{slope} and C_{slope}.

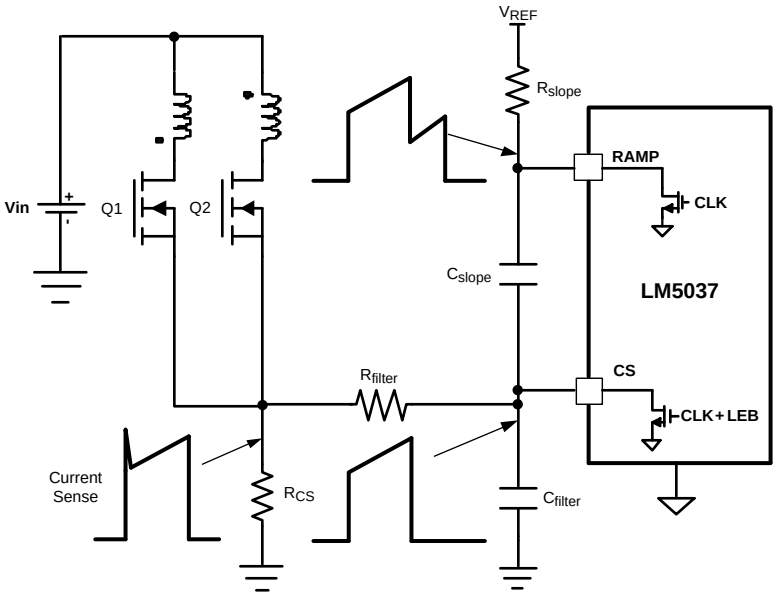


Figure 19. Current Mode Configuration

Current mode control inherently provides line voltage feed-forward, cycle-by-cycle current limiting and ease of loop compensation as it removes the additional pole due to output inductor. Also, in push-pull and full-bridge converters, current mode control inherently balances volt-second product in both the phases by varying the duty cycle as needed to terminate the cycle at the same peak current for each output phase. For duty cycles greater than 50% (25% for each phase), peak current mode controlled circuits are subject to sub-harmonic oscillation.

Device Functional Modes (continued)

Sub-harmonic oscillation is normally characterized by observing alternating wide and narrow duty cycles at the controller output. Adding an artificial ramp (slope compensation) to the current sense signal eliminates this potential oscillation. Current mode control is also susceptible to noise and layout considerations. It is recommended that C_{Filter} and C_{slope} be placed as close to the IC as possible to avoid any noise pickup and trace inductance. When the converter is operating at low duty cycles and light load, the primary current amplitude is small and is susceptible to noise. The artificial ramp, added to avoid sub-harmonic oscillations, provides additional benefits by improving the noise immunity of the converter.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Input Supply Voltage (VIN and VCC pins)

The voltage applied to the VIN pin, which may be the same as the system voltage applied to the power transformer's primary (V_{PWR}), can vary from 8 V to 100 V. The current into the VIN pin depends primarily on the gate charge provided by the output drivers, the switching frequency, and any external loads on the VCC and REF pins. This design uses the filter shown in Figure 20 to suppress transients that may occur at the input supply. A filter is particularly important when VIN is operated close to the maximum operating rating of the LM5037.

When power is applied to VIN and the UVLO pin voltage is greater than 0.45 V, the VCC regulator is enabled and supplies current into an external capacitor connected to the VCC pin. When the voltage on the VCC pin reaches the regulation point of 7.7 V, the voltage reference (REF) enables. The reference regulation set point is 5 V. The outputs (OUTA and OUTB) enable when the two bias regulators reach their set point and the UVLO pin potential is greater than 1.25 V. In typical applications, an auxiliary transformer winding connects through a diode to the VCC pin. In order to shut off the internal start-up regulator, this winding must raise the VCC voltage above 8.1 V.

After the outputs are enabled and the external VCC supply voltage has begun supplying power to the device, the current into the VIN pin drops below 1 mA. VIN should remain at a voltage equal to or above the VCC voltage to avoid reverse current through protection diodes.

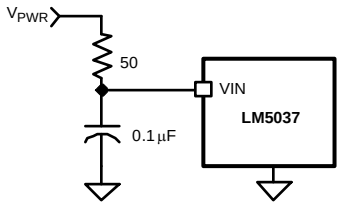


Figure 20. Input Transient Protection

8.1.2 100-V (or Higher) Input Voltage Applications

For applications where the system input voltage exceeds 100 V or the device power dissipation is of concern, the LM5037 device can be powered from an external start-up regulator as shown in Figure 21. This configuration shows the VIN and the VCC pins connected together. The voltage at the VCC and VIN pins must be greater than 8.1 V (> VCC_{MAX} reference voltage) and not exceed 15 V. Use an auxiliary winding to reduce the power dissipation in the external regulator after the power converter activates. The N-P-N base-emitter reverses breakdown voltage, which can be as low as 5 V for some transistors. Consider this breakdown voltage when selecting the transistor.

Application Information (continued)

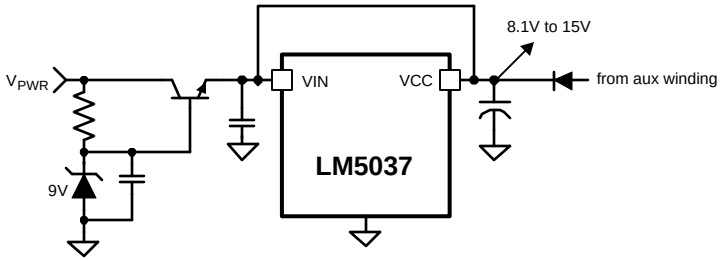


Figure 21. Start-up Regulator for V_{PWR} >100 V

8.1.3 Current Sense

The CS pin receives an input signal representative of the transformer primary current, either from a current sense transformer or from a resistor in series with the source of the OUTA and OUTB MOSFET switches. In both cases, the sensed current creates a voltage ramp across R1, and the R_FC_F filter suppresses noise and transients as shown in Figure 22 and Figure 23. Locate components R1, R_F and C_F as close to the device as possible. Use a dedicated track from the current sense transformer (R1) to the ground connection (AGND pin). Ensure that the current sense components provide greater than 220 mV at the CS pin when an over-current condition exists.

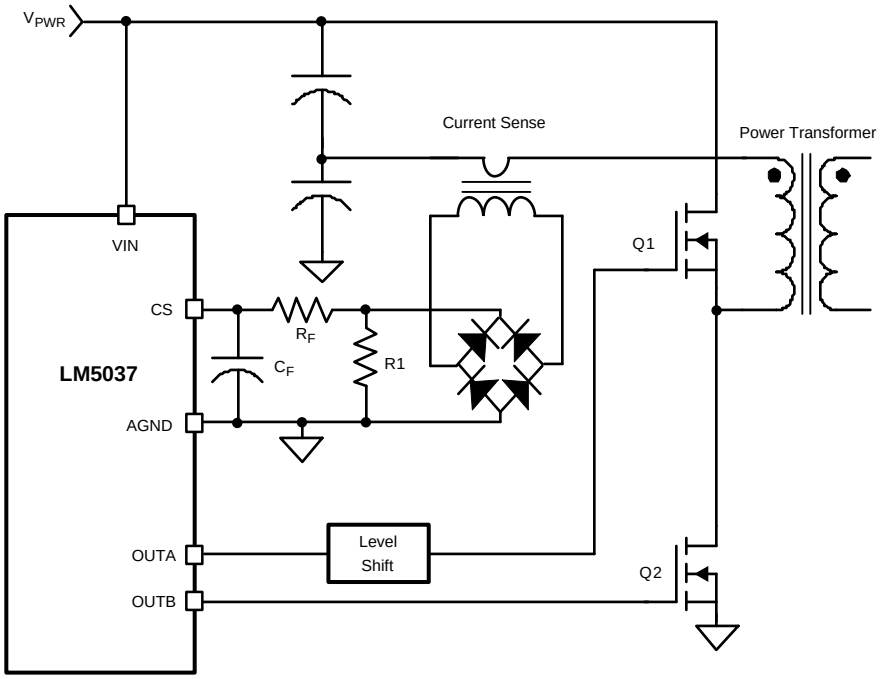


Figure 22. Current Sense Using Transformer

Application Information (continued)

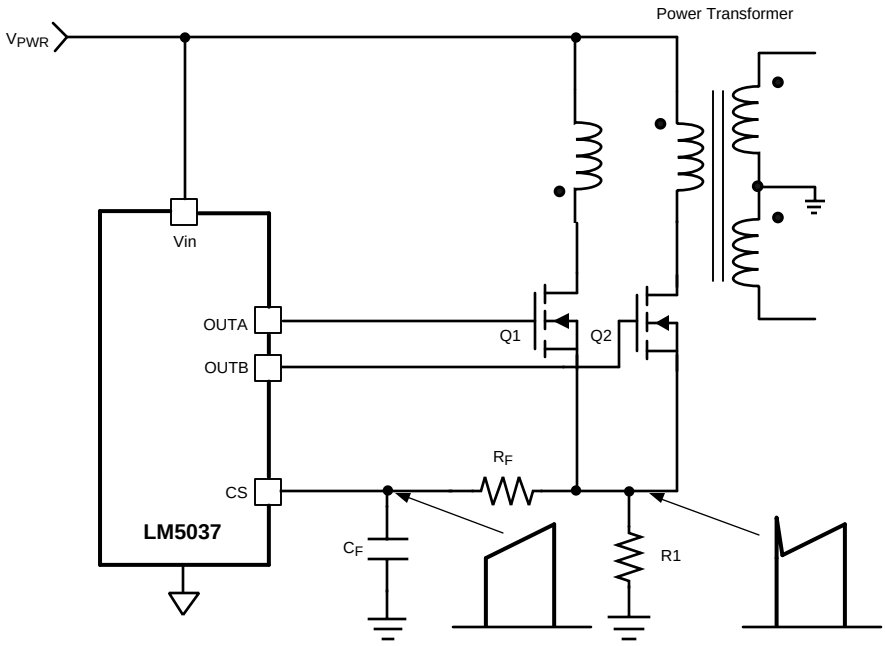


Figure 23. Current Sense Using Current Sense Resistor (R1)

Configuration and component selection for current mode control is recommended as follows: The current sense resistor is selected such that during over current condition, the voltage across the current sense resistor is above the minimum CS threshold of 220 mV. It is recommended to set the impedances of R_{Filter} and C_{Filter} as seen from C_{slope} at relatively low values, so that the slope compensation is primarily dictated by R_{slope} and C_{slope} components. For example, if the filtering time (R_{Filter} and C_{Filter}) for leading edge noise is selected for 50 ns and if the value selected for R_{Filter} = 25Ω, then

$$C_{Filter} = \frac{50 \times 10^{-9}}{3 \times 25\Omega} \quad (6)$$

Equation 6 results in a value of C_{Filter} = 680 pF (approximated to a standard value). In general, the amount of slope compensation required to avoid sub-harmonic oscillation is equal to at least one-half the down-slope of the output inductor current, transformed to the primary. To mitigate sub-harmonic oscillation after one switching period, the slope compensation has to be equal to one times the down slope of the filter inductor current transformed to primary. This is known as deadbeat control. For circuits where primary current is sensed using a resistor, the amount of slope compensation for dead-beat control required can be calculated from:

$$\text{Slope-Comp} = \frac{\text{Turns-Ratio} \times \text{Vout} \times R_{CS}}{F_{OSC} \times L_{filter}} \quad (7)$$

where

- turns-ratio is referred with respect to the primary

For example, for a 5-V output converter with a turns ratio between secondary and primary of 1:2, an oscillator frequency (f_{OSC}) of 250 kHz, a filter inductance of 4 µH (L_{Filter}) and a current sense resistor (R_{CS}) of 32 mΩ, slope compensation of 80 mV suffices. The slope compensation "volts" that results from the above expression is the maximum voltage of the artificial ramp added linearly to the RAMP pin till the end of maximum switching period. For circuits where a current sense transformer is used for primary current sensing, the turns-ratio of the current sense transformer has to be taken into account.

C_{slope} should be selected such that it can be fully discharged by the internal RAMP discharge FET. Capacitor values ranging from 100 pF to 1500 pF are recommended. The value must be small enough such that the capacitor can be discharged within the clock (CLK) pulse width each cycle.

Application Information (continued)

R_{slope} can be selected from the following formula:

$$R_{slope} = \frac{-1}{F_{OSC} \times C_{slope} \times \ln\left(1 - \frac{\text{Slope-Comp}}{V_{REF}}\right)} - R_{filter} \quad (8)$$

For example, with a C_{slope} of 1500 pF, F_{OSC} of 250 kHz, reference voltage of 5V (V_{REF}), slope compensation of 80 mV and R_{filter} = 25Ω results in R_{slope} value of 165 kΩ.

8.1.4 UVLO Divider Selection

A dedicated comparator connected to the UVLO pin detects an input under-voltage condition. When the UVLO pin voltage is below 0.45 V, the LM5037 controller is in a low current shutdown mode. For a UVLO pin voltage greater than 0.45 V but less than 1.25 V, the controller is in standby mode with VCC and REF regulators active but no switching. Once the UVLO pin voltage is greater than 1.25 V, the controller is fully enabled. When the UVLO pin voltage rises above the 1.25-V threshold, an internal 22-µA current source as shown in Figure 24, is activated thus providing threshold hysteresis. The 22-µA current source is deactivated when the voltage at the UVLO pin falls below 1.25 V. Use Equation 9 to calculate resistance values for R1 and R2.

$$R_1 = \frac{\left(V_{HYS} - \frac{20 \times 10^{-3} \times V_{PWR}}{1.25}\right)}{22\ \mu A}$$

$$R_2 = \frac{1.25 \times R_1}{V_{PWR} - 1.25}$$

where

- V_{PWR} is the desired turn-on voltage
- V_{HYS} is the desired UVLO hysteresis at V_{PWR} (9)

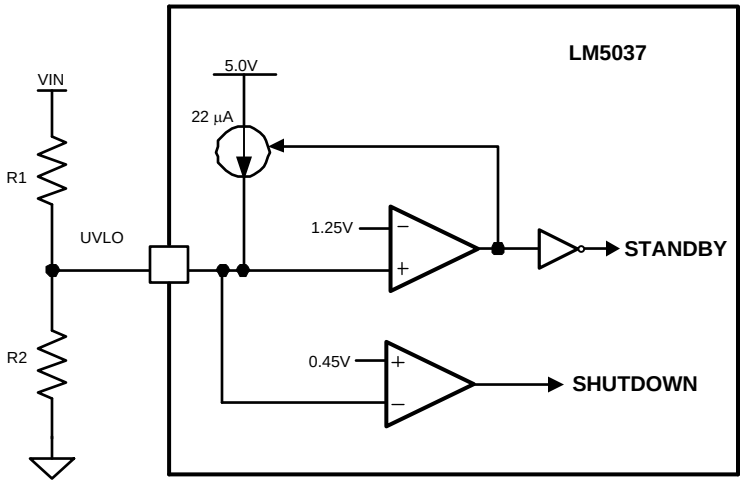


Figure 24. Basic UVLO Configuration

For example, if the device is to be enabled when V_{PWR} reaches 33 V, and disabled when V_{PWR} decreases to 30 V, R1 is 113 kΩ, and R2 is 4.42 kΩ.

CAUTION

Do not allow the voltage at the UVLO pin to exceed 7 V at any time.

Application Information (continued)

Ensure that both the power and voltage ratings are (0603 resistors can be rated as low as 50 V) for the selected R1 resistor. Maintain the UVLO threshold accuracy, by using a resistor tolerance of 1% or better.

Remote control of the LM5037 operational modes can be accomplished with open drain device(s) connected to the UVLO pin as shown in Figure 25.

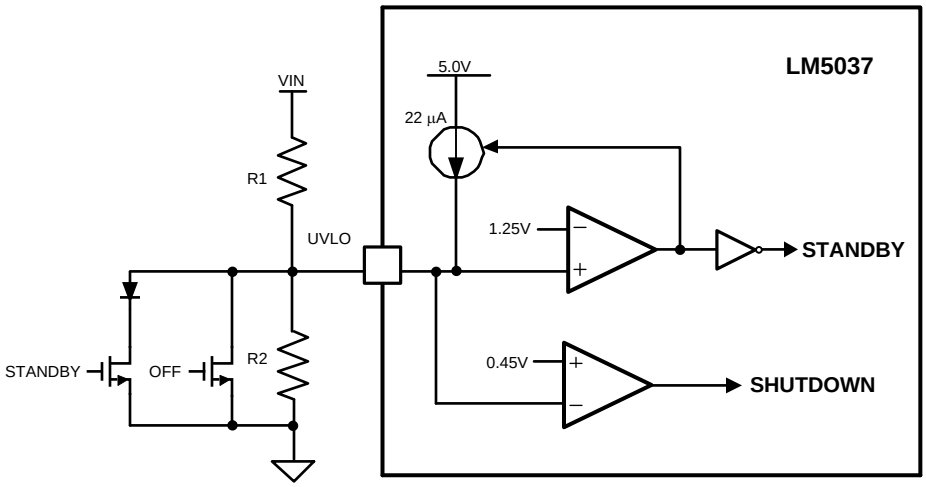


Figure 25. Remote Standby and Disable Control

8.1.5 Hiccup Mode Current Limit Restart (RES Pin)

The basic operation of the hiccup mode current limit is described in the functional description. The delay time to the initiation of a hiccup cycle is programmed by the selection of the RES pin capacitor C_{RES} as illustrated in Figure 26.

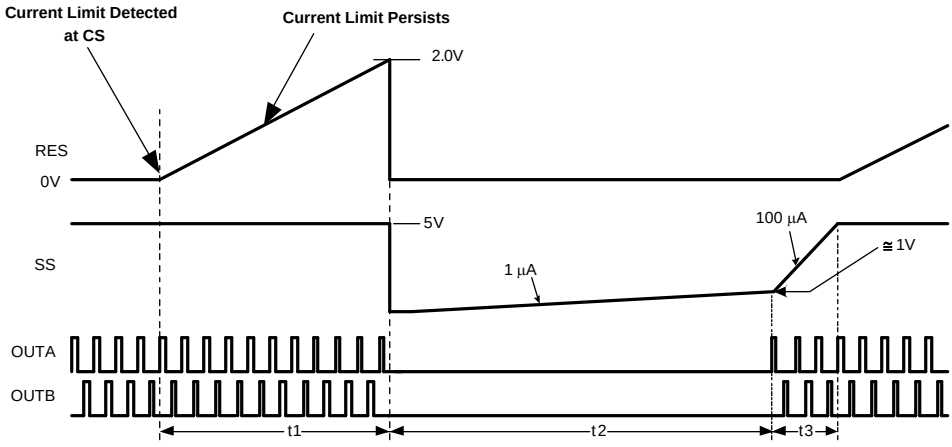


Figure 26. Hiccup Over-Load Restart Timing

In the case of continuous cycle-by-cycle current limit detection at the CS pin, the time required for C_{RES} to reach the 2.0 V hiccup mode threshold is:

$$t1 = \frac{C_{RES} \times 2.0V}{18\ \mu A} = 111K \times C_{RES} \tag{10}$$

For example, if C_{RES} = 0.01 µF the time t1 is approximately 2.0 ms. The cool down time, t2 is set by the soft-start capacitor (C_{SS}) and the internal 1 µA SS current source, and is equal to:

$$t2 = \frac{C_{SS} \times 1V}{1\ \mu A} = 1M \times C_{SS} \tag{11}$$

Application Information (continued)

If C_{SS} = 0.01 µF, t2 is ≅10 ms.

The soft-start time t3 is set by the internal 100 µA current source, and is equal to:

$$t3 = \frac{C_{SS} \times 4V}{100\ \mu A} = 40K \times C_{SS} \quad (12)$$

If C_{SS} = 0.01 µF, t3 is ≅ 400 µs.

The time t2 provides a periodic cool-down time for the power converter in the event of a sustained overload or short circuit. This off time results in lower average input current and lower power dissipation within the power components. It is recommended that the ratio of t2 / (t1 + t3) be in the range of 5 to 10 to take advantage of this feature.

If the application requires no delay from the first detection of a current limit condition to the onset of the hiccup mode (t1 = 0), the RES pin can be left open (no external capacitor). To disable the hiccup mode entirely, connect the RES pin to ground (AGND).

8.2 Typical Application

Figure 27 shows an example of an LM5037-controlled 50-W half-bridge converter. The converter provides a single regulated 5-V output at 10 A, from a standard Telecoms 36-V to 72-V input. The converter is configured for feed-forward voltage-mode control. An auxiliary winding on the power transformer is used to supply the VCC voltage externally, to reduce the power dissipation in the device.

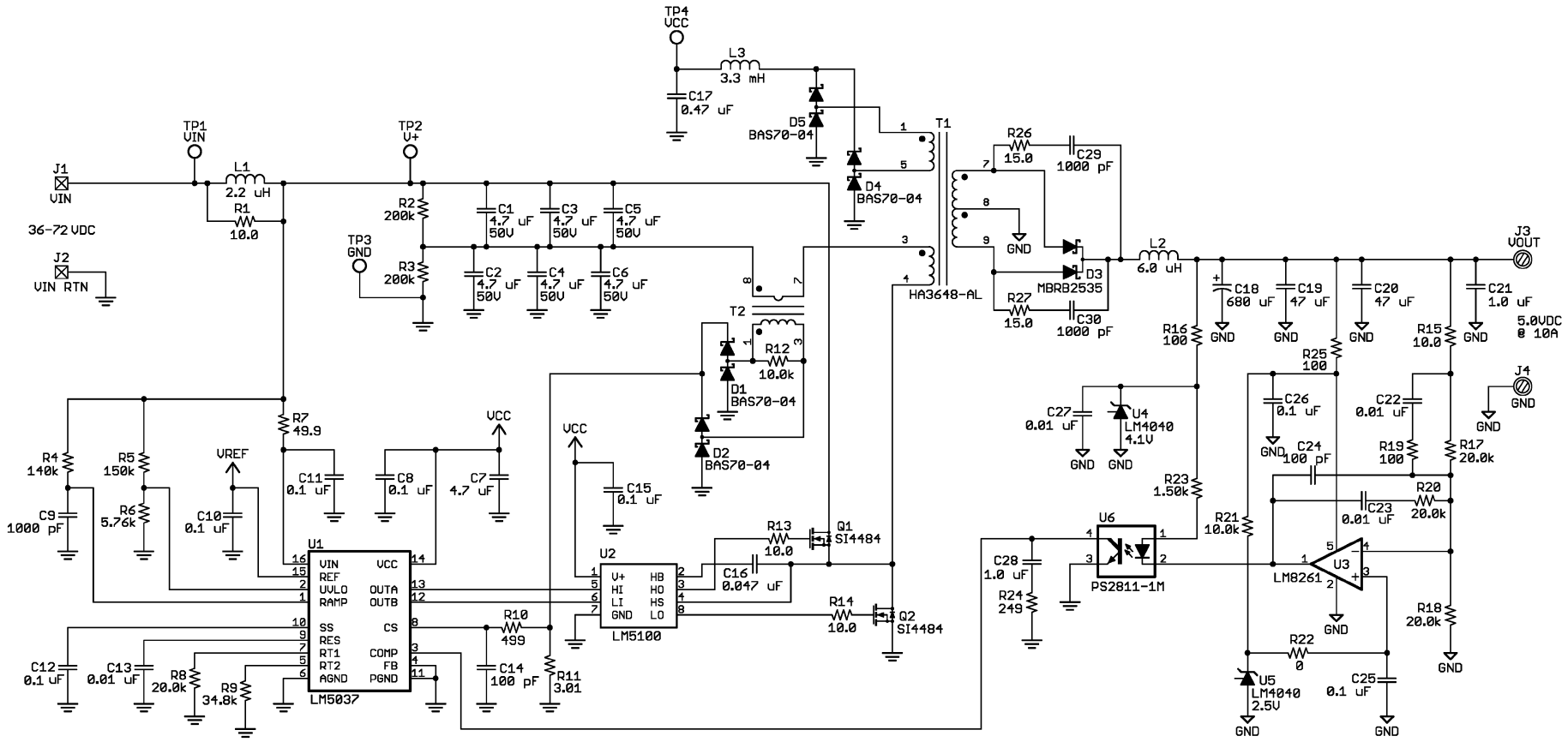


Figure 27. Typical Application Schematic, LM5037

8.2.1 Design Requirements

- Operating input voltage range: 36 V to 72 V
- Output voltage: 5 V
- Output current: 10 A
- UVLO On Level: 34 V On (rising)
- UVLO Off Level: 30 V Off (falling)
- Output ripple voltage, $V_{RIPPLE(OUT)}$: < 2% (960 mV_{P-P})
- Oscillator frequency (2× f_{SW} per phase): 300 kHz
- Switching frequency (f_{SW} per phase): 150 kHz

8.2.2 Detailed Design Procedure

8.2.2.1 Oscillator Frequency and Maximum Duty Cycle

The LM5037 oscillator frequency is twice the switching frequency of each switch in the half-bridge power stage.

$$f_{OSC} = 2 \times f_{SW} \tag{13}$$

Calculate the dead-time resistor value for R_{RT2}. The recommended of dead-time range is between 50 ns and 250 ns. A value of 175 ns is chosen, which sets a maximum duty cycle of approximately 95%. Equation 14 calculates the R_{RT2} resistor value, (R9 in Figure 27) .

$$R_{RT2} = \left(\frac{t_{DEAD}}{5 \times 10^{-12}} \right) = \frac{175 \times 10^{-9}}{5 \times 10^{-12}} = 35\ k\Omega \tag{14}$$

Use the nearest standard E96 value of 34.8 kΩ.

Use the resistor value on the RT2 pin to calculate the required resistor value for the RT1 pin (R8 in Figure 27) using Equation 15.

$$R_{RT1} = \left(\frac{\left(\frac{1}{f_{OSC}} \right) - t_{DEAD}}{0.162 \times 10^{-9}} \right) = \left(\frac{\left(\frac{1}{300 \times 10^{3}} \right) - 175 \times 10^{-9}}{0.162 \times 10^{-9}} \right) = 19.5\ k\Omega \tag{15}$$

Use the nearest E96 value of 20 kΩ.

8.2.2.2 Power Stage Design

As shown in the schematic in Figure 27, the primary components of the half-bridge power stage are:

- Half-bridge splitter capacitors (C1, C2, C3, C4, C5 and C6)
- Power MOSFETs (Q1 and Q2)
- Power transformer (T1)
- Output rectifier (D3)
- Output filter (L2 and C18, C19, and C20)

The half-bridge stage DC input voltage divides evenly across the splitter capacitors, so that one end of the primary-side of the power transformer connects to a DC level of approximately $V_{IN}/2$. The other end of the transformer primary is alternately connected by Q1 to the VIN pin, and then by Q2 to GND, with appropriate dead-time in between. The device modulates the dead-time or duty cycle in order to regulate the output voltage to the required level. Thus the primary winding is subjected to a bi-polar voltage swing of $\pm V_{IN}/2$. This voltage is then scaled by the secondary to primary turns ratio (N_S/N_P). The secondary winding is center-tapped, so that the double-diode, D3 can then full-wave rectify the bi-polar secondary waveform. A uni-polar pulse train occurs at the full f_{OSC} frequency of 300 kHz at the cathode of D3. Output filter inductor L2 and output capacitors C18, C19, C20 then filter this pulse train to a DC output voltage plus AC ripple at the f_{OSC} frequency.

The PWM controller adjusts the duty cycle with input line voltage in order to regulate the output voltage. The maximum duty cycle occurs at minimum operating input voltage, which is approximately 30 V (UVLO turn-off point).

$$D = \left(\frac{2 \times V_{OUT} \times N_P}{V_{IN} \times N_S}\right) = \left(\frac{2 \times 5 \times 2}{30 \times 1}\right) = 67\% \tag{16}$$

Equation 16 shows that there is sufficient tolerance to the oscillator 95% D_{MAX} setting (set by the RT2 resistor value). Use Equation 17 to estimate the peak-to-peak ripple current (I_{P-P}) in continuous conduction mode (CCM) once the duty cycle (D), f_{OSC} frequency and turns ratio, and output inductance (L_{OUT}) are calculated or chosen.

$$\Delta I_{P\_P} = \frac{\left(\left(\frac{V_{IN}}{2} \times \frac{N_S}{N_P}\right) - V_{OUT}\right)}{L_{OUT}} \times \frac{D}{f_{OSC}} = \frac{\left(V_{OUT} - \left(\frac{2 \times {V_{OUT}}^2}{V_{IN}} \times \frac{N_P}{N_S}\right)\right)}{L_{OUT} \times f_{OSC}} = 1.24\ A_{P\_P} \tag{17}$$

8.2.2.3 Half-Bridge MOSFET Driver

Because this application uses half-bridge power stage MOSFETs connected in series between the VIN pin and GND, the Q1 device is high-side or floating. No high-side floating driver or bootstrap circuit which are necessary to drive Q1 exists in this device. Both of the outputs (OUTA and OUTB) are low-side or ground referenced.

This design uses an external high-side and low-side half-bridge driver device (U2, LM5100) to interface between the gate drive outputs and the actual gates of Q1 and Q2. The design requires a bootstrap capacitor (C16) to generate the necessary high-side or floating bias supply for the high-side driver section of the LM5100.

8.2.2.4 UVLO Setting

To ensure start-up at the required minimum system input voltage of 34 V, with the 4 V of hysteresis to the desired turn-off level, calculate the UVLO divider resistors R5 and R6 using Equation 18 and Equation 19.

$$R5 = \left(\frac{V_{HYS} - \left(\frac{20 \times 10^{-3} \times V_{IN}}{1.25}\right)}{22\ \mu A}\right) = \left(\frac{4 - \left(\frac{20 \times 10^{-3} \times 34}{1.25}\right)}{22\ \mu A}\right) = 157.1\ k\Omega \tag{18}$$

Round this calculated value to the more convenient value of 150 kΩ.

$$R6 = \left(\frac{1.25 \times R_{R5}}{V_{IN} - 1.25}\right) = \frac{1.25 \times 150\ k\Omega}{34 - 1.25} = 5.73\ k\Omega \tag{19}$$

Use the nearest standard E96 value of 5.76 kΩ.

8.2.2.5 VIN, VCC, Start-Up

To reduce the power dissipation in the internal start-up regulator on the VIN pin, use a separate external VCC supply. Usually, it is the auxiliary winding on the transformer that derives this external VCC supply. The auxiliary to secondary turns ratio is 2:1, so when the output voltage regulates at 5 V, the auxiliary VCC voltage approximately 10 V. This is sufficiently greater than the maximum internal VCC regulator level of 8 V to back-bias the internal regulator after start-up.

8.2.2.6 Voltage-Mode Ramp Input

Because this design uses voltage-mode control, connect an R-C network from the system input voltage to the RAMP pin, R4 and C9 as shown in Figure 27. Use Equation 5 to calculate the required R-C values. Using a value of 1 nF for C9, and targeting a ramp amplitude of 850 mV at $V_{IN(min)}$ (a good compromise between signal range and noise immunity), Equation 20 calculates the required value R4.

$$R4 = \left(\frac{-1}{f_{OSC} \times C9 \times \ln\left(1 - \frac{V_{RAMP}}{V_{IN(min)}}\right)}\right) = \left(\frac{-1}{300\ k\Omega \times 1\ nF \times \ln\left(1 - \frac{0.85}{36}\right)}\right) = 139.5\ k\Omega \tag{20}$$

Use the nearest E96 value of 140 kΩ.

8.2.2.7 Soft-Start Delay

Use Equation 21 to calculate the time period from soft-start delay to commencement of first PWM switching.

$$t_{SS(dly)} = \left(\frac{1.0\ V \times C12}{100\ \mu A}\right) = \left(\frac{1.0\ V \times 0.1\ \mu F}{100\ \mu A}\right) = 1.0\ ms \tag{21}$$

After the soft-start delay period, the soft-start ramp time depends on the power stage design and the operating conditions (input voltage and output load).

8.2.2.8 Overload Timer

With a timing capacitance of 10 nF on the RES pin (C13), calculate hiccup-mode timing and duty cycle for a sustained over-current condition using Equation 22 and Equation 23. Time period t1 describes the hiccup-mode current-limit persist time and time period t2 describes hiccup-mode cool-down off-time.

$$t1 = \left(\frac{2.0\ V \times C13}{18\ \mu A}\right) = \left(\frac{2.0\ V \times 10\ nF}{18\ \mu A}\right) = 1.11\ ms \tag{22}$$

$$t2 = \left(\frac{1.0\ V \times C12}{1\ \mu A}\right) = \left(\frac{1.0\ V \times \times 100\ nF}{1\ \mu A}\right) = 100\ ms \tag{23}$$

Calculate the hiccup-mode duty cycle using Equation 24.

$$D_{HICCUP} = \frac{t1}{t1 + t2 + t_{SS}} = \frac{1.11}{1.11 + 100 + 1} = 1.09\% \tag{24}$$

8.2.2.9 Current Sense

In order to improve the efficiency, a current sense transformer (T2) is used. This transformer uses a 1:100 step-down ratio. This ratio reduces the power dissipation in the current-sense resistor, R11.

Set the current-limit point after calculating the

- output inductor peak-to-peak ripple current when the device operates in CCM
- the turns ratios of the main transformer (N_S/N_P)
- the turns ratios of the current-sense transformer (CSR)

Using the full load output current of 10 A, and the current limit target of 150%, or 15 A, calculate the required value for R11. The R11 resistance must generate a voltage at the CS pin to equal the internal cycle-by-cycle limit of nominally 0.25 V at the current limit level at the output.

$$R11 = \frac{0.25\ V}{\left(I_{ILIM} + \frac{\Delta I}{2}\right) \times \frac{N_S}{N_P} \times \frac{1}{CSR}} = \frac{0.25\ V}{\left(15 + \frac{1.24}{2}\right) \times \frac{1}{2} \times \frac{1}{100}} = 3.2\ \Omega \tag{25}$$

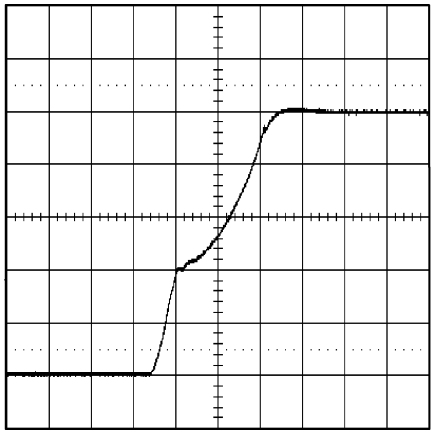
Round the calculated R11 resistance to a standard 3 Ω. If the power stage operates heavily in CCM, the output inductor ripple component can be ignored to yield a good first-order approximation to the required value.

8.2.2.10 Output Voltage Feedback

Because the output of the DC-DC converter is isolated from the input, this design uses a secondary-side reference (U5) and error amplifier (U3). The output of the error amplifier, U3 represents the required demand level to maintain regulation as a function of output load and input line. The design couples the demand signal across the isolation barrier to the primary through opto-coupler, U6.

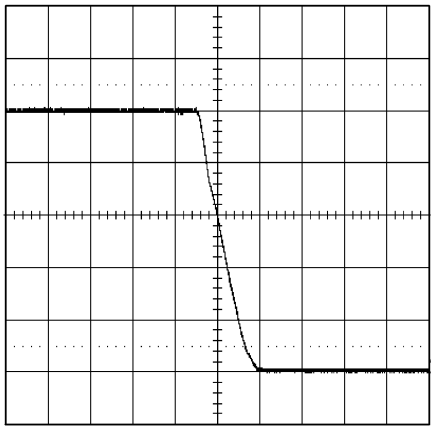
Because the error amplifier and reference reside on the secondary side, this design disregards the internal reference and error amplifier features of the LM5037 device. The FB pin of the LM5037 device is connected to GND, which forces the COMP pin to pull up to approximately 5 V through the internal 5-kΩ pull-up resistance. The opto-coupler, U6 then externally pulls down on the COMP pin to set the required level to achieve the required duty cycle at any given load or line level.

8.2.3 Application Curves



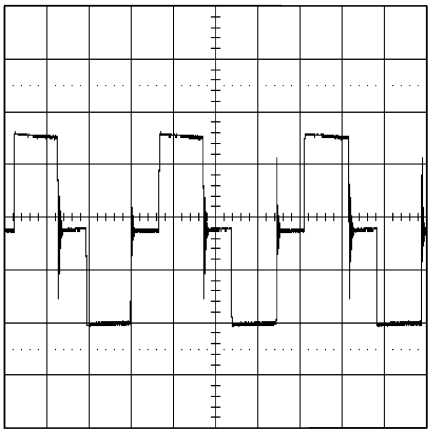
V_{IN} = 48 Vdc 1 V/div
I_{OUT} = 10 A Time = 1 ms/div

Figure 28. Output Voltage During Soft-Start Period



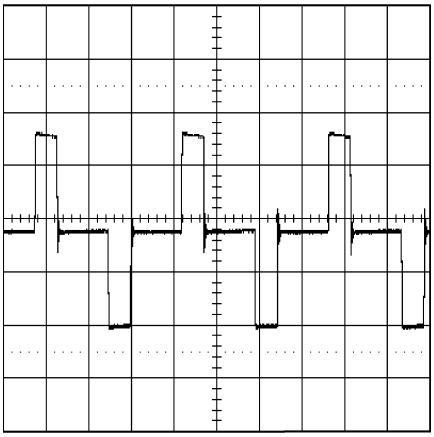
V_{IN} = 48 Vdc V/div = 1 V
Time = 1 µs/div

Figure 29. Output Voltage During Soft-Stop Period



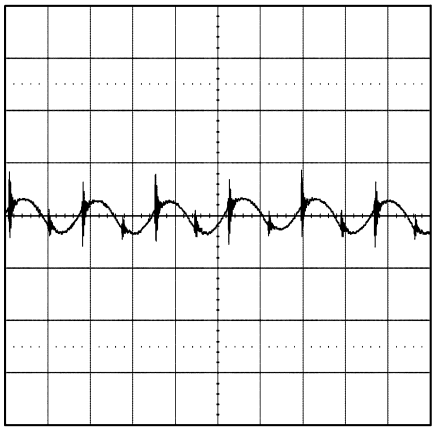
V_{IN} = 36 Vdc V/div = 10 V
I_{OUT} = 10 A Time = 2 µs/div

Figure 30. Drain Waveform of Q2



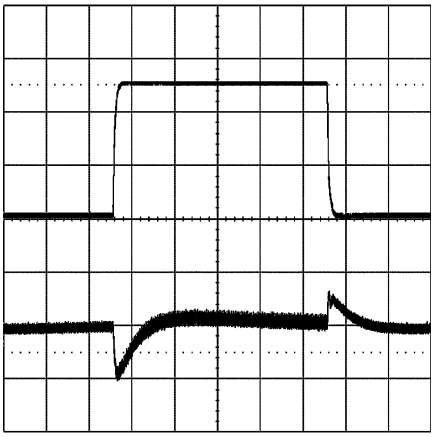
V_{IN} = 72 Vdc V/div = 20 V
I_{OUT} = 10 A Time = 2 µs/div

Figure 31. Drain Waveform of Q2



V_{IN} = 48 Vdc
I_{OUT} = 10 A
Bandwidth Limit = 20 MHz
$V_{OUT(P-P)}$, 50 mV/div
Time = 5 µs/div

Figure 32. Output Ripple



V_{IN} = 48 Vdc
I_{OUT} Step, 5 A to 10 A
Time = 200 µs/div
Top Trace: I_{OUT} Step, 5 A to 10 A
Bottom Trace: V_{OUT}, 100 mV/div
Bandwidth Limit = 20 MHz

Figure 33. Transient Response

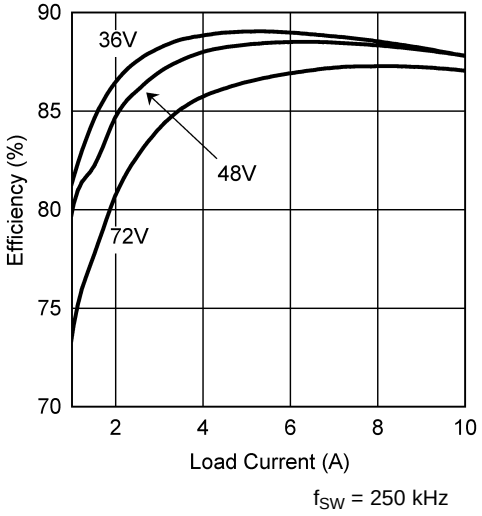


Figure 34. Efficiency vs. Load Current

9 Power Supply Recommendations

The VCC pin requires a local decoupling capacitor that is connected to GND. This capacitor ensures stability of the internal regulator from the VIN pin. The decoupling capacitor also provides the current pulses to drive the gates of the external MOSFETs through the driver output pins. Place the decoupling capacitor close to the VCC and PGND pins and track it directly to those pins.

The two ground pins (PGND and AGND) must be connected together with a short, direct PCB connection.

10 Layout

10.1 Layout Guidelines

The LM5037 device current sense and PWM comparators are very fast, and respond to short duration noise pulses. Place components for the CS, COMP, SS, UVLO, RT2 and the RT1/SYNC pins as physically close as possible to the device. This placement minimizes noise pickup on the PC board trace inductances.

Layout considerations are critical for the current sense filter. If a current sense transformer is used, both leads of the transformer secondary should be routed to the sense filter components and to the device pins. The ground side of the transformer should be connected via a dedicated PC board trace to the AGND pin, rather than through the ground plane.

If the current sense circuit employs a sense resistor in the drive transistor source, low inductance resistors should be used. In this case, all the noise sensitive, low-current ground trace should be connected in common near the device, and then a single connection made to the power ground (sense resistor ground point).

While employing current mode control, RAMP pin capacitor and CS pin capacitor must be placed close to the device. Also, a short direct trace should be employed to connect RAMP capacitor to the CS pin.

The gate drive outputs of the device should have short, direct paths to the power MOSFETs in order to minimize inductance in the PC board The two ground pins (AGND, PGND) must be connected together with a short, direct connection, to avoid jitter due to relative ground bounce.

If the internal dissipation of the device produces high junction temperatures during normal operation, the use of multiple vias under the device to a ground plane can help conduct heat away from the device. Judicious positioning of the PC board within the end product, along with use of any available air flow (forced or natural convection) helps reduce the junction temperatures. If using forced air cooling, avoid placing the device in the airflow shadow of tall components, such as input capacitors.

10.2 Layout Example

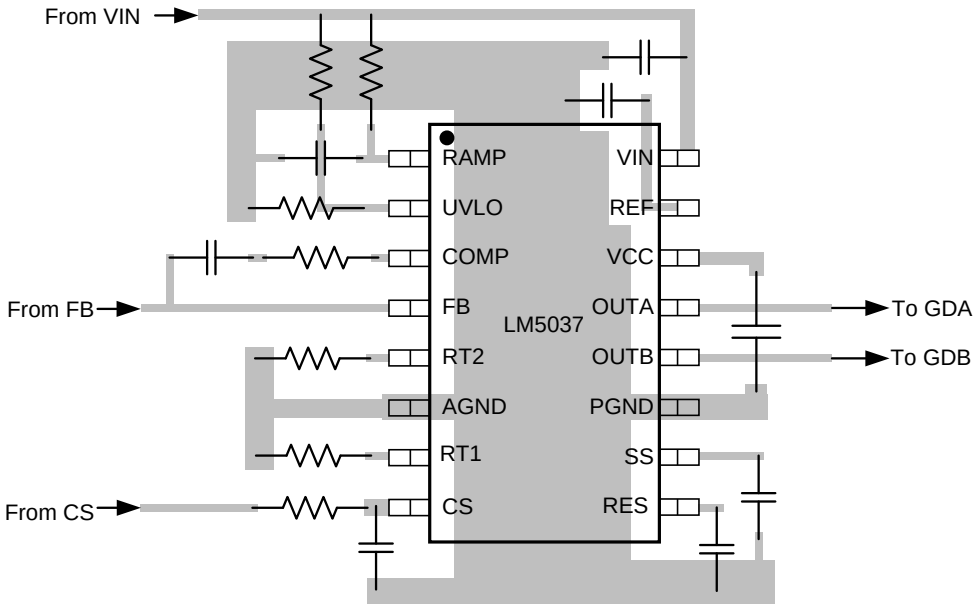


Figure 35. LM5037 Board Layout

11 Device and Documentation Support

11.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.2 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM5037MT/NOPB	LIFEBUY	TSSOP	PW	16	92	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LM5037 MT	
LM5037MTX/NOPB	LIFEBUY	TSSOP	PW	16	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LM5037 MT	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

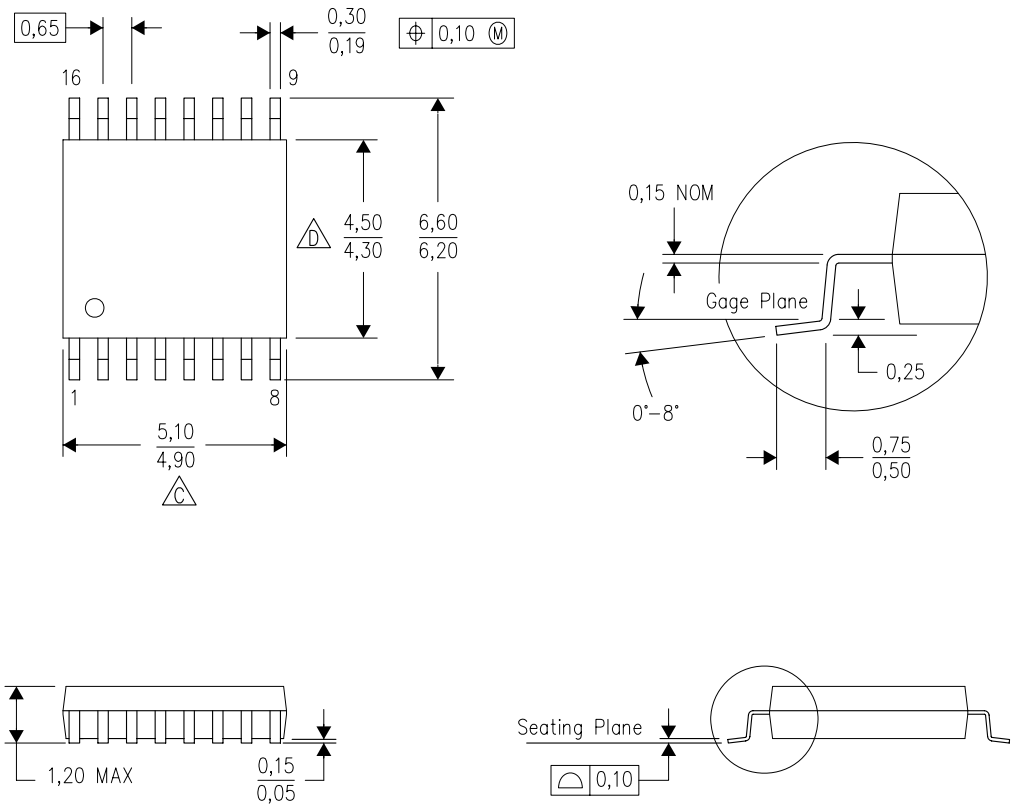
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

PW (R–PDSO–G16) PLASTIC SMALL OUTLINE



4040064–4/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

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