THE DATASHEET OF

LM5088QMHX-2/NOPB

LM5088, LM5088-Q1 Wide Input Range Non-Synchronous Buck Controller

1 Features

- LM5088-Q1 is an Automotive Grade Product that is AEC-Q100 Grade 1 Qualified (-40°C to +125°C Operating Junction Temperature)
- Emulated Current Mode Control
- Drives External High-Side N-channel MOSFET
- Ultra-Wide Input Voltage Range from 4.5V to 75V
- Low I_Q Shutdown and Standby Modes
- High Duty Cycle Ratio Feature for Reduced Dropout Voltage
- Spread Spectrum EMI Reduction (LM5088-1)
- Hiccup Timer for Overload Protection (LM5088-2)
- Adjustable Output Voltage from 1.205 V with 1.5% Feedback Reference Accuracy
- Wide Bandwidth Error Amplifier
- Single Resistor Oscillator Frequency Setting
- Oscillator Synchronization Capability
- Programmable Soft-Start
- High Voltage, Low Dropout Bias Regulator
- Thermal Shutdown Protection
- Package: HTSSOP (16 Pin)

2 Applications

- Automotive Infotainment
- Automotive USB Accessory Adapters
- Industrial DC-DC Bias and Motor Drivers

3 Description

The LM5088 high voltage non-synchronous buck controller features all the necessary functions to implement an efficient high voltage buck converter using a minimum number of external components. The LM5088 can be configured to operate over an ultra-wide input voltage range of 4.5 V to 75 V. This easy to use controller includes a level shifted gate driver capable of controlling an external N-channel buck switch. The control method is based upon peak current mode control utilizing an emulated current ramp. The use of an emulated control ramp reduces noise sensitivity of the pulse-width modulation circuit, allowing reliable control of very small duty cycles necessary in high input voltage/low output voltage applications. The LM5088 switching frequency is programmable from 50 kHz to 1 MHz.

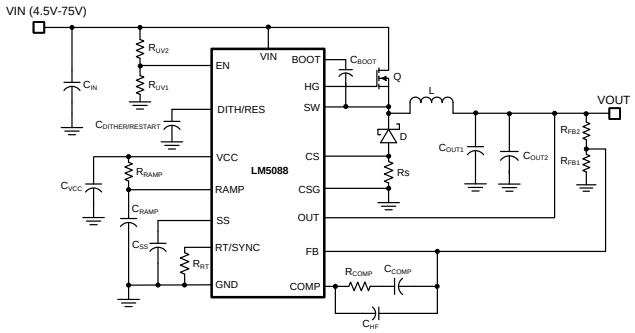
The LM5088 is available in two versions: The LM5088-1 provides a +/-5% frequency dithering function to reduce the conducted and radiated EMI, while the LM5088-2 provides a versatile restart timer for overload protection. Additional features include a low dropout bias regulator, tri-level enable input to control shutdown and standby modes, soft-start and oscillator synchronization capability. The device is available in a thermally enhanced HTSSOP-16 pin package.

Device Information(1)

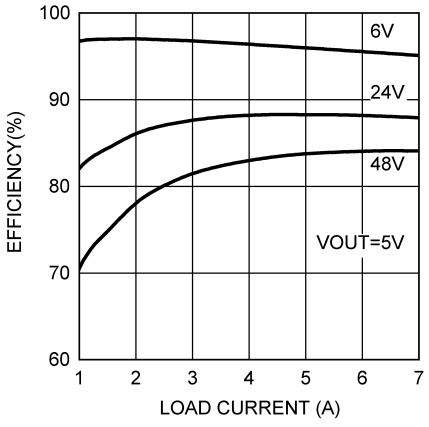
PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM5088	HTSSOP (16)	5.00 mm × 4.00 mm
LM5088-Q1	HTSSOP (16)	5.00 mm × 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

4 Simplified Schematic



Typical Application Circuit Efficiency



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5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision H (March 2013) to Revision I — **Page**

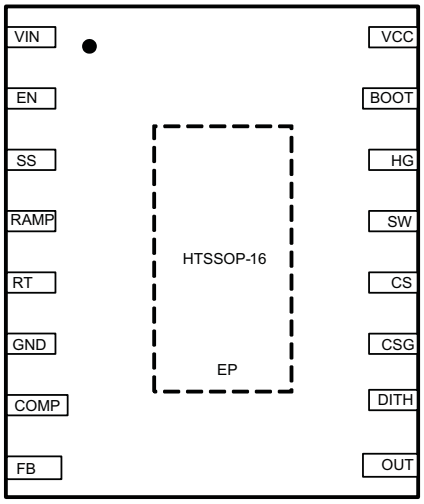
- Changed data sheet flow and layout to conform with new TI standards. Added the following sections: Device Information Table, Application and Implementation; Power Supply Recommendations; Layout; Device and Documentation Support; Mechanical, Packaging, and Ordering Information ... 1
- Changed "x" to "-" ... 13
- Added unit "kΩ" ... 20
- Deleted "/A" in the numerator of Equation 11 ... 22

Changes from Revision G (March 2013) to Revision H — **Page**

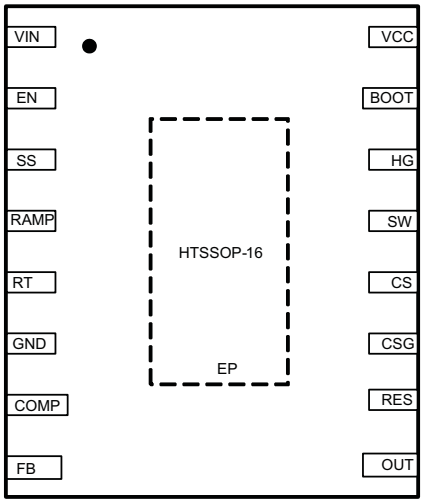
- Changed layout of data sheet from National to TI format ... 1

6 Pin Configuration and Functions

16-Pin (Dither Version)
PWP Package
Top View



16-Pin (Restart Version)
PWP Package
Top View



Pin Descriptions

PIN		DESCRIPTION	APPLICATION INFORMATION
NUMBER	NAME		
1	VIN	Input supply voltage	IC supply voltage. The operating range is 4.5 V to 75 V
2	EN	Enable input	If the EN pin voltage is below 0.4V the regulator will be in a low power state. If the EN pin voltage is between 0.4V and 1.2V the controller will be in standby mode. If the EN pin voltage is above 1.2 V the controller will be operational. An external voltage divider can be used to set a line under voltage shutdown threshold. If the EN pin is left open, a 5µA pull-up current forces the pin to the high state and enables the controller.
3	SS	Soft-start	When SS is below the internal 1.2V reference, the SS voltage will control the error amplifier. An internal 11 µA current source charges an external capacitor to set the start-up rate of the controller. The SS pin is held low in the standby, VCC UV and thermal shutdown states. The SS pin can be used for voltage tracking by connecting this pin to a master voltage supply less than 1.2 V. The applied voltage will act as the reference for the error amplifier.
4	RAMP	Ramp control signal	An external capacitor connected between this pin and the GND pin sets the ramp slope used for emulated current mode control. Recommended capacitor range 100 pF to 2000 pF. See the *Application and Implementation* section for selection of capacitor value.
5	RT/SYNC	Internal oscillator frequency set input and synchronization input	The internal oscillator is programmed with a single resistor between this pin and the GND pin. The recommended frequency range is 50 kHz to 1 MHz. An external synchronization signal, which is higher in frequency than the programmed frequency, can be applied to this pin through a small coupling capacitor. The RT resistor to ground is required even when using external synchronization.
6	GND	Ground	Ground return.
7	COMP	Output of the internal error amplifier	The loop compensation network should be connected between this pin and the FB pin.
8	FB	Feedback signal from the regulated output	This pin is connected to the inverting input of the internal error amplifier. The regulation threshold is 1.205V.
9	OUT	Output voltage connection	Connect directly to the regulated output voltage.
10	DITH	Frequency Dithering (LM5088-1 Only)	A capacitor connected between DITH pin and GND is charged and discharged by 27 µA current sources. As the voltage on the DITH pin ramps up and down, the oscillator frequency is modulated between -5% to +5% of the nominal frequency set by the RT resistor. Grounding the DITH pin will disable the frequency dithering mode.
10	RES	Hiccup Mode Restart (LM5088-2 Only)	The RES pin is normally connected to an external capacitor that sets the timing for hiccup mode current limiting. In normal operation, a 25µA current source discharges the RES pin capacitor to ground. If cycle-by-cycle current limit threshold is exceeded during any PWM cycle, the current sink is disabled and RES capacitor is charged by an internal 50 µA current. If the RES voltage reaches 1.2 V, the HG pin gate drive signal will be disabled and the RES pin capacitor will be discharged by a 1 µA current sink. Normal operation will resume when the RES pin falls below 0.2 V.
11	CSG	Current Sense Ground	Low side reference for the current sense resistor.
12	CS	Current sense	Current measurement connection for the re-circulating diode. An external sense resistor and an internal sample/hold circuit sense the diode current at the conclusion of the buck switch off-time. This current measurement provides the DC offset level for the emulated current ramp.
13	SW	Switching node	Connect to the source terminal of the external MOSFET switch.
14	HG	High Gate	Connect to the gate terminal of the external MOSFET switch.
15	BOOT	Input for bootstrap capacitor	An external capacitor is required between the BOOT and the SW pins to provide bias to the MOSFET gate driver. The capacitor is charged from VCC via an internal diode during the off-time of the buck switch.
16	VCC	Output of the bias regulator	VCC tracks VIN up to the regulation level (7.8 V Typ). A 0.1 µF to 10 µF ceramic decoupling capacitor is required. An external voltage between 8.3 V and 13 V can be applied to this pin to reduce internal power dissipation.

7 Specifications

7.1 Absolute Maximum Ratings(1)(2)

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
VIN, VOUT to GND		76	V
BOOT to GND		90	V
SW to GND	–2	76	V
VCC to GND	–0.3	16	V
HG to SW	–0.3	BOOT+0.3	V
EN to GND		14	V
BOOT to SW	–0.3	16	V
CS, CSG to GND	–0.3	0.3	V
All other inputs to GND	–0.3	7	V
Junction Temperature		+ 150	°C

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

7.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		–65	+ 150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)(2)		2	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) The human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin.

7.3 Recommended Operating Conditions(1)

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
VIN Voltage	4.5	75	V
VCC Voltage (externally supplied)	8.3	13	V
Operation Junction Temperature	–40	+125	°C

(1) Operating Ratings are conditions under which operation of the device is intended to be functional. For specified performance limits and associated test conditions, see the Electrical Characteristics.

7.4 Thermal Information

THERMAL METRIC(1)		LM5088(Q1) PWP 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	40	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	6	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics[1][2]

PARAMETER		TEST CONDITIONS	T_J = -40°C to +125°C.			T_J = 25°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
VIN SUPPLY									
I_{BIAS}	VIN Operating Current	V_{FB} = 1.3V			5.5		3.8		mA
$I_{STANDBY}$	VIN Standby Current	V_{EN} = 1V			3.6		2.9		mA
$I_{SHUTDOWN}$	VIN Shutdown Current	V_{EN} = 0V			26		15		µA
VCC REGULATOR									
$V_{VCC(Reg)}$	VCC Regulation	V_{VCC} = open	7.4		8.2		7.8		V
$V_{VCC(Reg)}$	VCC Regulation	V_{VIN} = 4.5V,VVCC=open	4.3		4.5				V
	VCC Sourcing Current Limit	V_{VCC} = 0	30				35		mA
$V_{VCC(UV)}$	VCC Under-Voltage Lockout Threshold	Positive going VVCC	3.7		4.2		4		V
	VCC Under-Voltage Hysteresis						200		mV
ENABLE THRESHOLDS									
	EN Shutdown Threshold	V_{EN} Rising	320		480		400		mV
	EN Shutdown Hysteresis	V_{EN} Falling					100		mV
	EN Standby Threshold	V_{EN} Rising	1.1		1.3		1.2		V
	EN Standby Hysteresis	V_{EN} Falling					120		mV
	EN Pull-up Current Source	V_{EN} = 0V					5		µA
SOFT- START									
	SS Pull-up Current Source	V_{SS} = 0V	8		13		11		µA
	FB to SS Offset	V_{FB} = 1.3V					150		mV
ERROR AMPLIFIER									
V_{REF}	FB Reference Voltage	Measured at FB Pin FB = COMP	1.187		1.223		1.205		V
	FB Input Bias Current	V_{FB} = 1.2V			100		18		nA
	COMP Sink/Source Current		3						mA
AOL	DC Gain						60		dB
FBW	Unity gain bandwidth						3		MHz
PWM COMPARATORS									
$T_{HG(OFF)}$	Forced HG Off-time		185		365		280		ns
$T_{ON(MIN)}$	Minimum HG On-time	V_{VIN} = 60V					55		ns
	COMP to PWM comparator offset						930		mV
OSCILLATOR (RT Pin)									
		LM5088-2 (Non-Dithering)							
F_{nom1}	Nominal Oscillator Frequency	R_{RT} = 31.6 kΩ	180		220		200		kHz
F_{nom2}		R_{RT} = 11.3 kΩ	430		565		500		kHz
		LM5088-1 (Dithering)							
F_{min}	Dithering Range	Minimum Dither Frequency					F_{nom}- 5%		kHz
F_{max}		Maximum Dither Frequency					F_{nom} +5%		kHz
SYNC									
	SYNC positive threshold						2.3		V
	SYNC Pulse Width		15		150				ns

(1) Typical specifications represent the most likely parametric norm at 25°C operation.
(2) Minimum and Maximum limits are specified through test, design, or statistical correlation. Typical values represent at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: V_{VIN} = 48V, V_{VCC}= 8V, V_{EN} = 5V R_{RT} = 31.6 kΩ, No load on HG.

Electrical Characteristics[1][2] (continued)

PARAMETER		TEST CONDITIONS	T_J = -40°C to +125°C.			T_J = 25°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
CURRENT LIMIT									
$V_{CS(TH)}$	Cycle by cycle sense voltage threshold	V_{RAMP} = 0V	112		136		120		mV
	Cycle by Cycle Current Limit Delay	V_{RAMP} = 2.5V					280		ns
	Buck Switch VDS protection	VIN to SW					1.5		V
CURRENT LIMIT RESTART (RES Pin)									
V_{resup}	RES Threshold Upper (rising)	V_{CS} = 0.125	1.1		1.3		1.2		V
$V_{resdown}$	RES Threshold Lower (falling)		0.1		0.3		0.2		V
I_{charge}	Charge source current	V_{CS} >= 0.125	40		65		50		µA
$I_{discharge}$	Discharge sink current	V_{CS} < 0.125	20		34		27		µA
$I_{rampdown}$	Discharge sink current -(post fault)		0.8		1.6		1.2		µA
RAMP GENERATOR[3]									
I_{RAMP1}	RAMP Current 1	V_{VIN} = 60V, V_{OUT} = 10V	235		345		295		µA
I_{RAMP2}	RAMP Current 2	V_{VIN} = 10V, V_{OUT} = 10V	18		30		25		µA
	VOUT Bias Current	V_{OUT} = 48V					250		µA
	RAMP Output Low Voltage	V_{VIN} = 60V, V_{OUT} = 10V					200		mV
HIGH SIDE (HG) GATE DRIVER									
V_{OLH}	HG Low-state Output Voltage	I_{HG} = 100 mA			215		115		mV
V_{OHH}	HG High-state Output Voltage	I_{HG} = -100 mA, V_{OHH} = V_{BOOT} - V_{HG}					240		mV
	HG Rise Time	C_{load} = 1000 pF					12		ns
	HG Fall Time	C_{load} = 1000 pF					6		ns
I_{OHH}	Peak HG Source Current	V_{HG} = 0V					1.5		A
I_{OLH}	Peak HG Sink Current	V_{HG} = V_{VCC}					2		A
	BOOT UVLO	BOOT to SW					3		V
Pre $R_{DS(ON)}$	Pre-Charge Switch ON- resistance	I_{VCC} = 1 mA					72		Ω
	Pre-Charge switch ON time						300		ns
THERMAL[4]									
T_{SD}	Thermal Shutdown Temperature	Junction Temperature Rising					165		°C
	Thermal Shutdown Hysterisis	Junction Temperature Falling					25		°C

(3) RAMP and COMP are output pins. As such they are not specified to have an external voltage applied.
(4) For detailed information on soldering plastic HTSSOP packages visit www.ti.com/packaging.

7.6 Typical Characteristics

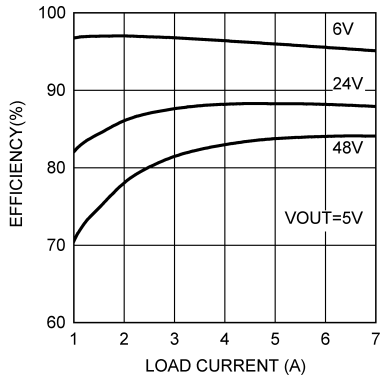


Figure 1. Typical Application Circuit Efficiency

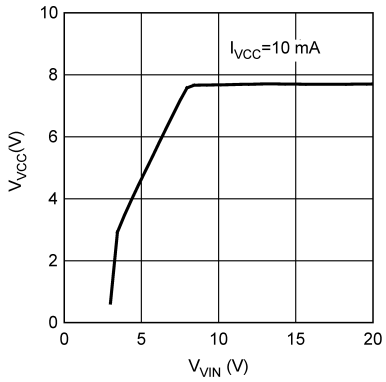


Figure 2. V_{CC} vs V_{IN}

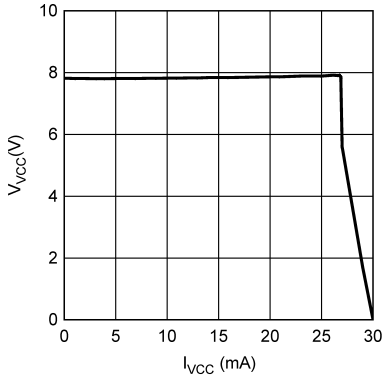


Figure 3. V_{VCC} vs I_{VCC}

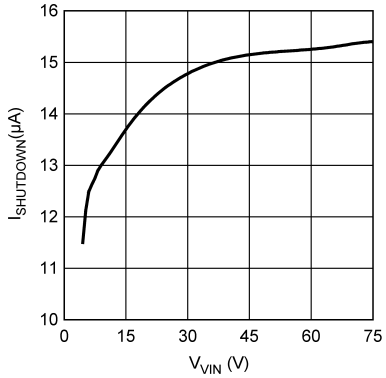


Figure 4. Shutdown Current

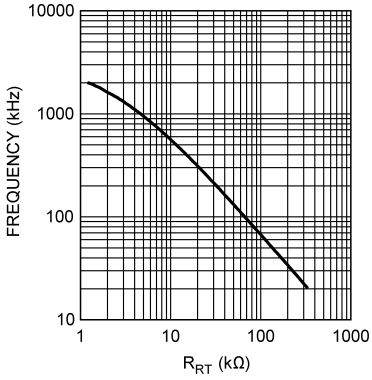


Figure 5. Frequency vs R_{RT}

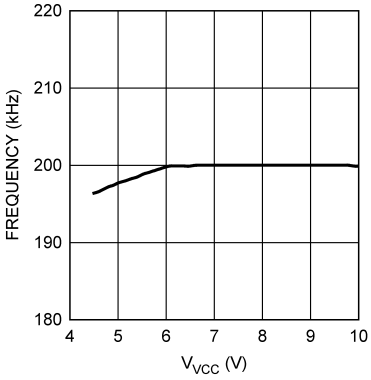


Figure 6. Frequency vs V_{VCC}

Typical Characteristics (continued)

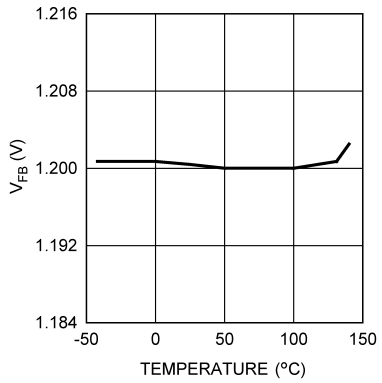


Figure 7. V_{FB} vs Temperature

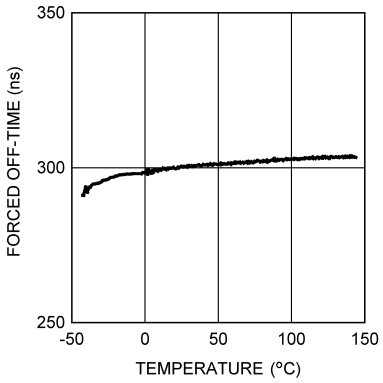


Figure 8. Forced-Off Time vs Temperature

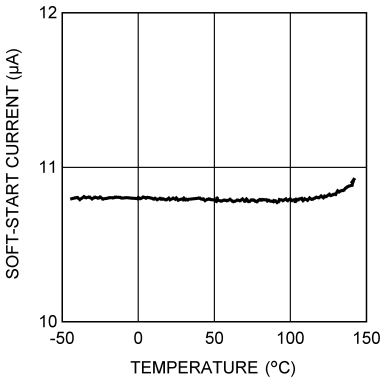


Figure 9. Soft-Start vs Temperature

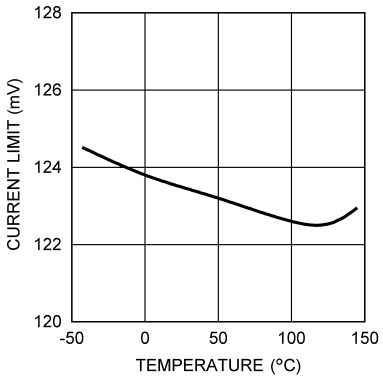


Figure 10. Current-Limit vs Temperature

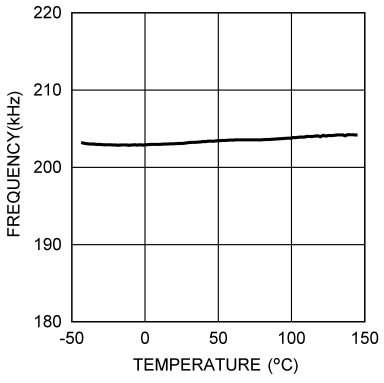


Figure 11. Frequency vs Temperature

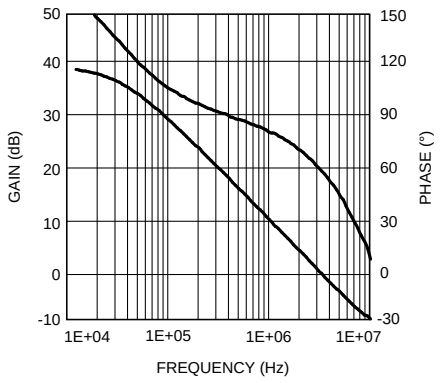


Figure 12. Error Amplifier Gain/Phase

8 Detailed Description

8.1 Overview

The LM5088 Wide Input Range Buck Controller features all the functions necessary to implement an efficient high voltage step-down converter using a minimum number of external components. The control method is based on peak current mode control utilizing an emulated current ramp. Peak current mode control provides inherent line voltage feed-forward, cycle-by-cycle current limiting and ease of loop compensation. The use of an emulated control ramp reduces noise sensitivity of the pulse-width modulation circuit, allowing reliable processing of very small duty cycles necessary in high input voltage applications. The operating frequency is user programmable from 50 kHz to 1 MHz. The LM5088-1 provides a ±5% frequency dithering function to reduce the conducted and radiated EMI, while the LM5088-2 provides a versatile restart timer for overload protection. Additional features include the low dropout bias regulator, tri-level enable input to control shutdown and standby modes, soft-start, and voltage tracking and oscillator synchronization capability. The device is available in a thermally enhanced HTSSOP-16 pin package.

See Figure 13 and Figure 27. The LM5088 is well suited for a wide range of applications where efficient step-down of high, unregulated input voltage is required. The LM5088's typical applications include Telecom, Industrial and Automotive.

8.2 Functional Block Diagram

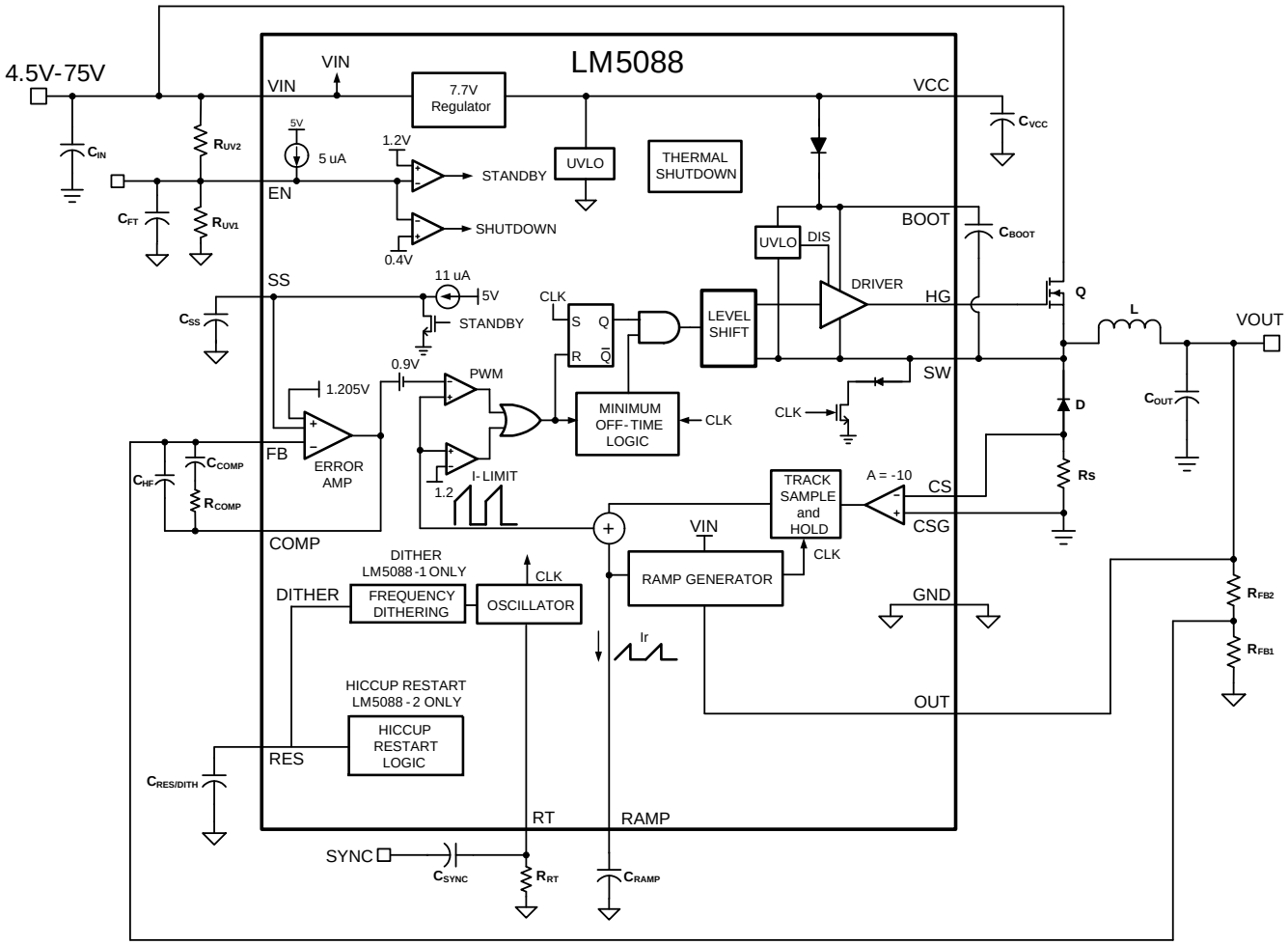


Figure 13. LM5088 Functional Block Diagram

8.3 Feature Description

8.3.1 High Voltage Low-Dropout Regulator

The LM5088 contains a high voltage, low-dropout regulator that provides the VCC bias supply for the controller and the bootstrap MOSFET gate driver. The input pin (VIN) can be connected directly to an input voltage as high as 75V. The output of the VCC regulator (7.8V) is internally current limited to 30 mA. Upon power up, the regulator sources current into the capacitor connected to the VCC pin. When the voltage at the VCC pin exceeds the upper VCC UV threshold of 4.0V and the EN pin is greater than 1.2 Volts, the output (HG) is enabled and a soft-start sequence begins. The output is terminated if VCC falls below its lower UV threshold (3.8V) or the EN pin falls below 1.1V. When VIN is less than VCC regulation point of 7.8V, then the internal pass device acts as a switch. Thereby, VCC tracks VIN with a voltage drop determined by the $R_{DS(ON)}$ of the internal switch and operating current of the controller. The required VCC capacitor value is dependant on system startup characteristics with a minimum value no less than 0.1 µF.

An auxiliary supply voltage can be applied to the VCC pin to reduce the IC power dissipation. If the auxiliary voltage is greater than 8.2V, the internal regulator will be disabled. The VCC regulator series pass transistor includes a diode between VCC and VIN that should not be forward biased in normal operation.

In high voltage applications, additional care should be taken to ensure that the VIN pin does not exceed the absolute maximum voltage rating of 76V. During line or load transients, voltage ringing on the VIN pin that exceeds the absolute maximum ratings may damage the IC. Both careful PC board layout and the use of high quality bypass capacitors located close to the VIN and GND pins are essential.

8.3.2 Line Under-Voltage Detector

The LM5088 contains a dual level under-voltage lockout (UVLO) circuit. When the EN pin is below 0.4V, the controller is in a low current shutdown mode. When the EN pin is greater than 0.4V but less than 1.2V, the controller is in a standby mode. In standby mode the VCC regulator is active but the output switch is disabled and the SS pin is held low. When the EN pin exceeds 1.2V and VCC exceeds the VCC UV threshold, the SS pin and the output switch is enabled and normal operation begins. An internal 5 µA pull-up current source at the EN pin configures the controller to be fully operational if the EN pin is left open.

An external VIN UVLO set-point voltage divider from VIN to GND can be used to set the minimum startup input voltage of the controller. The divider must be designed such that the voltage at the EN pin exceeds 1.2V (typ) when VIN is in the desired operating range. The internal 5 µA pull-up current source must be included in calculations of the external set-point divider. 100 mV of hysteresis is included for both the shutdown and standby thresholds. The EN pin is internally connected to a 1 kΩ resistor and an 8V zener clamp. If the voltage at the EN pin exceeds 8V, the bias current for the EN pin will increase at the rate of 1mA/V. The voltage at the EN pin should never exceed 14V.

8.3.3 Oscillator and Sync Capability

The LM5088 oscillator frequency is set by a single external resistor connected between the RT pin and the GND pin. The R_T resistor should be located very close to the device. To set a desired oscillator frequency (f_{SW}), the necessary value of R_T resistor can be calculated from the following equation:

$$R_{RT} = \frac{\frac{1}{f_{SW}} - 280\ ns}{152\ pF} \quad (1)$$

The RT pin can also be used to synchronize the internal oscillator to an external clock. The internal oscillator is synchronized to an external clock by AC coupling a positive edge into the RT/SYNC pin. The RT/SYNC pin voltage must exceed 3V to trip the internal clock synchronization pulse detector. The free-running frequency should be set nominally 15% below the external clock frequency and the pulse width applied to the RT/SYNC pin must be less than 150ns. Synchronization to an external clock more than twice the free-running frequency can produce abnormal behavior of the pulse-width modulator.

Feature Description (continued)

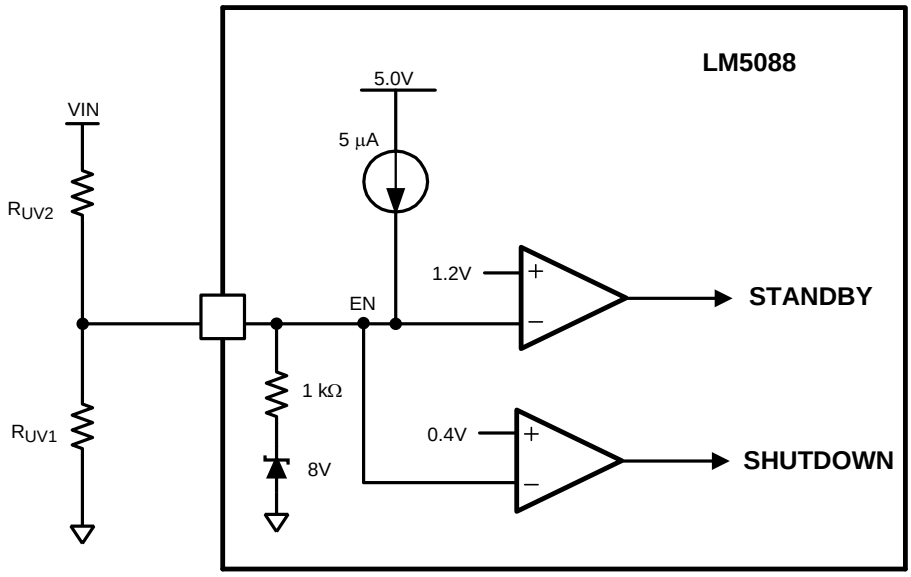


Figure 14. Basic Enable Configuration

8.3.4 Error Amplifier and PWM Comparator

The internal high gain error amplifier generates an error signal proportional to the difference between the regulated output voltage and an internal precision voltage reference (1.205V). The output of the error amplifier is connected to the COMP pin allowing the user to connect loop compensation components. Generally a type II network, as illustrated in the *Figure 13* , is sufficient. This network creates a pole at DC, a mid-band zero for phase boost and a high frequency pole for noise reduction. The PWM comparator compares the emulated current signal from the RAMP generator to the error amplifier output voltage at the COMP pin. A typical control loop gain/phase plot is shown in *Typical Characteristics*.

8.3.5 Ramp Generator

The ramp signal used for the pulse width modulator in current mode control is typically derived directly from the buck switch current. This signal corresponds to the positive slope portion of the buck inductor current. Using this signal for the PWM ramp simplifies the control loop transfer function to a single pole response and provides inherent input voltage feed-forward compensation. The disadvantage of using the buck switch current signal for PWM control is the large leading edge spike due to circuit parasitics which must be filtered or blanked. Also, the current measurement may introduce significant propagation delays. The filtering time, blanking time and propagation delay limit the minimum achievable pulse width. In applications where the input voltage may be relatively large in comparison to the output voltage, controlling small pulse widths and duty cycles is necessary for regulation. The LM5088 utilizes a unique ramp generator which does not actually measure the buck switch current but rather reconstructs or emulates the signal. Emulating the inductor current provides a ramp signal that is free of leading edge spikes and measurement or filtering delays. The current reconstruction is comprised of two elements; a sample & hold DC level and an emulated current ramp.

Feature Description (continued)

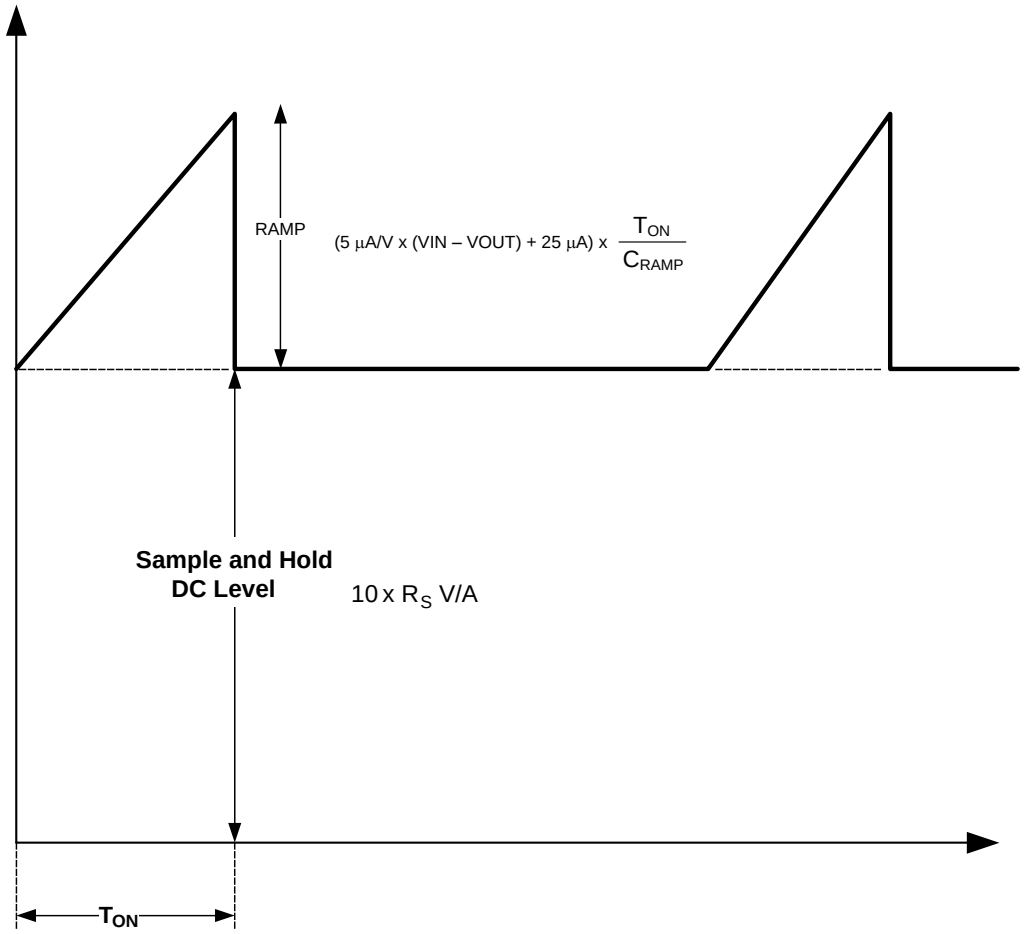


Figure 15. Composition of Current Sense Signal

The sample & hold DC level illustrated in Figure 15 is derived from a measurement of the re-circulating (or free-wheeling) diode current. The diode current flows through the current sense resistor connected between the CS and CSG pins. The voltage across the sense resistor is sampled and held just prior to the onset of the next conduction interval of the buck switch. The diode current sensing and sample & hold provide the DC level for the reconstructed current signal. The positive slope inductor current ramp is emulated by an external capacitor connected from the RAMP pin to GND and an internal voltage controlled current source. The ramp current source that emulates the inductor current is a function of the VIN and VOUT voltages per the following equation:

$$I_{RAMP} = 5\ \mu A/V \times (VIN - VOUT) + 25\ \mu A \quad (2)$$

Proper selection of the RAMP capacitor depends upon the selected value of the output inductor and the current sense resistor (R_S). For proper current emulation, the DC sample & hold value and the ramp amplitude must have the same dependence on the load current. That is:

$$C_{RAMP} = \frac{g_m \times L}{R_S \times A} \quad (3)$$

where

- g_m is the ramp current generator transconductance (5 µA/V)
- A is the gain of the current sense amplifier (10V/V)

The RAMP capacitor should connected directly to the RAMP and GND pins of the IC.

Feature Description (continued)

For duty cycles greater than 50%, peak current mode control circuits are subject to sub-harmonic oscillation. Sub-harmonic oscillation is normally characterized by alternating wide and narrow pulses at the SW pin. Adding a fixed slope voltage ramp (slope compensation) to the current sense signal prevents this oscillation. The 25 µA offset current supplied by the emulated current source provides a fixed slope to the ramp signal. In some high output voltage, high duty cycles applications; additional slope compensation may be required. In these applications, a pull-up resistor may be added between the RAMP and VCC pins to increase the ramp slope compensation. A formula to configure pull-up resistor is shown in Application and Implementation.

8.3.6 Dropout Voltage Reduction

The LM5088 features unique circuitry to reduce the dropout voltage. Dropout voltage is defined as the difference between the minimum input voltage to maintain regulation and the output voltage (VIN_{min} - Vout). Dropout voltage thus determines the lowest input voltage at which the converter maintains regulation. In a buck converter, dropout voltage primarily depends upon the maximum duty cycle. The maximum duty cycle is dependant on the oscillator frequency and minimum off-time.

An approximation for the dropout voltage is:

$$\text{Dropout\_Voltage} = V_{OUT} \times \frac{T_{OFF(max)}}{T_{OSC} - T_{OFF(max)}}$$

where

- $T_{OSC} = 1/f_{SW}$
- $T_{OFF\ (max)}$ is the forced off-time (280 ns typical, 365 ns maximum)
- f_{SW} is the oscillator frequency
- T_{OSC} is the oscillator period (4)

From the above equation, it can be seen that for a given output voltage, reducing the dropout voltage requires either reducing the forced off-time or oscillator frequency ($1/T_{OSC}$). The forced off-time is limited by the time required to replenish the bootstrap capacitor and time required to sample the re-circulating diode current. The 365 ns forced off-time of the LM5088 controller is a good trade-off between these two requirements. Thus the LM5088 reduces dropout voltage by dynamically decreasing the operating frequency during dropout. The Dynamic Frequency Control (DFC) is achieved using a dropout monitor, which detects a dropout condition and reduces the operating frequency. The operating frequency will continue to decrease with decreasing input voltage until the frequency falls to the minimum value set by the DFC circuitry.

$$f_{SW(minDFC)} \cong 1/3 \times f_{SW(nominal)} \quad (5)$$

If the VIN voltage continues to fall below this point, output regulation can no longer be maintained. The oscillator frequency will revert back to the nominal operating frequency set by the RT resistor when the input voltage increases above the dropout range. DFC circuitry does not affect the PWM during normal operating conditions.

Feature Description (continued)

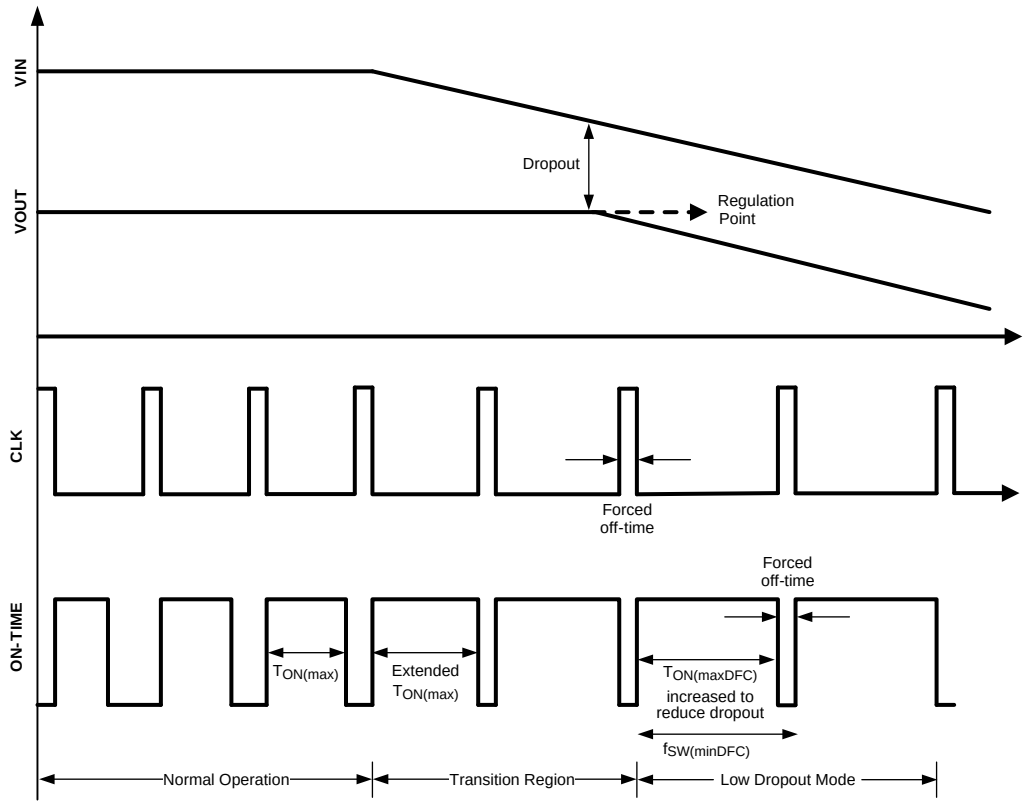


Figure 16. Dropout Voltage Reduction using Dynamic Frequency Control

8.3.7 Frequency Dithering (LM5088-1 Only)

Electro-Magnetic Interference (EMI) emissions are fundamentally associated with switch-mode power supplies due to sharp voltage transitions, diode reverse recovery currents and the ringing of parasitic L-C circuits. These emissions will conduct back to the power source or radiate into the environment and potentially interfering with nearby electronic systems. System designers typically use a combination of shielding, filtering and layout techniques to reduce the EMI emissions sufficiently to satisfy EMI emission standards established by regulatory bodies. In a typical fixed frequency switching converter, narrowband emissions typically peak at the switching frequency with the successive harmonics having less energy. Dithering the oscillator frequency spreads the EMI energy over a range of frequencies, thus reducing the peak levels. Dithering can also reduce the system cost by reducing the size and quantity of EMI filtering components.

The LM5088-1 provides an optional frequency dithering function which is enabled by connecting a capacitor from the dither pin (DITH) to GND. Connecting the DITH pin directly to GND disables frequency dithering causing the oscillator to operate at the frequency established by the RT resistor. As shown in Figure 17, the C_{dither} capacitor is used to generate a triangular wave centered at 1.2V. This triangular waveform is used to manipulate the oscillator circuit such that the oscillator frequency modulates from -5% to +5% of the nominal operating frequency set by the RT resistor. The C_{dither} capacitor value sets the rate of the low frequency modulation i.e., a lower value C_{dither} capacitor will modulate the oscillator frequency from -5% to +5% at a faster rate than a higher value capacitor. For the dither circuit to work effectively the modulation rate must be much less than the oscillator frequency (f_{SW}), C_{dither} should be selected such that;

$$C_{dither} \geq \frac{100 \times 25\ \mu A}{f_{SW} \times 0.12V} \quad (6)$$

Feature Description (continued)

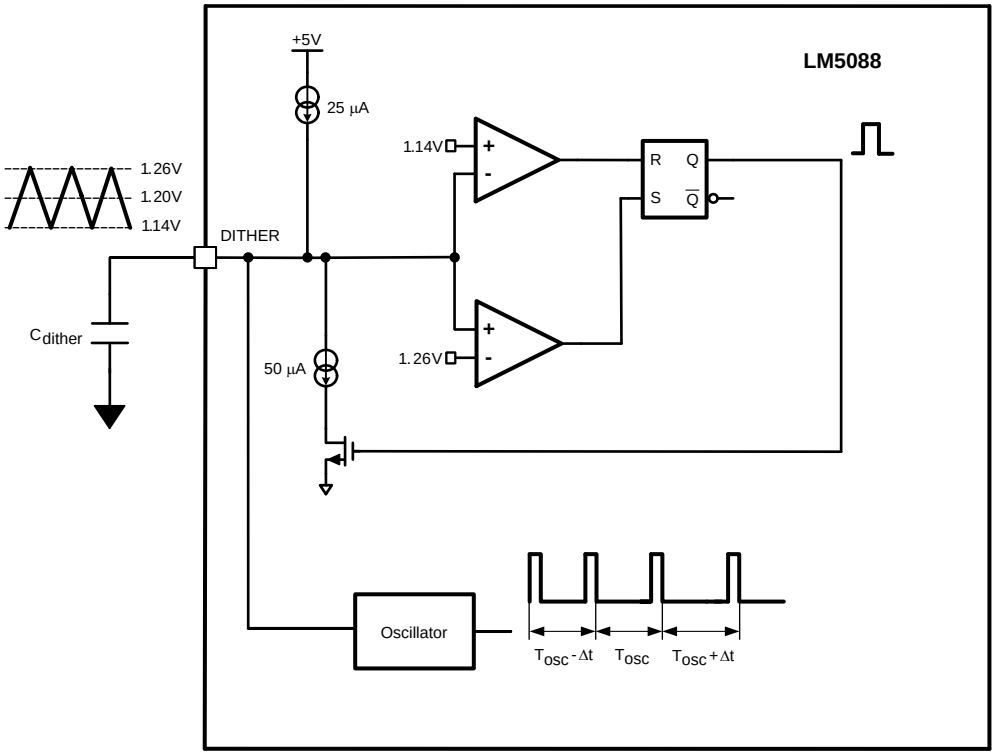


Figure 17. Frequency Dithering Scheme

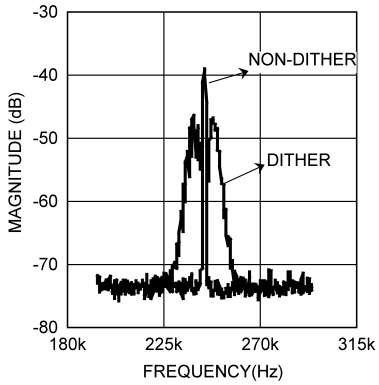


Figure 18. Conducted Emissions Measured at the Input of a LM5088 Based Buck Converter

Figure 18 shows the conducted emissions on the LM5088 evaluation board input power line. It can be seen from the above picture that, the peak emissions with non-dithering operation are centered narrowly at the operating frequency of the converter. With dithering operation, the conducted emissions are spread around the operating frequency and the maximum amplitude is reduced by approximately 10dB. (Figure 18 was captured using a Chroma DC power supply model number 62006P and an Agilent network analyzer model number 4395A).

Feature Description (continued)

8.3.8 Cycle-by-Cycle Current Limit

The LM5088 contains a current limit feature that protects the circuit from extended over current conditions. The emulated current signal is directly proportional to the buck switch current and is applied to the current limit comparator. If the emulated current exceeds 1.2V, the PWM cycle is terminated. The peak inductor current required to trigger the current limit comparator is given by:

$$I_{PEAK} = \frac{1.2V - 25\ \mu A \times \frac{V_{OUT}}{VIN \times f_{SW} \times C_{RAMP}}}{A \times R_S}$$

$$\text{or} \quad I_{PEAK} \cong \frac{0.12V}{R_S}$$

where

- A = 10V/V is the current sense amplifier gain
- C_{RAMP} is the ramp capacitor
- R_S is the sense resistor
- $25\ \mu A \times \frac{V_{OUT}}{VIN \times f_{SW} \times C_{RAMP}}$ is the voltage ramp added for slope compensation
- 1.2 V is the reference of the current limit comparator (7)

is the voltage ramp added for slope compensation and 1.2V is the reference of the current limit comparator.

Since the current that charges the RAMP capacitor is proportional to VIN-VOUT, if the output is suddenly shorted, the VOUT term is zero and the RAMP charging current increases. The increased RAMP charging current will immediately reduce the PWM duty cycle. The LM5088 also includes a buck switch protection scheme. A dedicated comparator monitors the drain to source voltage of the buck FET when it is turned ON, if the V_{DS} exceeds 1.5V, the comparator turns off the buck FET immediately. This feature will help protect the buck FET in catastrophic conditions such as a sudden saturation of the inductor.

8.3.9 Overload Protection Timer (LM5088-2 Only)

To further protect the external circuitry during a prolonged over current condition, the LM5088-2 provides a current limit timer to disable the switching regulator and provide a delay before restarting (hiccup mode). The number of current limit events required to trigger the restart mode is programmed by an external capacitor at the RES pin. During each PWM cycle, as shown in Figure 20, the LM5088 either sinks current from or sources current into the RES capacitor. If the emulated current ramp exceeds the 1.2V current limit threshold, the present PWM cycle is terminated and the LM5088 sources 50 µA into the RES pin capacitor during the next PWM clock cycle. If a current limit event is not detected in a given PWM cycle, the LM5088 disables the 50 µA source current and sinks 27 µA from the RES pin capacitor during the next cycle. In an overload condition, the LM5088 protects the converter with cycle-by-cycle current limiting until the voltage at RES pin reaches 1.2V. When RES reaches 1.2V, a hiccup mode sequence is initiated as follows:

- The SS capacitor is fully discharged.
- The RES capacitor is discharged with 1.2 µA
- Once the RES capacitor reaches 0.2V, a normal soft-start sequence begins. This provides a time delay before restart.
- If the overload condition persists after restart, the cycle repeats.
- If the overload condition no longer exists after restart, the RES pin is held at ground by the 27 µA discharge current source and normal operation resumes.

Feature Description (continued)

The overload protection timer is very versatile and can be configured for the following modes of protection:

1. **Cycle-by-Cycle only:** The hiccup mode can be completely disabled by connecting the RES pin to GND. In this configuration, the cycle-by-cycle protection will limit the output current indefinitely and no hiccup sequence will occur.
2. **Delayed Hiccup:** Connecting a capacitor to the RES pin provides a programmed number of cycle-by-cycle current limit events before initiating a hiccup mode restart, as previously described. The advantage of this configuration is that a short term overload will not cause a hiccup mode restart but during extended overload conditions, the average dissipation of the power converter will be very low.
3. **Externally Controlled Hiccup:** The RES pin can also be used as an input. By externally driving the pin to a level greater than the 1.2V hiccup threshold, the controller will be forced into the delayed restart sequence. For example, the external trigger for a delayed restart sequence could come from an over-temperature protection or an output over-voltage sensor.

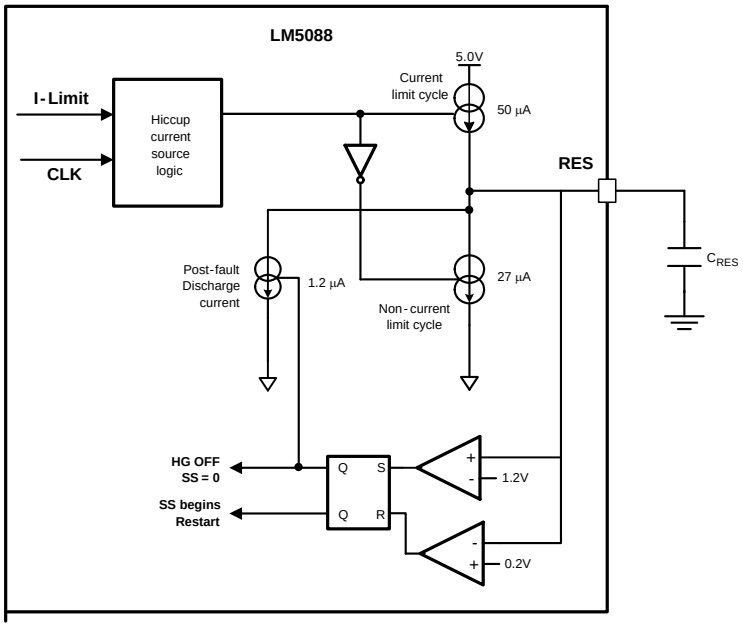


Figure 19. Current Limit Restart Circuit

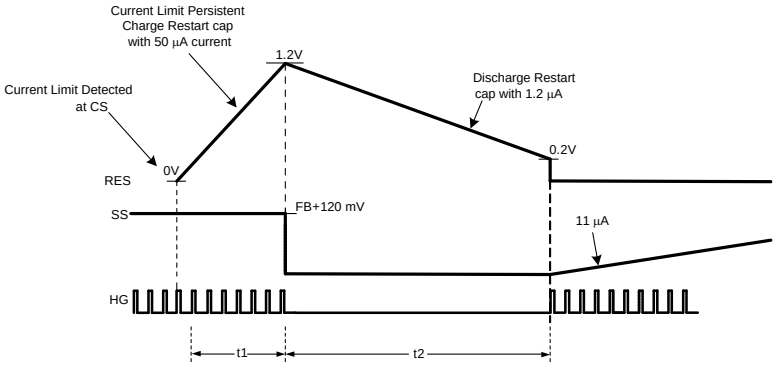


Figure 20. Current Limit Restart Timing Diagram

Feature Description (continued)

8.3.10 Soft-Start

The soft-start (SS) feature forces the output to rise linearly until it reaches the steady-state operating voltage set by the feedback resistors. The LM5088 will regulate the FB pin to the SS pin voltage or the internal 1.205V reference, which ever is lower. At the beginning of the soft-start sequence VSS = 0V and, an internal 11 µA current source gradually increases the voltage of the external soft-start capacitor (C_{SS}). An internal amplifier clamps the SS pin voltage at 120 mV above the FB voltage. This feature provides soft-start controlled recovery with reduced output overshoot in the event that the output voltage momentarily dips out of regulation.

8.3.11 HG Output

The LM5088 provides a high current, high-side driver and associated level shift circuit to drive an external N-Channel MOSFET. The gate driver works in conjunction with an internal diode and external bootstrap capacitor. A ceramic bootstrap capacitor is recommended, and should be connected directly between the BOOT and SW pins. During the off-time of the buck switch, the bootstrap capacitor charges from VCC through an internal diode. When operating with a high PWM duty cycle, the HG output will be forced-off each cycle for 365 ns (max) to ensure that BOOT capacitor is recharged. A “pre-charge” circuit, comprised of a MOSFET between SW and GND, is turned ON during the forced off-time to help replenish the BOOT capacitor. The pre-charge circuit provides charge to the BOOT capacitor under light load or pre-biased load conditions when the SW voltage does not remain low during the entire off-time.

8.3.12 Thermal Protection

Internal thermal shutdown circuitry is provided to protect the integrated circuit in the event the maximum operating temperature is exceeded. When activated, typically at 165°C, the controller is forced into a low power reset state, disabling the output driver and the bias supply of the controller. The feature prevents catastrophic failures from accidental device over-heating.

8.4 Device Functional Modes

8.4.1 EN Pin Modes

If the EN pin voltage is below 0.4 V, the regulator will be in a low power state. If the EN pin voltage is between 0.4 V and 1.2 V, the controller will be in standby mode. If the EN pin voltage is above 1.2 V, the controller will be operational. An external voltage divider can be used to set a line under the voltage shutdown threshold. If the EN pin is left open, a 5-µA pull-up current forces the pin to the high state and enables the controller.

9 Application and Implementation

9.1 Application Information

The LM5088 Wide Input Range buck Controller features all the functions necessary to implement an efficient high voltage step-down converter using a minimum number of external components. The LM5088 is well suited for a wide range of applications where efficient step-down of high, unregulated input voltage is required.

9.2 Typical Application

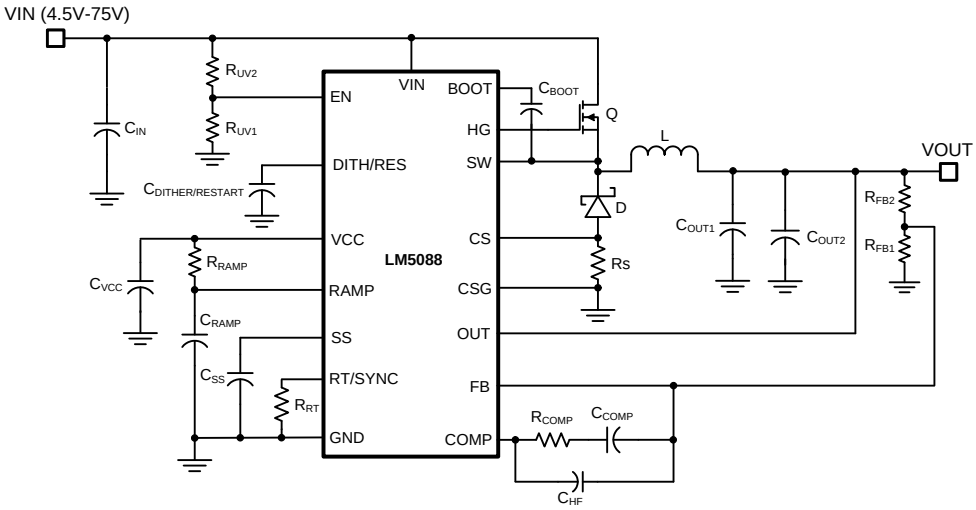


Figure 21. LM5088 Typical Application Schematic

9.3 Design Requirements

The procedure for calculating the external components is illustrated with the following design example. The circuit shown in Figure 27 and Figure 28 is configured for the following specifications:

- Output Voltage = 5V
- Input Voltage = 5.5V to 36V
- Maximum Load Current = 7A
- Switching Frequency = 250 kHz

9.4 Detailed Design Procedure

9.4.1 Timing Resistor

The RT resistor sets the oscillator switching frequency. Higher frequencies result in smaller size components such as the inductor and filter capacitors. However, operating at higher frequencies also results in higher MOSFET and diode switching losses. Operation at 250 kHz was selected for this example as a reasonable compromise between size and efficiency.

The value of RT resistor can be calculated as follows:

$$R_{RT} = \frac{\frac{1}{250\ kHz} - 280\ ns}{152\ pF} = 24.5\ k\Omega \quad (8)$$

The nearest standard value of 24.9 kΩ was chosen for RT.

Detailed Design Procedure (continued)

9.4.2 Output Inductor

The inductor value is determined based on the operating frequency, load current, ripple current and the input and output voltages.

Knowing the switching frequency (f_{SW}), maximum ripple current (I_{PP}), maximum input voltage ($VIN_{(max)}$) and the nominal output voltage (V_{OUT}), the inductor value can be calculated as follows:

$$L = \frac{V_{OUT}}{I_{PP} \times f_{SW}} \times \left(1 - \frac{V_{OUT}}{V_{IN(max)}}\right) \quad (9)$$

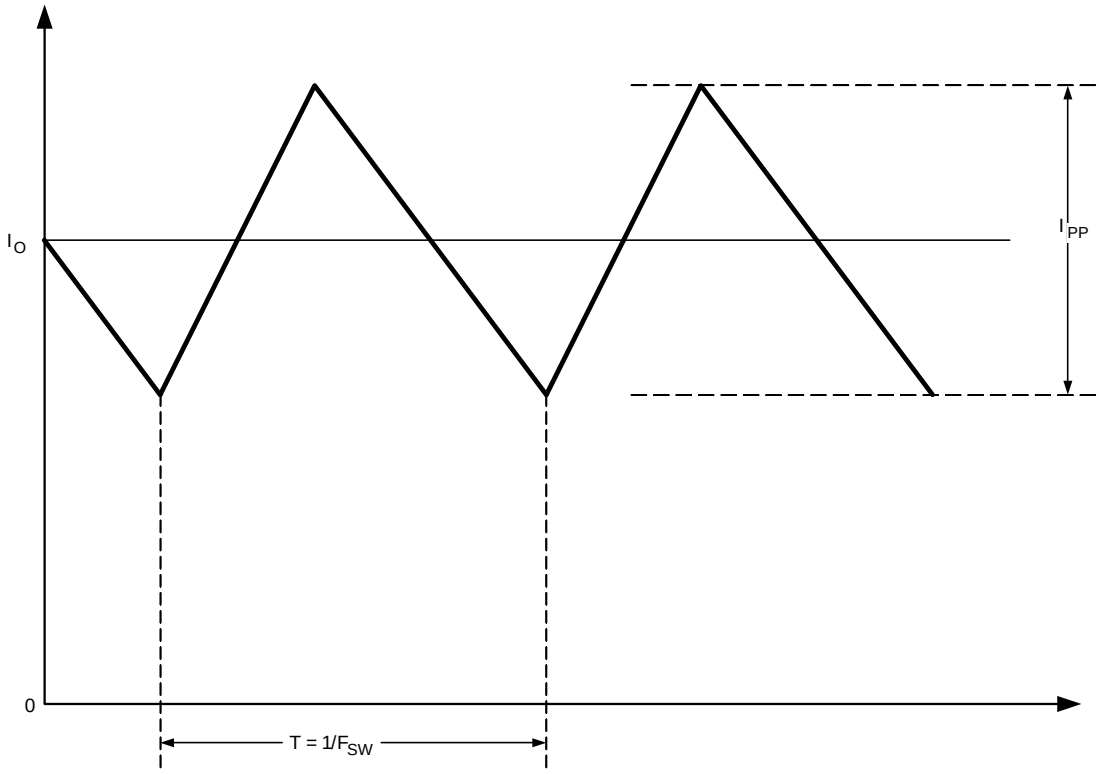


Figure 22. Inductor Current

The maximum ripple current occurs at the maximum input voltage. Typically, I_{PP} is selected between 20% and 40% of the full load current. Higher ripple current will result in a smaller inductor. However, it places more burden on the output capacitor to smooth out the ripple current to achieve low output ripple voltage. For this example 40% ripple was chosen for a smaller sized inductor.

$$L = \frac{5V}{0.4 \times 7A \times 250\ kHz} \times \left(1 - \frac{5V}{55V}\right) = 6.2\ \mu H \quad (10)$$

The nearest standard value of 6.8 µH will be used. To prevent saturation, the inductor must be rated for the peak current. During normal operation, the peak current occurs at maximum load current (plus maximum ripple). With properly scaled component values, the peak current is limited to $V_{CS(TH)}/R_S$ During overload conditions. At the maximum input voltage with a shorted output, the chosen inductor must be evaluated at elevated temperature. It should be noted that the saturation current rating of inductors drops significantly at elevated temperatures.

Detailed Design Procedure (continued)

9.4.3 Current Sense Resistor

The current limit value (I_{LIM}) is set by the current sense resistor (R_S).

R_S can be calculated by

$$R_S = \frac{V_{CS}}{(1 + \text{margin}) \times (I_{OUT} + 0.5 \times I_{PP}) + \frac{V_{OUT}}{L \times f_{sw}}}$$

$$= \frac{0.12}{(1 + 0.1) \times (7\,A + 0.5 \times 2.8) + \frac{5\,V}{6.8\,\mu H \times 250\,kHz}} \cong 10\ m\Omega \quad (11)$$

Some 'margin' beyond the maximum load current is recommended for the current limit threshold. In this design example, the current limit is set at 10% above the maximum load current, resulting in a R_S value of 10 mΩ. The CS and CSG pins should be Kelvin connected to the current sense resistor.

9.4.4 Ramp Capacitor

With the inductor and sense resistor value selected, the value of the ramp capacitor (C_{RAMP}) necessary for the emulation ramp circuit is given by:

$$C_{RAMP} = \frac{g_m \text{ x } L}{A \text{ x } R_S}$$

where

- L is the value of the output inductor
- gm is the ramp generator transconductance (5 µA/V)
- A is the current sense amplifier gain (10V/V) (12)

For the current design example, the ramp capacitor is calculated as:

$$C_{RAMP} = \frac{5\ \mu A/V \text{ x } 6.8\ \mu H}{10V/V \text{ x } 10\ m\Omega} = 340\ pF \quad (13)$$

The next lowest standard value 270 pF was selected for C_{RAMP}. An NPO capacitor with 5% or better tolerance is recommended. It should be noted that selecting a capacitor value lower than the calculated value will increase the slope compensation. Furthermore, selecting a ramp capacitor substantially lower or higher than the calculated value will also result in incorrect PWM operation.

For VOUT > 5V, internal slope compensation provided by the LM5088 may not be adequate for certain operating conditions especially at low input voltages. A pull-up resistor may be added from VCC to RAMP the pin to increase the slope compensation. Optimal slope compensation current may be calculated from

$$I_{OS} = V_{OUT} \text{ x } 5\ \mu A/V \quad (14)$$

and R_{RAMP} is given by

$$R_{RAMP} = \frac{V_{VCC} - V_{RAMP}}{I_{OS} - 25\ \mu A} \quad (15)$$

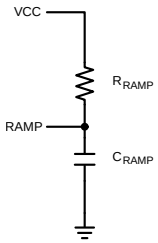


Figure 23. Additional Slope Compensation for VOUT > 5V

Detailed Design Procedure (continued)

9.4.5 Output Capacitors

The output capacitors smooth the inductor current ripple and provide a source of charge for load transient conditions. The output capacitor selection is primarily dictated by the following specifications:

1. Steady-state output peak-peak ripple (ΔV_{PK-PK})
2. Output voltage deviation during transient condition ($\Delta V_{Transient}$)

For the 5V output design example, ΔV_{PK-PK} = 50 mV (1% of VOUT) and $\Delta T_{Transient}$ = 100 mV (2% of VOUT) was chosen. The magnitude of output ripple primarily depends on ESR of the capacitors while load transient voltage deviation depends both on the output capacitance and ESR.

When a full load is suddenly removed from the output, the output capacitor must be large enough to prevent the inductor energy to raise the output voltage above the specified maximum voltage. In other words, the output capacitor must be large enough to absorb the inductor's maximum stored energy. Equating the stored energy equations of both the inductor and the output capacitor it can be shown that:

$$C_O = \frac{L \times \left(I_O + \frac{\Delta I_{PP}}{2}\right)^2}{(\Delta V + V_{OUT})^2 - V_{OUT}^2} \quad (16)$$

Evaluating, the above equation with a ΔVout of 100 mV results in an output capacitance of 475 µF. As stated earlier, the maximum peak to peak ripple primarily depends on the ESR of the output capacitor and the inductor ripple current. To satisfy the ΔV_{PK-PK} of 50 mV with 40% inductor current ripple, the ESR should be less than 15 mΩ. In this design example a 470 µF aluminum capacitor with an ESR of 10 mΩ is paralleled with two 47 µF ceramic capacitors to further reduce the ESR.

9.4.6 Input Capacitors

The input power supply typically has large source impedance at the switching frequency. Good quality input capacitors are necessary to limit the ripple voltage at the VIN pin while supplying most of the switch current during the on-time. When the buck switch turns ON, the current into the external FET steps to the valley of the inductor current waveform at turn-on, ramps up to the peak value, and then drops to zero at turn-off. The input capacitors should be selected for RMS current rating and minimum ripple voltage. A good approximation for the ripple current is $I_{RMS} > I_{OUT}/2$.

Quality ceramic capacitors with a low ESR should be selected for the input filter. To allow for capacitor tolerances and voltage rating, five 2.2 µF, 100V ceramic capacitors were selected. With ceramic capacitors, the input ripple voltage will be triangular and will peak at 50% duty cycle. Taking into account the capacitance change with DC bias a worst case input peak-to-peak ripple voltage can be approximated as:

$$\Delta V_{IN} = \frac{I_{OUT}}{4 \times f_{SW} \times C_{IN}} = \frac{7A}{4 \times 250\ kHz \times 11\ \mu F} = 636\ mV \quad (17)$$

When the converter is connected to an input power source, a resonant circuit is formed by the line impedance and the input capacitors. This can result in an overshoot at the VIN pin and could result in VIN exceeding its absolute maximum rating. Because of those conditions, it is recommended that either an aluminum type capacitor with an ESR or increasing CIN>10 x LIN While using aluminum type capacitor care should be taken to not exceed its maximum ripple current rating. Tantalum capacitors must be avoided at the input as they are prone to shorting.

Detailed Design Procedure (continued)

9.4.7 VCC Capacitor

The capacitor at the VCC pin provides noise filtering and stability for the VCC regulator. The recommended value should be no smaller than 0.1 µF, and should be a good quality, low ESR, ceramic capacitor. A value of 1 µF was selected for this design.

9.4.8 Bootstrap Capacitor

The bootstrap capacitor between HB and SW pins supplies the gate current to charge the high-side MOSFET gate at each cycle's turn-on as well as supplying the recovery charge for the bootstrap diode (D1).The peak current can be several amperes. The recommended value of the bootstrap capacitor is at least 0.022 µF and should be a good quality, low ESR, ceramic capacitor located close to the pins of the IC. The absolute minimum value for the bootstrap capacitor is calculated as:

$$C_{HB} \geq \frac{Q_g}{\Delta V_{HB}} \tag{18}$$

where

- Q_g is the high-side MOSFET gate charge
- ΔV_{HB} is the tolerable voltage droop on C_{HB}, which is typically less than 5% of the VCC

.A value of 0.1 µF was selected for this design.

9.4.9 Soft-start Capacitor

The capacitor at the SS capacitor determines the soft-start time, the output voltage to reach the final regulated value. The value of C_{SS} for a given time is determined from:

$$C_{SS} = \frac{t_{SS} \text{ x } 11\ \mu A}{1.205V} \tag{19}$$

For this design example, a value of 0.022 µF was chosen for a soft start time of approximately 2 ms.

9.4.10 Output Voltage Divider

R_{FB1} and R_{FB2} set the output voltage level, the ratio of these resistors can be calculated from:

$$\frac{R_{FB2}}{R_{FB1}} = \frac{VOUT}{1.205V} - 1 \tag{20}$$

1.62 kΩ was chosen for R_{FB1} in this design which results in a R_{FB2} value of 5.11 kΩ. A reasonable guide is to select the value of R_{FB1} value such that the current through the resistor (1.2V/ R_{FB1}) is in between 1 mA and 100 µA.

Detailed Design Procedure (continued)

9.4.11 UVLO Divider

A voltage divider can be connected to the EN pin to the set the minimum startup voltage ($VIN_{(min)}$) of the regulator. If this feature is required, set the value of R_{UV2} between 10 kΩ and 100 kΩ and then calculate R_{UV1} from:

$$R_{UV1} = 1.2V \times \frac{R_{UV2}}{(V_{IN(min)} + (5\ \mu A \times R_{UV2}) - 1.2V)} \quad (21)$$

In this design, for a $VIN_{(min)}$ of 5V, R_{UV2} was selected to be 54.9 kΩ resulting in a R_{UV1}value of 16.2 kΩ. it is recommended to install a capacitor parallel to R_{UV1} for filtering. If the EN pin is left open, the LM5088 will begin operation once the upper VCC UV threshold of 4.0V (typ) is reached.

9.4.12 Restart Capacitor (LM5008-2 only)

The basic operation of the hiccup mode current limit is described in Overload Protection Timer (LM5088-2 Only). In the LM5088-2 application example the RES pin is configured for delayed hiccup mode. Please refer to Overload Protection Timer (LM5088-2 Only) to configure this pin in alternate configurations and also refer to Figure 20. The delay time to initiate a hiccup cycle (t1) is programmed by the selection of RES pin capacitor. In the case of continuous cycle-by-cycle current limit detection at the CS pin, the time required for C_{RES} to reach the 1.2V is given by

$$T_{restart\_delay} = \frac{C_{RES} \times 1.2V}{50\ \mu A} = C_{RES} \times 24k \quad (22)$$

The cool down time (t2) is set by the time taken to discharge the RES cap with 1.2 µA current source. This feature will reduce the input power drawn by the converter during a prolonged over current condition. In this application 500 µs of delay time was selected. The minimum value of C_{RES} capacitor should be no less than 0.022 µF.

9.4.13 MOSFET Selection

Selection of the Buck MOSFET is governed by the same tradeoffs as the switching frequency. Losses in power MOSFETs can be broken down into conduction losses and switching losses. The conduction loss is given by:

$$P_{DC} = D \times (I_O^2 \times R_{DS(ON)} \times 1.3)$$

where

- D is the duty cycle
- IO is the maximum load current (23)

The factor 1.3 accounts for the increase in MOSFET on-resistance due to heating. Alternatively, for a more precise calculation, the factor of 1.3 can be ignored and the on-resistance of the MOSFET can be estimated using the $R_{DS(ON)}$ vs. Temperature curves in the MOSFET datasheet.

The switching loss occurs during the brief transition period as the MOSFET turns on and off. During the transition period both current and voltage are present in the MOSFET. The switching loss can be approximated as:

$$P_{SW} = 0.5 \times V_{IN} \times I_O \times (t_R + t_F) \times f_{SW}$$

where

- $t_R$the rise time of the MOSFET
- t_F is the fall time of the MOSFET (24)

The rise and fall times are usually mentioned in the MOSFET datasheet or can be empirically observed on the scope. Another loss, which is associated with the buck MOSFET is the “gate-charging loss”. This loss differs from the above two losses in the sense that it is dissipated in the LM5088 and not in the MOSFET itself. Gate charging loss, P_{GC}, results from the current driving charging the gate capacitance of the power MOSFETs and is approximated as:

$$P_{GC} = VCC \times Q_g \times f_{SW} \quad (25)$$

Detailed Design Procedure (continued)

For this example with the maximum input voltage of 55V, the Vds breakdown rating of the selected MOSFET must be greater than 55V plus any ringing across drain to source due to parasitics. In order to minimize switching time and gate drive losses, the selected MOSFET must also have low gate charge (Q_g). A good choice of MOSFET for this design example is the SI7148DP which has a total gate charge of 30nC and rise and fall times of 10 ns and 12 ns respectively.

9.4.14 Diode Selection

A Schottky type re-circulating diode is required for all LM5088 applications. The near ideal reverse recovery current transients and low forward voltage drop are particularly important diode characteristics for high input voltage and low output voltage applications common to LM5088. The diode switching loss is minimized in a Schottky diode because of near ideal reverse recovery. The conduction loss can be approximated by:

$$P_{dc\_diode} = (1 - D) \times I_O \times V_F$$

where

- V_F is the forward drop of the diode (26)

The worst case is to assume a short circuit load condition. In this case, the diode will carry the output current almost continuously. The reverse breakdown rating should be selected for the maximum input voltage level plus some additional safety margin to withstand ringing at the SW node. For this application a 60V On Semiconductor Schottky diode (MBRB2060) with a specified forward drop of 0.6V at 7A at a junction temperature of 50°C was selected. For output loads of 5A and greater and high input voltage applications, a diode in a D^2PAK package is recommended to support the worst case power dissipation

9.4.15 Snubber Components Selection

Excessive ringing and spikes can cause erratic operation and couple spikes and noise to the output. Voltage spikes beyond the rating of the LM5088 or the re-circulating diode can damage these devices. A snubber network across the power diode reduces ringing and spikes at the switching node. Selecting the values for the snubber is best accomplished through empirical methods. First, make sure that the lead lengths for the snubber connections are very short. For the current levels typical for the LM5088, a resistor value between 3 and 10Ω should be adequate. As a rule of thumb, a snubber capacitor which is 4~5 times the Schottky diode's junction capacitance will reduce spikes adequately. Increasing the value of the snubber capacitor will result in more damping but also results in higher losses. The resistor's power dissipation is independent of the resistance value as the resistor dissipates the energy stored by the snubber capacitor. The resistor's power dissipation can be approximated as:

$$P_{R\_SNUB} = C_{SNUB} \times VIN_{max}^2 \times f_{SW} \quad (27)$$

Detailed Design Procedure (continued)

9.4.16 Error Amplifier Compensation

R_{COMP}, C_{COMP} and C_{HF} configure the error amplifier gain characteristics to accomplish a stable voltage loop gain. One advantage of current mode control is the ability of to close the loop with only two feedback components R_{COMP} and C_{COMP}. The voltage loop gain is the product of the modulator gain and the error amplifier gain. For this example, the modulator can be treated as an ideal voltage-to-current (transconductance) converter, The DC modulator gain of the LM5088 can be modeled as:

DC Gain $_{(MOD)} = R_{LOAD} / (A \times R_S)$

The dominant low frequency pole of the modulator is determined by the load resistance (R_{LOAD}) and the output capacitance (C_{OUT}). The corner frequency of this pole is:

If R_{LOAD} = 5V/7A = 0.714Ω and C_{OUT} = 500 µF (effective), then $FP_{(MOD)}$ = 550 Hz. (28)

DC $Gain_{(MOD)}$ = 0.714/ (10 x 10 mΩ) = 7.14 = 17dB (29)

For the 5V design example the modulator gain vs. frequency characteristic was measured as shown in Figure 24.

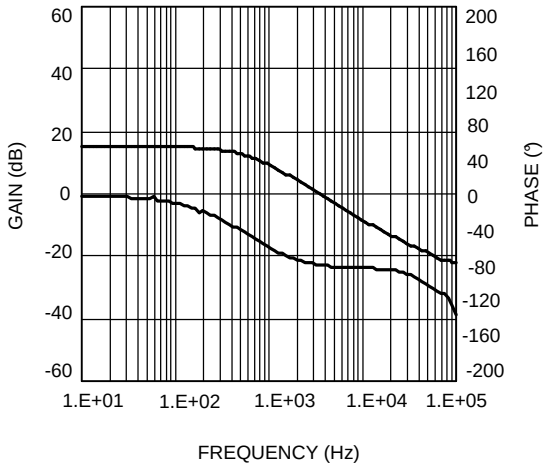


Figure 24. Modular Gain Phase

Detailed Design Procedure (continued)

Components R_{COMP} and C_{COMP} configure the error amplifier as a type II compensation configuration. The DC gain of the amplifier is 80dB which has a pole at low frequency and a zero at F_{Zero} = 1/(2π x R_{COMP} x C_{COMP}). The error amplifier zero is set such that it cancels the modulator pole leaving a single pole response at the crossover frequency of the voltage loop. A single pole response at the crossover frequency yields a very stable loop with 90° of phase margin. For the design example, a target loop bandwidth (crossover frequency) of 15 kHz was selected. The compensation network zero (F_{Zero}) should be at least an order of magnitude lower than the target crossover frequency. This constrains the product of R_{COMP} and C_{COMP} for a desired compensation network zero 1/ (2π x R_{COMP} x C_{COMP}) to be less than 1.5 kHz. Increasing R_{COMP}, while proportionally decreasing C_{COMP}, decreases the error amp gain. For the design example C_{COMP} was selected to be 0.015 µF and R_{COMP} was selected to be 18 kΩ. These values configure the compensation network zero at 0.6 kHz. The error amp gain at frequencies greater than F_{Zero} is R_{COMP} /R_{FB2}, which is approximately 3.56 (11dB).

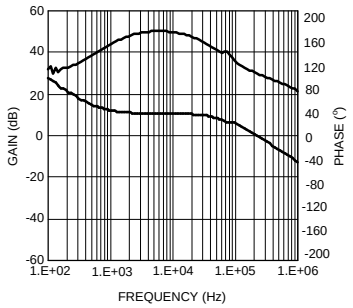


Figure 25. Error Amplifier Gain and Phase

The overall voltage loop gain can be predicted as the sum (in dB) of the modulator gain and the error amp gain. If a network analyzer is available, the modulator gain can be measured and the error amplifier gain can be configured for the desired loop transfer function. If a network analyzer is not available, the error amplifier compensation components can be designed with the suggested guidelines. Step load transient tests can be performed to verify performance. The step load goal is minimum overshoot with a damped response. C_{HF} can be added to the compensation network to decrease noise susceptibility of the error amplifier. The value of C_{HF} must be sufficiently small since the addition of this capacitor adds a pole in the error amplifier transfer function. A good approximation of the location of the pole added by C_{HF} is F_{P2} = F_{Zero} x C_{COMP}/ C_{HF}.Using C_{HF} is recommended to minimize coupling of any switching noise into the modulator. The value of C_{HF} was selected as 100 pF for this design example.

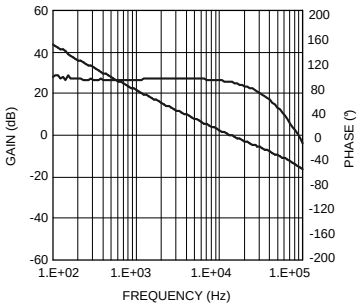


Figure 26. Overall Loop Gain and Phase

Detailed Design Procedure (continued)

9.4.17 Application Curves

See Figure 24 through Figure 26 for Typical Application Curves.

10 Power Supply Recommendations

10.1 Thermal Considerations

In a buck converter, most of the losses can be attributed to MOSFET conduction and switching loss, re-circulating diode conduction loss, inductor DCR loss and LM5088 VIN and VCC loss. The other dissipative components in a buck converter produce losses but these other losses collectively account for about 2% of the total loss. Formulae to calculate all the major losses are described in their respective sections of this datasheet. The easiest method to determine the power dissipated within the LM5088 is to measure the total conversion losses (Pin-Pout), then subtract the power losses in the Schottky diode, MOSFET, output inductor and snubber resistor. When operating at 7 A of output current and at 55 V, the power dissipation of the LM5088 is approximately 850 mW. The junction to ambient thermal resistance of the LM5088 mounted in the evaluation board is approximately 40°C with no airflow. At 25°C ambient temperature and no airflow, the predicted junction temperature will be 25+40*0.9 = 61°C. The LM5088 has an exposed thermal pad to aid in power dissipation. Adding several vias under the device will greatly reduce the controller junction temperature. The junction to ambient thermal resistance will vary with application. The most significant variables are the area of copper in the PC board; the number of vias under the IC exposed pad and the amount of forced air cooling. The integrity of solder connection from the IC exposed pad to the PC board is critical. Excessive voids will greatly diminish the thermal dissipation capacity.

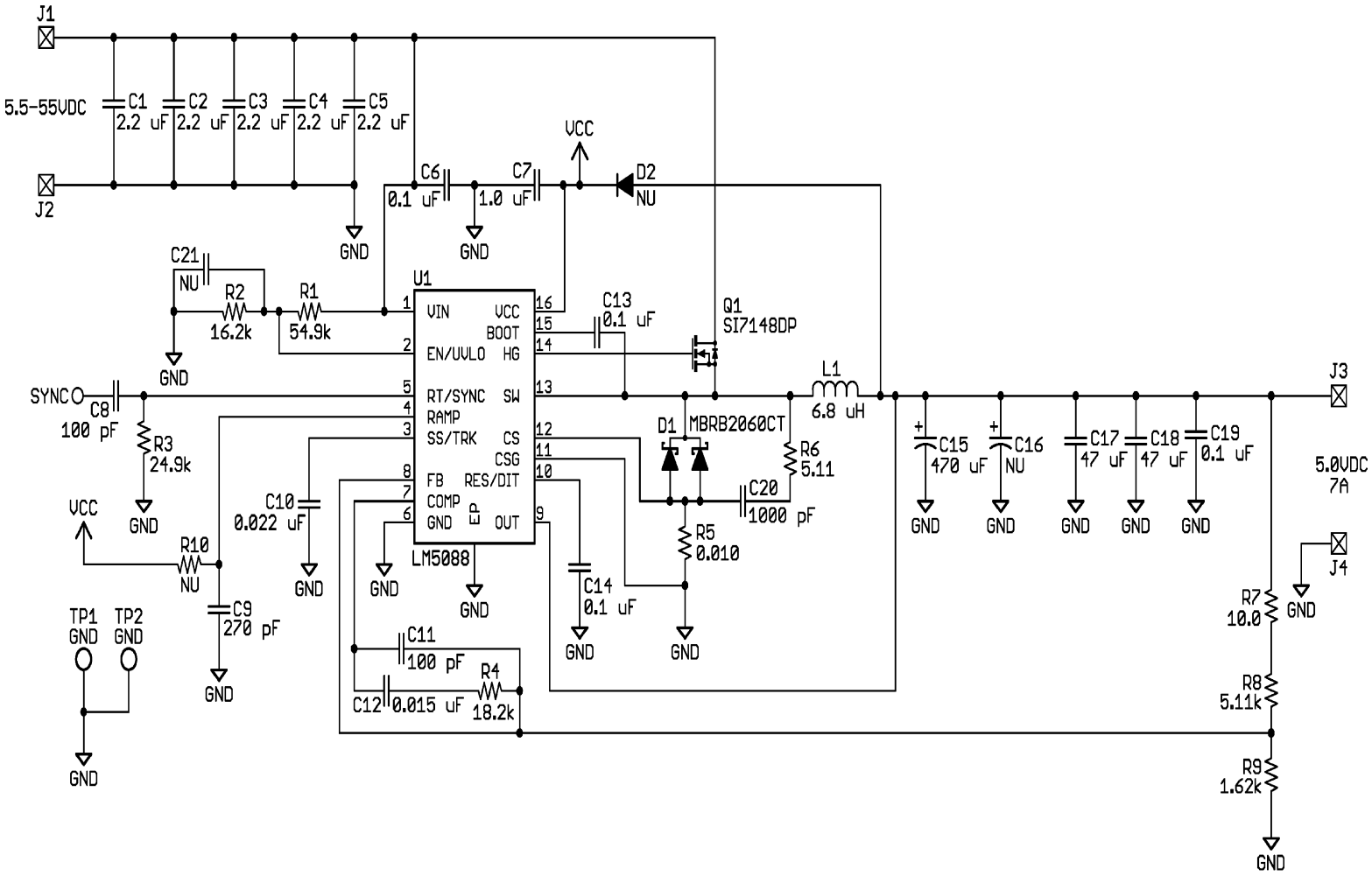


Figure 27. LM5088-1 Application Schematic

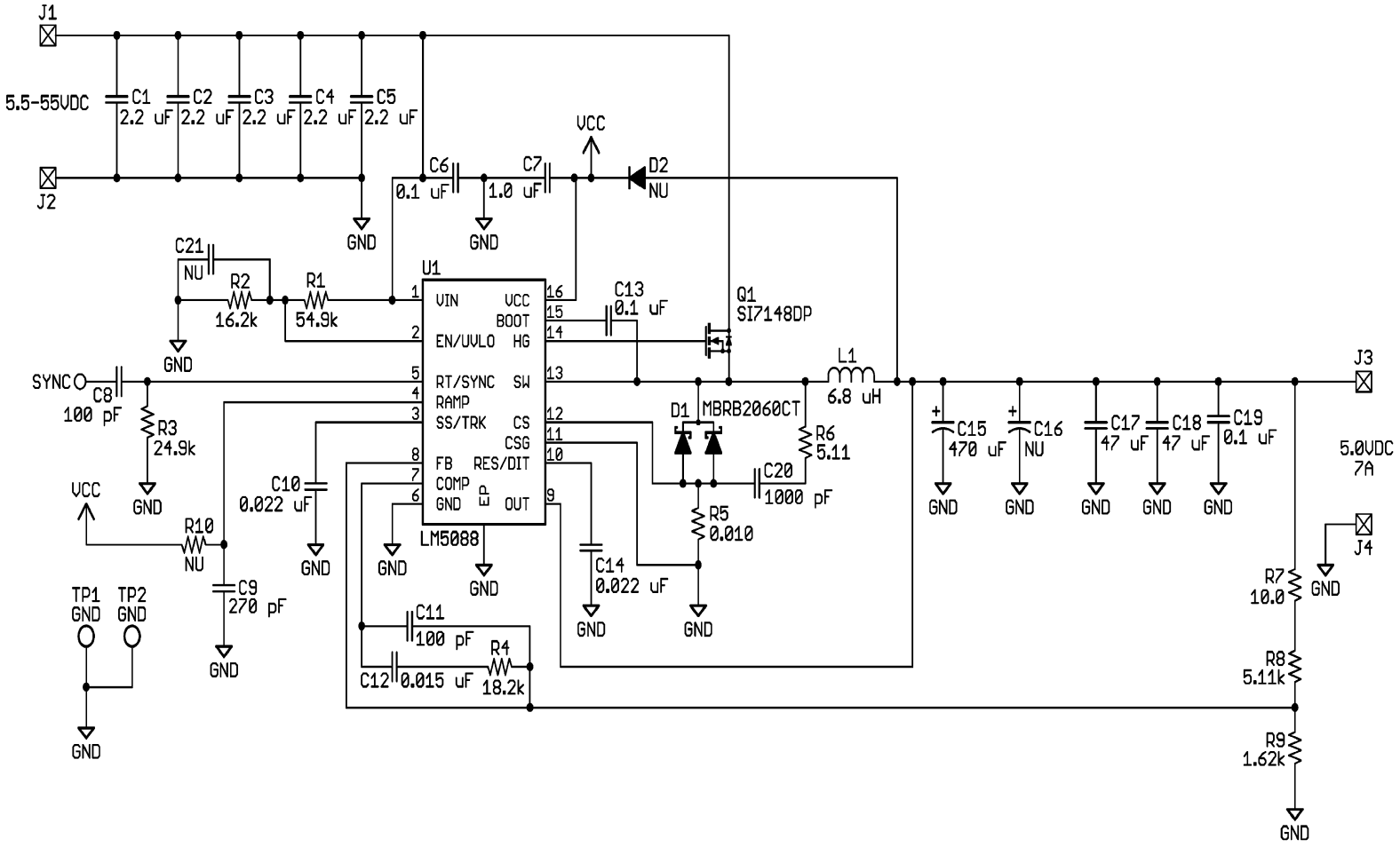


Figure 28. LM5088-2 Application Schematic

11 Layout

11.1 Layout Guidelines

In a buck regulator there are two loops where currents are switched very fast. The first loop starts from the input capacitors, through the buck MOSFET, to the inductor then out to the load. The second loop starts from the output capacitor ground, to the regulator PGND pins, to the current sense resistor, through the Schottky diode, to the inductor and then out to the load. Minimizing the area of these two loops reduces the stray inductance and minimizes noise which can cause erratic operation. A ground plane is recommended as a means to connect the input filter capacitors of the output filter capacitors and the PGND pin of the regulator. Connect all of the low power ground connections (C_{SS}, R_T, C_{RAMP}) directly to the regulator GND pin. Connect the GND pin and PGND pins together through to topside copper area covering the entire underside of the device. Place several vias in this underside copper area to the ground plane. The input capacitor ground connection should be as close as possible to the current sense ground connection.

11.2 Layout Example

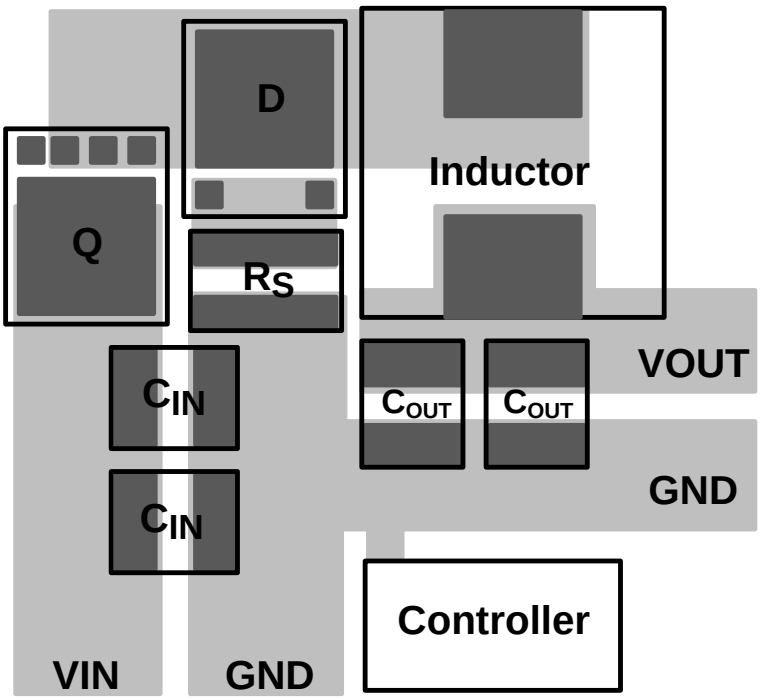


Figure 29. LM5088 Layout Example

12 Device and Documentation Support

12.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
LM5088	Click here	Click here	Click here	Click here	Click here
LM5088-Q1	Click here	Click here	Click here	Click here	Click here

12.2 Trademarks

All trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM5088MH-1/NOPB	ACTIVE	HTSSOP	PWP	16	92	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LM5088 MH-1	Samples
LM5088MH-2/NOPB	ACTIVE	HTSSOP	PWP	16	92	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LM5088 MH-2	Samples
LM5088MHX-1/NOPB	ACTIVE	HTSSOP	PWP	16	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LM5088 MH-1	Samples
LM5088MHX-2/NOPB	ACTIVE	HTSSOP	PWP	16	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LM5088 MH-2	Samples
LM5088QMH-1/NOPB	ACTIVE	HTSSOP	PWP	16	92	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LM5088 QMH-1	Samples
LM5088QMH-2/NOPB	ACTIVE	HTSSOP	PWP	16	92	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LM5088 QMH-2	Samples
LM5088QMHX-1/NOPB	ACTIVE	HTSSOP	PWP	16	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LM5088 QMH-1	Samples
LM5088QMHX-2/NOPB	ACTIVE	HTSSOP	PWP	16	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LM5088 QMH-2	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF LM5088, LM5088-Q1 :

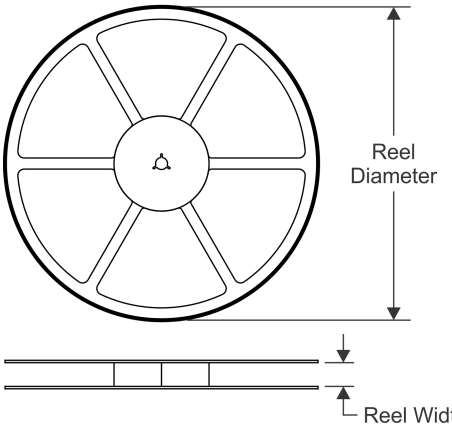
- Catalog: LM5088
- Automotive: LM5088-Q1

NOTE: Qualified Version Definitions:

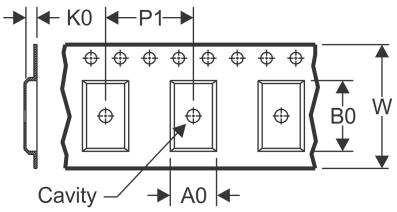
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

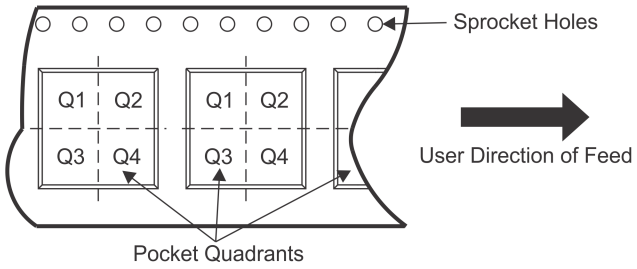


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

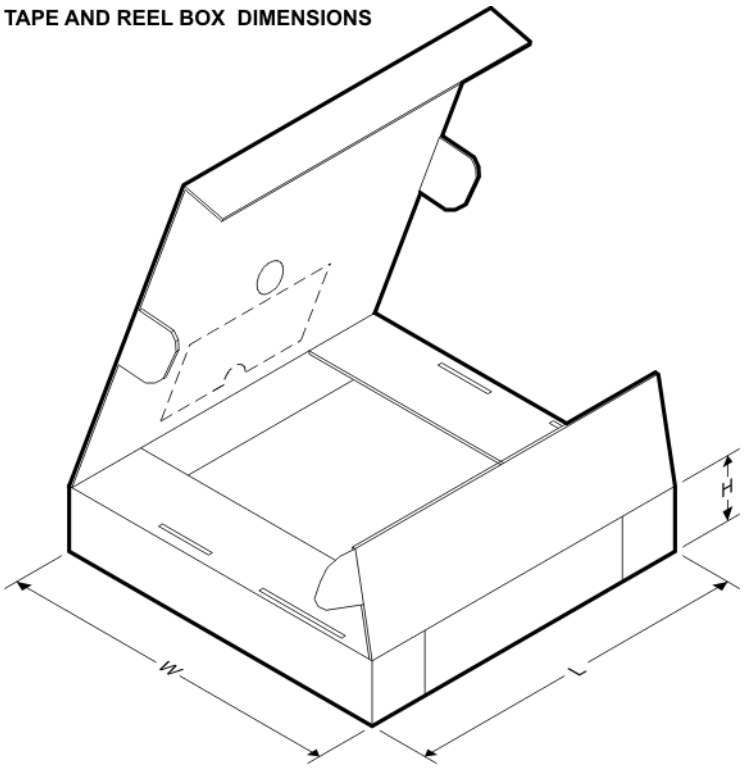
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

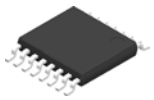
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM5088MHX-1/NOPB	HTSSOP	PWP	16	2500	330.0	12.4	6.95	5.6	1.6	8.0	12.0	Q1
LM5088MHX-2/NOPB	HTSSOP	PWP	16	2500	330.0	12.4	6.95	5.6	1.6	8.0	12.0	Q1
LM5088QMHX-1/NOPB	HTSSOP	PWP	16	2500	330.0	12.4	6.95	5.6	1.6	8.0	12.0	Q1
LM5088QMHX-2/NOPB	HTSSOP	PWP	16	2500	330.0	12.4	6.95	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM5088MHX-1/NOPB	HTSSOP	PWP	16	2500	367.0	367.0	35.0
LM5088MHX-2/NOPB	HTSSOP	PWP	16	2500	367.0	367.0	35.0
LM5088QMHX-1/NOPB	HTSSOP	PWP	16	2500	367.0	367.0	35.0
LM5088QMHX-2/NOPB	HTSSOP	PWP	16	2500	367.0	367.0	35.0

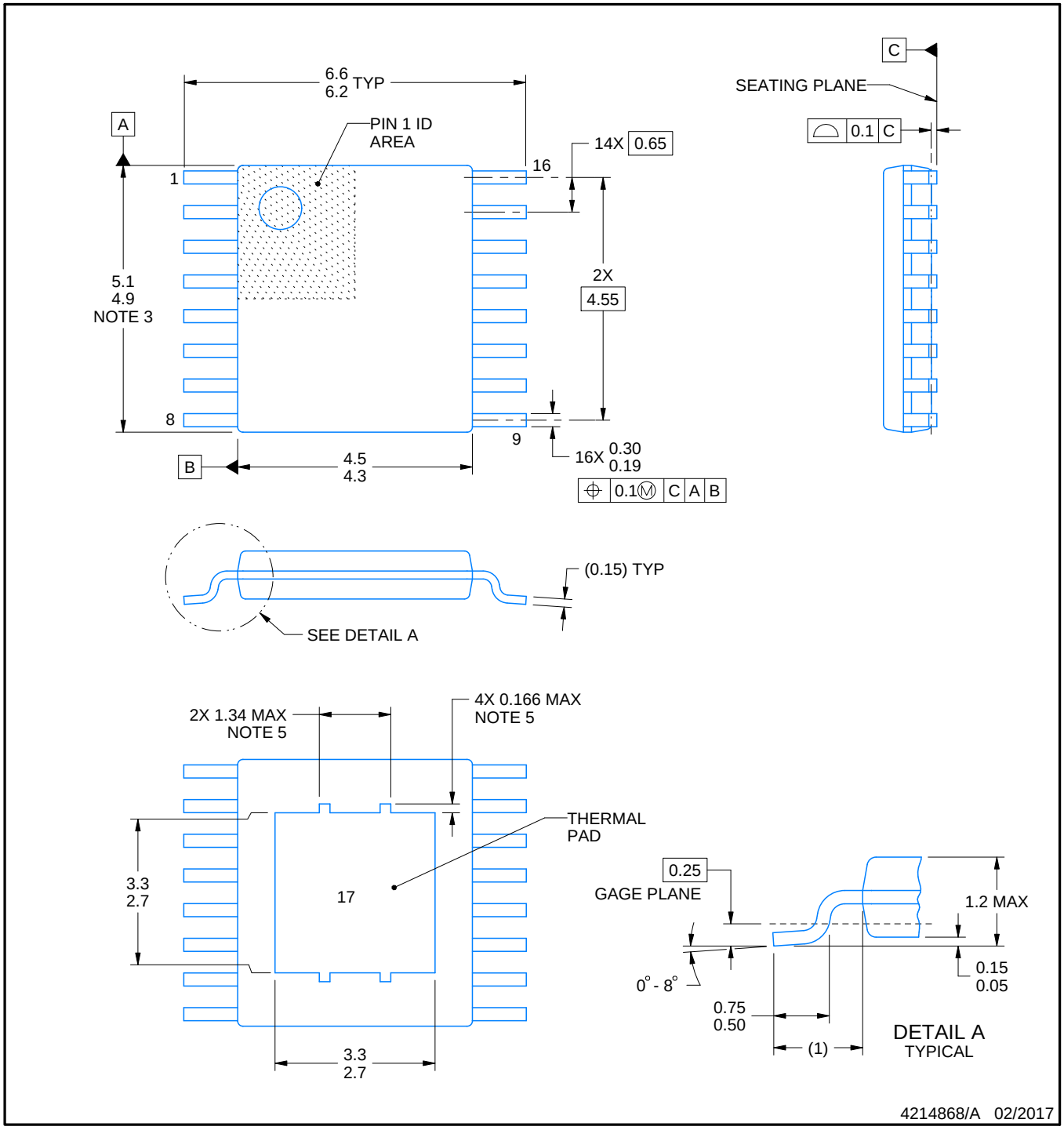


PACKAGE OUTLINE

PWP0016A

PowerPAD ™ HTSSOP - 1.2 mm max height

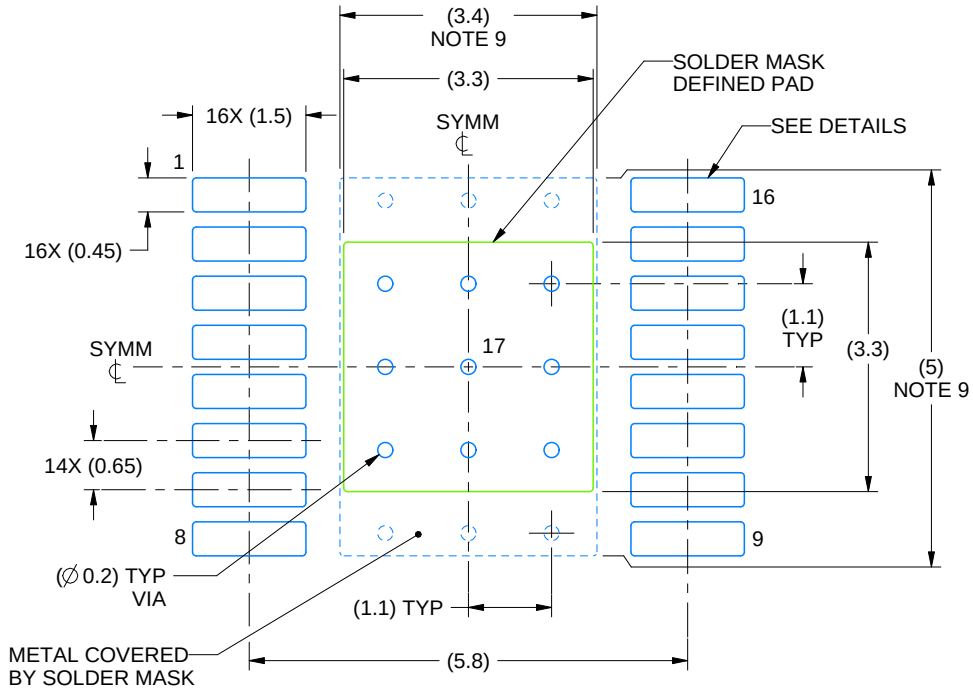
PLASTIC SMALL OUTLINE



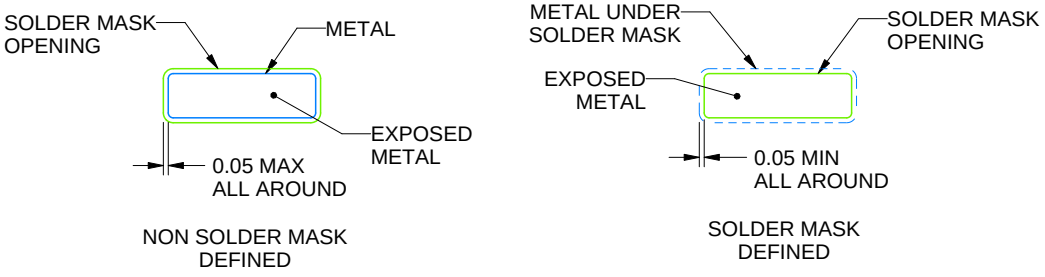
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:10X

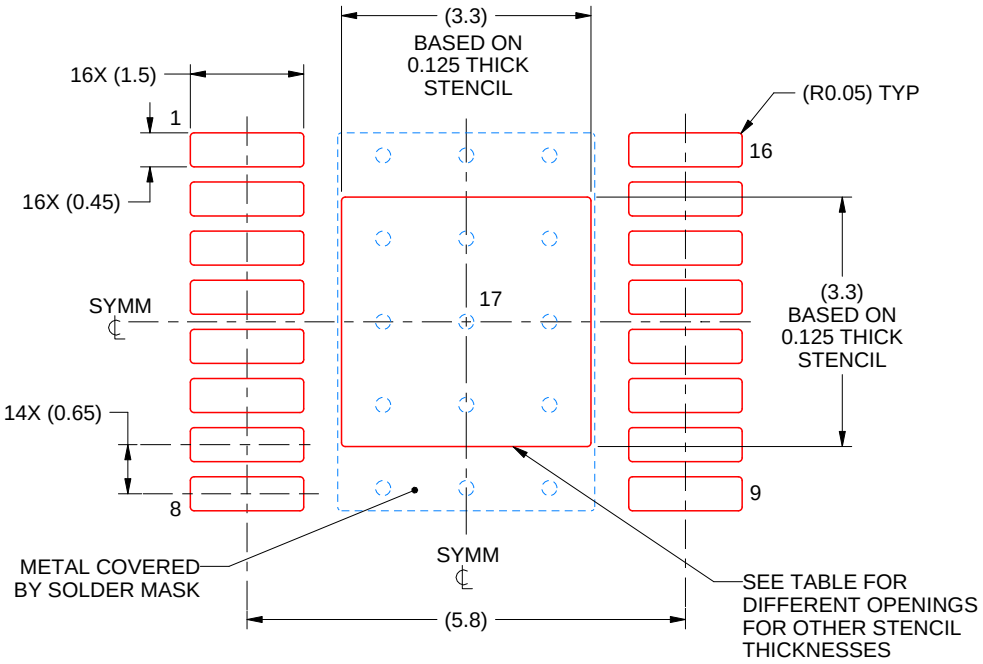


SOLDER MASK DETAILS
PADS 1-16

4214868/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.69 X 3.69
0.125	3.3 X 3.3 (SHOWN)
0.15	3.01 X 3.01
0.175	2.79 X 2.79

4214868/A 02/2017

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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Optimize Your Supply Chain with WIN SOURCE Solutions

- Global Sourcing Solution
- Obsolete Management
- Cost Control Management
- Shortage Management
- Alternative Solution
- Excess Inventory Management