THE DATASHEET OF

LM9011M/NOPB

LM9011 Electronic Ignition Interface

Check for Samples: LM9011

FEATURES

- **Single 5V Supply Operation**
- **VR Sensor Interface with Dynamic Hysteresis**
- **Four Channel Electronic Timing Spark Driver with Output Diagnostics**
- **Electronic Timing Interface Spark Driver Output Voltage from 5V to 16V**
- **One Non-Inverting Voltage Comparator with Hysteresis**
- **Three Inverting Voltage Comparators with Hysteresis**

DESCRIPTION

The LM9011 is an interface circuit which integrates the timing detection and logic control functions required for an automotive electronic ignition system into one device.

A VRS interface is provided for crankshaft position information via a toothed-wheel.

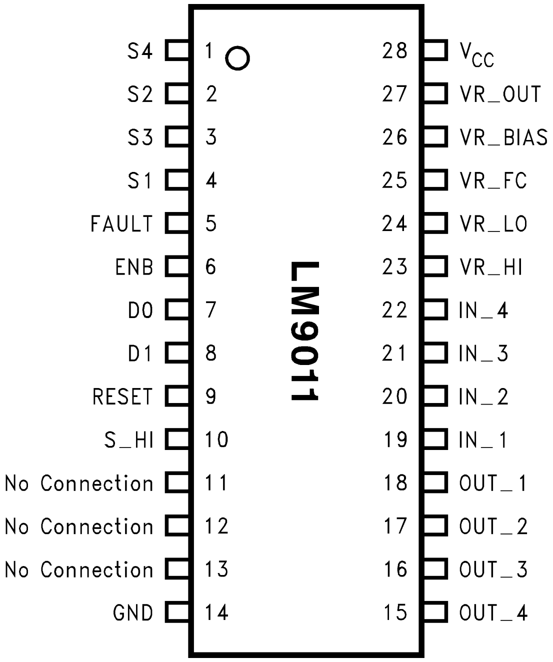
Four voltage comparators are provided for hardware diagnostics.

An electronic timing interface with output fault diagnostics is provided to enable a micro-processor to drive an external four channel ignition spark circuit.

The LM9011 is fully specified over the automotive temperature range of -40°C to +125°C, and is available in a 28 pin Small Outline surface mount package.

Connection Diagram

Top View



28 Pin SOIC
See Package Number DW

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)

Voltage	-0.3V to +7.0V
S_HI Voltage	-0.3V to 26.5V
VR_HI and VR_LO Inputs	+/-3mA
Comparator Inputs	-0.3V to +7.0V
Timing Interface Inputs	-0.3V to +7.0V
ESD Susceptibility(2)	+/-2000V
Maximum Junction Temperature	150°C
Storage Temperature Range	-65°C to +150°C
Lead Soldering Information:	
Vapor Phase (60 Seconds)	215°C
Infrared (15 Seconds)	220°C

(1) Absolute Maximum Ratings indicate the limits beyond which damage may occur.
(2) ESD Ratings is with Human Body Model: 100pF discharged through a 1500Ω resistor.

Operating Ratings(1)

V_{CC} Voltage	4.75V to 5.25V
S_HI Voltage	V_{CC} to 26V
Sx Outputs	-0.3V to S_HI +0.3V
Comparator Inputs VR_HI and VR_LO Inputs	-0.3V to V_{CC} +0.3V +/-2.75mA
Timing Interface Inputs	-0.3V to V_{CC} +0.3V
Thermal Resistances (DW):	
Junction to Case (θJ-C)	15°C/W
Junction to Ambient (θJ-C)	69°C/W

(1) Operating ratings indicate conditions for which the device is intended to be functional, but may not meet the ensured specific performance limits. For ensured specifications and conditions, see the Electrical Characteristics.

DC Electrical Characteristics

The following specifications apply for V_{CC} = 5V, V_{RESET} = V_{CC}, V_{S_HI} = V_{CC}, -40°C ≤ T_A ≤ +125°C, Typical Application Circuit, Figure 24, unless otherwise specified.

Symbol	Parameter	Conditions	Minimum	Maximum	Units
I_{CC}	Supply Current	RESET, IN_4 = V_{CC}		25	mA
		ENB, D0, D1, IN_1, IN_2, IN_3 = 0V			
		VR_HI = +12.5μA			
		VR_LO = -12.5μA			
Comparators					
V_{TH}1	Input Threshold	V_{IN} _1 Decreasing from V_{CC} to 0V until V_{OUT}_1 > V_{CC}/2	V_{CC} X 0.435	V_{CC} X 0.485	V
V_{TH}2	Input Threshold	V_{IN}_2 Decreasing from V_{CC} to 0V until V_{OUT}_2 > V_{CC}/2	V_{CC} X 0.435	V_{CC} X 0.485	V
V_{TH}3	Input Threshold	V_{IN}_3 Decreasing from V_{CC} to 0V until V_{OUT}_3 > V_{CC}/2	V_{CC} X 0.40	V_{CC} X 0.45	V
V_{TH}4	Input Threshold	V_{IN}_4 Decreasing from V_{CC} to 0V until V_{OUT}_4 < V_{CC}/2	V_{CC} X 0.45	V_{CC} X 0.50	V
V_{HYST}	Input Hysteresis	All Comparators	150	400	mV
I_{BIAS}	Input Bias Current	IN_1, IN_2, IN_3 = 0V ≤ V_{IN}≤V_{CC} IN_4 = 0V ≤ V_{IN}_4 ≤ V_{CC}-1V		750	μA
V_{OH}	Output High Voltage	I_{LOAD} = -100μAV	V_{CC} -1		V
V_{OL}	Output Low Voltage	I_{LOAD} = +100μAV		750	mV
VR Sensor Interface					
V_{OH}	Output High Voltage	I_{LOAD} = -15μA VR_HI= -1mA, VR_LO = +1mA	V_{CC} -1		V
V_{OL}	Output Low Voltage	Load = +15μA VR_HI=+1mA, VR_LO = -1mA		750	mV
$I_{DIFF(MIN)}$	Minimum Detect Differential Input Current(1)	-40°C ≤ T_A≤ +25°C	0.5	3.0	uA Pk-Pk
		T_A = +85°C(1)	0.6	3.5	uA Pk-Pk
		T_A = +125°C	1.0	5.0	uA Pk-Pk
I_{HYS}1	Input Hysteresis(2)	I_{DIFF} = 1mA pk-pk	75	250	uA Pk
I_{HYS}2	Input Hysteresis(2)	I_{DIFF} = 2.5mA pk-pk	185	625	uA Pk
Electronic Timing Interface					
V_{IH}	Input Logic 1 D0, D1, ENB, RESET		V_{CC} X 0.7		V
V_{IL}	Input Logic 0 D0, D1, ENB, RESET			V_{CC} X 0.3	V
I_{IH}	Input High Current Inputs D0, D1, RESET	V_{IN} = V_{CC}		10	μA
I_{IH}	Input High Current Input ENB	V_{IN} = V_{CC}		125	μA
I_{IL}	Input Low Current Inputs D0, D1, ENB	V_{IN} = 0V		-10	μA
I_{IL}	Input Low Current Input RESET	V_{IN} = 0V		-125	μA
V_{OH}	Output High Voltage Outputs S1, S2, S3, S4	I_{LOAD} = -10mA, V_{S_HI} = 5V	3.75		V
V_{OL}	Output Low Voltage Outputs S1, S2, S3, S4	I_{LOAD} = 1mA, $V_{S\_ HI}$ = 5V		300	mV
V_{OH}	Output High Voltage Outputs S1, S2, S3, S4	I_{LOAD} = -10mA, V_{S_HI} = 16V	14		V
V_{OL}	Output Low Voltage Outputs S1, S2, S3, S4	I_{LOAD} = 1mA, V_{S_HI} =16V		450	mV
V_{OH}	Output High Voltage Outputs S1, S2, S3, S4	I_{LOAD} = -10mA, V_{S_HI} =26V	22		V

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(1) Minimum Detect Current is not production tested at +85C. Specifications are ensured through device characterization and Test Limits at 25°C and 125°C.

(2) Tested per VR Sensor Interface test circuit. See Figure 17 and Figure 18.

DC Electrical Characteristics (continued)

The following specifications apply for V_{CC} = 5V, V_{RESET} = V_{CC}, V_{S_HI} = V_{CC}, -40°C ≤ T_A ≤ +125°C, Typical Application Circuit, Figure 24, unless otherwise specified.

Symbol	Parameter	Conditions	Minimum	Maximum	Units
V_{OL}	Output Low Voltage Outputs S1, S2, S3, S4	I_{LOAD} = 1mA, V_{S_HI} =26V		600	mV
V_{OH}	FAULT Pin Output High Voltage	I_{FAULT} = -100µA, no fault	V_{CC} -1		V
V_{OL}	FAULT Pin Output Low Voltage	I_{FAULT} = 100µA, any fault		750	mV
V_{FAULT}	Fault Treshold Voltage Outputs S1, S2, S3, S4	Sx Output Short Fault	V_{CC} X 0.2	V_{CC} X 0.5	V
I_{FOL}	Tri-State Output Current Outputs S1, S2, S3, S4	V_{RESET} = 0V, V_{S_HI} = 5V R_{LOAD} = 10KΩ	-12	-50	µA

AC Electrical Characteristics

The following specifications apply for V_{CC} = 5V, V_{S_HI} = V_{CC}, V_{RESET} = V_{CC}, -40°C≤T_A≤+125°C. The AC Timing Characteristics are not production tested. Minimum and Maximum limits are ensured by device characterization.

Symbol	Parameter	Conditions	Minimum	Maximum	Units
Comparators					
T_{RISE}	Output Rise Time	10% to 90%, C_{LOAD} = 25pF		5	µs
T_{FALL}	Output Fall Time	90% to10%, C_{LOAD} = 25pF		5	µs
VR Sensor Interface (1)					
T_{RISE}	Output Rise Time	10% to 90%, C_{LOAD} = 100pF, R_{LOAD} = 100KΩ		10	µs
T_{FALL}	Output Fall Time	90% to10%, C_{LOAD} = 100pF, R_{LOAD} = 100kΩ		5	µs
T_{DELAY}	Zero Crossing Delay Time (2)	I_{DIFF} = 5µA pk-pk, F_{VRS} = 200Hz		1	ms
		I_{DIFF} = 50µA pk-pk, F_{VRS} = 2.5KHz		10	µs
F_{MAX}	Maximum VRS Frequency	C_{LOAD} = 100pF, R_{LOAD} = 100KΩ I_{DIFF} = 5µA pk-pk		50	KHz
Electronic Timing Interface					
$T_{RISE}1$	Sx Output Rise Time	Sx Rises10% to 90%			
		C_{LOAD} = 6.8nF, R_{LOAD} = 10KΩ		5	µs
		C_{LOAD} = 12.7nF, R_{LOAD} = 10KΩ		8	µs
$T_{FALL}1$	Sx Output Fall Time	Sx Falls 90% to 10%			
		C_{LOAD} = 6.8nF, R_{LOAD} = 10KΩ		15	µs
		C_{LOAD} = 12.7nF, R_{LOAD} = 10KΩ		25	µs
T_{SETUP}	SetupTime (3) (4) (5)		1		µs
T_{HOLD}	Hold Time		0.5		µs
$T_{DF}1$	Fault Delay Time	Sx Output Short to Ground Fault From ENB = 1 to FAULT ≤ 10%			
		C_{FAULT} = 25pF		2	µs
$T_{DF}2$	Fault Delay Time	Sx Output Short to Battery Fault From ENB = 0 to FAULT ≤ 10%			
		C_{FAULT} = 25pF		2	µs
T_{TRI}	Tri-State Delay Time	From RESET = 0 to All Sx Outputs Off		2	µs
T_{RISE} 2	Fault Pin Rise Time	10% to 90%, C_{FAULT} = 25pF		5	µs
$T_{FF(OFF)}$	False Fault Time	From ENB = 0 to FAULT ≥ 90%			
		C_{FAULT} = 25pF			
		C_{LOAD} = 6.8nF, R_{LOAD} = 10KΩ		25	µs
		C_{LOAD} = 12.7nF, R_{LOAD} = 10KΩ		30	µs
$T_{FF(ON)}$	False Fault Time	From ENB = 1 to FAULT ≥ 90%			
		C_{FAULT} = 25pF			
		C_{LOAD} = 6.8nF, R_{LOAD} = 10KΩ		8	µs
		C_{LOAD} = 12.7nF, R_{LOAD} = 10KΩ		10	µs
T_{UDF}	Undefined Fault Time	From ENB = 0 for 8uSec, to Valid FAULT			
		C_{LOAD} = 6.8nF, R_{LOAD} = 10KΩ		20	µs
		C_{LOAD} = 12.7nF, R_{LOAD} = 10KΩ		25	µs

(1) Tested per VR Sensor Interface test circuit. See Figure 17 and Figure 18.
(2) VR Sensor Interface Tdelay, measured from VR input sine wave zero-crossing to VR_OUT going high. See Figure 18.
(3) Electronic Timing Interface Tsetup, minimum time between Vcc > 4.75V and RESET = 1.
(4) Electronic Timing Interface Tsetup, minimum time between RESET = 1 and D0 = 1.
(5) Electronic Timing Interface Tsetup, minimum time between D0 / D1 = valid and ENB = 1.

Typical Performance Characteristics

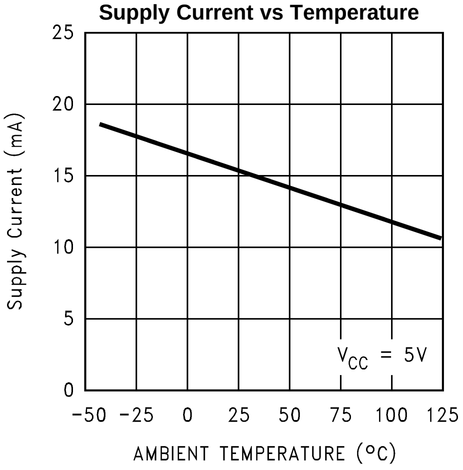

Figure 1.

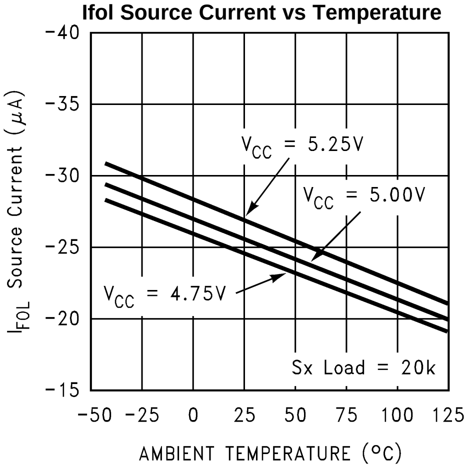

Figure 2.

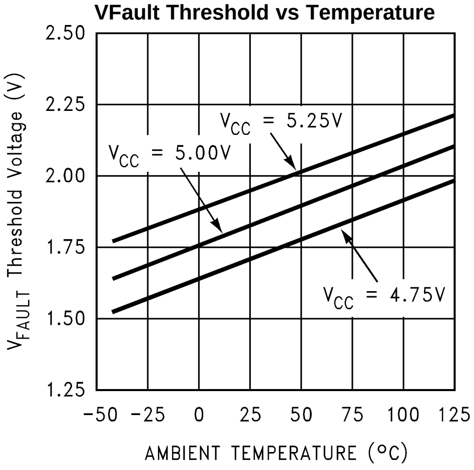

Figure 3.

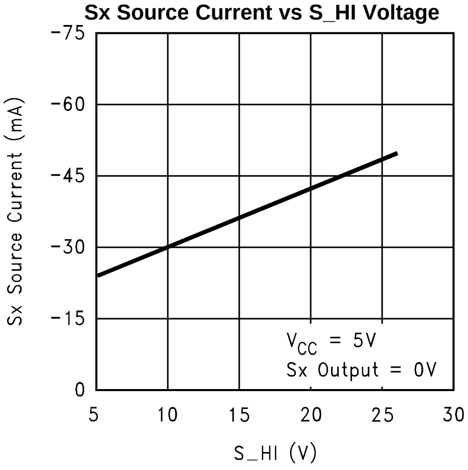

Figure 4.

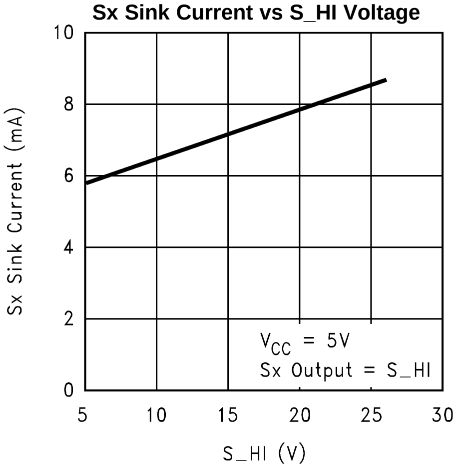

Figure 5.

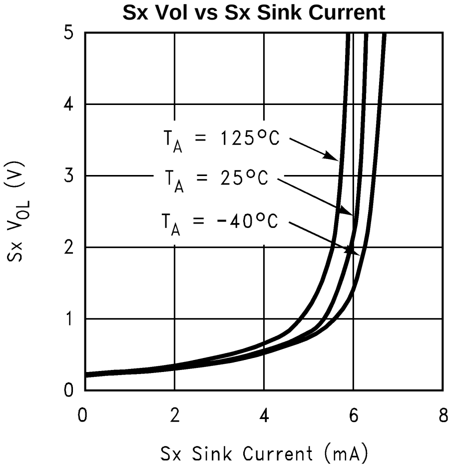

Figure 6.

Typical Performance Characteristics (continued)

Sx Voh vs Sx Source Current

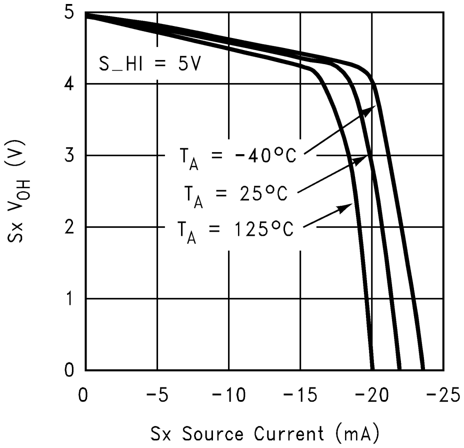

Figure 7.

VRS Interface Minimum Detect vs Temperature

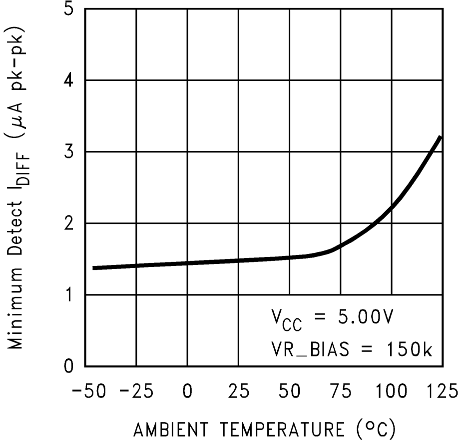

Figure 8.

VRS Interface Minimum Detect vs VR_BIAS

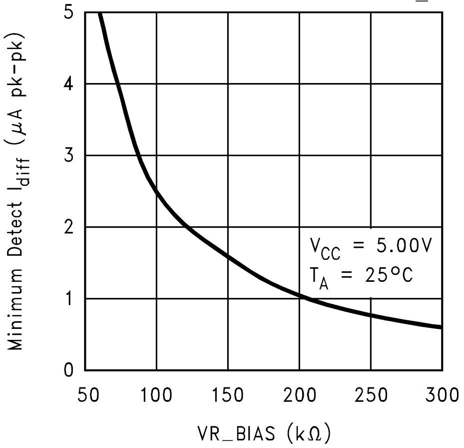

Figure 9.

TEST CIRCUIT DIAGRAMS

Timing Diagrams

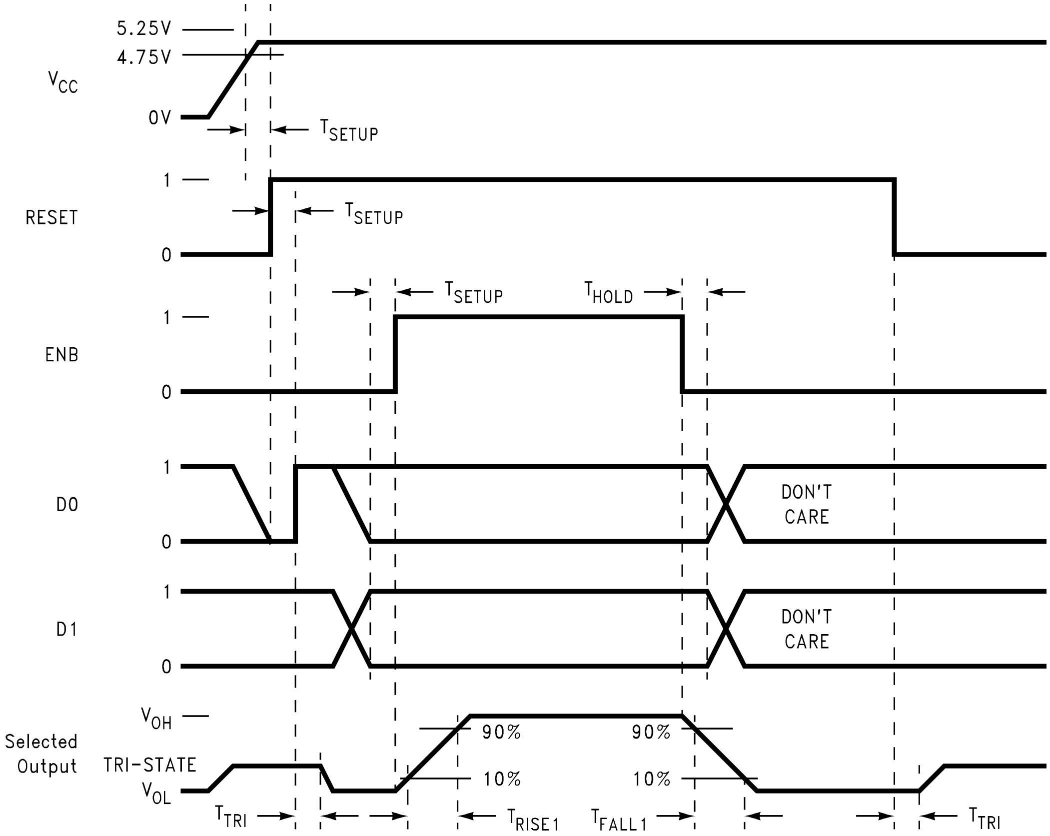

Figure 10. Electronic Timing Interface Timing Diagram

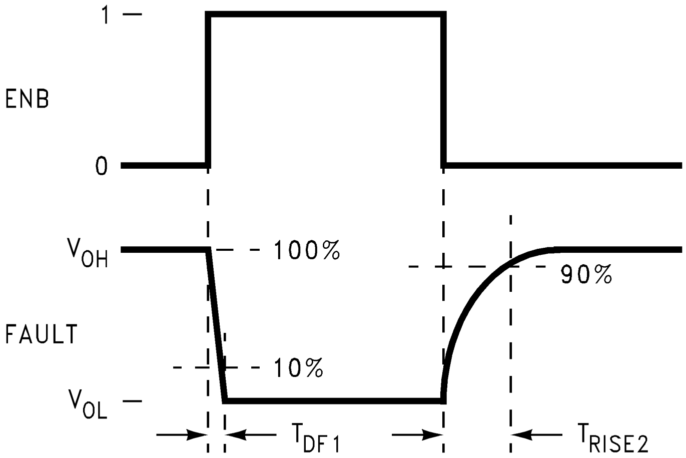

Figure 11. Fault Pin Timing During Sx Shorted to Ground

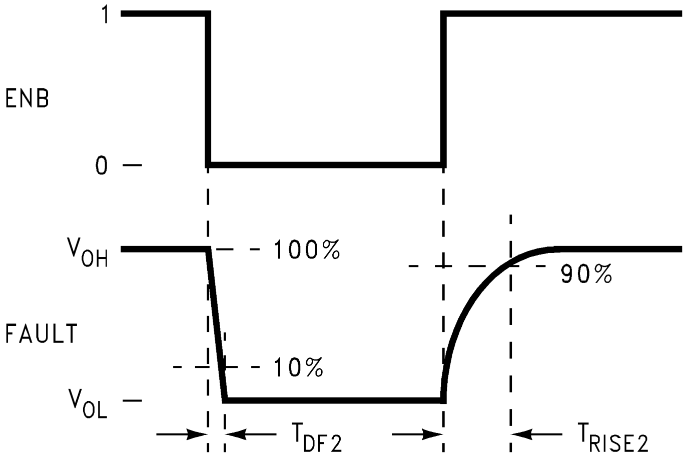

Figure 12. Fault Pin Timing During Sx Shorted to Battery

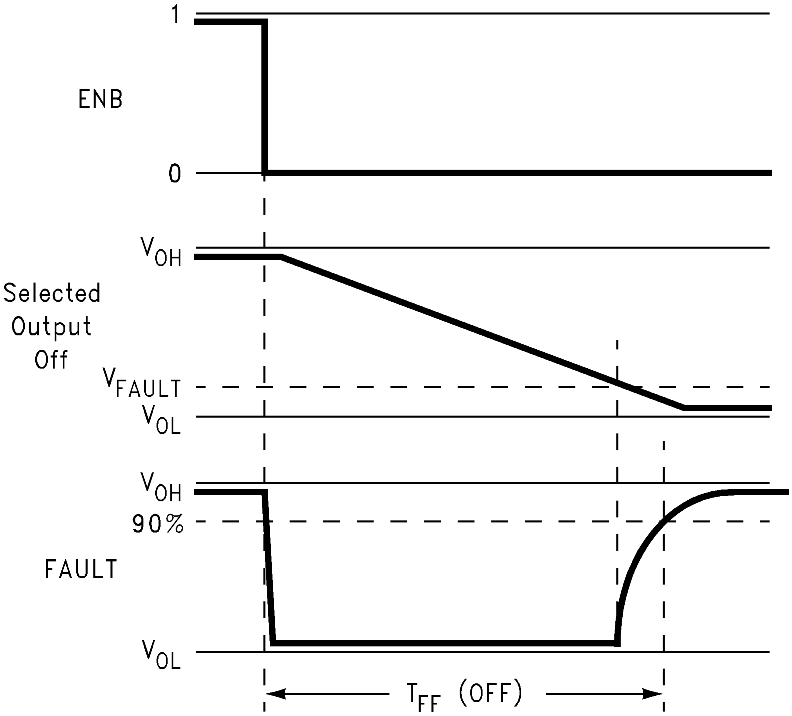

Figure 13. False FAULT Time for Disabled Sx Output

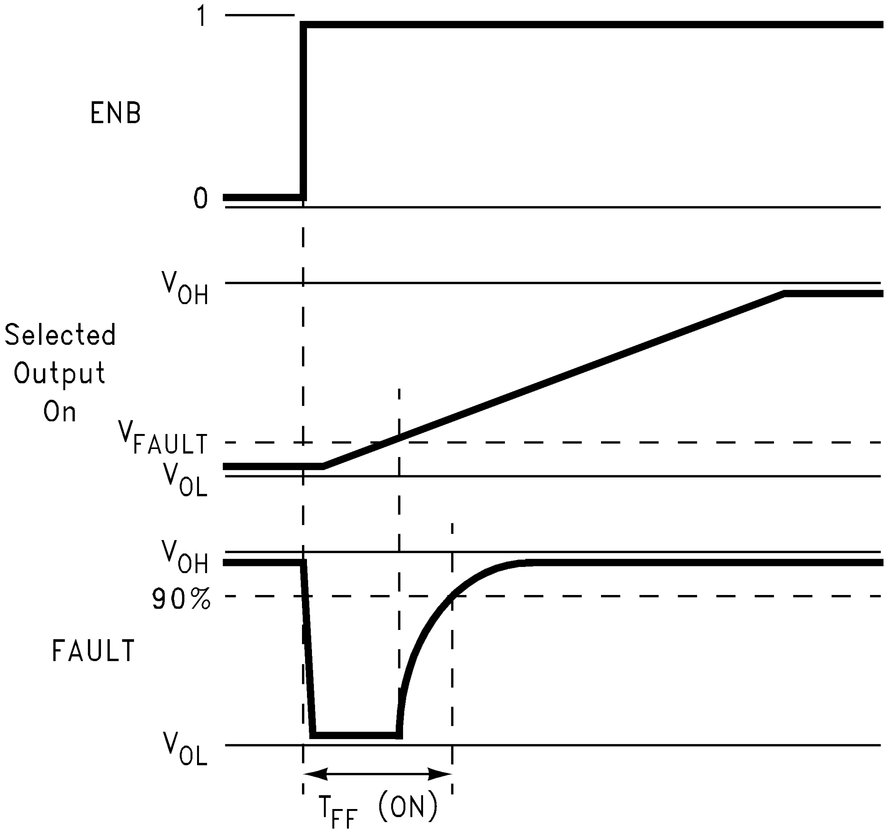

Figure 14. False FAULT Time for Enabled Sx Output

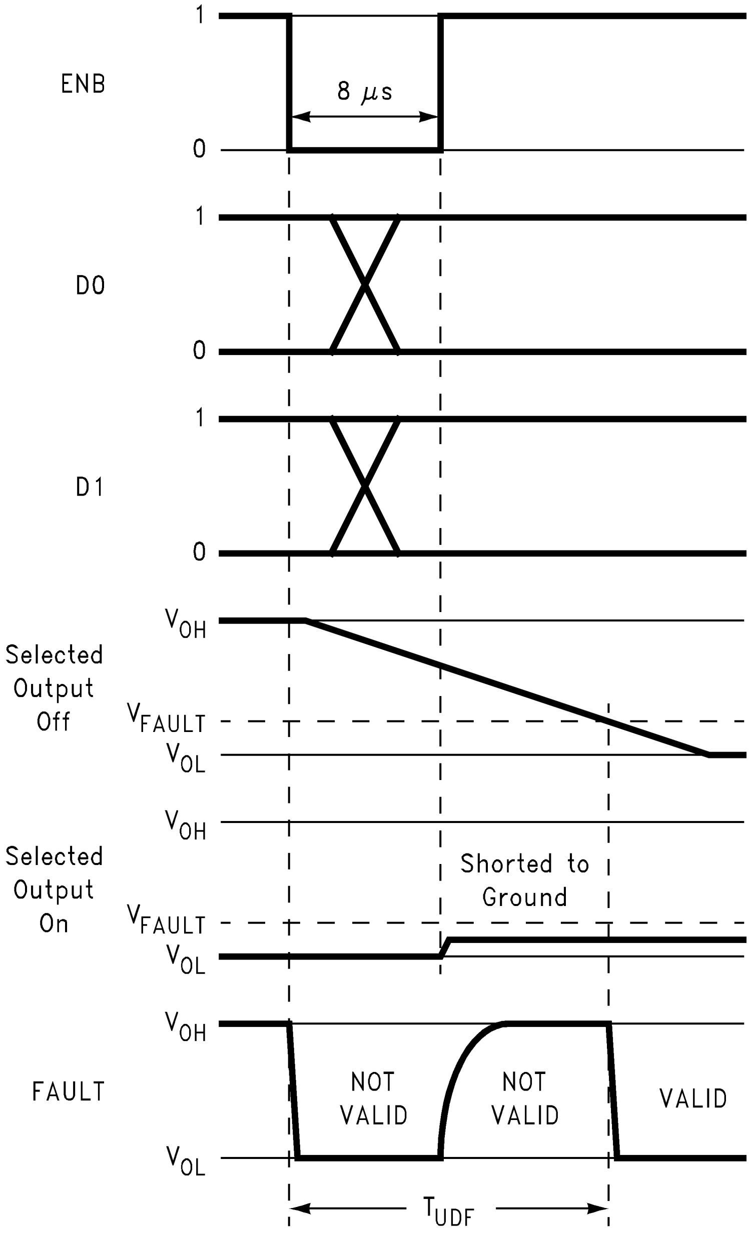

Figure 15. Time for Valid Fault Detection

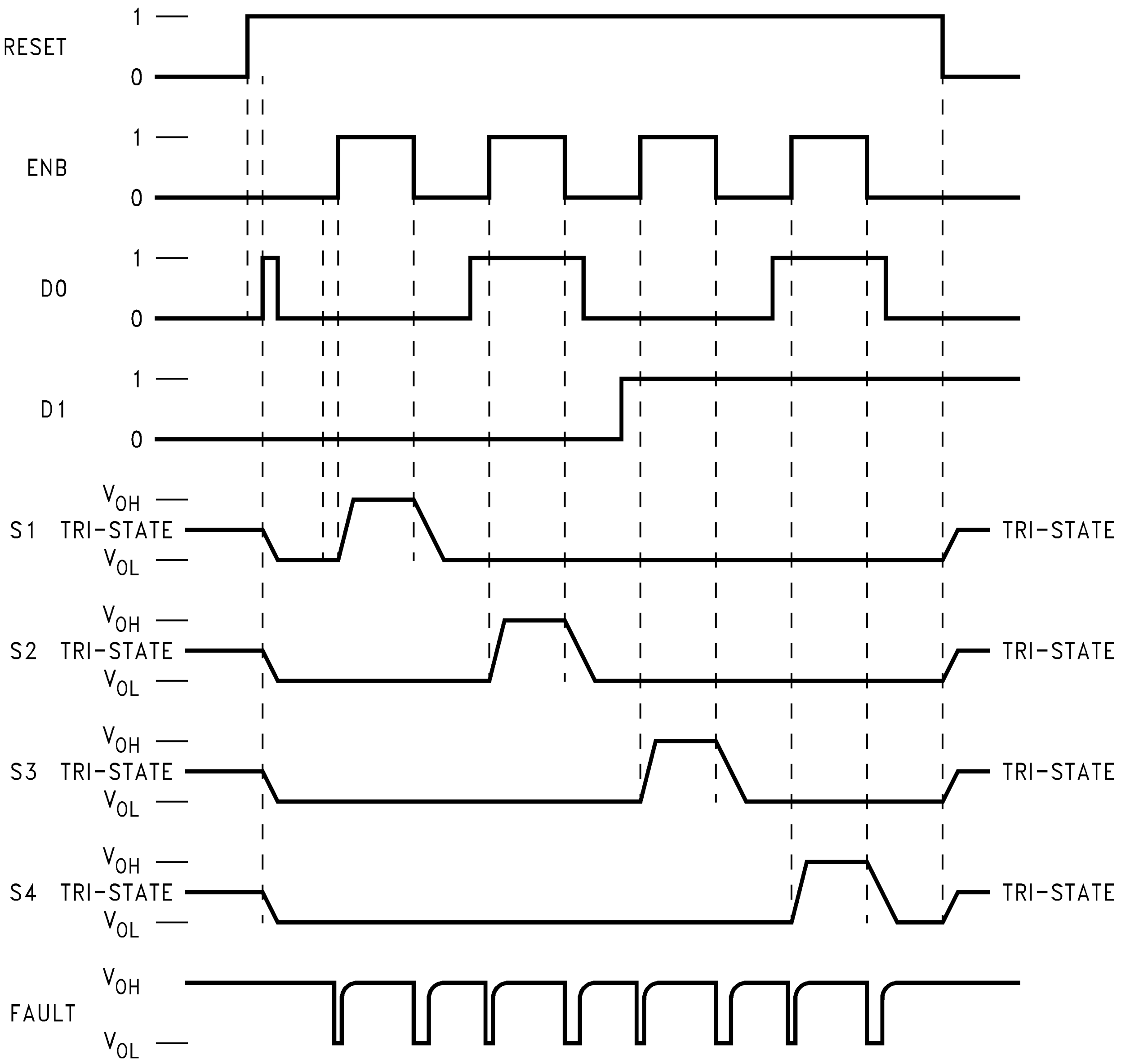

Figure 16. Electronic Timing Interface Typical Waveforms

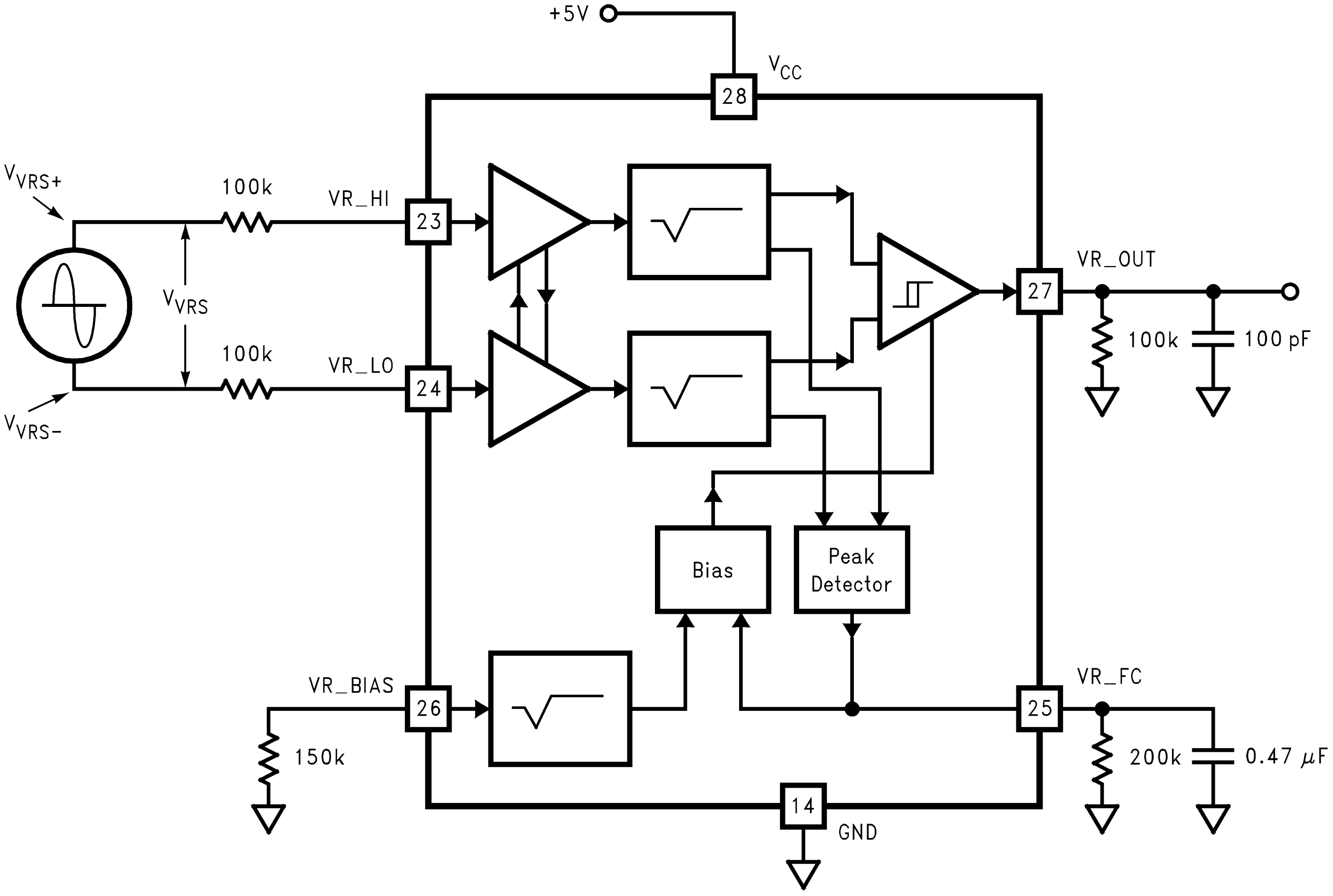

Figure 17. VR Interface Test Circuit

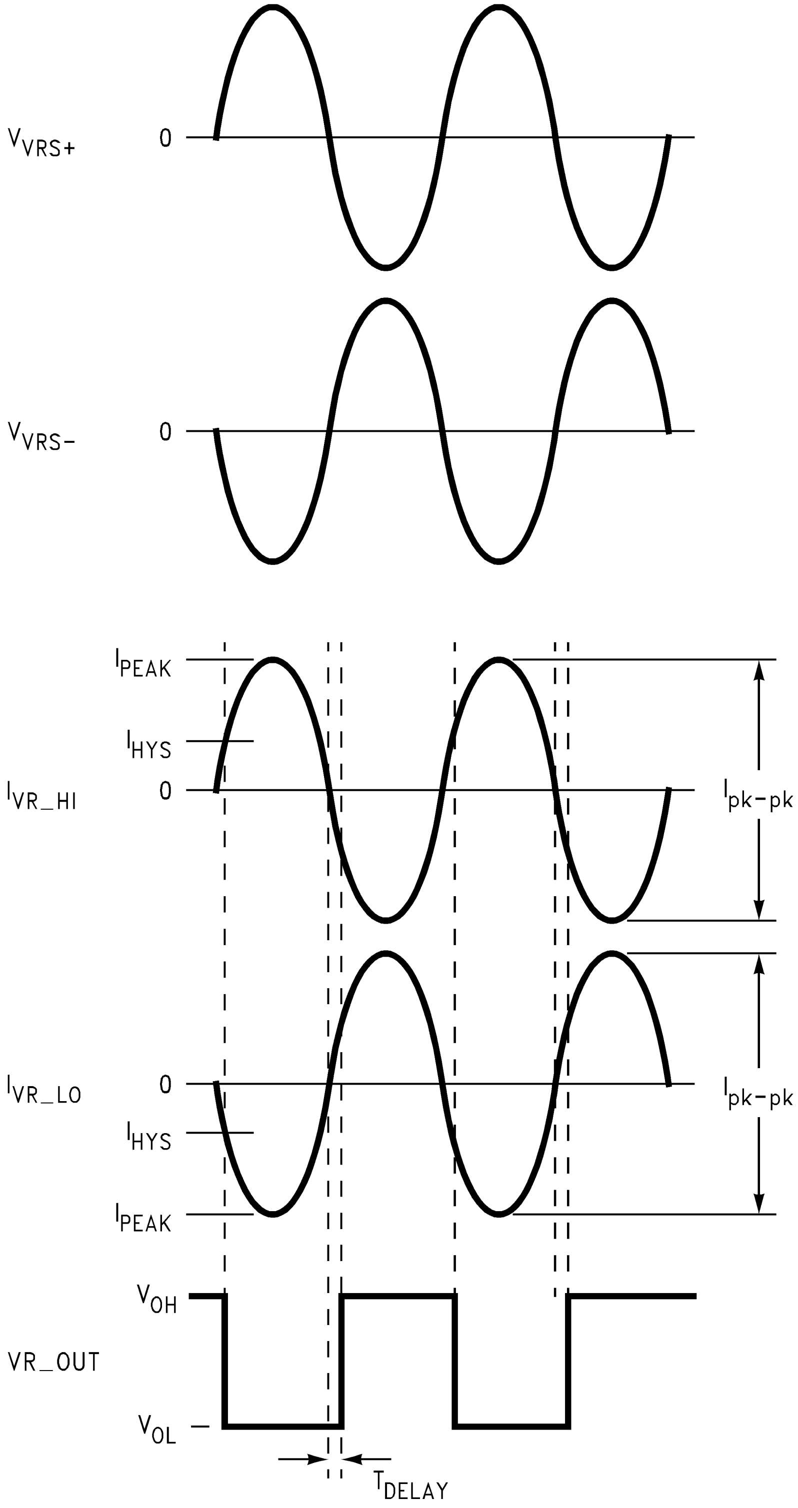

Figure 18. VR Interface Timing Diagram

CIRCUIT DESCRIPTION

VR SENSOR INTERFACE

The differential inputs, VR_HI and VR_LO are low impedance inputs with a DC voltage bias of one half of Vcc, Both inputs require equal value series resistance on their respective pins to convert the VR sensor voltage to a differential input current. The differential input current range is typically 2.5µA peak-to-peak to 2.5mA peak-to-peak. Each input has active current limiting that will clamp the current at typically +/-5mA. This is intended for short circuit protection and not for input signal limiting.

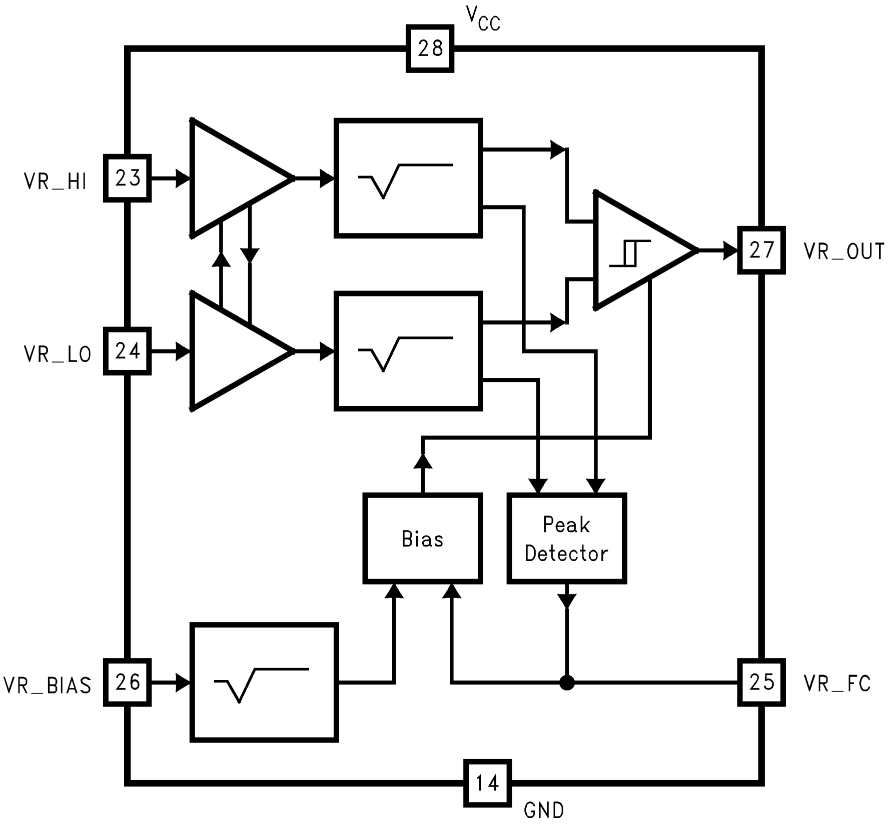

Figure 19. VR Sensor Interface Block Diagram

Differential voltages of 500mV peak-to-peak to 500V peak-to-peak can be processed with the specified 100KΩ series resistor on each input. Numerous variables will determine the output voltage signal from a VR sensor across a frequency range. The input resistors can be scaled from typically 50KΩ to 200KΩ to keep the differential input current with-in the recommended range for a given VR Sensor output voltage. Bypass capacitors can be added to form a low pass filter to limit the differential input signal at the higher frequencies.

The VR Sensor interface utilizes a dynamic hysteresis which will increase the hysteresis level as the input signal from the VR Sensor increases. The circuit requires two external components to fully implement the hysteresis function: a capacitor on VR_FC to filter and store the peak detector signals; and a 150KΩ resistor on VR_BIAS to set a reference current for the hysteresis circuit. The typical value range for the peak detector storage capacitor is 0.1µF to 0.47µF.

The peak detector has an internal 3KΩ (typical) current limiting resistor to Vcc for charging the storage capacitor. An external resistor in parallel with the peak detector storage capacitor is used to set the RC discharge rate of the peak detector capacitor.

For input levels greater than typically 10µA peak-to-peak the voltage on the peak detector output pin VR_FC is used to actively derive the hysteresis level. The active hysteresis will typically be 30% of the peak input signal. As the input level falls below typically 10µA peak-to-peak the hysteresis level will begin to rise as the static hysteresis level takes effect. The static hysteresis level is set by the current out of the VR_BIAS pin and is a constant level of typically 1µA peak with a VR_BIAS resistor of 150KΩ. This static hysteresis level acts as the minimum detect threshold as there will be no output if the input signal is not greater than the static hysteresis level.

The VR_BIAS resistor can be scaled from typically 50KΩ to 500KΩ, but the practical range is typically 75KΩ to 300KΩ. Increasing the resistance (i.e. reducing the current) will lower the minimum hysteresis level. Conversely, reducing the resistance will raise the minimum hysteresis level. Since the VR_BIAS current is modified by the same square root circuit used for the input signal, the relationship between the VR_BIAS resistor value and the minimum detect level is not linear. For VR_BIAS values greater than 500KΩ, the minimum detect level is typically determined more by the internal device offsets, and thermal effects.

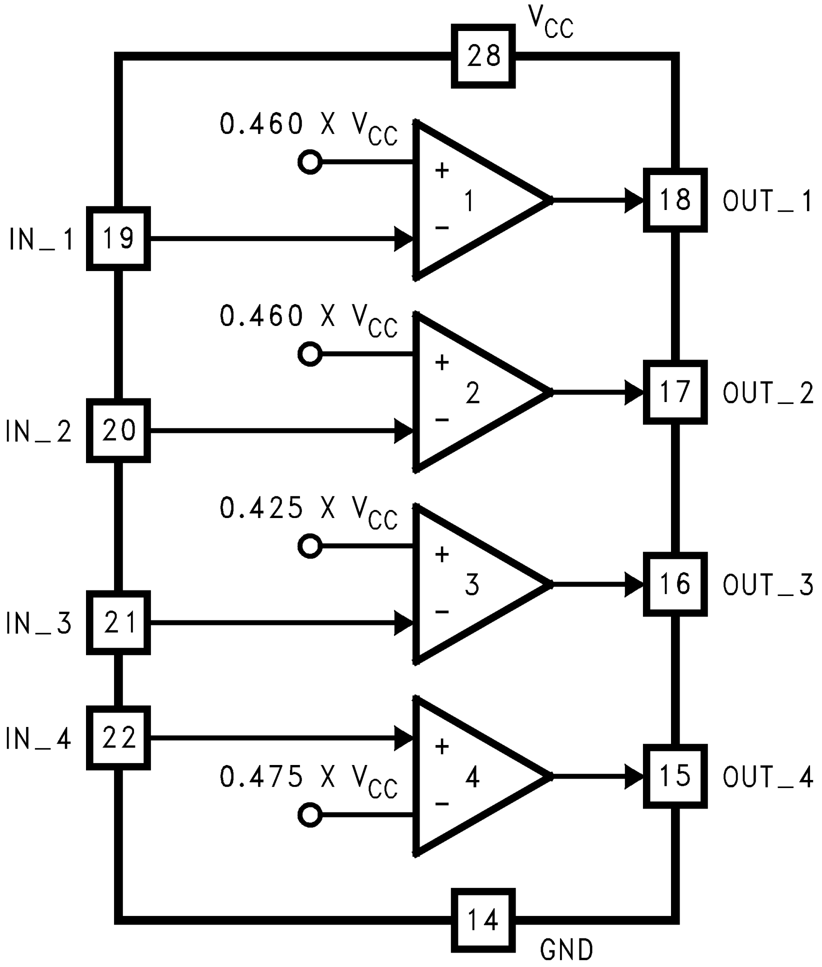

Figure 20. Voltage Comparator Block Diagram

VOLTAGE COMPARATORS

The circuit includes four general purpose voltage comparators that use an internal reference voltage to set their voltage thresholds. Three of the comparators have their non-inverting inputs tied to the internal reference voltage, and their inverting-inputs are brought out. The remaining one comparator has its inverting input tied to the internal voltage reference, and its non-inverting input is brought out. All four comparators include hysteresis to improve noise immunity. The comparator outputs are internally pulled up to V_{CC}. Any un-used comparator should have its input connected to device ground.

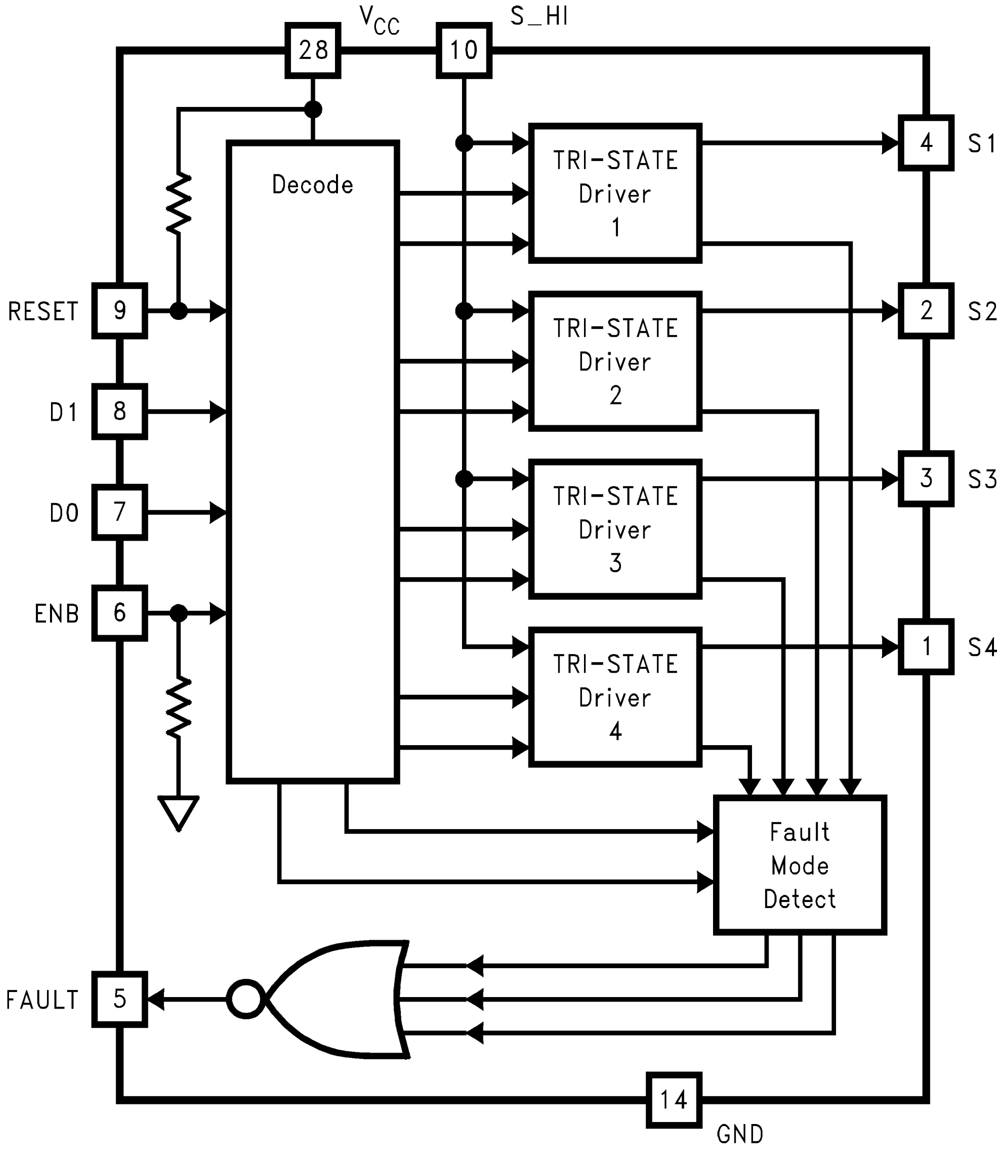

Figure 21. Electronic Timing Interface Block Diagram

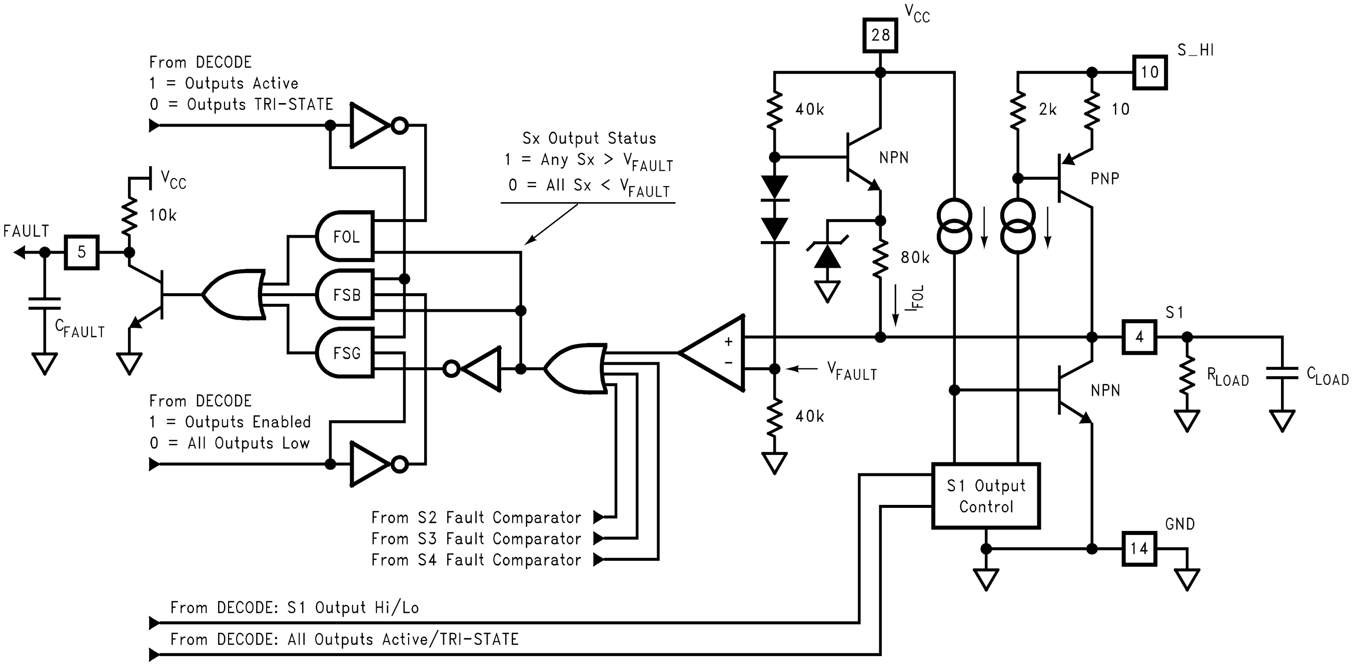

Figure 22. Output Fault Detection Block Diagram

Table 1. Electronic Timing Interface

Inputs				Output			
RESET	ENB	D0	D1	S1	S2	S3	S4
0	X	X	X	Tri	Tri	Tri	Tri
1	0	X	X	L	L	L	L
1	1	0	0	H	L	L	L
1	1	1	0	L	H	L	L
1	1	0	1	L	L	H	L
1	1	1	1	L	L	L	H

The Electronic Timing Interface provide signals to the spark module from the micro-processor. The interface requires four input data signals, and provides four output control channels.

The interface also provides one output channel for diagnostic information for any open or shorted loads on S1 to S4. The RESET pin has an internal pull-up resistor to V_{CC} of typically 100KΩ, and the ENB pin has an internal pull-down resistor to ground of typically 100KΩ.

To put the outputs into the Tri-State mode at power-on, the RESET pin should be held low until V_{CC} is above 4.75V. This can be accomplished by micro-processor control, or by adding a capacitor from the RESET pin to ground.

The RESET pin is used to disable the spark driver outputs by putting them in a Tri-State mode. While in the Tri-State mode the Open Output Fault detection circuitry is active. An open Output is detected by forcing a small current (I_{FOL}) through the outputs to the loads, and monitoring the voltage on the output pins rises above the Output Fault Threshold Voltage (V_{FAULT}) the FAULT pin will be forced low. The intent is to detect an open wire condition, and not necessarily to detect a local resistance threshold.

Note that if any output has a Short to battery fault, the fault pin will go low during this Tri-State mode. The internal comparator is unable to discern why an output pin may be above the Fault Threshold Voltage, only that it is. In any case, a fault is reported, even if it is not the anticipated fault.

The Tri-State mode is a latched condition. For the outputs to come out of the Tri-State mode, the RESET pin must be high, and then the data input pin D0 must toggle from a low state to a high state. The state of the outputs will now be set by the data inputs D0 and D1, and the ENB input. If ENB is low when the Tri-State mode is cleared, all of the outputs will go low.

Pins D0 and D1 are used select an output, and ENB will enable the selected output. The outputs have have active pull up to S_HI, and the active pull down to Ground. The default not enabled output conditions is low, and the enabled output condition is high. Only one output can be enabled (high) at a time. The outputs are not latched in any state and will follow the input selected with D0 and D1 as long as ENB is high.

The detection of an output shorted to ground, or battery, is dependent on the status of ENB. While ENB is logical 0, all of the outputs are forced low and the Short to Battery fault detection circuitry is active. A Short to Battery is detected by monitoring the voltage on the output pins. If the voltage on any output pin is above the Fault Threshold Voltage (V_{FAULT}) the FAULT pin will go low. The output current sink is limited to typically 8mA. The short to battery condition must be able to provide enough current to overcome the current limit and raise the output pin voltage above the V_{FAULT} threshold.

When ENB is logical 1, the selected output will be high and the Short to Ground detection circuitry is active. A Short to Ground is detected by monitoring the voltage on the output pins. If the voltage on the selected output pin is below the Fault Threshold Voltage (V_{FAULT}) the FAULT pin will go low. The output current source is from S_HI limited to typically 25mA to 50mA across the S_HI voltage range. The short to ground condition must be allow enough resistance to allow the output pin voltage to fall below the V_{FAULT} threshold with the output sourcing short circuit current. Typically, a short to ground which has 100 Ohms of resistance, or more, can not be reliably detected. Typically, a short to ground of 20 Ohms, or less, can be reliably detected across the entire S_HI voltage range and device operating temperature range. Note that if any output has a Short to Battery fault, a Short to Ground cannot be detected.

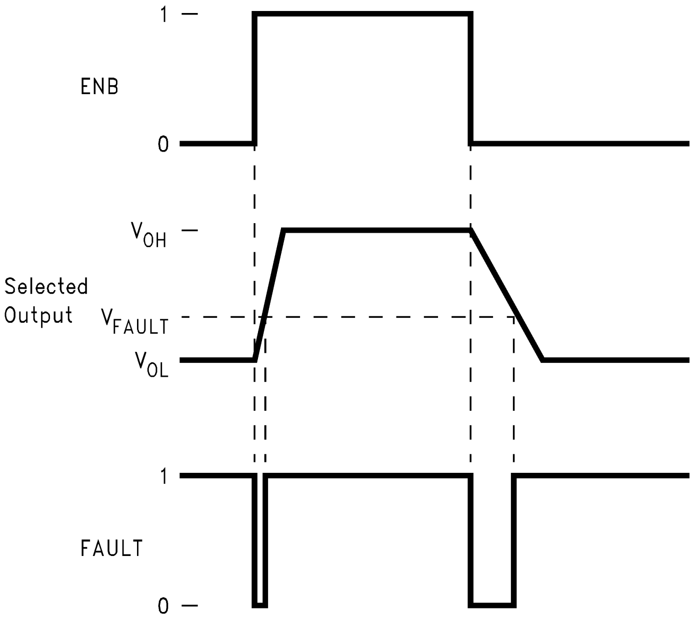

Figure 23. FAULT Pin Output During Normal Operation

The internal logic is unable to discern which output pin is above the Fault Threshold Voltage, only that a pin is. Thus, the logical requirement of an Sx pin voltage above the Fault Threshold voltage is met and no fault is reported.

The output rise and fall times are basically a function of the output current drive (source and sink) and the output load characteristics. Due to the scaling of the output stages, and variations in the value of S_HI, the fall time will typically be two to ten times longer than the rise time for a given capacitive load.

Since the output fault detection mode changes immediately with the status of the ENB pin, and the voltage on the output pin cannot change instantly, the FAULT pin will go low during the output transition times. The FAULT pin will stay low until the output voltage rises above, or falls below, the active fault threshold. See Figure 23.

When switching the outputs from the active mode to the Tri-State mode the ENB should be taken low first. This will take all of the outputs low. Then the RESET pin can be taken low. This will eliminate false 'open' faults that will be generated while waiting for the one output that was high, to discharge any capacitance below the V_{FAULT} threshold.

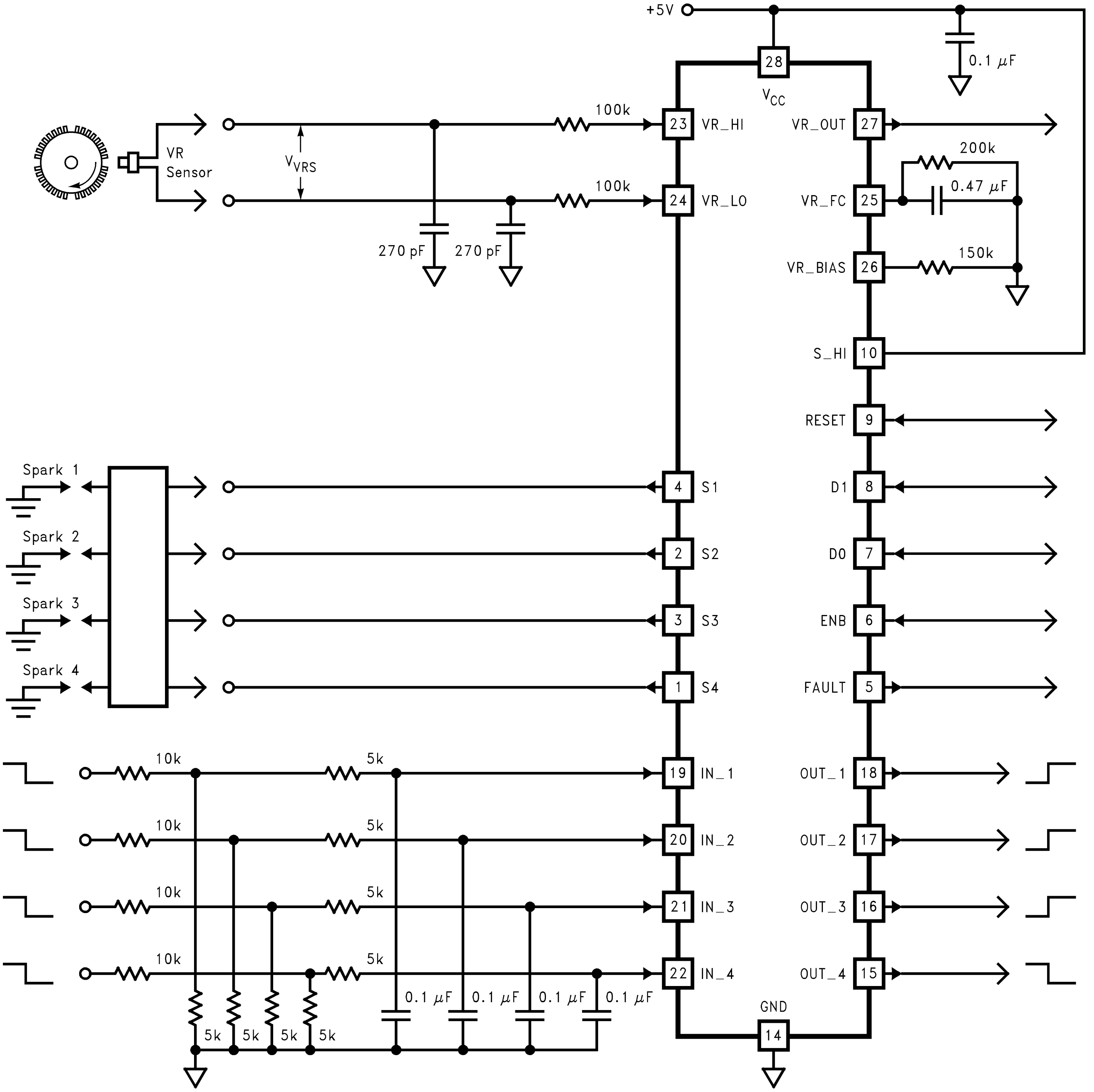

Figure 24. Typical Application

REVISION HISTORY

Changes from Revision C (April 2013) to Revision D **Page**

- Changed layout of National Data Sheet to TI format 21

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