THE DATASHEET OF

LM96550SQ/NOPB

National Semiconductor

October 3, 2011

LM96550

Ultrasound Transmit Pulser

General Description

The LM96550 is an eight-channel monolithic high-voltage, high-speed pulse generator for multi-channel medical ultrasound applications. It is well-suited for use with National's LM965XX series chipset which offers a complete medical ultrasound solution targeted towards low-power, portable systems.

The LM96550 contains eight high-voltage pulsers with integrated diodes generating ±50V bipolar pulses with peak currents of up to 2A and pulse rates of up to 15 MHz. Advanced features include low-jitter and low-phase-noise output pulses ideal for continuous-wave (CW) modes of operation. Active clamp circuitry is integrated for ensuring low harmonic distortion of the output signal waveform.

The LM96550 also featuers a low-power operation mode and over-temperature protection (OTP) which are enabled by on-chip temperature sensing and power-down logic.

Applications

- Ultrasound Imaging

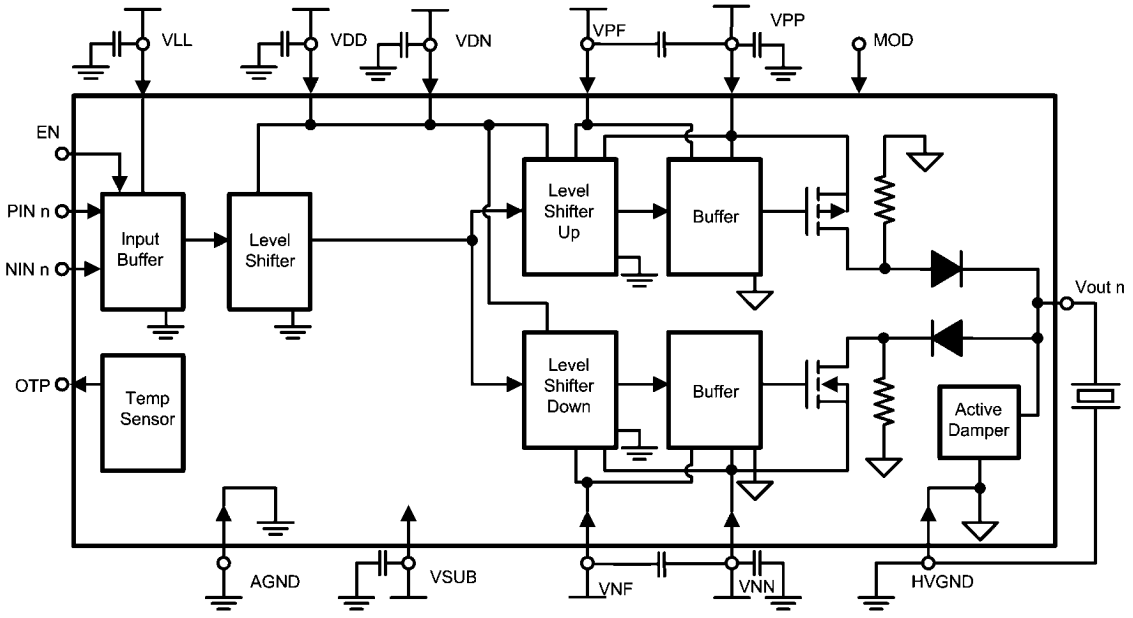
Features

- 8-channel high-voltage CMOS pulse generator
- Output pulses with ±50V and 2A peak current
- Active damper with built-in blocking diodes
- Up to 15 MHz operating frequency
- Matched delays for rising and falling edges
- Low second harmonic distortion allows and improves harmonic imaging
- Continuous-wave (CW) operation down to ±3.3V
- Low Phase noise enables Doppler measurements
- Output state over-temperature protection
- Blocking diodes for direct interface to transducer
- 2.5V to 5.0V CMOS logic interface
- Low-power consumption per channel
- Over Temperature Protection

Key Specifications

Output voltage	±50	V
Output peak current	±2.0	A
Output pulse rate	Up to 15	MHz
Rise/fall delay matching (max)	< 3	ns
Phase Noise (Fin=5MHz, 1KHz offset)	-114	dBc/Hz
Pulser HD2 (5 MHz)	-40	dB
Operating Temp.	0 to +70	°C

Block Diagram



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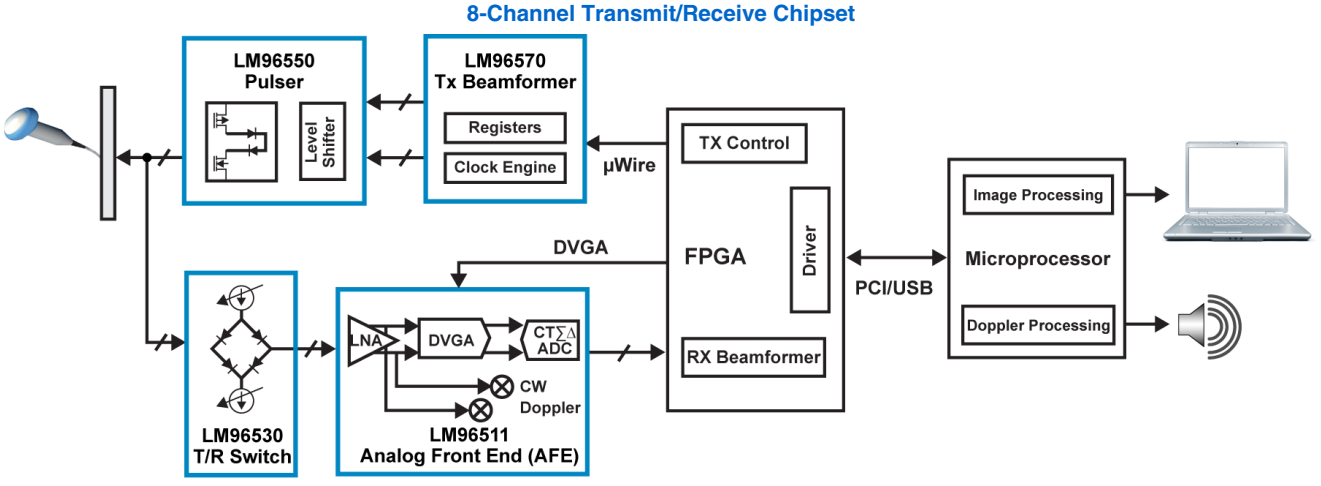
Typical Application



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Pin Diagram

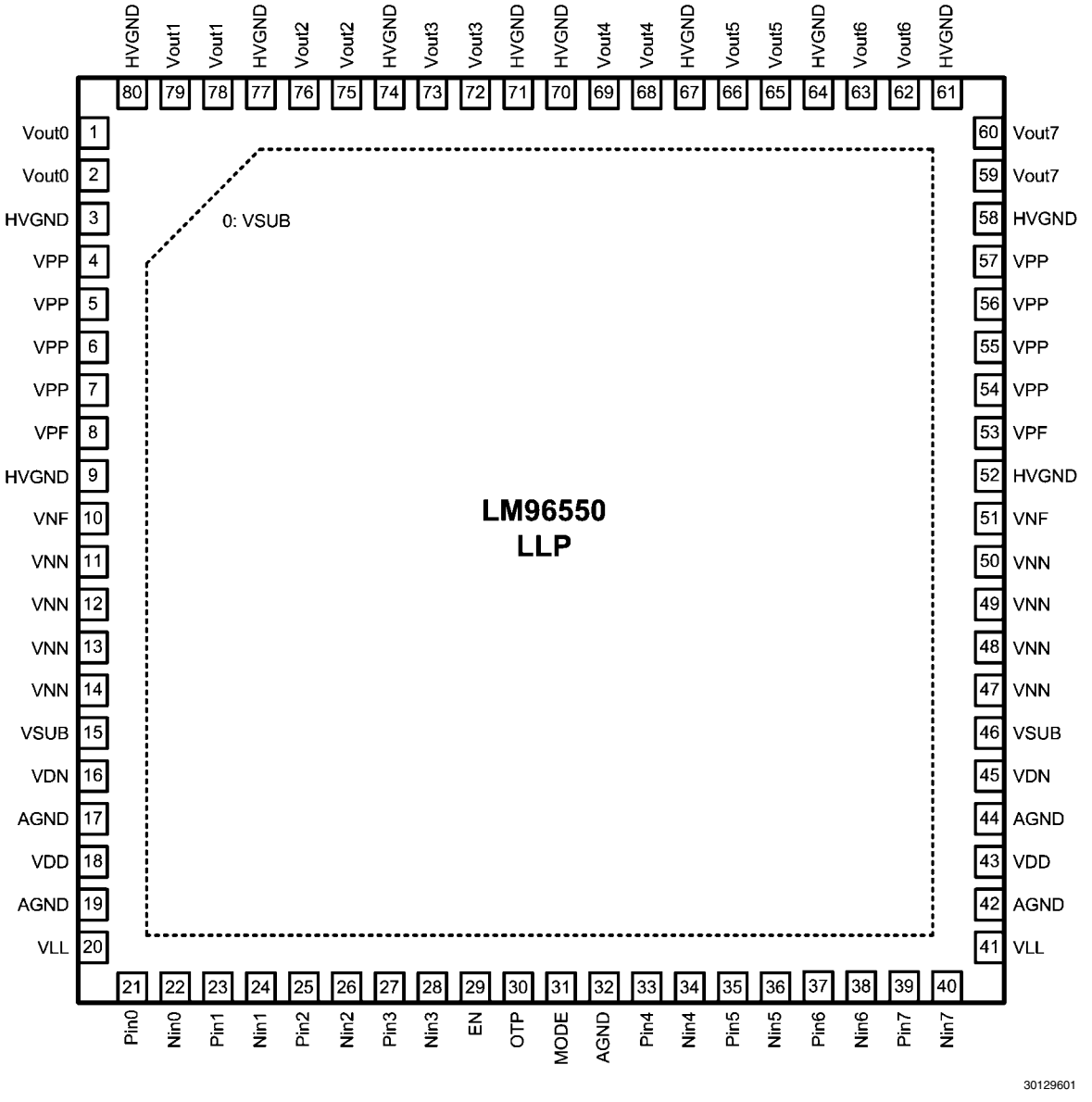


FIGURE 1. Pin Diagram of LM96550

Ordering Information

Order Number	Package Type	NSC Package Drawing	Supplied As
LM96550SQ	80 Lead LLP	SQA80A	1000
LM96550SQE			250
LM96550SQX			2000

TABLE 1. Pin Descriptions

Pin No.	Name	Type	Function and Connection
21, 23, 25, 27, 33, 35, 37, 39	PIN n=0...7	Input	Logic control positive output channel P 1 = ON 0 = OFF
22, 24, 26, 28, 34, 36, 38, 40	NIN n=0...7	Input	Logic control negative output channel N 1 = ON 0 = OFF
59, 60	V_{OUT7}	Output	High voltage output of channels 0 to 7
62, 63	V_{OUT6}		
65, 66	V_{OUT5}		
68, 69	V_{OUT4}		
72, 73	V_{OUT3}		
75, 76	V_{OUT2}		
78, 79	V_{OUT1}		
1, 2	V_{OUT0}		
29	EN	Input	Chip power enable 1 = ON 0 = OFF
31	MODE	Input	Output current mode control 1 = Max Current 0 = Low Current
30	OTP	Output	Over-temperature indicating IC temp > 125°C 0 = Over-temperature 1 = Normal temperature This pin is open-drain.
4, 5, 6, 7, 54, 55, 56, 57	VPP	Power	Positive high voltage power supply (+3.3V to +50V)
11, 12, 13, 14, 47, 48, 49, 50	VNN	Power	Negative high voltage power supply (-3.3V to -50V)
8, 53	VPF	Power	Positive floating power supply (VPP -10V)
10, 51	VNF	Power	Negative floating power supply (VNN +10V)
18, 43	VDD	Power	Positive level-shifter supply voltage (+10V)
16, 45	VDN	Power	Negative level-shifter supply voltage (-10V)
20, 41	VLL	Power	Logic supply voltage. Hi voltage reference input (+2.5 to +5V)
0, 15, 46	VSUB	Power	All VSUB pins must be connected to most negative potential of the IC. NOTE: The exposed thermal pad is connected to VSUB.
3, 9, 52, 58, 61, 64, 67, 70, 71, 74, 77, 80	HVGND	Ground	High voltage reference potential (0V)
17, 19, 32, 42, 44	AGND	Ground	Analog and Logic voltage reference input, logic ground (0V)

Absolute Maximum Ratings (*Note 1*)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Maximum Junction Temperature (T_{JMAX})	+150°C
Storage Temperature Range	−40°C to +125°C
Supply Voltage (VDD)	−0.3V to +12V
Supply Voltage (VDN)	+0.3V and −12V
Supply Voltage (VPP)	−0.3V and +55V
Supply Voltage (VPF)	VPP −14V
Supply Voltage (VNN)	+0.3V and −55V
Supply Voltage (VNF)	VNN +14V
Supply Voltage (VSUB)	−65V
IO Supply Voltage (VLL)	−0.3V to +5.5V
Voltage at Logic Inputs	−0.3V to VLL +0.3V

Operating Ratings

Operation Junction Temperature	0°C to + 70°C
VPP, −VNN; High-voltage supply	+3.3V to +50V
VPF, −VNF; Floating supply	VPP −10V
VDD, −VDN; Level-shift supply	+9V to 11V
VLL, Logic Supply	+2.4V to +5.3V
VSUB, Substrate bias supply	must be most negative supply
Package Thermal Resistance (θ_{JA})	19.7°C/W
ESD Tolerance	
Human Body Model	2kV
Machine Model	150V
Charge Device Model	750V

Analog Characteristics

Unless otherwise stated, the following conditions apply

VLL = +3.3V, VPP = −VNN = 50V, VPF = −VNF = VPP-10V, VDD = −VDN = 10V, VSUB = −55V, R_L = 2 KΩ, T_A = 25°C, Mode = LO, EN = HI, Fin=5MHz

Symbol	Parameter	Conditions		Min	Typ	Max	Units
F_{OUT}	Output Frequency Range	R_L = 100Ω		1		15	MHz
	Output Voltage Range			-48.5		+48.5	V
	Output Current	2% Duty Cycle			2		A
	Output Current	100% Duty Cycle, Mode=HI			0.6		
HD2	Second harmonic distortion	R_L = 100Ω || C_L = 330pF See (*Note 2*)			-40		dBc
R_{ON}	Output ON Resistance	100 mA			7	11	Ω
	Output Phase Noise	5MHz carrier, 1kHz offset, Mode=HI, VPP=-VNN=5V, R_L = 100Ω || C_L = 330pF			−114		dBc/Hz
	Output clamp	Positive or Negative pulse			2		A
	Power Supply Current	Pin = Nin = 0	VPP		0.7	3	mA
			VNN		0.5	4.5	
			VDD		8	13	
			VDN		4	7	
			VLL		25	50	µA
			VSUB		1.2	6	mA
			VPF		0.1	1.5	
			VNF		0.1	1.5	
		En = 0	VPP		0.7	3	mA
			VNN		0.5	4.5	
			VDD		0.4	2.7	
			VDN		0.1	2.2	
			VLL		25	50	µA
			VSUB		1.2	6	mA
			VPF		0.1	1.5	
			VNF		0.1	1.5	
OPT	Over Temperature Protection				125		°C

Symbol	Parameter	Conditions	Min	Typ	Max	Units
σ_{OTP}	OTP sigma			3.0		°C
$Hsys_{OTP}$	OTP hysteresis			5.5		°C

AC and Timing Characteristics

Unless otherwise stated, the following conditions apply.

VLL = +3.3V, VDD = −VDN = 10V, VSUB = −55V, VPP = −VNN = 50V, VPF = −VNF = 40V, C_L = 330pF, R_L = 100 Ω, T_A = 25°C, Fin=5MHz, Mode=LO, EN=HI

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_r	Output rise time	See (*Note 2*)		18	26	ns
t_f	Output fall time			18	26	
t_E	Enable time			1		µs
t_{dr}	Delay time on inputs rise	See (*Note 2*)		32	39	ns
t_{df}	Delay time on inputs fall			32	39	
$\lvert t_{dr} - t_{dr} \rvert$	Delay time mismatch	P-to-N See (*Note 2*) & 3			3	
t_{dm}	Delay on mode change			1		µs

DC Characteristics

Unless otherwise stated, the following conditions apply.

VLL = +3.3V, VDD = −VDN = 10V, VSUB = −55V, VPP = −VNN = 50V, VPF = −VNF = 40V, T_A = 25°C,

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Low Input “LO” threshold				1	V
V_{IH}	High Input “HI” threshold		2.3			V
I_{IN}	input current			1		µA

Note 1: Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is guaranteed to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics.

Note 2: VNF = -42V, VPF = 38V

Note 3: The delay time mismatch can be adjust to be less than 0.8ns with the LM96570 duty cycle control function.

Overview

The LM96550 pulser provides an 8-channel transmit side solution for medical ultrasound applications suitable for integration into multi-channel (128/256 channel) systems. Its flexible, integrated ±50V pulser architecture enables low-power designs targeting portable systems. A complete system can be designed using National's companion LM965XX chipset.

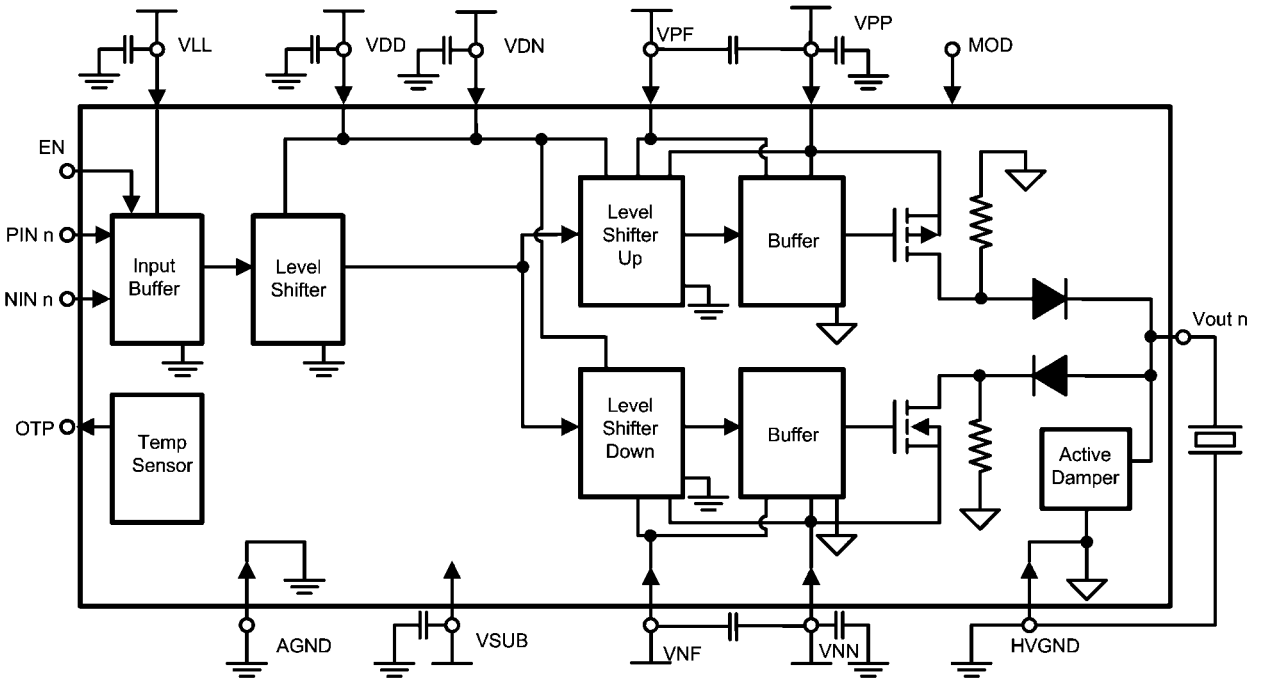


FIGURE 2. Block Diagram of High-Voltage Pulser Channel

A functional block diagram of the LM96550 is shown in . It has an input buffer at its CMOS logic interface, which is powered by VLL (2.5 to 5.0V). When EN=HI, driving a channel's inputs (PIN n or NIN n) HI will result in a positive or negative pulse at the channel's output pin (V_{OUT} n), respectively. The output pins V_{OUT} are pulled to either the positive or negative supplies, VPP or VNN by power MOSFETs.

When PIN and NIN are both LO, Vout is actively clamped to GNDHI at 0V. This clamping reduces harmonic distortions compared to competing architectures that use bleeding resistors for implementing the return to zero of the output. **The user must avoid the condition in which PIN and NIN are both HI simultaneously, as this will damage the output stage!**

The impedance of the output stage can be controlled via the Mode-pin. When the Mode = HI as shown, only one output transistor pair drives the output resulting in a peak current of 600 mA at VPP = -VNN = 50V. When Mode=LO, a peak-current of 2A is achievable resulting in faster transients at the output. However, faster output transients can lead to significant overshoot of the output signal. This can be avoided using the lower drive current option.

Continuous-wave (CW) applications are supported for low power consumption down to VPP = -VNN = 3.3V with Mode =HI.

Internally, the CMOS logic input signals are level shifted to VDD = 10V and VDN = -10V for pulse transmission. The outputs of the level shifter drive the high-voltage P and N drivers that control the output power MOSFETs, which are supplied from the positive and negative rails VPP and VNN, respectively. The high-voltage rails are designed for a maximum of 50V; however, they can be operated down to 3.3V. The necessary gate-overdrive voltage levels for the output drivers are internally generated from the high-voltage rails.

Over-Temperature Protection (OTP) is implemented by continuously monitoring the on-chip temperature. The OTP output (open drain) pin goes LO when the chip temperature exceeds a critical level. Prior to this event, the user must ensure that the chip is powered down before fatal damage occurs. In addition to a primary software controlled safety shutdown, the OTP pin can be also be hard-wired to the EN pin as a secondary safety measure.

Timing Diagrams

RISE AND FALL TIME

The timing diagram shown in *Figure 3* defines the rise and fall times tr and tf.

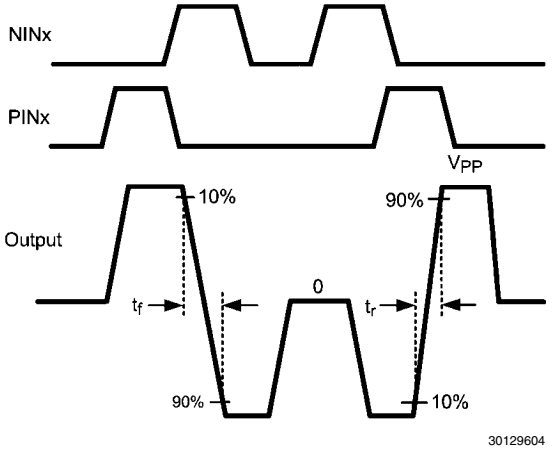


FIGURE 3. Timing Diagram Defining Rise and Fall Times tr and tf, respectively

INPUT TO OUTPUT DELAY

The timing diagram shown in *Figure 4* defines the delays between the input and output signals.

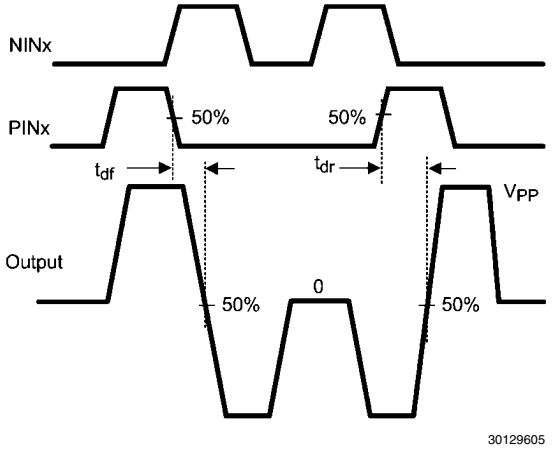


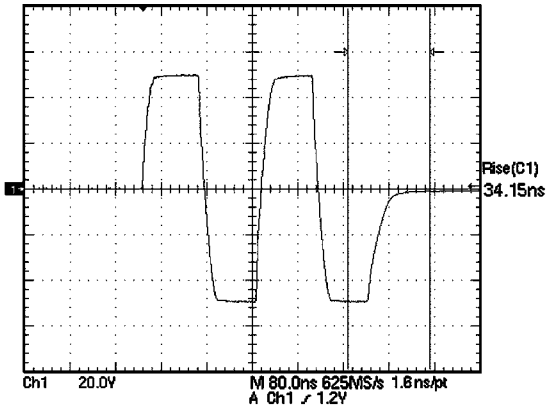
FIGURE 4. Timing Diagram Defining Input-to-Output Delays Times

Typical Performance Characteristics

Unless otherwise stated, the following conditions apply.

VLL = +3.3V, VDD = −VDN = 10V, VSUB = −55V, VPP = −VNN = 50V, VPF = VPP-12V, VNF = VNN+8V, C_L = 330pF, R_L = 100Ω, T_A = 25°C, Fin=5MHz, Mode=LO, EN=HI

Return-to-Zero Rise Time (R_L = 2KΩ)



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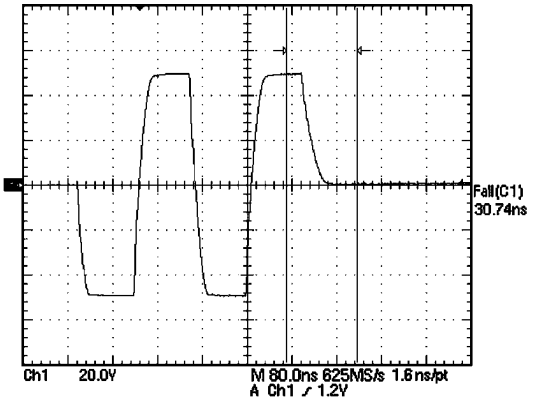
Return-to-Zero Fall Time (R_L = 2KΩ)



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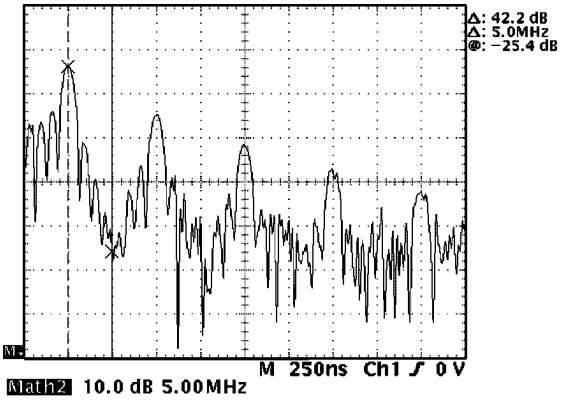
Harmonic Distortion (8 pulses)



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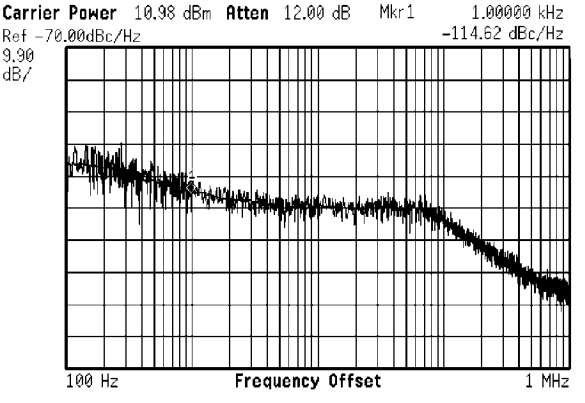
CW Phase Noise (Mode=HI, VPP=-VNN=5V)



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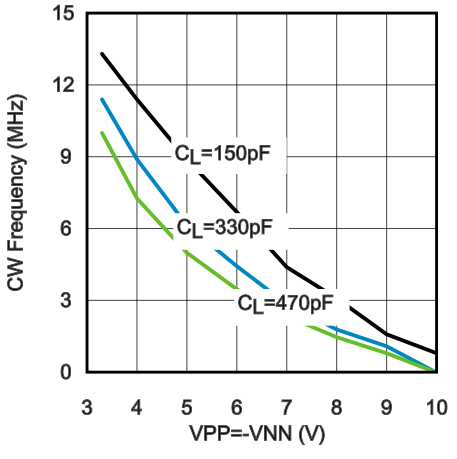
Constant 5W Total Power (R_L = 300Ω)
100% CW mode, Mode=HI, VSUB=-10V, VPF=-VNF=VPP-10V



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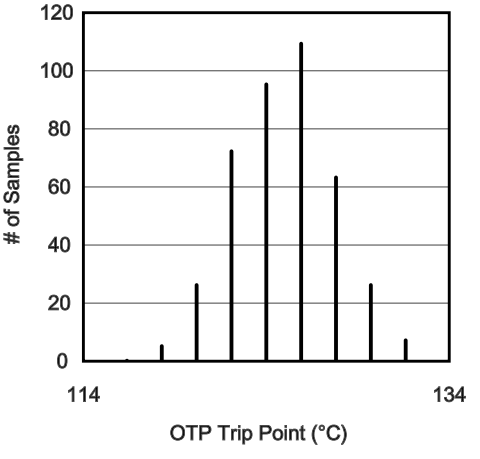
Over Temperature Protection



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Functional Description

Note that the case, PINn = NNn = HI is not allowed as it will damage the output transistors.

Logic inputs			Output
EN	PINn	NINn	Voutn
1	0	0	0V
1	1	0	VPP - 0.7V
1	0	1	VNN + 0.7V
1	1	1	**not allowed**
0	X	X	0V

Applications

POWER-UP AND POWER-DOWN SEQUENCES

VSUB must always be the most negative supply, i.e., it must be equal to or more negative than the most negative supply, VNN or VDN. VPF ≥ VPP −14V AND VNF = ≤ VNN +14V at all times.

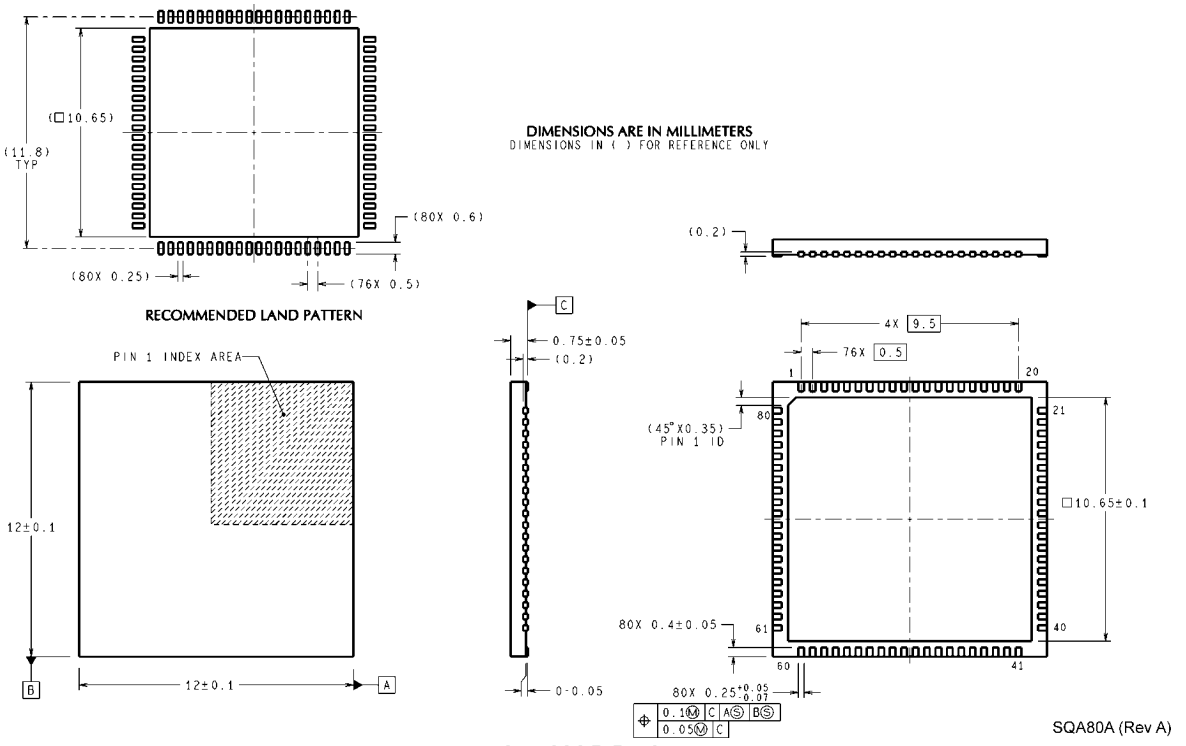
Power UP Sequence:

1. Turn ON VSUB, hold EN pin LO
2. Turn ON VLL
3. Turn ON VDD, VDN, VPP, VPF, VNN and VNF

Power DOWN Sequence:

1. Turn OFF VDD, VDN, VPP, VPF, VNN and VNF
2. Turn OFF VLL
3. Turn OFF VSUB

Physical Dimensions inches (millimeters) unless otherwise noted



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