THE DATASHEET OF

LM97600CIUT/NOPB

LM97600 7.6-Bit, 1/2/4 Channel, 5/2.5/1.25 GSPS, High Performance, Low Power A/D Converter

Check for Samples: LM97600

FEATURES

- **10 Lane High Speed Serial Data Output**
- **Serial Interface for Extended Control**
- **Adjustment of Input Full-Scale Range and Offset**
- **Duty Cycle Corrected Sample Clock**
- **Multiple Test Patterns**
- **Dual +1.2V ±0.06V and 2.5V ±0.125V Operation**

KEY SPECIFICATIONS

- **Average Output Word Size: 7.6 bits**
- **Max Conversion Rate: 1.25/2.5/5.0 GSPS (min)**
- **Error Rate: 10^{-18} (typ)**
- **ENOB @ 998 MHz Input: 6.4 Bits (typ)**
- **SNR @ 998 MHz: 41 dB (typ)**
- **Full Power Bandwidth (-3dB) Dual Mode: 1.2 GHz (typ)**
- **Power Consumption**
  - **Operating: 3.0 W (typ)**
  - **Power Down Mode: 60 mW (typ)**

APPLICATIONS

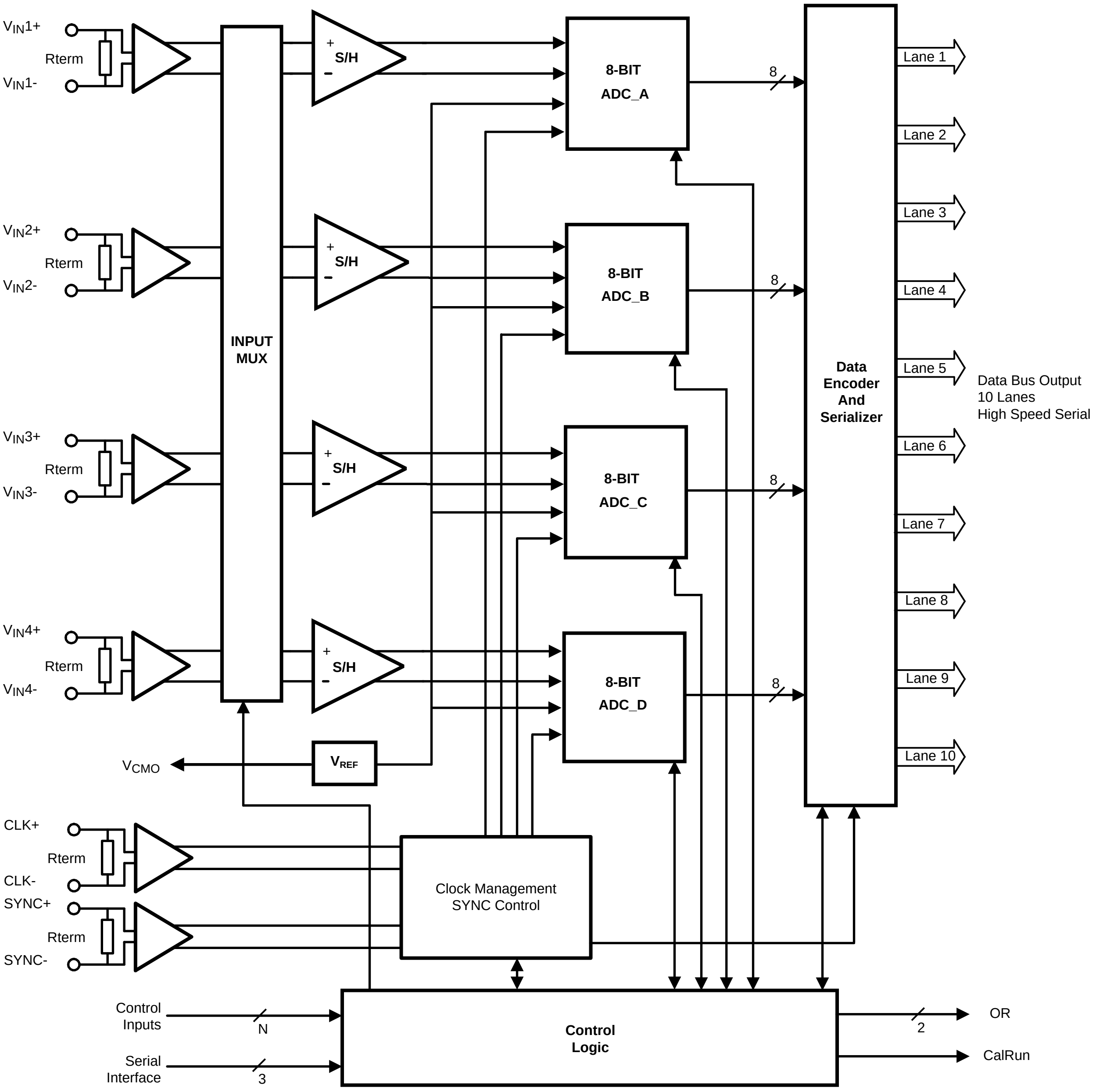
- **Digital Oscilloscopes**
- **Test Instrumentation**
- **Industrial Digitizers**
- **Automated Test Equipment**

DESCRIPTION

The LM97600 is a single/dual/quad, low power, high performance SiGe BiCMOS analog-to-digital converter that digitizes signals at sampling rates up to 5.0/2.5/1.25 GSPS. Consuming a typical 3.1 Watts at 5 GSPS from 1.2 and 2.5 Volt dual supplies, this device is ensured to have no missing codes over the full operating temperature range. The unique folding and interpolating architecture, the fully differential comparator design, the innovative design of the internal sample-and-hold amplifier and the self-calibration scheme enable an excellent response of all dynamic parameters, producing a high 6.6 Effective Number Of Bits, (ENOB) with a 248 MHz input signal and a 5 GHz sample rate. The LM97600 achieves a 5 GSPS sampling rate by utilizing both the rising and falling edge of a 2.5 GHz input clock. Data encoding is 8 bits offset binary. Average output word size is 7.6 bits. The serialized data is 8b10b encoded providing DC balance and AC coupling capability. Decoding can be accomplished using existing FPGA serial I/O modules.

The converter typically consumes less than 65 mW in the Power Down Mode and is available in a 292 ball, thermally enhanced substrate BGA, and operates over the Industrial (-40°C ≤ T_A ≤ +85°C) ambient temperature range.

Block Diagram

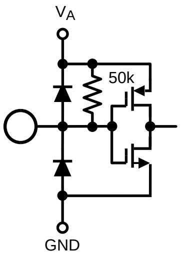
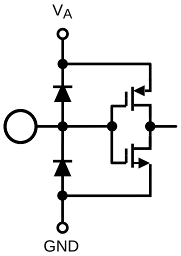
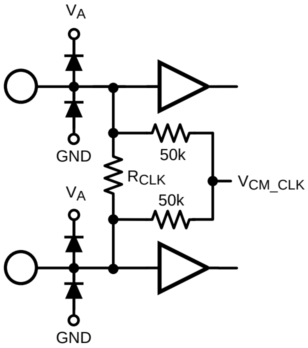


Pin Configuration

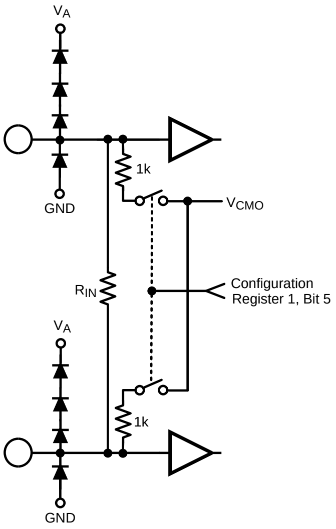
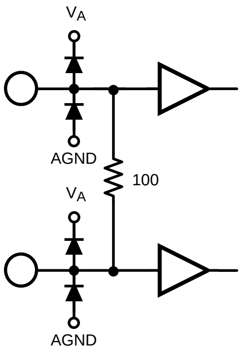
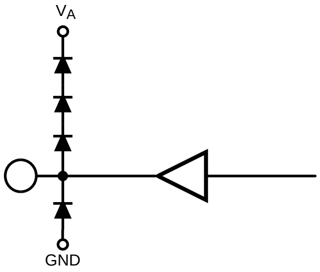
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
A	GND	CLK-	CLK+	GND	SYNC+	V_O	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	V_O	GND	V_O	GND	A
B	GND	GND	GND	GND	SYNC-	GND	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	B
C	V_TH	V_C	V_C	V_C	V_C	V_O	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	C
D	GND	V_TH	SCSb	V_C	V_C	GND	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	D
E	IN1+	GND	SCLK	GND													NC	NC	ORAC+	ORAC-	E
F	IN1-	GND	SDI	DNC													NC	NC	DS9+	DS9-	F
G	GND	V_TH	SDO	GND													NC	NC	DS8+	DS8-	G
H	IN3-	GND	V_TH	GND				GND	GND	GND	GND	GND	GND				NC	NC	DS7+	DS7-	H
J	IN3+	GND	V_TH	V_TH				GND	GND	GND	GND	GND	GND				NC	NC	DS6+	DS6-	J
K	GND	V_TH	V_TH	V_TH				GND	GND	GND	GND	GND	GND				NC	NC	DS5+	DS5-	K
L	GND	V_TH	V_25	V_25				GND	GND	GND	GND	GND	GND				NC	NC	DS4+	DS4-	L
M	IN4+	GND	V_25	V_25				GND	GND	GND	GND	GND	GND				NC	NC	DS3+	DS3-	M
N	IN4-	GND	V_A	V_A				GND	GND	GND	GND	GND	GND				NC	NC	DS2+	DS2-	N
P	GND	V_TH	V_A	V_A													NC	NC	DS1+	DS1-	P
R	IN2-	GND	V_A	V_A													NC	NC	DS0+	DS0-	R
T	IN2+	GND	V_A	V_A													NC	NC	ORBD+	ORBD-	T
U	GND	V_TH	V_A	Tdiode-	NC	GND	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	U
V	V_TH	V_A	Vcmo	Tdiode+	CalRun	V_O	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	V
W	V_A	V_A	Rext	VBG	CAL	GND	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	W
Y	V_A	V_A	RGND	Rtrim	PD	V_O	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	V_O	GND	V_O	GND	Y
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	

Note: The center GND balls must be thermally and electrically connected to a ground plane to ensure rated performance.

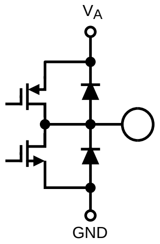
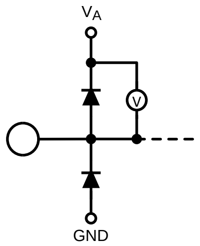
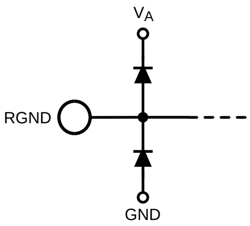
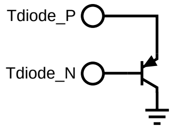
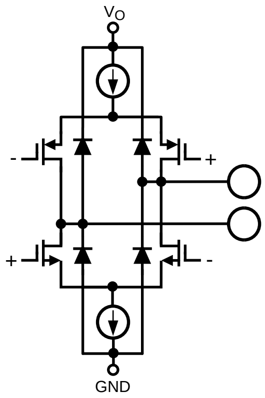
PIN DESCRIPTIONS and EQUIVALENT CIRCUITS

Pin No.	Symbol	Equivalent Circuit	Description
D3	$\overline{\text{SCS}}$		**Serial Chip Select (active low)** **(Input):LVCMOS** This pin functions as the serial interface chip select. See USING THE SERIAL INTERFACE for description of the serial interface.
E3	SCLK		**Serial Interface Clock** **(Input):LVCMOS** This pin functions as the SCLK input which clocks the serial data. See USING THE SERIAL INTERFACE for description of the serial interface.
F3	SDI		**Serial Data In** **(Input):LVCMOS** This pin functions as the SDATA input. See USING THE SERIAL INTERFACE for description of the serial interface.
Y5	PD		**Power Down** **(Input):LVCMOS** A logic high on the PD pin puts the entire device into the Power Down Mode.
W5	CAL		**Calibration Cycle Initiate** **(Input):LVCMOS** A minimum 80 input clock cycles logic low followed by a minimum of 80 input clock cycles high on this pin initiates the calibration sequence. See Calibration for an overview of self-calibration and On-Command Calibration for a description of on-command calibration.
A3 A2	CLK+ CLK−		**Sampling Clock Input** **(Input):LVDS** The differential clock signal must be a.c. coupled to these pins. The input signal is sampled on both the rising and falling edge of CLK. See Acquiring the Input for a description of acquiring the input and THE SAMPLE CLOCK INPUT for an overview of the clock inputs.

PIN DESCRIPTIONS and EQUIVALENT CIRCUITS (continued)

Pin No.	Symbol	Equivalent Circuit	Description
E1 F1	$V_{IN1}+$ $V_{IN1}-$		**Signal Input 1** **(Input):Analog** The differential full-scale input range is determined by the Full-Scale Voltage Adjust register for the selected ADC Channel. The coupling mode (AC or DC) is selected via Configuration Register 1, Bit 5. Unused inputs should be connected to pin V3 V_{CMO}.
J1 H1	$V_{IN3}+$ $V_{IN3}-$		**Signal Input 3** **(Input):Analog** The differential full-scale input range is determined by the Full-Scale Voltage Adjust register for the selected ADC Channel. The coupling mode (AC or DC) is selected via Configuration Register 1, Bit 5. Unused inputs should be connected to pin V3 V_{CMO}
M1 N1	$V_{IN4}+$ $V_{IN4}-$		**Signal Input 4** **(Input):Analog** The differential full-scale input range is determined by the Full-Scale Voltage Adjust register for the selected ADC Channel. The coupling mode (AC or DC) is selected via Configuration Register 1, Bit 5. Unused inputs should be connected to pin V3 V_{CMO}
T1 R1	$V_{IN2}+$ $V_{IN2}-$		**Signal Input 2** **(Input):Analog** The differential full-scale input range is determined by the Full-Scale Voltage Adjust register for the selected ADC Channel. The coupling mode (AC or DC) is selected via Configuration Register 1, Bit 5. Unused inputs should be connected to pin V3 V_{CMO}
A5 B5	SYNC+ SYNC−		**ADC Sync** **(Input):LVDS** A positive differential pulse on these pins is used to reset and synchronize multiple converters. See Multiple ADC Synchronization for detailed description.
V3	V_{CMO}		**Common Mode Voltage** **(Output):Analog -** The voltage output at this pin is required to be the common mode input voltage at $V_{IN}+$ and $V_{IN}-$ when d.c. coupling is used. This pin is capable of sourcing or sinking 100µA and can drive a load up to 80 pF.
W4	V_{BG}		**Bandgap Output Voltage** **(Output):Analog -** Capable of 100 µA source/sink and can drive a load up to 80 pF.

PIN DESCRIPTIONS and EQUIVALENT CIRCUITS (continued)

Pin No.	Symbol	Equivalent Circuit	Description
G3	SDO		**Serial Data Out** **Output):LVCMOS** This pin functions as the SDATA output. See USING THE SERIAL INTERFACE for description of the serial interface.
V5	CalRun		**Calibration Running** **(Output):LVCMOS -** This pin is at a logic high while a calibration is running.
W3	R_{EXT}		**External Bias Resistor Connection** **Analog -** Nominal value is 3.6k-Ohms (±0.1%) to RGND pin. See Table 13.
Y4	R_{TRIM}		**External Trim Resistor Connection** **Analog -** Nominal value is 3.6k-Ohms (±0.1%) to RGND pin. See Table 13.
Y3	RGND		**External Resistor Connection Return** **Analog -** R_{EXT} and R_{TRIM} resistors must be connected to this pin. This pin must be isolated from all other signals and grounds. DO NOT CONNECT TO GROUND.
V4 U4	Tdiode+ Tdiode−		**Temperature Diode** **Analog -** Positive (Anode) and Negative (Cathode) for die temperature measurements. See Thermal Management
R19 / R20 P19 / P20 N19 / N20 M19 / M20 L19 / L20 K19 / K20 J19 / J20 H19 / H20 G19 / G20 F19 / F20	DS0+ / DS0− DS1+ / DS1− DS2+ / DS2− DS3+ / DS3− DS4+ / DS4− DS5+ / DS5− DS6+ / DS6− DS7+ / DS7− DS8+ / DS8− DS9+ / DS9−		**Data** **(Output):LVDS** High Speed Serialized Data Outputs. The data must be 10b8b decoded and then mapped from the 10 lanes to the corresponding 4 internal ADC converters as needed. These outputs should always be terminated with a 100Ω differential resistor at the receiver.
E19 E20	ORAC+ ORAC−		**Out Of Range AC** **(Output):LVDS -** A differential high at these pins indicates that the differential input is out of range (as defined by the FSR setting for channels A and C). These outputs should always be terminated with a 100Ω differential resistor at the receiver.
T19 T20	ORBD+ ORBD−		**Out Of Range BD** **(Output):LVDS -** A differential high at these pins indicates that the differential input is out of range (as defined by the FSR setting for channels B and D). These outputs should always be terminated with a 100Ω differential resistor at the receiver.

PIN DESCRIPTIONS and EQUIVALENT CIRCUITS (continued)

Pin No.	Symbol	Equivalent Circuit	Description
N3, N4, P3, P4, R3, R4, T3, T4, U3, V2, W1, W2, Y1, Y2	V_A		**Analog power supply pins** **(Power)** - Bypass these pins to ground.
A6, A17, A19, C6, V6, Y6, Y17, Y19	V_O		**Output Driver power supply pins** **(Power) -** Bypass these pins to ground.
L3, L4, M3, M4	V_{25}		**2.5V power supply pins** **(Power)** - Bypass these pins to ground.
C1, D2, G2, H3, J3, J4, K2, K3, K4, L2, P2, U2, V1	V_{TH}		**Track and Hold power supply pins** **(Power)** - Bypass these pins to ground.
C2, C3, C4, C5, D4, D5	V_C		**Clock power supply pins** **(Power)** - Bypass these pins to ground.
A1, A4, A18, A20, B1, B2, B3, B4, B6, D1, D6, E2, E4, F2, G1, G4, H2, H4, H8–H13, J2, J8–J13, K1, K8–K13, L1, L8–L13, M2, M8–M13, N2, N8–N13, P1, R2, T2, U1, U6, W6, Y18, Y20	GND		**(Gnd) -** Ground return for all supplies.
F4	DNC		Do Not Connect to Any Circuitry, Power or Ground Signals
A7–A16, B7–B20, C7–C20, D7–D20, E17, E18, F17, F18, G17, G18, H17, H18, J17, J18, K17, K18, L17, L18, M17, M18, N17, N18, P17, P18, R17, R18, T17, T18, U5, U7–U20, V7–V20, W7–W20, Y7–Y16	NC		**No Connection** Make no connection to these pins

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings[1][2][3]

1.2V Supply Voltage (V_A, V_{TH}, V_C)		1.32V
2.5V Supply Voltage (V_O, V_{25})		2.75V
1.2V Supply Difference between V_A, V_{TH}, V_C.		100mV
2.5V Supply Difference between V_O, V_{25}.		100mV
Supply Sequence (Power-up and Power-down)		2.5V Supply ≥1.2V Supply
Voltage on Any Input Pin (except V_{IN}x+/-)		−0.15V to (V_A + 0.15V)
Voltage on V_{IN}x+/-		−0.15V to +2.0V
Voltage difference: Any VINx+ to VINy+ or VINx- to VINy-		≤1.5V
Input Current at Any Pin[4]		±25mA
Package Input Current [4]		±50mA
Power Dissipation at $T_A \leq 85°C$		3.77W
ESD Susceptibility[5]	Human Body Model	2500V
	Charged Device Model	400V
	Machine Model	250V
Storage Temperature		−65°C to +150°C
Soldering process must comply with Reflow Temperature Profile specifications. Refer to http://www.ti.com/packaging. See [6].		

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(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. There is no ensurance of operation at the Absolute Maximum Ratings. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see Converter Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

(2) All voltages are measured with respect to GND = 0V, unless otherwise specified.

(3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

(4) When the input voltage at any pin exceeds the power supply limits (that is, less than GND or greater than VA), the current at that pin should be limited to 25 mA. The 50 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 25 mA to two. This limit is not placed upon the power and ground pins.

(5) Human body model is 100 pF capacitor discharged through a 1.5 kΩ resistor. Machine model is 220 pF discharged through ZERO Ohms.

(6) Reflow temperature profiles are different for lead-free and non-lead-free packages.

Operating Ratings[1][2]

Ambient Temperature Range	$-40°C \leq T_A \leq +85°C$
1.2V Supply Voltage (V_A, V_{TH}, V_C)	+1.14V to +1.26V $V_A \geq V_{TH}$
2.5V Supply Voltage (V_O, V_{25})	+2.375V to +2.625V
Supply Sequence (Power-up and Power-down)	2.5V Supply ≥1.2V Supply
Analog Input Common Mode Voltage	V_{CMO} ±50mV
V_{IN}+, V_{IN}- Voltage Range (Maintaining Common Mode)	+200mV to +1.85V
Voltage difference: Any VINx+ to VINy+ or VINx- to VINy-	≤1.5V
CLK Pins Voltage Range	0V to V_A
Differential CLK Amplitude	$0.4V_{P-P}$ to $2.0V_{P-P}$
Common Mode Input Voltage	$V_{CMO} - 50mV < V_{CMI} < V_{CMO} + 50mV$

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(1) All voltages are measured with respect to GND = 0V, unless otherwise specified.

(2) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. There is no ensurance of operation at the Absolute Maximum Ratings. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see Converter Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Package Thermal Resistance

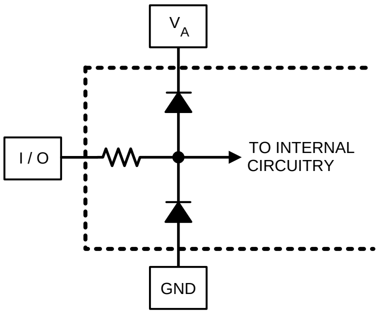
Package	θ_{JA}	θ_{JC1} (Top of Package)	θ_{JC2} (Center Balls)
292–Ball BGA Thermally Enhanced Package	15.9°C / W	5.6°C / W	5.1°C / W

Converter Electrical Characteristics

The following specifications apply after calibration for $V_A = V_{TH} = V_C = +1.2V_{DC}$, $V_O = V_{25} = +2.5V_{DC}$, V_{IN} FSR (a.c. coupled) = Default ECM setting, $C_L = 10$ pF, Differential a.c. coupled Sinewave Input Clock, $f_{CLK} = 2.5$ GHz at $0.5V_{P\text{-}P}$ with 50% duty cycle, $R_{EXT} = 3600\Omega \pm 0.1\%$, $R_{TRIM} = 3600\Omega \pm 0.1\%$, Analog Signal Source Impedance = 100Ω Differential, after calibration. **Boldface limits apply for $T_A = T_{MIN}$ to T_{MAX}.** All other limits $T_A = 25°C$, unless otherwise noted.(1)(2)

Symbol	Parameter	Conditions	Typical (3)	Limits (3)	Units (Limits)
STATIC CONVERTER CHARACTERISTICS					
INL	Integral Non-Linearity (Best fit)	DC Coupled, 1MHz Sine Wave Over Ranged, Single ADC Mode	±0.6	**±1**	lsb (max)
DNL	Differential Non-Linearity	DC Coupled, 1MHz Sine Wave Over Ranged, Single ADC Mode	+0.65/ −0.50	**+1/−0.70**	lsb (max)
	Resolution with No Missing Codes	See the Selective Truncation section		**7.6**	Bits
V_{OFF}	Offset Error		−1		lsb
V_{OFF}_ADJ	Input Offset Adjustment Range	Extended Control Mode	±28		mV
PFSE	Positive Full-Scale Error(4)		−5	**±30**	mV (max)
NFSE	Negative Full-Scale Error(4)		−2	**±30**	mV (max)
FS_ADJ	Full-Scale Adjustment Range	Extended Control Mode	±20	**±15**	%FS (min)
DYNAMIC CONVERTER CHARACTERISTICS					
FPBW	Full Power Bandwidth		1.3		GHz
	Gain Flatness	0.0 to -1.0 dBFS	DC to 400		MHz
	Code Error Rate		10^{-18}		Errors/ Sample

(1) The analog inputs are protected as shown below. Input voltage magnitudes beyond the Absolute Maximum Ratings may damage this device.



(2) To ensure accuracy, it is required that V_A, V_{TH}, V_C, V_{25}, and V_O be well bypassed. Each supply pin must be decoupled with separate bypass capacitors.

(3) Typical figures are at $T_A = 25°C$, and represent most likely parametric norms. Test limits are ensured to AOQL (Average Outgoing Quality Level).

(4) Calculation of Full-Scale Error for this device assumes that the actual reference voltage is exactly its nominal value. Full-Scale Error for this device, therefore, is a combination of Full-Scale Error and Reference Voltage Error. See Figure 2. For relationship between Gain Error and Full-Scale Error, see Specification Definitions.

Converter Electrical Characteristics (continued)

The following specifications apply after calibration for $V_A = V_{TH} = V_C = +1.2V_{DC}$, $V_O = V_{25} = +2.5V_{DC}$, V_{IN} FSR (a.c. coupled) = Default ECM setting, C_L = 10 pF, Differential a.c. coupled Sinewave Input Clock, f_{CLK} = 2.5 GHz at $0.5V_{P-P}$ with 50% duty cycle, R_{EXT} = 3600Ω ±0.1%, R_{TRIM} = 3600Ω ±0.1%, Analog Signal Source Impedance = 100Ω Differential, after calibration. **Boldface limits apply for $T_A = T_{MIN}$ to T_{MAX}**. All other limits T_A = 25°C, unless otherwise noted.(1)(2)

Symbol	Parameter	Conditions	Typical (3)	Limits (3)	Units (Limits)
Single ADC Mode (F_S = 2 x F_{CLK})					
ENOB	Effective Number of Bits	f_{IN} =248 MHz, V_{IN} = FSR − 0.5 dB	6.6		Bits
		f_{IN} = 998 MHz, V_{IN} = FSR − 0.5 dB	6.4	**5.8**	Bits (min)
SINAD	Signal-to-Noise Plus Distortion Ratio	f_{IN} =248 MHz, V_{IN} = FSR − 0.5 dB	42		dB
		f_{IN} = 998 MHz, V_{IN} = FSR − 0.5 dB	40.5	**36.5**	dB (min)
SNR	Signal-to-Noise Ratio	f_{IN} = 248MHz, V_{IN} = FSR − 0.5 dB	42.5		dB
		f_{IN} = 998 MHz, V_{IN} = FSR − 0.5 dB	41.0	**37.0**	dB (min)
THD	Total Harmonic Distortion	f_{IN} = 248 MHz, V_{IN} = FSR − 0.5 dB	−49		dB
		f_{IN} = 998 MHz, V_{IN} = FSR − 0.5 dB	−50	**−46.5**	dB (max)
2nd Harm	Second Harmonic Distortion	f_{IN} = 248 MHz, V_{IN} = FSR − 0.5 dB	−50		dB
		f_{IN} = 998 MHz, V_{IN} = FSR − 0.5 dB	−60		dB
3rd Harm	Third Harmonic Distortion	f_{IN} = 248 MHz, V_{IN} = FSR − 0.5 dB	−51		dB
		f_{IN} = 998 MHz, V_{IN} = FSR − 0.5 dB	−50		dB
SFDR	Spurious-Free dynamic Range	f_{IN} = 248 MHz, V_{IN} = FSR − 0.5 dB	50		dB
		f_{IN} = 998 MHz, V_{IN} = FSR − 0.5 dB	49	**41.5**	dB (min)
Dual ADC Mode (F_S = F_{CLK})					
ENOB	Effective Number of Bits	f_{IN} =248 MHz, V_{IN} = FSR − 0.5 dB	6.7		Bits
		f_{IN} = 998 MHz, V_{IN} = FSR − 0.5 dB	6.5	**5.9**	Bits (min)
SINAD	Signal-to-Noise Plus Distortion Ratio	f_{IN} =248 MHz, V_{IN} = FSR − 0.5 dB	42.5		dB
		f_{IN} = 998 MHz, V_{IN} = FSR − 0.5 dB	41.1	**37.1**	dB (min)
SNR	Signal-to-Noise Ratio	f_{IN} = 248MHz, V_{IN} = FSR − 0.5 dB	43.8		dB
		f_{IN} = 998 MHz, V_{IN} = FSR − 0.5 dB	41.7	**37.7**	dB (min)
THD	Total Harmonic Distortion	f_{IN} = 248 MHz, V_{IN} = FSR − 0.5 dB	−50		dB
		f_{IN} = 998 MHz, V_{IN} = FSR − 0.5 dB	−50	**−45.7**	dB (max)
2nd Harm	Second Harmonic Distortion	f_{IN} = 248 MHz, V_{IN} = FSR − 0.5 dB	−50		dB
		f_{IN} = 998 MHz, V_{IN} = FSR − 0.5 dB	−60		dB
3rd Harm	Third Harmonic Distortion	f_{IN} = 248 MHz, V_{IN} = FSR − 0.5 dB	−51		dB
		f_{IN} = 998 MHz, V_{IN} = FSR − 0.5 dB	−50		dB
SFDR	Spurious-Free dynamic Range	f_{IN} = 248 MHz, V_{IN} = FSR − 0.5 dB	50		dB
		f_{IN} = 998 MHz, V_{IN} = FSR − 0.5 dB	49	**41.5**	dB (min)
Quad ADC Mode (F_S = F_{CLK} / 2)					
ENOB	Effective Number of Bits	f_{IN} =248 MHz, V_{IN} = FSR − 0.5 dB	6.7		Bits
		f_{IN} = 998 MHz, V_{IN} = FSR − 0.5 dB	6.6		Bits
SINAD	Signal-to-Noise Plus Distortion Ratio	f_{IN} =248 MHz, V_{IN} = FSR − 0.5 dB	42.6		dB
		f_{IN} = 998 MHz, V_{IN} = FSR − 0.5 dB	41.5		dB
SNR	Signal-to-Noise Ratio	f_{IN} = 248MHz, V_{IN} = FSR − 0.5 dB	43.2		dB
		f_{IN} = 998 MHz, V_{IN} = FSR − 0.5 dB	42.1		dB
THD	Total Harmonic Distortion	f_{IN} = 248 MHz, V_{IN} = FSR − 0.5 dB	−50		dB
		f_{IN} = 998 MHz, V_{IN} = FSR − 0.5 dB	−50		dB
2nd Harm	Second Harmonic Distortion	f_{IN} = 248 MHz, V_{IN} = FSR − 0.5 dB	−51		dB
		f_{IN} = 998 MHz, V_{IN} = FSR − 0.5 dB	−60		dB
3rd Harm	Third Harmonic Distortion	f_{IN} = 248 MHz, V_{IN} = FSR − 0.5 dB	−49		dB
		f_{IN} = 998 MHz, V_{IN} = FSR − 0.5 dB	−48		dB

Converter Electrical Characteristics (continued)

The following specifications apply after calibration for $V_A = V_{TH} = V_C = +1.2V_{DC}$, $V_O = V_{25} = +2.5V_{DC}$, V_{IN} FSR (a.c. coupled) = Default ECM setting, C_L = 10 pF, Differential a.c. coupled Sinewave Input Clock, f_{CLK} = 2.5 GHz at $0.5V_{P-P}$ with 50% duty cycle, R_{EXT} = 3600Ω ±0.1%, R_{TRIM} = 3600Ω ±0.1%, Analog Signal Source Impedance = 100Ω Differential, after calibration. **Boldface limits apply for $T_A = T_{MIN}$ to T_{MAX}.** All other limits T_A = 25°C, unless otherwise noted.(1)(2)

Symbol	Parameter	Conditions	Typical (3)	Limits (3)	Units (Limits)
SFDR	Spurious-Free dynamic Range	f_{IN} = 248 MHz, V_{IN} = FSR − 0.5 dB	49		dB
		f_{IN} = 998 MHz, V_{IN} = FSR − 0.5 dB	48		dB
ANALOG INPUT AND REFERENCE CHARACTERISTICS					
V_{IN}	Full Scale Analog Differential Input Range	Min FSR Setting	560	**490**	mV_{P-P} (min)
				610	mV_{P-P} (max)
		Max FSR Setting	850	**760**	mV_{P-P} (min)
				930	mV_{P-P} (max)
C_{IN}	Analog Input Capacitance (5)	Differential	0.08		pF
		Each input pin to ground	2.2		pF
R_{IN}	Differential Input Resistance		100	**94** **107**	Ω (min) Ω (max)
ANALOG OUTPUT CHARACTERISTICS(V_{CMO}, V_{BG})					
V_{CMO}	Common Mode Output Voltage	I_{CMO} = ±100 µA	1.26	**1.16** **1.36**	V (min) V (max)
TC V_{CMO}	Common Mode Output Voltage Temperature Coefficient	T_A = −40°C to +85°C (6)	118		ppm/°C
C_{LOAD} V_{CMO}	Maximum V_{CMO} load Capacitance	See (7)		**80**	pF (min)
V_{BG}	Bandgap Reference Output Voltage	I_{BG} = ±100 µA	1.1	**1.0** **1.2**	V (min) V (max)
TC V_{BG}	Bandgap Reference Voltage Temperature Coefficient	T_A = −40°C to +85°C, I_{BG} = ±100 µA (6)	28		ppm/°C
C_{LOAD} V_{BG}	Maximum Bandgap Reference load Capacitance	See (7)		**80**	pF (min)
TEMPERATURE DIODE CHARACTERISTICS					
ΔV_{BE}	Temperature Diode Voltage	192 µA vs. 12 µA, T_J = 25°C	71.23		mV
		192 µA vs. 12 µA, T_J = 85°C	85.54		mV
LVDS INPUT CHARACTERISTICS(CLK+/-, SYNC+/-)					
V_{ID}	Differential Clock Input Level (8)	Sine Wave Clock	0.6	**0.4** **2.0**	V_{P-P} (min) V_{P-P} (max)
		Square Wave Clock	0.6	**0.4** **2.0**	V_{P-P} (min) V_{P-P} (max)
C_{IN}	Input Capacitance (7)	Differential	0.02		pF
		Each input to ground	1.5		pF

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(5) This parameter is ensured by design and is not tested in production.
(6) This parameter is ensured by design and/or characterization and is not tested in production.
(7) This parameter is ensured by design and is not tested in production.
(8) The digital control pin capacitances are die capacitances only. Additional package capacitance of 1.6 pF each pin to ground are isolated from the die capacitances by lead and bond wire inductances.

Converter Electrical Characteristics (continued)

The following specifications apply after calibration for $V_A = V_{TH} = V_C = +1.2V_{DC}$, $V_O = V_{25} = +2.5V_{DC}$, V_{IN} FSR (a.c. coupled) = Default ECM setting, $C_L = 10$ pF, Differential a.c. coupled Sinewave Input Clock, $f_{CLK} = 2.5$ GHz at $0.5V_{P-P}$ with 50% duty cycle, $R_{EXT} = 3600\Omega \pm 0.1\%$, $R_{TRIM} = 3600\Omega \pm 0.1\%$, Analog Signal Source Impedance = 100Ω Differential, after calibration. **Boldface limits apply for $T_A = T_{MIN}$ to T_{MAX}.** All other limits $T_A = 25°C$, unless otherwise noted.(1)(2)

Symbol	Parameter	Conditions	Typical (3)	Limits (3)	Units (Limits)
LVDS OUTPUT CHARACTERISTICS (DS1–DS9+/-, ORAC+/-, ORBD+/-)					
V_{OD}	LVDS Differential Output Voltage	Measured differentially Output Voltage Select = 00	375	**320**	mV_{P-P} (min)
				430	mV_{P-P} (max)
		Measured differentially Output Voltage Select = 01	535	**465**	mV_{P-P} (min)
				605	mV_{P-P} (max)
		Measured differentially Output Voltage Select = 10	625	**540**	mV_{P-P} (min)
				705	mV_{P-P} (max)
		Measured differentially Output Voltage Select = 11	715	**615**	mV_{P-P} (min)
				805	mV_{P-P} (max)
$\Delta V_{O\ DIFF}$	Change in LVDS Output Swing Between Logic Levels		±1		mV
V_{OS}	For Output Offset Voltage, see Figure 1	Output Offset Select = 00	0.77		V
		Output Offset Select = 01	0.95		V
		Output Offset Select = 10	1.14		V
		Output Offset Select = 11	$V_O - 1.14$		V
ΔV_{OS}	Output Offset Voltage Change Between Logic Levels		±1		mV
I_{OS}	Output Short Circuit Current	Output+ & Output- connected to 0.8V	±4		mA
Z_O	Differential Output Impedance		100		Ohms
LVCMOS INPUT CHARACTERISTICS (PD, CAL, SDI, SCLK, SCSb)					
V_{IH}	Logic High Input Voltage	See (9)		**0.85 x V_A**	V (min)
V_{IL}	Logic Low Input Voltage	See (9)		**0.15 x V_A**	V (max)
C_{IN}	Input Capacitance(10)(11)	Each input to ground	0.5		pF
LVCMOS OUTPUT CHARACTERISTICS (SDO, CalRun)					
V_{OH}	CMOS H level output	I_{OH} = -400uA(9)	1.0	**0.80**	V (min)
V_{OL}	CMOS L level output	I_{OH} = 400uA(9)	0.15	**0.3**	V (max)

(9) This parameter is ensured by design and/or characterization and is not tested in production.
(10) This parameter is ensured by design and is not tested in production.
(11) The digital control pin capacitances are die capacitances only. Additional package capacitance of 1.6 pF each pin to ground are isolated from the die capacitances by lead and bond wire inductances.

Converter Electrical Characteristics (continued)

The following specifications apply after calibration for $V_A = V_{TH} = V_C = +1.2V_{DC}$, $V_O = V_{25} = +2.5V_{DC}$, V_{IN} FSR (a.c. coupled) = Default ECM setting, $C_L = 10$ pF, Differential a.c. coupled Sinewave Input Clock, $f_{CLK} = 2.5$ GHz at $0.5V_{P-P}$ with 50% duty cycle, $R_{EXT} = 3600\Omega \pm 0.1\%$, $R_{TRIM} = 3600\Omega \pm 0.1\%$, Analog Signal Source Impedance = 100Ω Differential, after calibration. **Boldface limits apply for $T_A = T_{MIN}$ to T_{MAX}.** All other limits T_A = 25°C, unless otherwise noted.(1)(2)

Symbol	Parameter	Conditions	Typical (3)	Limits (3)	Units (Limits)
POWER SUPPLY CHARACTERISTICS					
I_A	Analog Supply Current	PD = Low	835		mA
I_{TH}	Track and Hold Supply Current	PD = Low	675		mA
I_C	Clock Supply Current	PD = Low	150		mA
I_{25}	2.5V Supply current	PD = Low	290		mA
I_O	Output Driver Supply Current	PD = Low	105		mA
P_D	Power Consumption	PD = Low	3.0	**3.25**	W (max)
		PD = High	60		mW
PSRR1	D.C. Power Supply Rejection Ratio	Change in offset with change in supplies from Min to Max Operating values	70		dB
PSRR2	A.C. Power Supply Rejection Ratio	248 MHz, $100mV_{P-P}$ riding on supplies	50		dB
AC ELECTRICAL CHARACTERISTICS - Sampling Clock					
f_{CLK1}	Maximum Input Clock Frequency	Sampling rate is 2x clock input		**2.5**	GHz (min)
f_{CLK2}	Minimum Input Clock Frequency	Sampling rate is 2x clock input		**1.0**	GHz (max)
t_{CYC}	Input Clock Duty Cycle	$f_{CLK2} \leq$ Input clock frequency $\leq f_{CLK1}$ (12)	50	**30** **70**	% (min) % (max)
t_{LC}	Input Clock Low Time	$f_{CLK} = f_{CLK1}$ (13)		**120**	ps (min)
t_{HC}	Input Clock High Time	$f_{CLK} = f_{CLK1}$ (13)		**120**	ps (min)
t_{AJ}	Aperture Jitter		0.55		ps rms

(12) This parameter is ensured by design and/or characterization and is not tested in production.
(13) This parameter is ensured by design and is not tested in production.

Converter Electrical Characteristics (continued)

The following specifications apply after calibration for $V_A = V_{TH} = V_C = +1.2V_{DC}$, $V_O = V_{25} = +2.5V_{DC}$, V_{IN} FSR (a.c. coupled) = Default ECM setting, C_L = 10 pF, Differential a.c. coupled Sinewave Input Clock, f_{CLK} = 2.5 GHz at $0.5V_{P-P}$ with 50% duty cycle, R_{EXT} = 3600Ω ±0.1%, R_{TRIM} = 3600Ω ±0.1%, Analog Signal Source Impedance = 100Ω Differential, after calibration. **Boldface limits apply for $T_A = T_{MIN}$ to T_{MAX}.** All other limits T_A = 25°C, unless otherwise noted.(1)(2)

Symbol	Parameter	Conditions	Typical (3)	Limits (3)	Units (Limits)
t_{LAT_Ad1}	Pipeline Delay (Latency)(14)	Single Mode		**42**	Input Clock Cycles
t_{LAT_Bd1}				**41.5**	
t_{LAT_Cd1}				**41**	
t_{LAT_Dd1}				**40.5**	
t_{LAT_A1}				**40**	
t_{LAT_B1}				**39.5**	
t_{LAT_C1}				**39**	
t_{LAT_D1}				**38.5**	
t_{LAT_ABd1}		Dual Mode		**42**	
t_{LAT_CDd1}				**41**	
t_{LAT_AB1}				**40**	
t_{LAT_CD1}				**39**	
t_{LAT_ABCDd1}		Quad Mode		**42**	
t_{LAT_ABCD1}				**40**	
AC ELECTRICAL CHARACTERISTICS - Output Data(15)					
t_{LHT}	LH Transition Time - Differential	10% to 90%	150		ps
t_{HLT}	HL Transition Time - Differential	10% to 90%	150		ps
AC ELECTRICAL CHARACTERISTICS - Serial Interface Clock					
f_{SCLK}	Serial Clock Frequency			**15**	MHz (max)
	Serial Clock Low Time			**30**	ns (min)
	Serial Clock High Time			**30**	ns (min)
t_{SSU}	Serial Data to Serial Clock Rising Setup Time	See (14)		**2.5**	ns (min)
t_{SH}	Serial Data to Serial Clock Rising Hold Time	See (14)		**2.5**	ns (min)
t_{SCS}	SCSb-to-Serial Clock Rising Setup Time		2.5		ns
t_{HCS}	SCSb-to-Serial Clock Falling Hold time		2.5		ns
t_{BSU}	Bus turn-around time		10		ns
AC ELECTRICAL CHARACTERISTICS - General Signals					
t_{PWR}	Pulse Width SYNC±	See (14)		**4**	CLK± Cyc. (min)
t_{LAT_SYNC}	Latency SYNC transition capture to Frame Edge	See (14)		**28**	CLK± Cyc.
t_{WU}	PD low to Rated Accuracy Conversion (Wake-Up Time)	See (14)	100		ms
t_{CAL}	Calibration Cycle Time		2.895×10^6		CLK± Cyc.
t_{CAL_L}	CAL Pin Low Time	See Figure 9 (14)		**80**	CLK± Cyc. (min)
t_{CAL_H}	CAL Pin High Time	See Figure 9 (14)		**80**	CLK± Cyc. (min)

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(14) This parameter is ensured by design and is not tested in production.
(15) All parameters are measured through a transmission line and 100Ω termination using a 0.33pF load oscilloscope probe.

Specification Definitions

APERTURE (SAMPLING) DELAY is the amount of delay, measured from the sampling edge of the Clock input, after which the signal present at the input pin is sampled inside the device.

APERTURE JITTER (t_{AJ}) is the variation in aperture delay from sample to sample. Aperture jitter shows up as input noise.

CLOCK DUTY CYCLE is the ratio of the time that the clock wave form is at a logic high to the total time of one clock period.

DIFFERENTIAL NON-LINEARITY (DNL) is the maximum deviation from the ideal step size of 1 LSB. Measured at 4 GSPS with a sine wave input.

EFFECTIVE NUMBER OF BITS (ENOB, or EFFECTIVE BITS) is another method of specifying Signal-to-Noise and Distortion Ratio, or SINAD. ENOB is defined as (SINAD − 1.76) / 6.02 and says that the converter is equivalent to a perfect ADC of this (ENOB) number of bits.

FULL POWER BANDWIDTH (FPBW) is a measure of the frequency at which the reconstructed output fundamental drops 3 dB below its low frequency value for a full scale input.

GAIN ERROR is the deviation from the ideal slope of the transfer function. It can be calculated from Offset and Full-Scale Errors:

- Positive Gain Error = Offset Error − Positive Full-Scale Error
- Negative Gain Error = −(Offset Error − Negative Full-Scale Error)
- Gain Error = Negative Full-Scale Error − Positive Full-Scale Error = Positive Gain Error + Negative Gain Error

INTEGRAL NON-LINEARITY (INL) is the maximum departure of the transfer curve of each individual code from a straight line through the input to output transfer function. The deviation of any given code from this straight line is measured from the center of that code value. The best fit method is used.

INTERMODULATION DISTORTION (IMD) is the creation of additional spectral components as a result of two sinusoidal frequencies being applied to the ADC input at the same time. It is defined as the ratio of the power in the second and third order intermodulation products to the power in one of the original frequencies. IMD is usually expressed in dBFS.

LSB (LEAST SIGNIFICANT BIT) is the bit that has the smallest value or weight of all bits. This value is

$$V_{FS} / 2^n \tag{1}$$

where V_{FS} is the differential full-scale amplitude of V_{IN} as set by the FSR input (pin-14) and "n" is the ADC resolution in bits, which is 8 for the LM97600.

LVDS DIFFERENTIAL OUTPUT VOLTAGE (V_{OD}) is the absolute value of the difference between the V_D+ & V_D- outputs; each measured with respect to Ground.

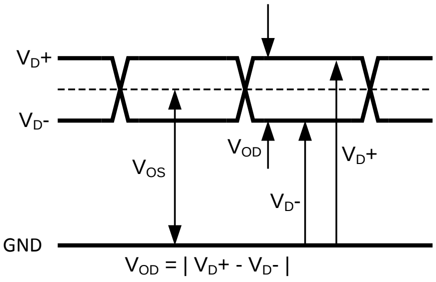


Figure 1. LVDS Output Signal Levels

LVDS OUTPUT OFFSET VOLTAGE (V_{OS}) is the midpoint between the D+ and D- pins output voltage; i.e., [(V_D+) +(V_D-)]/2.

MISSING CODES are those output codes that are skipped and will never appear at the ADC outputs. These codes cannot be reached with any input value.

MSB (MOST SIGNIFICANT BIT) is the bit that has the largest value or weight. Its value is one half of full scale.

NEGATIVE FULL-SCALE ERROR (NFSE) is a measure of how far the first code transition is from the ideal 1/2 LSB above a differential -V_{IN} / 2. For the LM97600 the reference voltage is assumed to be ideal, so this error is a combination of full-scale error and reference voltage error.

OFFSET ERROR (V_{OFF}) is a measure of how far the mid-scale point is from the ideal zero voltage differential input.

Offset Error = Actual Input causing average of 8k samples to result in an average code of 128.

OVER-RANGE RECOVERY TIME is the time required after the differential input voltages goes from ±1.2V to 0V for the converter to recover and make a conversion with its rated accuracy.

PIPELINE DELAY (LATENCY) is the number of input clock cycles between initiation of conversion and when that data is present at the serializer output. New data words are available at every clock cycle, but the data lags the conversion by the Pipeline Delay.

POSITIVE FULL-SCALE ERROR (PFSE) is a measure of how far the last code transition is from the ideal 1-1/2 LSB below a differential +V_{IN} / 2. For the LM97600 the reference voltage is assumed to be ideal, so this error is a combination of full-scale error and reference voltage error.

POWER SUPPLY REJECTION RATIO (PSRR) can be one of two specifications. PSRR1 (DC PSRR) is the ratio of the change in full-scale error that results from a power supply voltage change from 1.8V to 2.0V. PSRR2 (AC PSRR) is a measure of how well an a.c. signal riding upon the power supply is rejected from the output and is measured with a 248 MHz, 100 mV_{P-P} signal riding upon the power supply. It is the ratio of the output amplitude of that signal at the output to its amplitude on the power supply pin. PSRR is expressed in dB.

SIGNAL TO NOISE RATIO (SNR) is the ratio, expressed in dB, of the rms value of the input signal at the output to the rms value of the sum of all other spectral components below one-half the sampling frequency, not including harmonics or d.c.

SIGNAL TO NOISE PLUS DISTORTION (S/(N+D) or SINAD) is the ratio, expressed in dB, of the rms value of the input signal at the output to the rms value of all of the other spectral components below half the input clock frequency, including harmonics but excluding d.c.

SPURIOUS-FREE DYNAMIC RANGE (SFDR) is the difference, expressed in dB, between the rms values of the input signal at the output and the peak spurious signal, where a spurious signal is any signal present in the output spectrum that is not present at the input, excluding d.c.

TOTAL HARMONIC DISTORTION (THD) is the ratio expressed in dB, of the rms total of the first nine harmonic levels at the output to the level of the fundamental at the output. THD is calculated as

$$\text{THD} = 20 \text{ x } \log \sqrt{\frac{A_{f2}^{2} + \ldots + A_{f10}^{2}}{A_{f1}^{2}}} \tag{2}$$

where A_{f1} is the RMS power of the fundamental (output) frequency and A_{f2} through A_{f10} are the RMS power of the first 9 harmonic frequencies in the output spectrum

Second Harmonic Distortion (2nd Harm) is the difference, expressed in dB, between the RMS power in the input frequency seen at the output and the power in its 2nd harmonic level at the output.

Third Harmonic Distortion (3rd Harm) is the difference expressed in dB between the RMS power in the input frequency seen at the output and the power in its 3rd harmonic level at the output.

WORD ERROR RATE is the probability of error and is defined as the probable number of errors per unit of time divided by the number of words seen in that amount of time. A Word Error Rate of 10^{-18} corresponds to a statistical error in one conversion about every four (4) years.

Transfer Characteristic

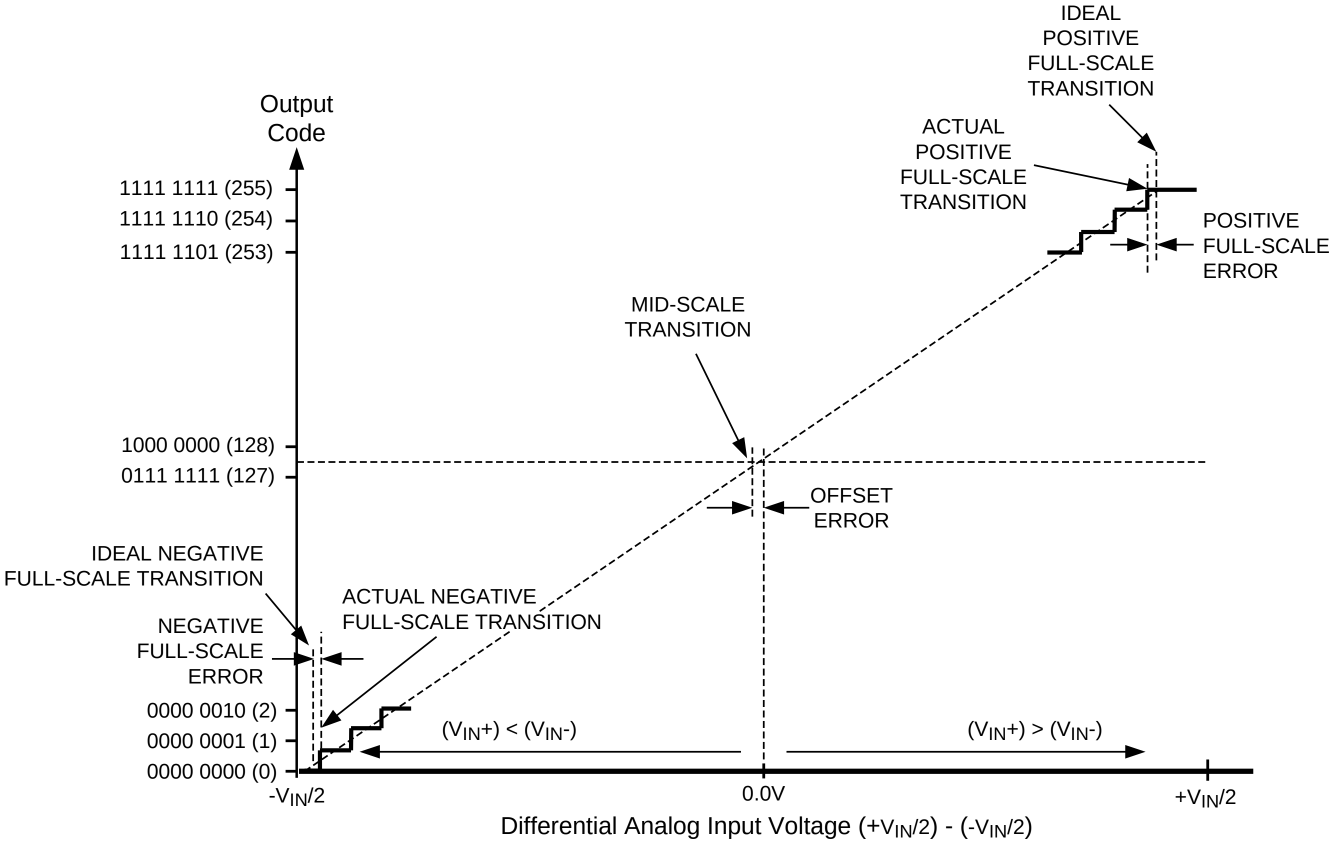


Figure 2. Input / Output Transfer Characteristic

TIMING DIAGRAMS

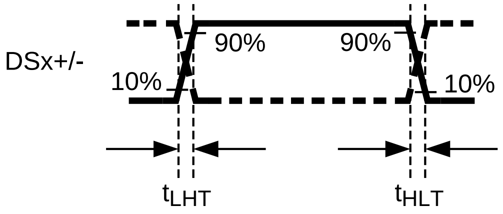


Figure 3. Output Data Timing

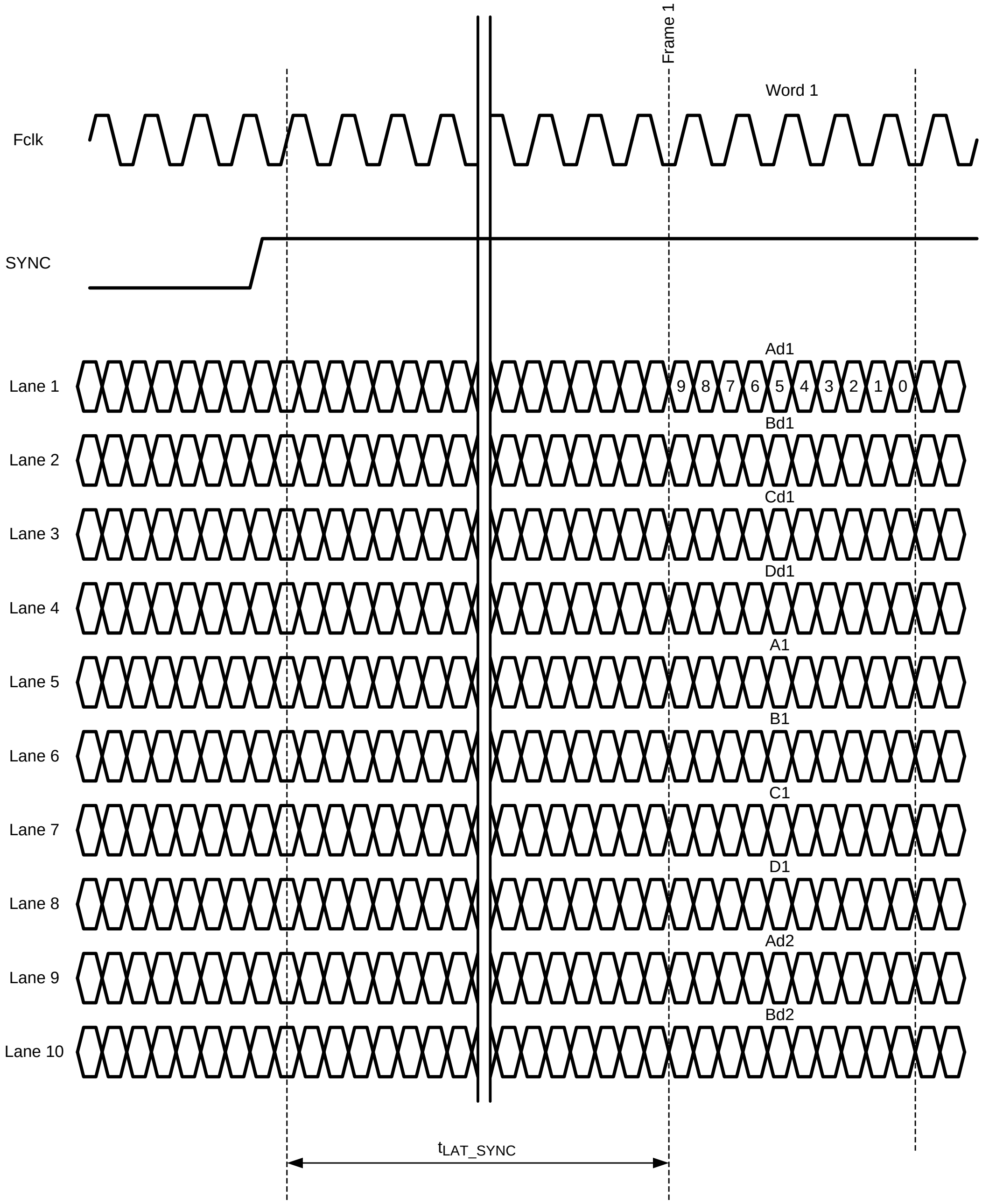


Figure 4. SYNC Timing - Rising Edge

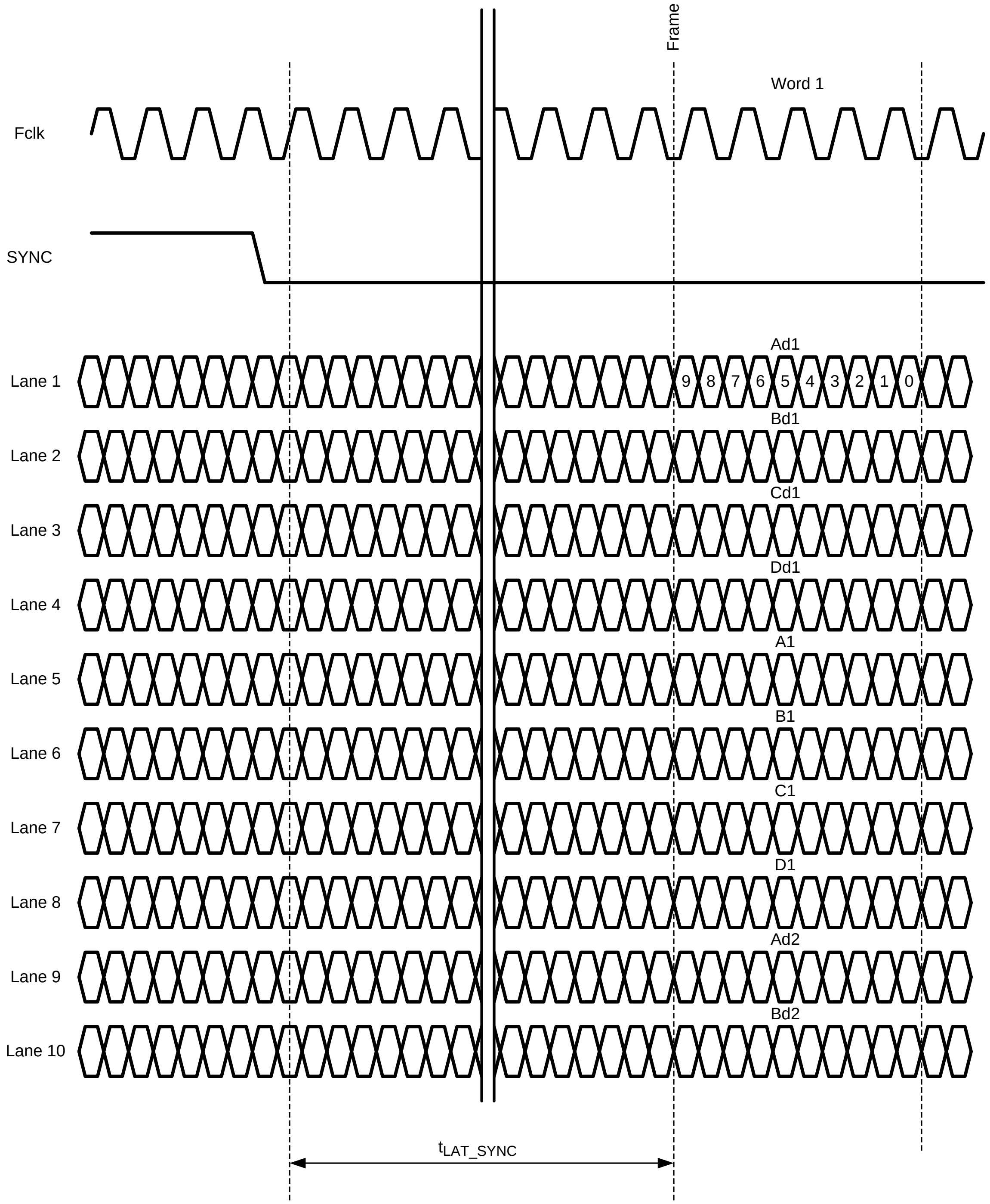


Figure 5. SYNC Timing - Falling Edge

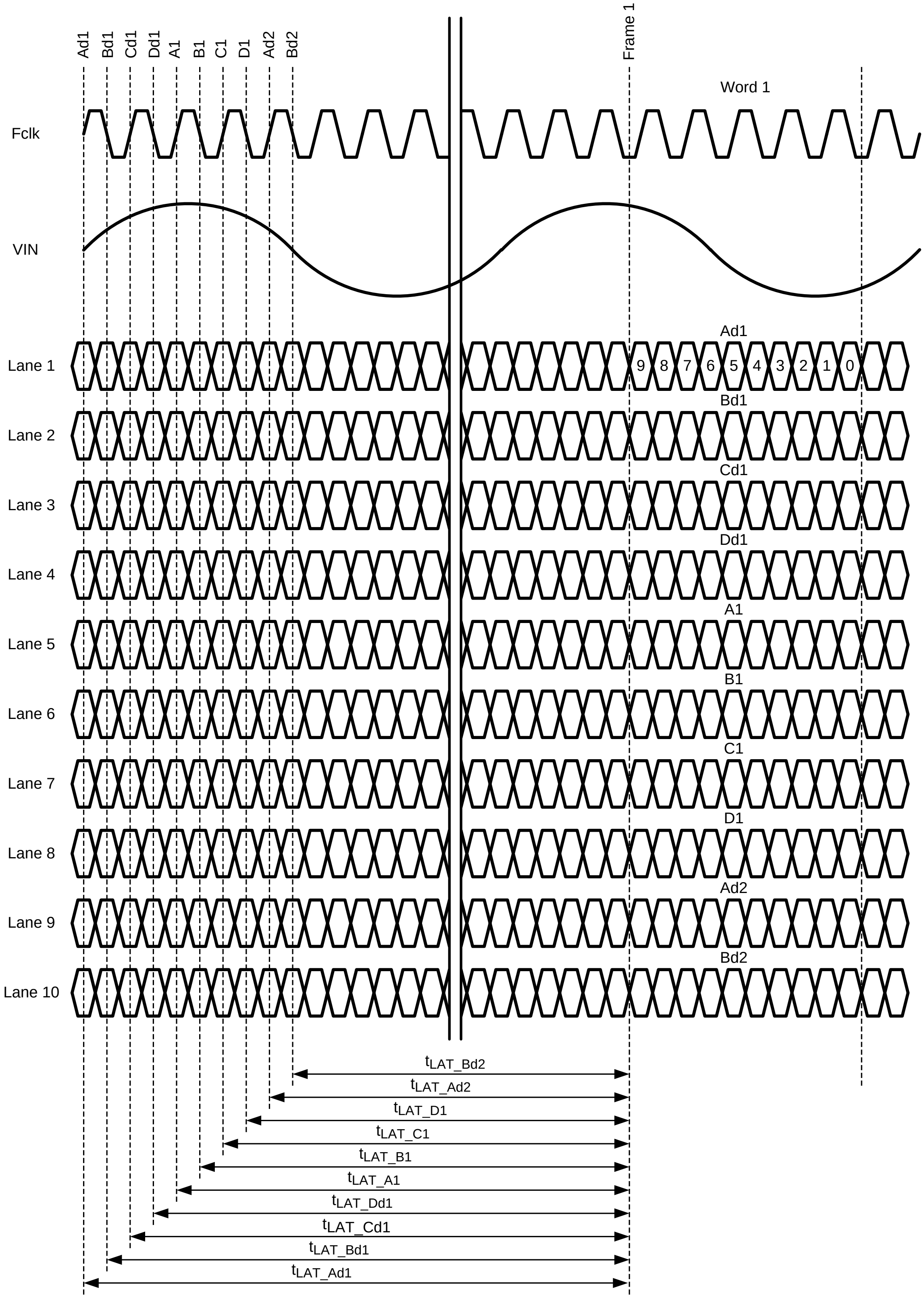


Figure 6. Latency - Single ADC Mode

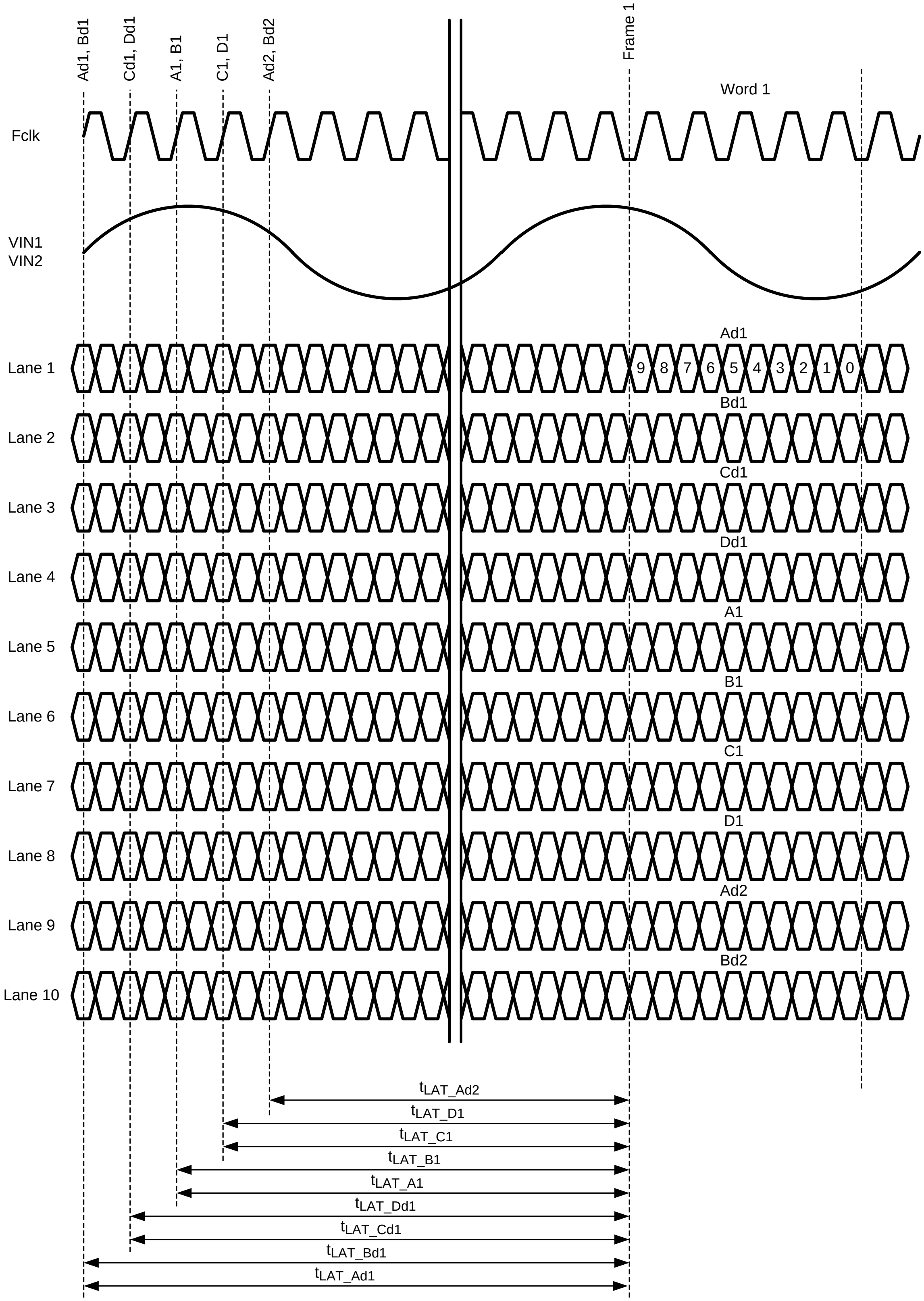


Figure 7. Latency - Dual ADC Mode

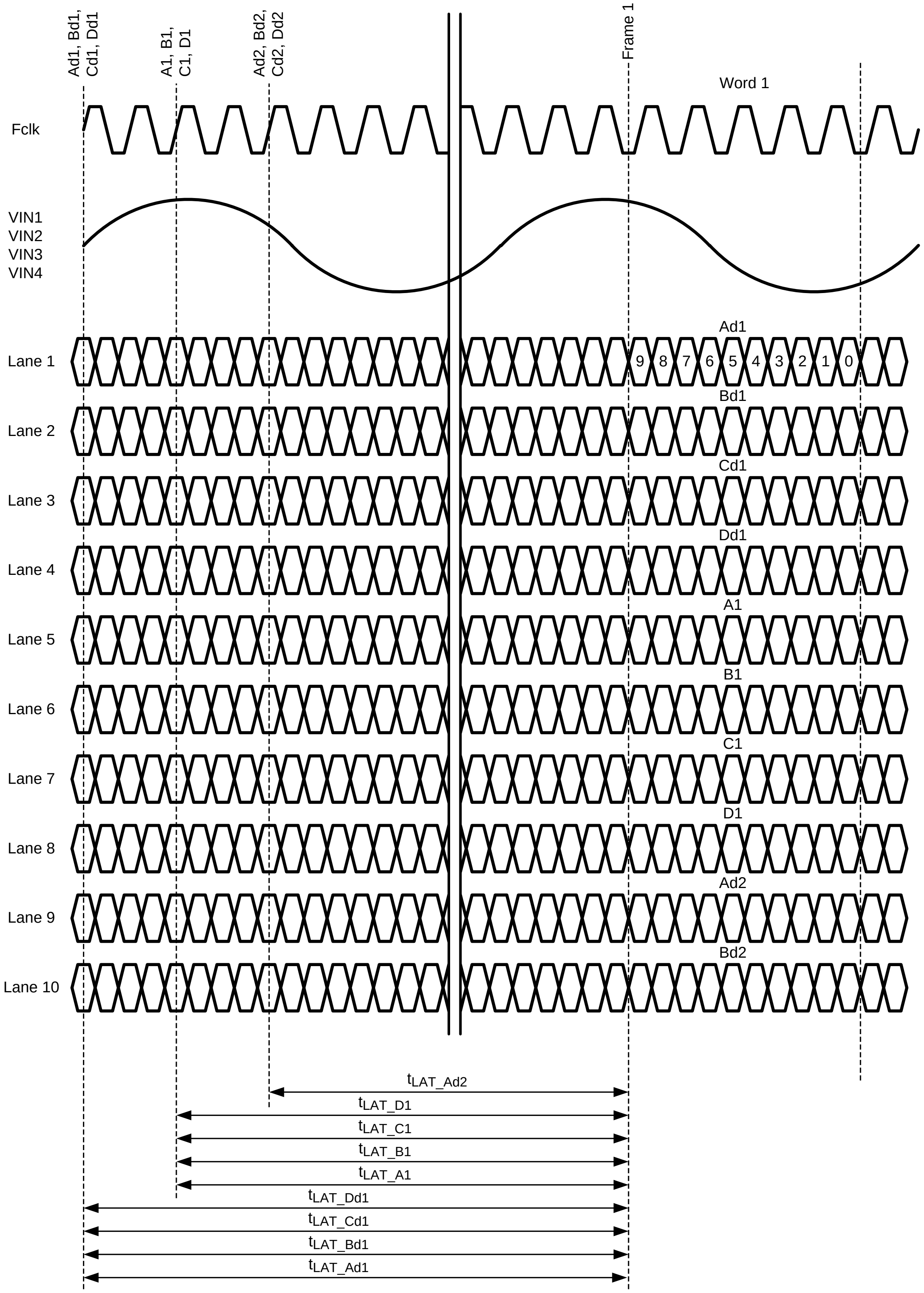


Figure 8. Latency - Quad ADC Mode

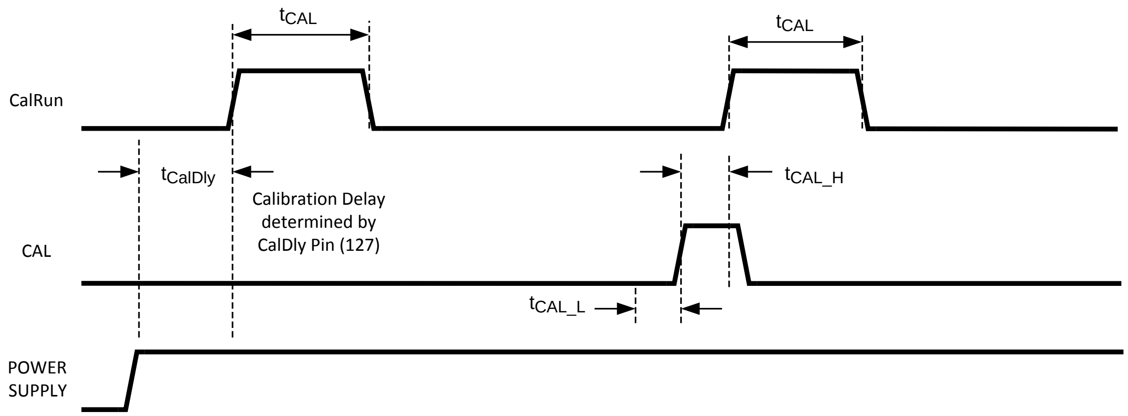


Figure 9. Calibration and On-Command Calibration Timing

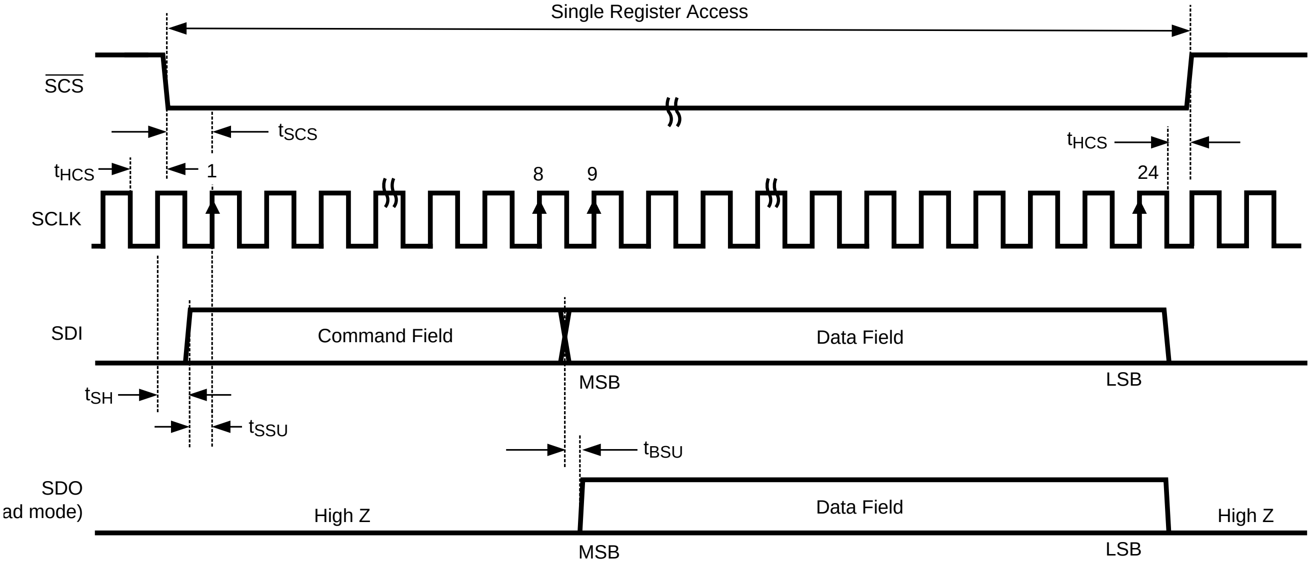


Figure 10. Serial Interface Timing

Typical Performance Characteristics

V_A=V_{TH}=V_C=1.2V, V_O=V_{25}=2.5V, F_{CLK}=2500 MHz, T_A=25°C unless otherwise stated.

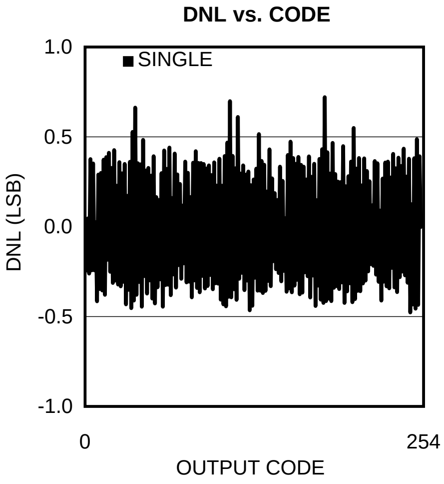


Figure 11.

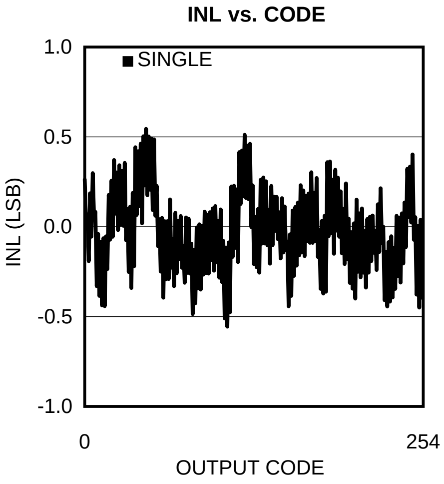


Figure 12.

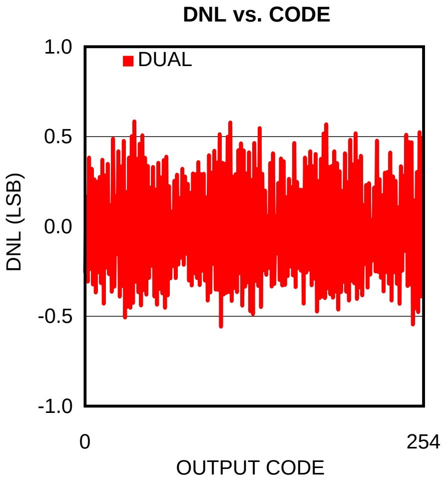
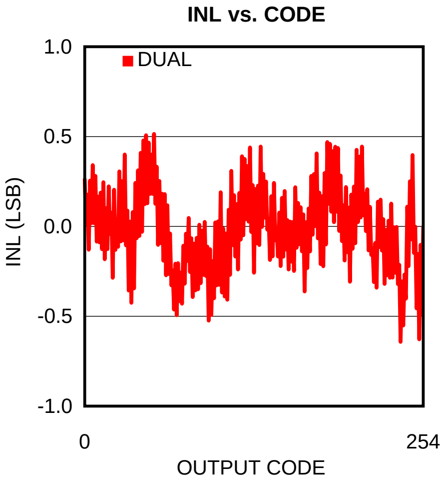


Figure 13.



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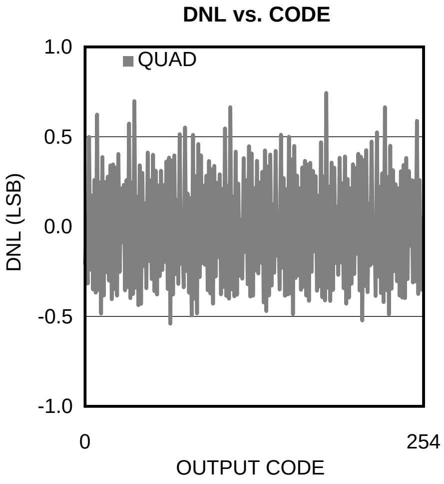

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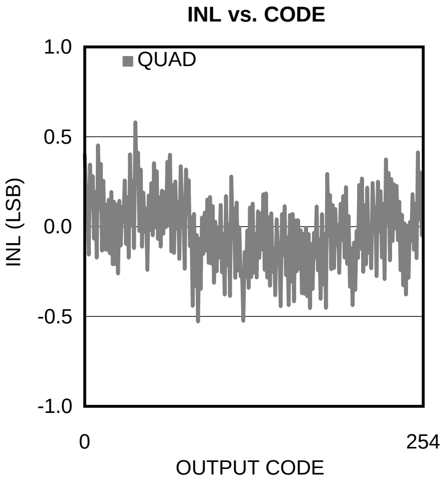


Figure 16.

Typical Performance Characteristics (continued)

V_A=V_{TH}=V_C=1.2V, V_O=V_{25}=2.5V, F_{CLK}=2500 MHz, T_A=25°C unless otherwise stated.

MAX DNL vs. TEMPERATURE

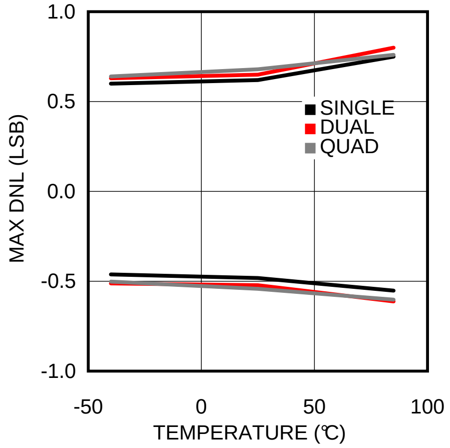


Figure 17.

MAX INL vs. TEMPERATURE

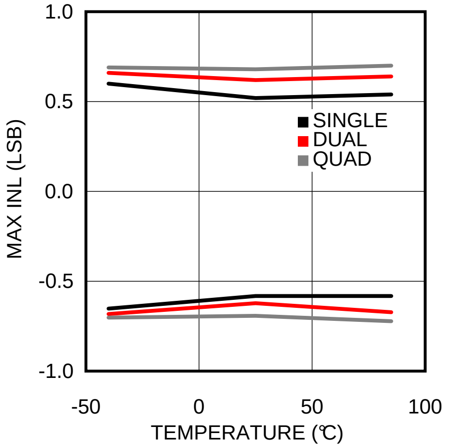


Figure 18.

ENOB vs. AMBIENT TEMPERATURE

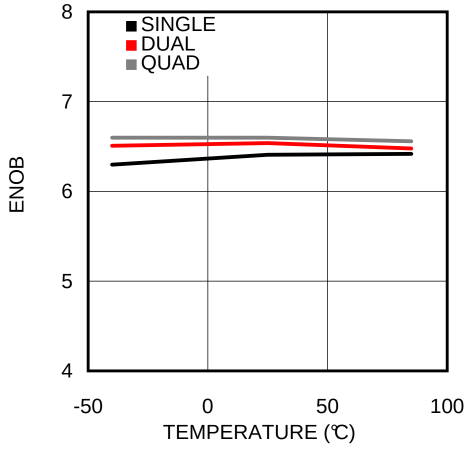


Figure 19.

ENOB vs. SUPPLY VOLTAGE

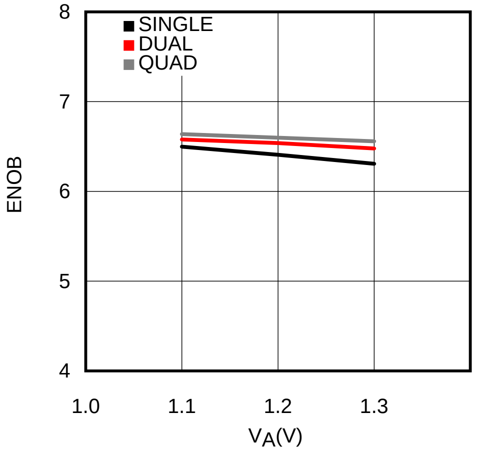


Figure 20.

ENOB vs. SAMPLE RATE

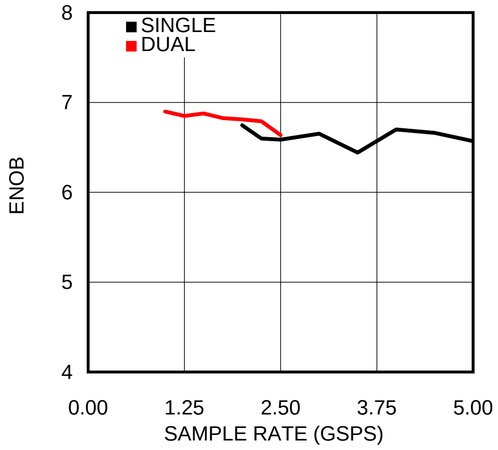


Figure 21.

ENOB vs. INPUT FREQUENCY

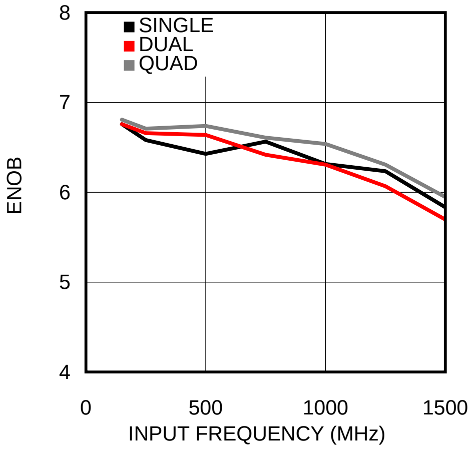


Figure 22.

Typical Performance Characteristics (continued)

V_A=V_{TH}=V_C=1.2V, V_O=V_{25}=2.5V, F_{CLK}=2500 MHz, T_A=25°C unless otherwise stated.

SNR vs. AMBIENT TEMPERATURE

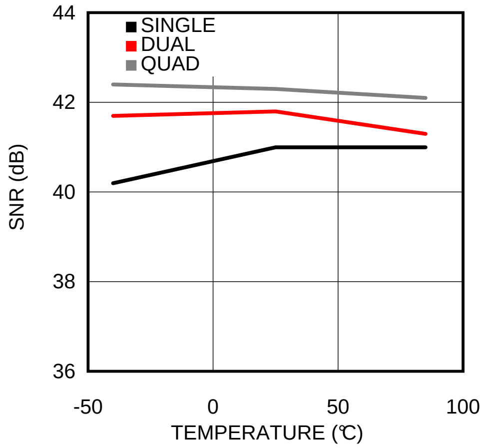


Figure 23.

SNR vs. SUPPLY VOLTAGE

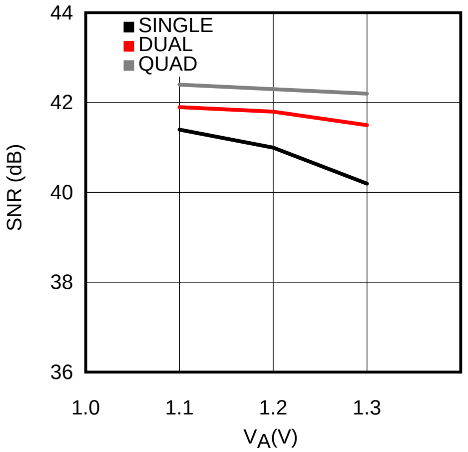


Figure 24.

SNR vs. SAMPLE RATE

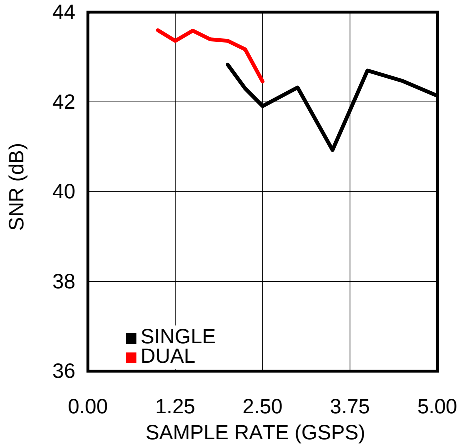


Figure 25.

SNR vs. INPUT FREQUENCY

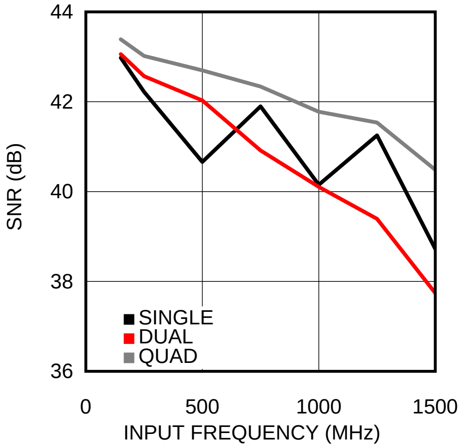


Figure 26.

THD vs. AMBIENT TEMPERATURE

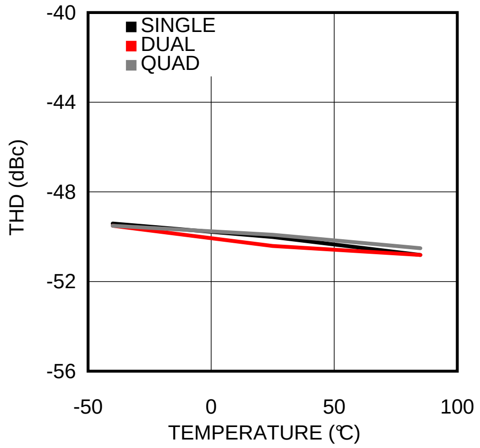


Figure 27.

THD vs. SUPPLY VOLTAGE

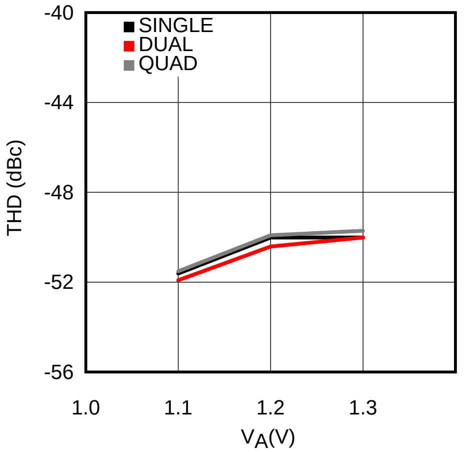


Figure 28.

Typical Performance Characteristics (continued)

V_A=V_{TH}=V_C=1.2V, V_O=V_{25}=2.5V, F_{CLK}=2500 MHz, T_A=25°C unless otherwise stated.

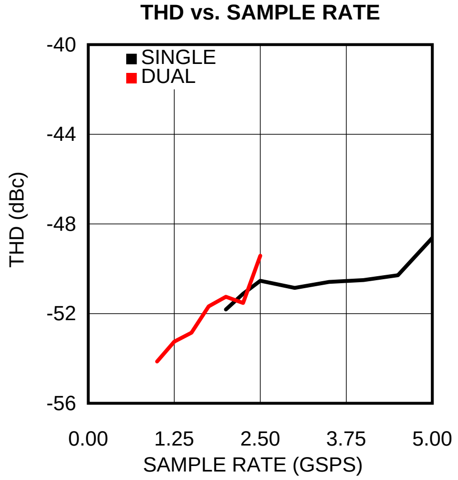


Figure 29.

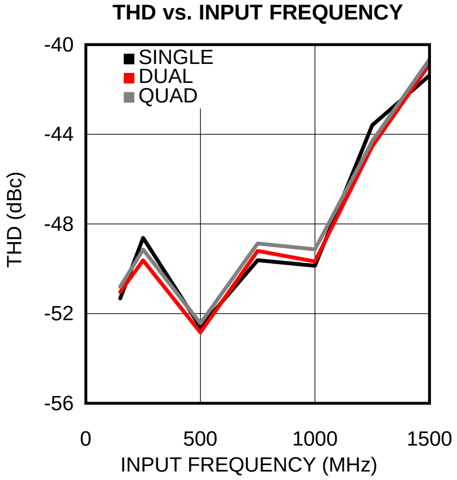


Figure 30.

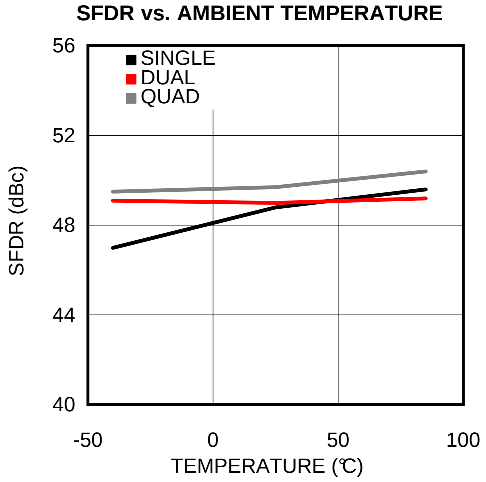


Figure 31.

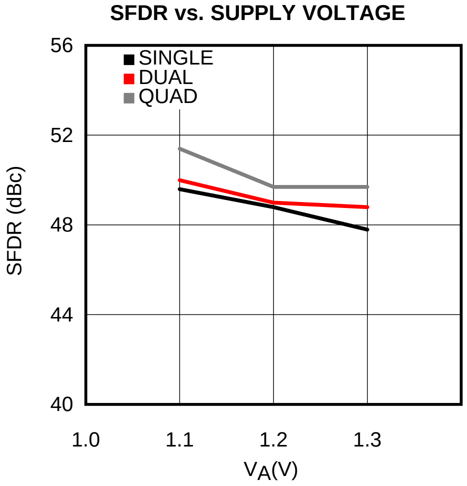


Figure 32.

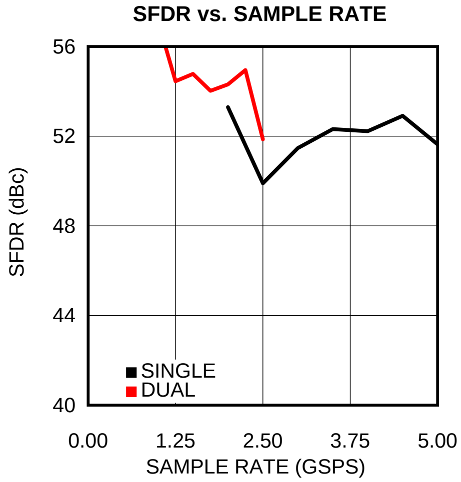


Figure 33.

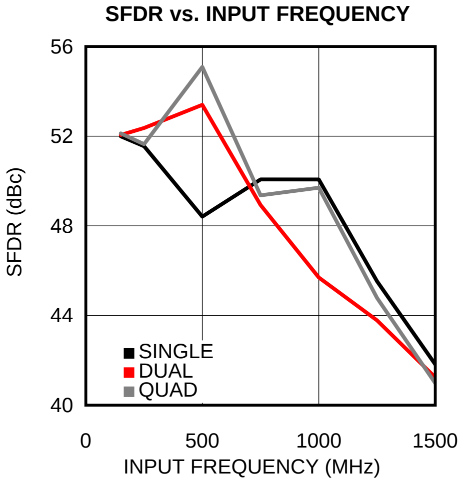
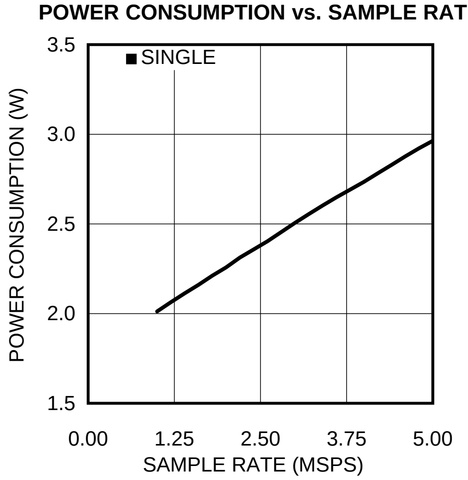


Figure 34.

Typical Performance Characteristics (continued)

V_A=V_{TH}=V_C=1.2V, V_O=V_{25}=2.5V, F_{CLK}=2500 MHz, T_A=25°C unless otherwise stated.



Power consumption is similar for dual and quad modes.

Figure 35.

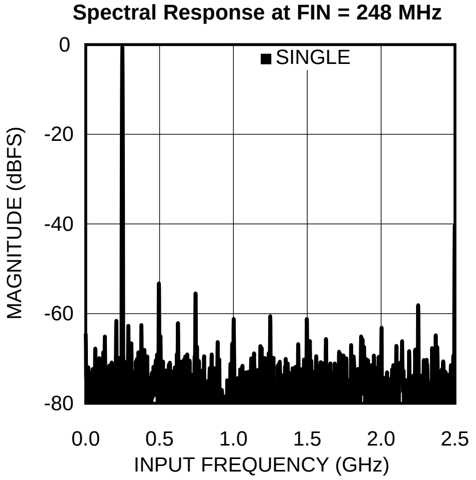


Figure 36.

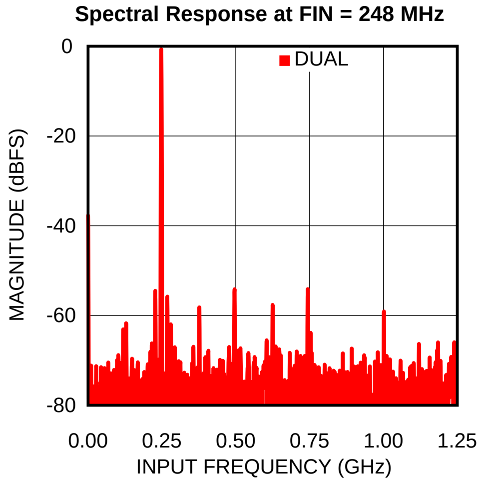


Figure 37.

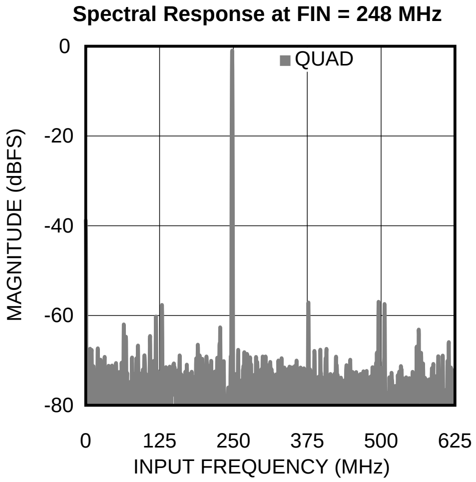


Figure 38.

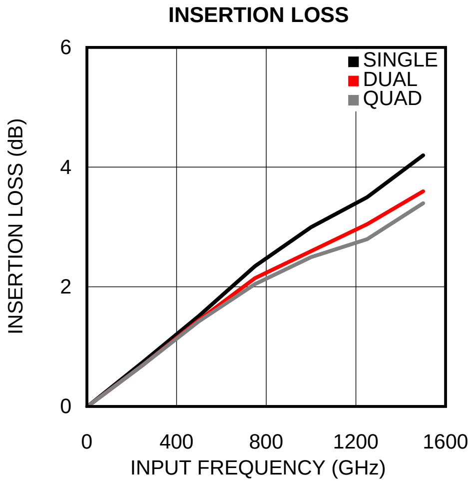


Figure 39.

FUNCTIONAL DESCRIPTION

The LM97600 is a versatile A/D Converter with an innovative architecture permitting very high speed operation. The controls available ease the application of the device to circuit solutions. Optimum performance requires adherence to the provisions discussed here and in the Applications Information section.

OVERVIEW

The LM97600 uses a calibrated folding and interpolating architecture that achieves 7.0 effective bits at sampling rates up to 5.0 GS/s.

One clock input serves all converters. Special clock duty-cycle correction and alignment circuitry plus a high-bandwidth input signal MUX allows the user to operate the four converters in the following three configurations:

- Four converters operated independently (Input 1 to Channel A, Input 2 to Channel C, etc.)
- Two groups of two converters interleaved into two independent channels (Input 1 or 2 to Channel A+C; and Input 3 or 4 to Channel B+D)
- Four converters interleaved into one channel with one input

Channel labels A, B, C, D indicate the time-order of sampling by the four converters when interleaved. Note that each of the four ADCs is made up of two interleaved sub-ADCs, for a total of eight sub-ADCs. The outputs of these sub-ADCs must be interleaved at the receiver in the proper order to re-create the sampled data sequence.

The digital output samples are 8B/10B encoded and serialized before being driven out at a maximum of 5-Gbps per lane. Each 7 or 8 bit sample (see below for explanation of sample size) is encoded to a 10-bit, dc-balanced word, and mapped to output lanes 1 to 10 in succession. Encoding and mapping is independent of whether the device is operating as a single, dual, or quad ADC.

Selective Truncation

Each of the eight interleaved sub-ADCs digitizes its analog input to 8-bit resolution at a rate equal to 1/4th the input clock rate (or 1/8th the fully-interleaved sample rate). The output of each sub-ADC is then truncated to 7-bits for three out every eight consecutive samples. In a truncated sample the least-significant-bit (LSB) is forced to zero.

Table 1. Truncation Pattern

Sample Number	n	n+1	n+2	n+3	n+4	n+5	n+6	n+7
LSB Truncated			X		X			X
Digital Word Size	8	8	7	8	7	8	8	7

Each of the eight sub-ADCs has its own divide-by-N (N=26) counter incrementing once every clock cycle. The fixed truncation pattern shown above repeats continuously, but is delayed by one clock cycle every time the counter reaches a pre-programmed value. The value that causes the pattern to delay is unique for each sub-ADC, which reduces the occurrence of long, contiguous sequences of truncated words. Data is not truncated when the pattern is delayed.

For N=26, there are (5/8 * 26) = 16.25 non-truncated words every 27 samples. On average this equates to (16.25 / 27) = 0.601 (rounded to 0.6) valid bits in the LSB position at the interleaved sample rate.

The initial value of each of the eight counters is determined at power-up through a combination of random noise and part-to-part process variation. Since each sub-ADC truncates its data at unpredictable points in time, it is not possible to under-sample the output data stream at pre-determined instants to obtain only non-truncated data.

Table 2. Example Truncation Pattern With Delay

Sample Number	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
Divide by N count	18	19	20	21	22	23	24	25	0	1	2	3	4	5	6	7	8	9
Delay triggered									X									
LSB truncated			X		X			X				X		X			X	

Calibration

A calibration is performed upon power-up and can also be invoked by the user upon command. Calibration trims the INx and CLK input differential termination resistors and minimizes full-scale error, offset error, DNL and INL, resulting in maximizing SNR, THD, SINAD (SNDR) and ENOB. Internal bias currents are also set with the calibration process. All of this is true whether the calibration is performed upon power up or is performed upon command. Running the calibration is an important part of this chip's functionality and is required in order to obtain adequate performance. In addition to the requirement to be run at power-up, calibration must be re-run by the user whenever the input Full Scale Range is changed significantly. For best performance, we recommend an on command calibration be run after initial power up and the device has reached a stable temperature. Also, we recommend that an on command calibration be run whenever the operating temperature changes significantly relative to the specific system performance requirements.

In normal operation, calibration is performed just after application of power and whenever a valid calibration command is given, which is holding the CAL pin low for at least 80 input clock cycles, then hold it high for at least another 80 input clock cycles. The time taken by the calibration procedure is specified in the A.C. Characteristics table. Holding the CAL pin high during power up will prevent the calibration process from running until the CAL pin experiences the above-mentioned 80 input clock cycles low followed by 80 cycles high.

The CAL bit does not reset itself to zero automatically, but must be manually reset before another calibration event can be initiated. If no further calibration event is desired, the CAL bit may be left high indefinitely, with no negative consequences.

Acquiring the Input

Depending on operating mode, data is acquired at the rising, or both the rising and falling edges of CLK and the digital equivalent of that data is available in the serialized data stream 38 to 42 input clock cycles later.

The LM97600 will convert as long as the input clock signal is present. The fully differential comparator design and the innovative design of the sample-and-hold amplifier, together with calibration, enables very good SINAD/ENOB response beyond 1.5 GHz. The LM97600 output data signaling is serialized LVDS and the data is encoding is offset binary.

Configuration and Control

The LM97600 configuration and control is achieved via a number of logic input pins in combination with a number configuration registers accessed via a serial interface. For more details refer to the DEVICE CONTROL section.

The Analog Inputs

The LM97600 must be driven with a differential input signal. Operation with a single-ended signal is not recommended as performance will suffer. It is important that the input signals are either a.c. coupled to the inputs (Configuration Register 1 Bit 5 = 0), or d.c. coupled (Configuration Register 1, Bit 5 = 1). An input common mode voltage equal to the V_{CMO} output must be provided when d.c. coupling is used.

The full-scale input range for each converter can be set to values between 560 mV_{P-P} and 840 mV_{P-P} through the serial interface. See THE ANALOG INPUT.

Clocking

The LM97600 sampling clock (CLK+/CLK-) must be driven with an a.c. coupled, differential clock signal. The THE SAMPLE CLOCK INPUT section describes the use of the clock input pins.

The sampling clock CLK has duty cycle correction as part of its circuit. This circuitry allows the ADC to be clocked with a signal source having a duty cycle of 70 to 30 % (worst case).

The LVDS Outputs

The data outputs (DS#) and Out Of Range (ORAC, ORBD) are LVDS. The differential output voltage swing is set via the Output Voltage Select setting in Serial Config 1, Bits 11:10. The default setting of 400 mVp-p should work for typical short distance interfaces. If large swings are necessary to compensate for additional distance, noise pickup, etc., the output swing can be set as high as 800 mVp-p with a slight increase in device power consumption.

The LVDS data outputs have an adjustable common mode voltage which is set via the Output Offset Select setting in Serial Config 1, Bits 13:12. The default output offset is approximately 0.8V which should be compatible with most applications, especially since the serialized interface is usually AC coupled.

Power Down

The LM97600 is in the active state when the Power Down pin (PD) is low. When the PD pin is high, the device is in the power down mode. In this power down mode the data output pins (positive and negative) including OR +/- are put into a high impedance state and the device power consumption is reduced to a minimal level.

If the PD input is brought high while a calibration is running, the device will not go into power down until the calibration sequence is complete. Additionally, if the PD input rises at the same time as initial power-up, the device will not begin the calibration sequence until the PD input goes low. If a manual calibration is requested while the device is powered down, the calibration will not begin at all. That is, the manual calibration input is completely ignored in the power down state.

DEVICE CONTROL

The LM97600 is controlled via logic inputs and register control. The table below summarizes which features are controlled via logic pin or register.

Table 3. Features and Modes

Feature	Pin Control	Register Control
LVDS output level	n/a	Selected with Output Voltage Select (11h; Bits 11:10).
LVDS output offset	n/a	Selected with Output Offset Select (11h, Bits 13:12)
ADC Mode	n/a	ADC operating mode (Single, Dual, Quad) set via ADC Mode. (01h, Bits 15:14)
Input Select	n/a	Selected with Input Select. (01h, Bits 13:6)
AC/DC Coupling	n/a	AC/DC coupling mode is set by the DC Coupled Mode Select bit. (01h, Bit 5)
Channel Full-Scale Range	n/a	Up to 512 step adjustments over a nominal range of 560 mV to 840 mV in the Full-Scale Range Setting Registers (4,6,8,Ah; Bits 15:7).
Channel Offset	n/a	Up to ±45 mV adjustments in 512 steps in the Offset Setting Registers (5,7,9,Bh; Bits 15:7,6).
Sampling Clock Delay	n/a	The clock phase can be adjusted manually through the Fine, Intermediate & Coarse Aperture Delay settings (0Ch). This feature is enabled/disabled via the Set t_{AD} adjust bit. (01h, Bit 0)
ADC Test Patterns	n/a	A test pattern can be made present at the output of each ADC by setting the ADC Test Pattern Mode Select bit. (01h; Bit 3).
Calibration Settings	n/a	Calibration Configuration (03h)
Multi-ADC Sync	SYNC+/−, Balls A5/B5	SYNC (10h) Clock Bump (01h, Bit 1)
Input Termination Impedance	n/a	Selected by Termination Value (02h, Bit 14)
Data Serializer Settings	n/a	Selected via Serial Config 1–4. (11h, 12h, 13h, 14h)
Initiate Training Pattern	SYNC+/−, Balls A5/B5	n/a
Initiate Calibration	CAL, Ball W5	Initiate CALibration (02h, Bit 15)
Power Down	PD, Ball Y5	n/a

SERIAL OUTPUT DATA FORMATTING

ADC data is generated by the 4 internal ADCs. Each ADC generates a current and a delayed (sampled earlier in time) sample. For exampled, converter A outputs a normal A sampled, and an Ad delayed sample simultaneously. The outputs of all 4 converters (4 current and 4 delayed samples) are transferred to 8b10b encoder blocks. To keep the sampling clock and output data clock operating at the same frequency, it is easiest to have 10 lanes of data output . To accomplish this, the ADC output data is mapped into a frame which is 4 samples long and 10 lanes wide. This mapping function is performed before 8b10b encoding and serialization.

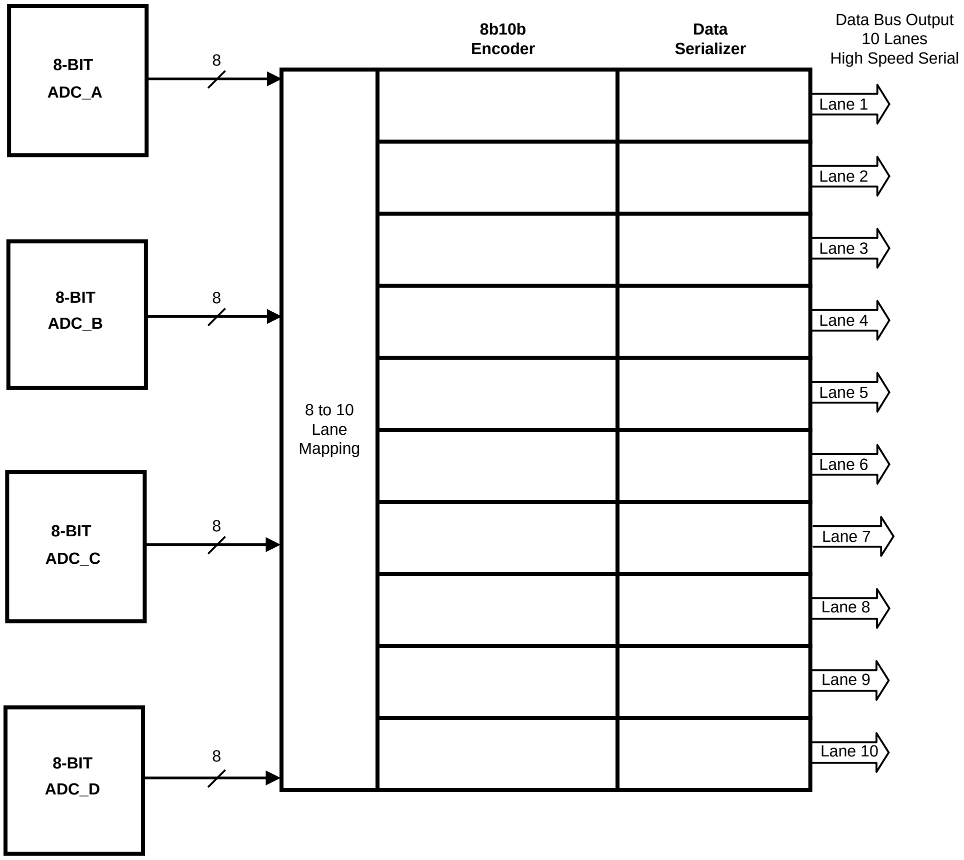


Figure 40. ADC Data Flow

The mapping sequence is shown below:

Table 4. Output Data Mapping

Lane	Word 1	Word 2	Word 3	Word 4	Word 5
	Frame 1				Frame 2...
1	**Ad_1**	Cd_2	A_3	C_4	**Ad_6**
2	Bd_1	Dd_2	B_3	D_4	Bd_6
3	Cd_1	A_2	C_3	Ad_5	Cd_6
4	Dd_1	B_2	D_3	Bd_5	Dd_6
5	A_1	C_2	Ad_4	Cd_5	A_6
6	B_1	D_2	Bd_4	Dd_5	B_6
7	C_1	Ad_3	Cd_4	A_5	C_6
8	D_1	Bd_3	Dd_4	B_5	D_6
9	Ad_2	Cd_3	A_4	C_5	Ad_7
10	Bd_2	Dd_3	B_4	D_5	Bd_7

The ADC Mode (Quad/Dual/Single) does not change the mapping arrangement. Data is always mapped in the above fashion. The mapped data is then 8b10b encoded and output on the 10 serial lanes. The 8b10b encoding provides a number of specific benefits:

- Standard encoding format, so IP is readily available in off-the-shelf FPGAs and ASIC building blocks
- Inherent DC balance allows AC coupling of lanes with small on-chip capacitors
- Inherent error checking

SYNC

The SYNC input is a differential LVDS logic input. To assert the SYNC input, a differential 1 is applied. To de-assert SYNC a differential 0 must be applied. SYNC+/− has an internal 100 ohm termination resistor and must not be AC coupled.

Serial Data Training Sequence

The SYNC input performs two key functions. The primary function, discussed here, is to enable the output of the serial data training pattern. This pattern is necessary to allow downstream deserializer circuitry to correctly synchronize to the output data stream. Synchronization involves clock recovery as well as data word and frame boundary location. Once this synchronization is established, the ADC can transition to outputting normal ADC data. The SYNC input signal, when asserted, causes the ADC to begin outputting the training sequence. The sequence is 8 characters long, twice the length of a data frame. The sequence is repeated indefinitely while the SYNC input is asserted and is output on all 10 lanes simultaneously. The sequence follows below:

Table 5. Serial Data Training Sequence

Word	0	1	2	3	4	5	6	7
Character	K27.7	D5.6	K28.5	D5.6	K28.5	D5.6	K28.5	D5.6

K27.7 is a start symbol to help identify the start of frame. K28.5 is a comma symbol for alignment. D5.6 is a data symbol with a lot of transitions to assist with bit alignment. When SYNC is de-asserted, an incomplete sync frame will complete before outputting the first data frame.

Multiple ADC Synchronization

The second function for the SYNC input, is to facilitate the precise synchronization of multiple ADCs in a system. The LM97600 input clock is internally process through a counter which creates a CLK/4 internal clocking system fed to the 4 internal ADCs. To ensure synchronization between multiple LM97600 devices in a system, it is important to align the CLK/4 counters in the multiple ADCs to the same divide by four state. The multiple ADC synchronization features facilitate that process.

When SYNC is asserted, it is captured by the internal CLK signal and the state of the internal CLK/4 counter at that instant is loaded in to bits-6:5 of the SYNC register. If the CLK and SYNC signals are fed into multiple LM97600 at the same time, the relative state of the internal CLK/4 counters can be captured.

Once the relative CLK/4 states are known, it is then desired to adjust the phase of some of the LM97600 devices until all CLK/4 counters are in the same state. Setting Configuration Register 4, bit-1 bumps or swallows one input clock, causing the CLK/4 counter to shift one later with respect to other devices. Each time this bit is changed from 0 to 1, the ADC will swallow one input clock, so it is a straightforward task to shift the CLK/4 counters until they are aligned.

One key challenge to making all of this work is ensuring that the SYNC inputs are captured by the input CLK in a repeatable fashion. There are two key elements to ensuring this. First, the SYNC input must be created so that it is synchronous to the input CLK, with a frequency relationship that is an integer multiple of CLK/4 (ie. CLK/8, CLK/12, CLK/16, etc.) and a repeatable and fixed phase offset. Once this constraint is achieved it is easier to capture it in a repeatable fashion. To further ease this task, the SYNC pulse is routed through a user adjustable delay set via bits 15:7 of the SYNC register. This eases the timing requirements with respect to the input CLK signal. As long as the SYNC pulse has a fixed timing relationship to the CLK rising edge, the internal delay can be used to maximize the setup and hold times between the internally delayed SYNC, and the internal CLK signal. These timing relationships are detailed in Figure 4 of the Timing Diagrams. The SYNC pulse must be of a minimum width and its delayed assertion edge must observe setup and hold times with respect to the internal CLK rising edge. Repetitive assertion of SYNC, and read back of the CLK/4 counter state will indicate if the reading is repeatable or not. If the reading is not repeatable, the setup and hold time between SYNC and CLK is not being reliably met. To find the proper delay setting, the Delay value can be adjusted from minimum to maximum while applying SYNC and reading the CLK/4 state. This will allow the range of delay settings where the CLK/4 reading is stable to be found. The Delay value at the center of the stable range should be loaded as the final Delay setting.

By default, asserting the SYNC input enables the output of the serial data training pattern. In some instances (as when performing the multi-ADC synchronization steps above) it is not desired to output the training pattern every time. The Disable Training Pattern bit in Serial Config 3 (Register 13h, Bit 14) allows the encoder to continue outputting normal ADC data when SYNC is applied.

The SYNC input should NOT be asserted while the calibration process is running (while CalRun is high). Doing so could cause a glitch in the digital circuitry, resulting in corruption and invalidation of the calibration.

TEST PATTERNS

ADC Test Patterns

To aid in system debug, the LM97600 has the capability of providing a test pattern at the output of each internal ADC completely independent of the input signal. The test pattern is selected by setting bit-3 (ADC Test Pattern Mode Select) in Configuration Register 1 (address 01h). The test pattern sequence can be controlled via the 16–Bit Test Pattern Register (0Dh). This pattern register sets the sequence of Low Code/High Code data values output by the internal ADCs. See the description for the 16–Bit Test Pattern (0Dh) settings for more details.

The ADC Test Pattern data is mapped into frames and 8b10b encoded in the same manner as normal ADC data.

Serializer Test Patterns

The serializer test patterns are output directly by the serializers, and are not passed through the 8b10b encoder. This allows direct control over specific types of test information. Two different types of serializer test patterns are provided, as selected at Serial Config 4 (Register 14h, Bits 12:10).

The LFSR Modes provide pseudo-random sequences which can be used to debug data channel performance issues, bit errors, etc. The LFSR patterns begin with two fixed symbols, followed by 62 pseudo-random symbols, for a total of 64 symbols. Different LFSR modes allow all lanes to start simultaneously, or offset by either 10 or 50 bits (1 or 5 symbols).

Table 6. LFSR Test Pattern

K28.5	K28.5/K28.7	LFSR Pseudo Random Data
64 symbols total length		

The Table Modes provide a user selected sequence of symbols that can be arbitrarily loaded to create any necessary fixed data pattern. This can be used to create static 1 or 0 values, or other patterns as needed. Two Table Modes exist. Table Mode 0 provides a user-set 4–symbol pattern that is output simultaneously on as many lanes as desired. Lanes can be disabled on a per-lane basis as needed.

Table 7. Table Test Mode 0

Test Lane (n) Setting	Lane (n) Data Output			
0	Logic 0	Logic 0	Logic 0	Logic 0
1	Test Table 0	Test Table 1	Test Table 2	Test Table 3

Table Mode 1 provides two user-set 2–symbol patterns. The user can choose on a per-lane basis which of the two patterns are output. The specific symbols are loaded via Test Table 0 to Test Table 3 in Registers 12h, 13h, 14h. The specific per-lane enable/disable or pattern choices are set via Serial Config 1, Test Lane (Register 11h, Bits 9:0).

Table 8. Table Test Mode 1

Test Lane (n) Setting	Lane (n) Data Output	
0	Test Table 0	Test Table 1
1	Test Table 2	Test Table 3

APPLICATION INFORMATION

THE REFERENCE VOLTAGE

The voltage reference for the LM97600 is derived from a 1.1 V bandgap reference, a buffered version of which is made available at pin 31, V_{BG}, for user convenience. This output has an output current capability of ±100 µA. This reference voltage should be buffered if more current is required.

The internal bandgap-derived reference voltage has a nominal value of 600 mV or 820 mV, as determined by the FSR pin and described in Configuration and Control

There is no provision for the use of an external reference voltage, but the full-scale input voltage can be adjusted through a Configuration Register in the Extended Control mode, as explained in DEVICE CONTROL.

Differential input signals up to the chosen full-scale level will be digitized to 7.6 bits. Signal excursions beyond the full-scale range will be clipped at the output. These large signal excursions will also activate the OR output for the time that the signal is out of range. See THE ANALOG INPUT.

One extra feature of the V_{BG} pin is that it can be used to raise the common mode voltage level of the LVDS outputs. The output offset voltage (V_{OS}) is typically 800mV when the V_{BG} pin is used as an output or left unconnected. To raise the LVDS offset voltage to a typical value of 1150mV the V_{BG} pin can be connected directly to the supply rails.

THE ANALOG INPUT

The analog input is a differential one to which the signal source may be a.c. coupled or d.c. coupled. The full-scale input range is selected with the FSR pin to be 600 mV_{P-P} or 820 mV_{P-P}, or can be adjusted to values between 560 mV_{P-P} and 840 mV_{P-P} in the Extended Control mode through the Serial Interface. For best performance, it is recommended that the full-scale range be kept between 595 mV_{P-P} and 805 mV_{P-P} in the Extended Control mode because the internal DAC which sets the full-scale range is not as linear at the ends of its range.

Table 9 gives the input to output relationship with the FSR pin high when the normal (non-extended) mode is used. With the FSR pin grounded, the millivolt values in Table 9 are reduced to 75% of the values indicated. In the Enhanced Control Mode, these values will be determined by the full scale range and offset settings in the Control Registers.

Table 9. DIFFERENTIAL INPUT TO OUTPUT RELATIONSHIP (Non-Extended Control Mode, FSR High)(1)

$V_{IN}+$	$V_{IN}−$	Output Code
V_{CM} − 205mV	V_{CM} + 205mV	0000 0000
V_{CM} − 102.5 mV	V_{CM} + 102.5 mV	0100 0000
V_{CM}	V_{CM}	0111 1111 / 1000 0000
V_{CM} + 102.5 mV	V_{CM} −102.5 mV	1100 0000
V_{CM} + 205mV	V_{CM} − 205mV	1111 1111

(1) The Full Scale Range registers for each of the four ADCs must be written consistent with the ADC Mode and Input Select settings

The buffered analog inputs simplify the task of driving these inputs and the RC pole that is generally used at sampling ADC inputs is not required. If it is desired to use an amplifier circuit before the ADC, use care in choosing an amplifier with adequate noise and distortion performance and adequate gain at the frequencies used for the application.

The Input impedance of V_{IN+} / V_{IN-}in the d.c. coupled mode (V_{CMO} pin not grounded) consists of a precision 100Ω resistor across the inputs and a capacitance from each of these inputs to ground. In the a.c. coupled mode, the input appears the same except there is also a resistor of 50KΩ between each analog input pin and the on-chip V_{CMO} potential.

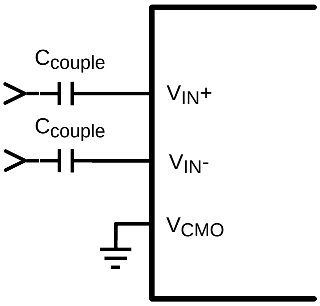


Figure 41. Differential Analog Input Connection

When the d.c. coupled mode is used, a precise common mode voltage must be provided at the differential inputs. This common mode voltage should track the V_{CMO} output pin. Note that the V_{CMO} output potential will change with temperature. The common mode output of the driving device should track this change.

Full-scale distortion performance falls off rapidly as the input common mode voltage deviates from V_{CMO}. This is a direct result of using a very low supply voltage to minimize power. Keep the input common voltage within 50 mV of V_{CMO}.

Performance is as good in the d.c. coupled mode as it is in the a.c. coupled mode, provided the input common mode voltage at both analog inputs remain within 50 mV of V_{CMO}.

Unused inputs should be connected to the V_{CMO} pin.

Handling Single-Ended Input Signals

There is no provision for the LM97600 to adequately process single-ended input signals. The best way to handle single-ended signals is to convert them to differential signals before presenting them to the ADC.

A.C. Coupled Input

The easiest way to accomplish single-ended a.c. input to differential a.c. signal is with an appropriate balun, as shown in Figure 42.

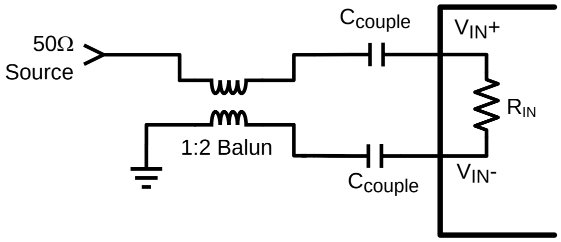


Figure 42. Single-Ended to Differential signal conversion with a balun

Figure 42 is a generic depiction of a single-ended to differential signal conversion using a balun. The circuitry specific to the balun will depend on the type of balun selected and the overall board layout. It is recommended that the system designer contact the manufacturer of the balun they have selected to aid in designing the best performing single-ended to differential conversion circuit using that particular balun.

When selecting a balun, it is important to understand the input architecture of the ADC. There are specific balun parameters of which the system designer should be mindful. They should match the impedance of their analog source to the LM97600's on-chip 100Ω differential input termination resistor. The range of this input termination resistor is described in the Converter Electrical Characteristics as the specification R_{IN}.

Also, as a result of the ADC architecture, the phase and amplitude balance are important. The lowest possible phase and amplitude imbalance is desired when selecting a balun. The phase imbalance should be no more than ±2.5° and the amplitude imbalance should be limited to less than 1dB at the desired input frequency range.

Finally, when selecting a balun, the VSWR (Voltage Standing Wave Ratio), bandwidth and insertion loss of the balun should also be considered. The VSWR aids in determining the overall transmission line termination capability of the balun when interfacing to the ADC input. The insertion loss should be considered so that the signal at the balun output is within the specified input range of the ADC as described in the Converter Electrical Characteristics as the specification V_{IN}.

D.C. Coupled Input

When d.c. coupling to the LM97600 analog inputs is required, single-ended to differential conversion may be easily accomplished with the LMH6555 or a similar differential amplifier. An example of this type of circuit is shown in Figure 43. In such applications, the LMH6555 performs the task of single-ended to differential conversion while delivering low distortion and noise, as well as output balance, that supports the operation of the LM97600. Connecting the LM97600 V_{CMO} pin to the V_{CM_REF} pin of the LMH6555, through an appropriate buffer, will ensure that the common mode input voltage is as needed for optimum performance of the LM97600. The LMV321 was chosen to buffer V_{CMO} for its low voltage operation and reasonable offset voltage.

Be sure that the current drawn from the V_{CMO} output does not exceed 100 μA.

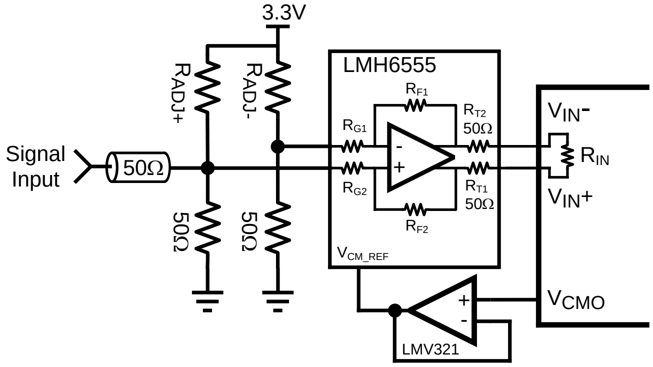


Figure 43. Example of Servoing the Analog Input with V_{CMO}

In Figure 43, $R_{ADJ-}$and R_{ADJ+} are used to adjust the differential offset that can be measured at the ADC inputs V_{IN+} / V_{IN-}. An unadjusted positive offset with reference to V_{IN-}greater than |15mV| should be reduced with a resistor in the R_{ADJ-}position. Likewise, an unadjusted negative offset with reference to V_{IN-}greater than |15mV| should be reduced with a resistor in the R_{ADJ+} position. Table 10 gives suggested $R_{ADJ-}$and R_{ADJ+} values for various unadjusted differential offsets to bring the V_{IN+} / V_{IN-}offset back to within |15mV|.

Table 10. D.C. Coupled Offset Adjustment

Unadjusted Offset Reading	Resistor Value
0mV to 10mV	no resistor needed
11mV to 30mV	20.0kΩ
31mV to 50mV	10.0kΩ
51mV to 70mV	6.81kΩ
71mV to 90mV	4.75kΩ
91mV to 110mV	3.92kΩ

Out Of Range (OR) Indication

When the conversion result is clipped the Out of Range output is asserted such that ORxx+ goes high and ORxx- goes low. This output is active as long as accurate data on either of the converters would be outside the range of 00h to FFh. During a calibration cycle, the OR output is invalid. Refer to OVERVIEW for more details.

Please note that the Out Of Range indication feature is disabled with the default register settings. The feature can be enabled by setting the Power Down Over-Range bit at Register 0x14h, Bit 14 = 0 (default = 1).

Full-Scale Input Range

As with all A/D Converters, the input range is determined by the value of the ADC's reference voltage. The reference voltage of the LM97600 is derived from an internal band-gap reference. The Full Scale Range of each converter can be set anywhere from 560mV to 840mV. Best SNR is obtained with higher Full Scale Ranges, but better distortion and SFDR are obtained with lower Full Scale Ranges. When operating in Dual or Single ADC mode, where multiple converters are operating in combination on a single input, it is important that the Full Scale Range (and Offset) settings of each converter are set to the same value.

The LMH6555 is suitable for any of the available Full Scale Range settings.

THE SAMPLE CLOCK INPUT

The LM97600 has a differential LVDS clock input, CLK+ / CLK-, which must be driven with an a.c. coupled, differential clock signal. The clock inputs are internally terminated and biased. The input clock signal must be capacitively coupled to the clock pins as indicated in Figure 44.

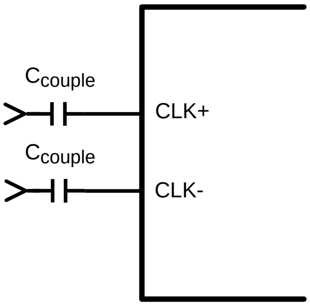


Figure 44. Differential Sample Clock Connection

The differential sample clock line pair should have a characteristic impedance of 100Ω and be terminated at the clock source in that (100Ω) characteristic impedance. The input clock line should be as short and as direct as possible. By default, the LM97600 clock input is internally terminated with a trimmed 100Ω resistor. If the Select Termination Value (Register 0x02h, Bit 14) is changed from 0 to 1 the termination value will be calibrated to 150 ohms.

Insufficient input clock levels will result in poor dynamic performance. Excessively high input clock levels could cause a change in the analog input offset voltage. To avoid these problems, keep the input clock level within the range specified in the Electrical Characteristics table.

The low and high times of the input clock signal can affect the performance of any A/D Converter. The LM97600 features a duty cycle clock correction circuit which can maintain performance over temperature. The ADC will meet its performance specification if the input clock high and low times are maintained as specified in Converter Electrical Characteristics.

High speed, high performance ADCs such as the LM97600 require a very stable input clock signal with minimum phase noise or jitter. ADC jitter requirements are defined by the ADC resolution (number of bits), maximum ADC input frequency and the input signal amplitude relative to the ADC input full scale range. The maximum jitter (the sum of the jitter from all sources) allowed to prevent a jitter-induced reduction in SNR is found to be

$$t_{J(MAX)} = (V_{INFSR}/V_{IN(P-P)}) \times (1/(2^{(N+1)} \times \pi \times f_{IN}))$$

where

- $t_{J(MAX)}$ is the rms total of all jitter sources in seconds, $V_{IN(P-P)}$ is the peak-to-peak analog input signal, V_{INFSR} is the full-scale range of the ADC, "N" is the ADC resolution in bits and f_{IN} is the maximum input frequency, in

Hertz, at the ADC analog input. (3)

Note that the maximum jitter described above is the Root Sum Square, (RSS), of the jitter from all sources, including that in the ADC input clock, that added by the system to the ADC input clock and input signals and that added by the ADC itself. Since the effective jitter added by the ADC is beyond user control, the best the user can do is to keep the sum of the externally added input clock jitter and the jitter added by the analog circuitry to the analog signal to a minimum.

Input clock amplitudes above those specified in the Electrical Characteristics table may result in increased input offset voltage. This would cause the converter to produce an output code other than the expected 128 when both input pins are at the same potential.

Aperture Delay

The sample clock aperture delay can be manually increased to accommodate subtle layout differences when synchronizing multiple ADCs. Adjustments are made via the Aperture Delay register (0Ch, Bits 15:0).

It should be noted that by just enabling the aperture delay capability (register 01h; Bit 0), degradation of dynamic performance is expected, specifically SFDR. It is intended that very small adjustments are used. Larger increases in phase adjustments will begin to affect SNR and ultimately ENOB. Therefore, the use of coarse phase adjustment should be minimized in favor of better system design.

CONTROL PINS

Three control pins (without the use of the serial interface) provide control over the operation of the LM97600 and facilitate its use. These control pins support Calibration, Synchronization of serial data and multiple ADCs, and a Power Down feature.

Calibration

The LM97600 calibration must be run to achieve specified performance. The calibration procedure is run upon power-up and can be run any time on command. The calibration procedure is exactly the same whether there is an input clock present upon power up or if the clock begins some time after application of power. The CalRun output indicator is high while a calibration is in progress. The calibration duration is nominally 1.16ms (with a 2.5 GHz input clock).

Power-On Calibration

Power-on calibration begins after a time delay following the application of power. This time delay is fixed at 8,388,608 input CLK cycles. With a 2.5 GHz input CLK, this gives an approximate delay of 3.36 ms.

The calibration process will be not be performed if the CAL pin is concurrently high with the application of power. In this case, the calibration cycle will not begin until the on-command calibration conditions are met. The LM97600 will function with the CAL pin held high at power up, but no calibration will be done and performance will be impaired. A manual calibration, however, may be performed after powering up with the CAL pin high. See the On-Command Calibration section.

On-Command Calibration

To initiate an on-command calibration, bring the CAL pin high for a minimum of 80 input clock cycles after it has been low for a minimum of 80 input clock cycles. Holding the CAL pin high upon power up will prevent execution of power-on calibration until the CAL pin is low for a minimum of 80 input clock cycles, then brought high for a minimum of another 80 input clock cycles. The calibration cycle will begin 80 input clock cycles after the CAL pin is thus brought high. The CalRun signal should be monitored to determine when the calibration cycle has completed.

The minimum 80 input clock cycle sequences are required to ensure that random noise does not cause a calibration to begin when it is not desired. As mentioned in the OVERVIEW section for best performance, a calibration should be performed 20 seconds or more after power up and repeated when the operating temperature changes significantly relative to the specific system design performance requirements. ENOB changes slightly with increasing junction temperature and can be easily corrected by performing an on-command calibration.

Power Down Feature

The Power Down pin (PD) allows the LM97600 to be entirely powered down. See Power Down Feature for details on the power down feature.

The digital data (+/-) output pins are put into a high impedance state when the PD pin is high. Upon return to normal operation, the pipeline will contain meaningless information and must be flushed.

If the PD input is brought high while a calibration is running, the device will not go into power down until the calibration sequence is complete. However, if power is applied and PD is concurrently high, the device will not begin the calibration sequence until the PD input goes low. If a manual calibration is requested while the device is powered down, the calibration will not begin at all. That is, the manual calibration input is completely ignored in the power down state.

THE DIGITAL OUTPUTS

The LM97600 output data is transmitted on 10 high speed serial data lanes. The output data from the four internal converters is formatted to the 10 lanes, 8b10b encoded, and serialized. Examining the resulting data rates, we have: 5 Gigasamples/sec x 8 bits = 40 Gigabits/second.

8b10b encoding adds a 10/8 overhead, resulting in a net data rate of 50 Gigabits/second.

The serial output data clock rate is therefore the same as the total aggregate ADC sampling rate (5 Gigasamples/sec gives 5 Gigabits/sec on each of the 10 lanes).

The ADC data is encoded in Offset Binary. Accordingly, a full-scale input level with $V_{IN}+$ positive with respect to $V_{IN}-$ will produce an output code of all ones, a full-scale input level with $V_{IN}-$ positive with respect to $V_{IN}+$ will produce an output code of all zeros and when $V_{IN}+$ and $V_{IN}-$ are equal, the output code will be 128.

POWER CONSIDERATIONS

A/D converters draw sufficient transient current to corrupt their own power supplies if not adequately bypassed. A 33 µF capacitor should be placed within an inch (2.5 cm) of the A/D converter power pins for each supply voltage. A 0.1 µF capacitor should be placed as close as possible to each supply pin, preferably within one-half centimeter. Leadless chip capacitors are preferred because they have low lead inductance.

As is the case with all high speed converters, the LM97600 should be assumed to have little power supply noise rejection. Any power supply used for digital circuitry in a system where a lot of digital power is being consumed should not be used to supply power to the LM97600. The ADC supplies should be the same supply used for other analog circuitry, if not a dedicated supply.

Supply Voltage

The LM97600 is specified to operate with nominal supply voltages of 1.2V (V_A, V_{TH}, V_C) and 2.5V (V_{25}, V_O). For detailed information regarding the operating voltage minimums and maximums, refer to the Operating Ratings section. It is very important to note that, while this device will function with slightly higher supply voltages, these higher supply voltages may reduce product lifetime.

During Power-up, the voltage on all 2.5V supplies should always be equal to, or greater than the voltage on the 1.2V supplies. Similarly, during Power-down, the voltage on the 1.2V supplies should always be equal to or lower than that of the 2.5V supplies. In general, it is simplest to supply all 2.5V buses from a single regulator, and all 1.2V buses from a single regulator. If the 1.2V buses are generated from separate regulators, they should all rise and fall together, or the user should ensure that the $V_C \geq V_A \geq V_{TH}$ during power up.

No pin should ever have a voltage on it that is in excess of the supply voltage or below ground by more than 150 mV, not even on a transient basis. This can be a problem upon application of power and power shut-down. Be sure that the supplies to circuits driving any of the input pins, analog or digital, do not come up any faster than does the voltage at the LM97600 power pins.

The Absolute Maximum Ratings should be strictly observed, even during power up and power down. A power supply that produces a voltage spike at turn-on and/or turn-off of power can destroy the LM97600. Please refer to the documentation provided with the LM97600RB reference board for specific guidance on voltage regulators and power sequencing.

Thermal Management

The LM97600 is capable of impressive speeds and performance at very low power levels for its speed. However, the power consumption is still high enough to require attention to thermal management. The Thermally Enhanced BGA package has 2 primary heat transfer paths. The copper heat slug mounted to the top of the substrate, and exposed in the center top of the package is the first path. The thermal resistance of this path is referred to as θ_{JC_1}. The other main heat path is via the center group of ground balls on the bottom of the package. The thermal resistance of this path is provided as θ_{JC_2}. In most applications, the center ground balls will form the primary thermal path.

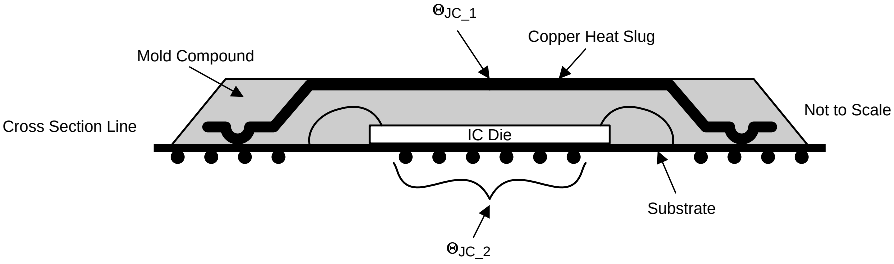


Figure 45. HSBGA Conceptual Drawing

For reliability reasons, the die temperature should be kept to a maximum of 130°C. That is, T_A (ambient temperature) plus ADC power consumption times the net θ_{JA} (junction to ambient thermal resistance) should not exceed 130°C. This is not a problem if the ambient temperature is kept to a maximum of +85°C as specified in the Operating Ratings section and the center ground balls on the bottom of the package are thermally connected to a large enough copper area of the PC board.

Please note that the following are general recommendations for mounting Thermally Enhanced BGA devices onto a PCB. This should be considered the starting point in PCB and assembly process development. It is recommended that the process be developed based upon past experience in package mounting.

The package of the LM97600 has a central group of ground balls that provide the primary heat removal path as well as excellent electrical grounding to the printed circuit board. The land pattern design for attachment to the PCB should be as recommended for the conventional BGA package (per AN-1126), but the center balls should be connected to internal ground planes to remove the maximum amount of heat from the package, as well as to ensure best product parametric performance.

To minimize junction temperature, it is recommended that a simple heat sink be built into the PCB. This is done by including a copper area of about 2 square inches (6.5 square cm) on the opposite side of the PCB. This copper area may be plated or solder coated to prevent corrosion, but should not have a conformal coating, which could provide some thermal insulation. Thermal vias should be used to connect these top and bottom copper areas. These thermal vias act as "heat pipes" to carry the thermal energy from the device side of the board to the opposite side of the board where it can be more effectively dissipated. The use of 9 to 16 thermal vias is recommended.

LAYOUT AND GROUNDING

Proper grounding and proper routing of all signals are essential to ensure accurate conversion. A single ground plane should be used, instead of splitting the ground plane into analog and digital areas.

Since digital switching transients are composed largely of high frequency components, the skin effect tells us that total ground plane copper weight will have little effect upon the logic-generated noise. Total surface area is more important than is total ground plane volume. Coupling between the typically noisy digital circuitry and the sensitive analog circuitry can lead to poor performance that may seem impossible to isolate and remedy. The solution is to keep the analog circuitry well separated from the digital circuitry.

High power digital components should not be located on or near any linear component or power supply trace or plane that services analog or mixed signal components as the resulting common return current path could cause fluctuation in the analog input “ground” return of the ADC, causing excessive noise in the conversion result.

Generally, we assume that analog and digital lines should cross each other at 90° to avoid getting digital noise into the analog path. In high frequency systems, however, avoid crossing analog and digital lines altogether. The input clock lines should be isolated from ALL other lines, analog AND digital. The generally accepted 90° crossing should be avoided as even a little coupling can cause problems at high frequencies. Best performance at high frequencies is obtained with a straight signal path.

The analog input should be isolated from noisy signal traces to avoid coupling of spurious signals into the input. This is especially important with the low level drive required of the LM97600. Any external component (e.g., a filter capacitor) connected between the converter's input and ground should be connected to a very clean point in the analog ground plane. All analog circuitry (input amplifiers, filters, etc.) should be separated from any digital components.

Layout of the high speed serial data lines is of particular importance. These traces should be routed as tightly coupled differential pairs, with minimal vias. Where vias must be used, care should be taken to implement control impedance (ie. 50 Ω) vias with adjacent ground vias for image current control.

DYNAMIC PERFORMANCE

The LM97600 is a.c. tested and its dynamic performance is ensured. To meet the published specifications and avoid jitter-induced noise, the clock source driving the CLK input must exhibit low rms jitter. The allowable jitter is a function of the input frequency and the input signal level, as described in THE SAMPLE CLOCK INPUT.

It is good practice to keep the ADC input clock line as short as possible, to keep it well away from any other signals and to treat it as a transmission line. Other signals can introduce jitter into the input clock signal. The clock signal can also introduce noise into the analog path if not isolated from that path.

USING THE SERIAL INTERFACE

The serial interface is accessed using the following four pins; Serial Clock (SCLK), Serial Data In (SDI), Serial Data Out (SDO) and Serial Interface Chip Select ($\overline{\text{SCS}}$). Twenty-one registers are accessible through this serial interface.

$\overline{\text{SCS}}$: This signal must be asserted low to access a register through the serial interface. Setup and hold times with respect to the SCLK must be observed.

SCLK: Serial data input is accepted at the rising edge of this signal. There is no minimum frequency requirement for SCLK.

SDI: Each register access requires a specific 24-bit pattern at this input. This pattern consists of a header, register address and register value. The data is shifted in MSB first. Setup and hold times with respect to the SCLK must be observed. See Figure 10.

Each Register access consists of 24 bits, as shown in Figure 10 of the Timing Diagrams. The following header patterns define the Write and Read operations.

Write = 010

Read = 110

The next 5 bits are the address of the register that is to be written to. During Write operations, the last 16 bits are the data written to the addressed register. During Read operations, the last 16 bits on SDI are ignored, and the SDO will output the data from the addressed register during this time.

Refer to REGISTER DEFINITIONS for detailed information regarding the registers.

NOTE

The Serial Interface should not be accessed when calibrating the ADC. Doing so will impair the performance of the device until it is re-calibrated correctly. Programming the serial registers will also reduce dynamic performance of the ADC for the duration of the register access time.

COMMON APPLICATION PITFALLS

Driving the inputs (analog or digital) beyond the power supply rails. For device reliability, no input should go more than 150 mV below the ground pins or 150 mV above the supply pins. Exceeding these limits on even a transient basis may not only cause faulty or erratic operation, but may impair device reliability. It is not uncommon for high speed digital circuits to exhibit undershoot that goes more than a volt below ground. Controlling the impedance of high speed lines and terminating these lines in their characteristic impedance should control overshoot.

Care should be taken not to overdrive the inputs of the LM97600. Such practice may lead to conversion inaccuracies and even to device damage.

Incorrect analog input common mode voltage in the d.c. coupled mode. As discussed in The Analog Inputs and THE ANALOG INPUT sections, the Input common mode voltage (V_{CMI}) must remain the specified range as referenced to V_{CMO}, which has a variability with temperature that must also be tracked. Distortion performance will be degraded if the input common mode voltage is outside the specified V_{CMI} range.

Using an inadequate amplifier to drive the analog input. Use care when choosing a high frequency amplifier to drive the LM97600 as many high speed amplifiers will have higher distortion than will the LM97600, resulting in overall system performance degradation.

Driving the clock input with an excessively high level signal. The ADC input clock level should not exceed the level described in the Operating Ratings table or the input offset could change.

Inadequate input clock levels. As described in THE SAMPLE CLOCK INPUT, insufficient input clock levels can result in poor performance. Excessive input clock levels could result in the introduction of an input offset.

Using a clock source with excessive jitter, using an excessively long input clock signal trace, or having other signals coupled to the input clock signal trace. This will cause the sampling interval to vary, causing excessive output noise and a reduction in SNR performance.

Failure to provide adequate heat removal. As described in Thermal Management, it is important to provide adequate heat removal to ensure device reliability. This can be done either with adequate air flow or the use of a simple heat sink built into the board. The backside pad should be grounded for best performance.

REGISTER DEFINITIONS

Table 11. Register Addresses

4-Bit Address						
Loading Sequence: A4 loaded after H0, A0 loaded last						
A4	A3	A2	A1	A0	Hex	Register Addressed
0	0	0	0	1	01h	Config 1
0	0	0	1	0	02h	Config 2
0	0	0	1	1	03h	Calibration Config
0	0	1	0	0	04h	Ch A Gain & Config
0	0	1	0	1	05h	Ch A Offset
0	0	1	1	0	06h	Ch B Gain & Config
0	0	1	1	1	07h	Ch B Offset
0	1	0	0	0	08h	Ch C Gain & Config
0	1	0	0	1	09h	Ch C Offset
0	1	0	1	0	0Ah	Ch D Gain & Config
0	1	0	1	1	0Bh	Ch D Offset
0	1	1	0	0	0Ch	Aperture Adjust
0	1	1	0	1	0Dh	ADC Test Pattern
0	1	1	1	0	0Eh	Cal Scan Register
0	1	1	1	1	0Fh	Reserved
1	0	0	0	0	10h	SYNC
1	0	0	0	1	11h	Serial Config 1

Table 11. Register Addresses (continued)

1	0	0	1	0	12h	Serial Config 2
1	0	0	1	1	13h	Serial Config 3
1	0	1	0	0	14h	Serial Config 4
1	1	1	1	0	1Eh	Revision

REGISTER DESCRIPTION

Twenty read/write registers provide several control and configuration options. Each register description below also shows the Power-On Reset (POR) state of each control bit.

Table 12. Configuration Register 1

Addr: 01**h** (0 0001**b**)									POR state: 0000**h**							
Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	Mode		Input Select								DC	Res	TPM	Res	BMP	STA
POR	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 15:14	ADC Mode: Selects the operating mode as follows: 00 = Single ADC (Samples at 2xFclk) 01 = Dual ADC (Samples at Fclk) 10 = Quad ADC (Samples at Fclk/2) 11 = Invalid setting. Do not use.
Bits 13:6	Input Select: Depending on the ADC Mode selection, determines which inputs are used as follows: Mode = Single ADC Selected input for all converters set by bits 7:6. Other bits unused. 00 = Input 1 01 = Input 2 10 = Input 3 11 = Input 4 Mode = Dual ADC Selected input for converters A and C set by bits 7:6 Selected input for converters B and D set by bits 9:8 Other bits unused. 00 = Input 1 01 = Input 2 10 = Input 3 11 = Input 4 Mode = Quad ADC Selected input for converter A set by bits 7:6 Selected input for converter B set by bits 9:8 Selected input for converter C set by bits 11:10 Selected input for converter D set by bits 13:12 Other bits unused. 00 = Input 1 01 = Input 2 10 = Input 3 11 = Input 4
Bit 5	DC Coupled Mode Select The default setting of 0b selects AC coupled mode for all inputs. Setting this bit to 1b selects DC coupled mode for all inputs.
Bit 4	Reserved Must be set to 0b.
Bit 3	ADC Test Pattern Mode Select Settings this bit to 1b replaces the normal ADC output with a configurable test pattern output as set by Register Dh.
Bit 2	Reserved Must be set to 0b.
Bit 1	Clock Bump Setting this bit to 1b “bumps” or “swallows” one input clock, to shift the order of the interleaved converters one later. This bit must be cleared before setting it again.
Bit 0	Set t_{AD} Adjust Setting this bit to 1b enables the built in t_{AD} adjustment circuitry. The amount of aperture delay added is selected via Register Ch.

Table 13. Configuration Register 2

Addr: 02**h** (0 0010**b**)								POR state: 0530**h**								
Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	CAL	STV	Res													
POR	0	0	0	0	0	1	0	1	0	0	1	1	0	0	0	0

Bit 15	Initiate CALibration When this bit is set to 1b, an on-command calibration is initiated. This bit is not reset automatically upon completion of the calibration. Therefore, the user must reset this bit to 0b and then set it to 1b again to execute another calibration. This bit is logically OR'd with the CAL pin, both bit and pin must be set to 0 before either is used to initiate another calibration
Bit 14	Select Termination Value When this bit is set to 0b (default) the analog and clock input terminations are set to 100 ohms. When this bit is set to 1b, the analog and clock input terminations are set to 150 ohms. In either case, the external Rtrim resistor value must be 3.6k ohms ±0.1%.
Bits 13:0	Reserved Must be set to 00 0101 0011 0000b.

Table 14. Calibration Configuration

Addr: 03**h** (0 0011**b**)								POR state: F580**h**								
Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	Res			RTE	Res						SSC	Res				
POR	1	1	1	1	0	1	0	1	1	0	0	0	0	0	0	0

Bits 15:13	Reserved Must be set to 111b.
Bit 12	Resistor Trim Enable When set to 1b, the input termination resistor values are calibrated normally. When set to 0b, the input termination resistor values are not calibrated.
Bits 11:6	Reserved Must be set to 00 0000b.
Bit 5	SPI Scan Control When set to 1b this bit enables the readout and writeback of the SPI calibration coefficient vector, accessed via Register 0Eh.
Bits 4:0	Reserved Must be set to 0 0000b.

Table 15. Channel A Full Scale Range Setting(1)

Addr: 04**h** (0 0100**b**)								POR state: 8000**h**								
Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	FM									Res						
POR	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

(1) Note: The Full Scale Range registers for each of the four ADCs must be written consistent with the ADC Mode and Input Select settings

Bits 15:7	Full Scale Range Magnitude Setting These 9 bits set the addressed ADC channel full scale range as follows: 0d = 560 mV pk-pk 255d = 700 mV pk-pk (default) 511d = 840 mV pk-pk
Bits 6:0	Reserved Must be set to 000 0000b.

Table 16. Channel A Offset Setting(1)

Addr: 05**h** (0 0101**b**)									POR state: 0000**h**							
Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	OM									OP	Res					
POR	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

(1) Note: The Offset registers for each of the four ADCs must be written consistent with the ADC Mode and Input Select settings

Bits 15:7	Offset Magnitude These 9 bits set the addressed ADC channel offset as follows: 0d = 0 mV 255d = 20 mV 511d = 45 mV
Bit 6	Offset Polarity When set to 0b, the addressed ADC channel offset is positive. (ADC output code increases). When set to 1b, the addressed ADC channel offset is negative. (ADC output code decreases).
Bits 5:0	Reserved Must be set to 000000b

Table 17. Channel B Full Scale Range Setting(1)

Addr: 06**h** (0 0110**b**)									POR state: 8000**h**							
Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	FM									Res						
POR	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

(1) Note: The Full Scale Range registers for each of the four ADCs must be written consistent with the ADC Mode and Input Select settings

Bits 15:7	Full Scale Range Magnitude Setting These 9 bits set the addressed ADC channel full scale range as follows: 0d = 560 mV pk-pk 255d = 700 mV pk-pk (default) 511d = 840 mV pk-pk
Bits 6:0	Reserved Must be set to 000 0000b.

Table 18. Channel B Offset Setting(1)

Addr: 07**h** (0 0111**b**)									POR state: 0000**h**							
Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	OM									OP	Res					
POR	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

(1) Note: The Offset registers for each of the four ADCs must be written consistent with the ADC Mode and Input Select settings

Bits 15:7	Offset Magnitude These 9 bits set the addressed ADC channel offset as follows: 0d = 0 mV 255d = 20 mV 511d = 45 mV
Bit 6	Offset Polarity When set to 0b, the addressed ADC channel offset is positive. (ADC output code increases). When set to 1b, the addressed ADC channel offset is negative. (ADC output code decreases).
Bits 5:0	Reserved Must be set to 000000b

Table 19. Channel C Full Scale Range Setting(1)

Addr: 08**h** (0 1000**b**)															POR state: 8000**h**
Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	FM									Res						
POR	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

(1) Note: The Full Scale Range registers for each of the four ADCs must be written consistent with the ADC Mode and Input Select settings

Bits 15:7	Full Scale Range Magnitude Setting These 9 bits set the addressed ADC channel full scale range as follows: 0d = 560 mV pk-pk 255d = 700 mV pk-pk (default) 511d = 840 mV pk-pk
Bits 6:0	Reserved Must be set to 000 0000b.

Table 20. Channel C Offset Setting(1)

Addr: 09**h** (0 1001**b**)															POR state: 0000**h**
Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	OM									OP	Res					
POR	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

(1) Note: The Offset registers for each of the four ADCs must be written consistent with the ADC Mode and Input Select settings

Bits 15:7	Offset Magnitude These 9 bits set the addressed ADC channel offset as follows: 0d = 0 mV 255d = 20 mV 511d = 45 mV
Bit 6	Offset Polarity When set to 0b, the addressed ADC channel offset is positive. (ADC output code increases). When set to 1b, the addressed ADC channel offset is negative. (ADC output code decreases).
Bits 5:0	Reserved Must be set to 000000b

Table 21. Channel D Full Scale Range Setting(1)

Addr: 0A**h** (0 1010**b**)															POR state: 8000**h**
Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	FM									Res						
POR	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

(1) Note: The Full Scale Range registers for each of the four ADCs must be written consistent with the ADC Mode and Input Select settings

Bits 15:7	Full Scale Range Magnitude Setting These 9 bits set the addressed ADC channel full scale range as follows: 0d = 560 mV pk-pk 255d = 700 mV pk-pk (default) 511d = 840 mV pk-pk
Bits 6:0	Reserved Must be set to 000 0000b

Table 22. Channel D Offset Setting[1]

Addr: 0B**h** (0 1011**b**)									POR state: 0000**h**							
Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	OM									OP	Res					
POR	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

(1) Note: The Offset registers for each of the four ADCs must be written consistent with the ADC Mode and Input Select settings

Bits 15:7	Offset Magnitude These 9 bits set the addressed ADC channel offset as follows: 0d = 0 mV 255d = 20 mV 511d = 45 mV
Bit 6	Offset Polarity When set to 0b, the addressed ADC channel offset is positive. (ADC output code increases). When set to 1b, the addressed ADC channel offset is negative. (ADC output code decreases).
Bits 5:0	Reserved Must be set to 000000b

Table 23. Aperture Delay

Addr: 0C**h** (0 1100**b**)									POR state: 0000**h**							
Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	CD						ID					FD				
POR	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 15:10	Coarse Delay These 6 bits select the amount of additional coarse aperture delay. Typical delay values are: 0d = 0 ps 1d = 20 ps 2d = 40 ps … 63d = 1260 ps
Bits 9:5	Intermediate Delay These 5 bits select the amount of additional intermediate aperture delay. Typical delay values are: 0d = 0 ps 1d = 5 ps 2d = 10 ps … 63d = 155 ps
Bits 4:0	Fine Delay These 5 bits select the amount of additional fine aperture delay. Typical delay values are: 0d = 0 ps 1d = 0.4 ps 2d = 0.8 ps … 63d = 12.4 ps

Table 24. 16–Bit Test Pattern

Addr: 0D**h** (0 1101**b**)																POR state: EA68**h**
Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	16–Bit ADC Test Pattern															
POR	1	1	1	0	1	0	1	0	0	1	1	0	1	0	0	0

Bits 15:0	16 Bit ADC Test Pattern These 16 bits select the test pattern sequence that will be generated by each bank of the ADC as follows: 0b = Low Code Selected 1b = High Code Selected Low and High Codes for each sub-converter are defined as shown in the table below. The pattern is output in sequence as determined by the Test Pattern Bits, starting from MSb and running to LSb. So the pattern in time for the default register settings is: High, High, High, Low, High, Low, High, Low, Low, etc.

ADC Bank	Low Code	High Code
Ad	01h	FEh
Bd	02h	FDh
Cd	03h	FCh
Dd	04h	FBh
A	05h	FAh
B	06h	F9h
C	07h	F8h
D	08h	F7h

Table 25. SPI Scan Read/Write

Addr: 0E**h** (0 1110**b**)																POR state: 0000**h**
Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	SPI Scan Read/Write															
POR	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 15:0	SPI Scan Read/Write Value These 16 bits provide the Read/Write access to the SPI Scan Calibration Vector.

Table 26. Reserved

Addr: 0F**h** (0 1111**b**)																POR state: 0001**h**
Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	Res															
POR	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits 15:0	Reserved Must be set to 0000 0000 0000 0001b.

Table 27. SYNC

Addr: 10**h** (1 0000**b**)									POR state: 8000**h**							
Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	SDE	SDV								D4S		Res				
POR	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit 15	Sync/Delay Enable When set to 1b, the serializer training pattern and multi-ADC Sync feature is enabled along with the Sync Delay controlled via Bits 14:7. When set to 0b, the Sync feature is disabled. (Power consumption reduced when off)
Bits14:7	Sync Delay Value These bits select the Sync Delay line setting as follows: Typical delay values are: 0d = 0 ps 1d = 6.3 ps 2d = 12.5 ps … 255d = 1600 ps
Bits 6:5	Divide by 4 State (Read Only) These bits allow readout of the Divide by 4 counter State as register during the Sync procedure. The value read back is indicated by these 2 bits as follows: 00 = Divider State 1 01 = Divider State 2 10 = Divider State 3 11 = Divider State 4
Bits 4:0	Reserved Must be set to 0 0000b.

Table 28. Serial Config 1

Addr: 11**h** (1 0001**b**)									POR state: 0000**h**							
Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	DeEm		V_{CM}		V_{OD}		TL[9:0]									
POR	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 15:14	DeEMphasis These bits set the line driver de-emphasis level as follows: 00 = No de-emphasis 01 = 10” FR4 (3.3 dB) 10 = 20” FR4 (5.6 dB) 11 = 30” FR4 (7.2 dB)
Bits13:12	Output Offset Select These bits set the line driver common mode voltage, as follows: 00 = 0.8V 01 = 1.0V 10 = 1.2V 11 = Maximum (Tracks V_O)
Bits 11:10	Output Voltage Select These bits set the line driver differential output voltage, as follows: 00 = 400 mVp-p 01 = 600 mVp-p 10 = 700 mVp-p 11 = 800 mVp-p
Bits 9:0	Test Lane These bits configure the functionality of the serial lane test features, in conjunction with the Test Mode settings in Serial Config 4, Bits 12:10, and the look up tables at Serial Config 2, 3 and 4.

Table 29. Serial Config 2

Addr: 12**h** (1 0010**b**)									POR state: 0000**h**							
Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	TT1[5:0]						TT0[9:0]									
POR	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits15:10	Test Table 1 (Lower 6 LSBits) These bits set the lower 6 least significant bits of Test Lookup Table 1.
Bits 9:0	Test Table 0 These bits set the 10 bits of Test Lookup Table 0.

Table 30. Serial Config 3

Addr: 13**h** (1 0011**b**)									POR state: 0000**h**							
Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	Res	DTP	TT2[9:0]										TT1[9:6]			
POR	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit 15	Reserved Must be set to 0b.
Bit 14	Disable Training Pattern When set to 1b, the SYNC pin will not put the encoder in training pattern mode. Useful to allow reading of divide-by-4 counter state using SYNC pin without putting the part into training mode.
Bits 13:4	Test Table 2 These bits set the 10 bits of Test Lookup Table 2.
Bits 3:0	Test Table 1 (Upper 4 MSBits) These bits set the 4 most significant bits of Test Lookup Table 1.

Table 31. Serial Config 4

Addr: 14**h** (1 0100**b**)									POR state: 4000**h**							
Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	FT	PDO	SPD				TT3[9:0]									
POR	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit 15	Force Test Forces 8B10B encoders to enter Test Table mode during chip calibration (forces TestMode[2] high). With Test Table values set to all zeros, this should create less noise during calibration.
Bit 14	Power Down Over-Range When set to 1b, powers down the two over-range output pairs.
Bit 13	Short Circuit Protection Disable When set to 1b, disables the serial output driver short circuit protection.
Bits 12:10	Test Mode Configures the serial output test modes as follows: 000 = Normal ADC mode 001 = LFSR — all lanes same 010 = LFSR — all lanes different, offset = 10 bits lane to lane 011 = LFSR — all lanes different, offset = 50 bits lane to lane For the LFSR offsets, lane_n(t) will have the same pattern as lane_n+1(t+offset) 100 = Table Mode 0 101 = Table Mode 1 In Table Mode 0, each 10 bit data value is output from MSb to LSb and all the inputs are output in the order Test Table 0 to Test Table 3. In addition, the TestLane[9:0] settings allow individual lanes to be disabled, by setting the appropriate TestLane[n] bit = 1. In Table Mode 1 the TestLane[9:0] values select one of two sequences to be output on each lane. If TestLane[n] = 0, the lane outputs data from Test Table 0 and Test Table 1. If TestLane[n]=1, the lane outputs data from Test Table 2 and Test Table 3. 110 = Unused 111 = Unused

Bits9:0	Test Table 3 These bits set the 10 bits of Test Lookup Table 3.

Table 32. Revision (Read Only)

Addr: 1E**h** (1 1110**b**)															POR state: F708**h**
Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name																
POR	1	1	1	1	0	1	1	1	0	0	0	0	1	0	0	0

Bits 15:0	Revision This register returns the revision information for this device.

REVISION HISTORY

Changes from Original (March 2013) to Revision A **Page**

- Changed layout of National Data Sheet to TI format 53

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM97600CIUT/NOPB	ACTIVE	BGA	NXA	292	40	Green (RoHS & no Sb/Br)	SNAG	Level-3-250C-168 HR	-40 to 85	LM97600CIUT	Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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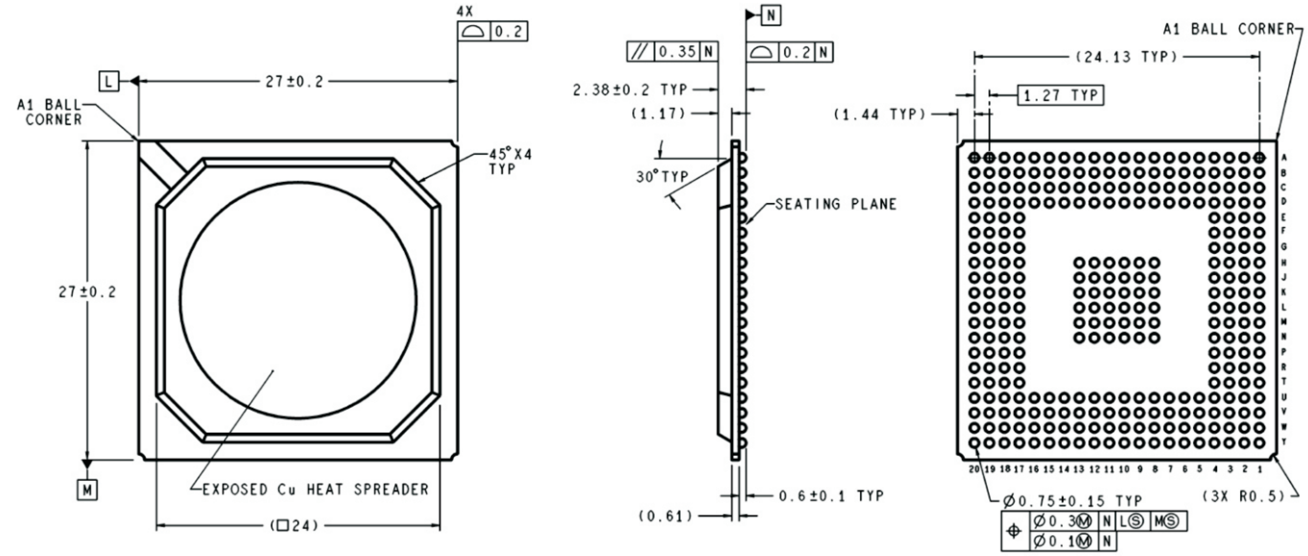

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