THE DATASHEET OF

LP5952TL-1.6/NOPB

LP5952 350-mA Dual-Rail Linear Regulator

1 Features

- Input Voltage Range: 0.7 V to 4.5 V
- 2.5 V ≤ V_{BATT} ≤ 5.5 V
- 0.5V ≤ V_{OUT} ≤ 2 V
- Ensured 350-mA Output Current
- For I_{LOAD} = 350 mA:
  - V_{BATT} ≥ $V_{OUT(NOM)}$ + 1.5 V or 2.5 V (Whichever is Higher)
- For I_{LOAD} = 150 mA:
  - V_{BATT} ≥ $V_{OUT(NOM)}$ + 1.3 V or 2.5 V (Whichever is Higher)
- Excellent Load Transient Response: ±15 mV Typical
- Excellent Line Transient Response: ±1 mV Typical
- 50-µA Typical Quiescent Current from V_{BATT}
- 10-µA Typical Quiescent Current from V_{IN}
- 0.1-µA Typical Quiescent Current in Shutdown
- Noise voltage = 100 μV_{RMS} Typical
- Operates from a Single Li-Ion Cell or 3-Cell NiMH/NiCd Battery
- Thermal-Overload and Short-Circuit Protection

2 Applications

- Mobile Phones
- Hand-Held Radios
- Personal Digital Assistants
- Palm-Top PCs
- Portable Instruments
- Battery-Powered Devices

3 Description

The LP5952 is a dual-supply-rail linear regulator optimized for powering ultralow-voltage circuits from a single Li-Ion cell or 3-cell NiMH/NiCd battery.

In the typical post-regulation application V_{BATT} is directly connected to the battery (range 2.5 V to 5.5 V), and V_{IN} is supplied by the output voltage of the DC-DC converter (range 0.7 V to 4.5 V).

The device offers superior dropout and transient features combined with very low quiescent currents. In shutdown mode (Enable (EN) pin pulled low) the device turns off and reduces battery consumption to 0.1 µA (typical). The LP5952 also features internal protection against overtemperature, overcurrent, and undervoltage conditions.

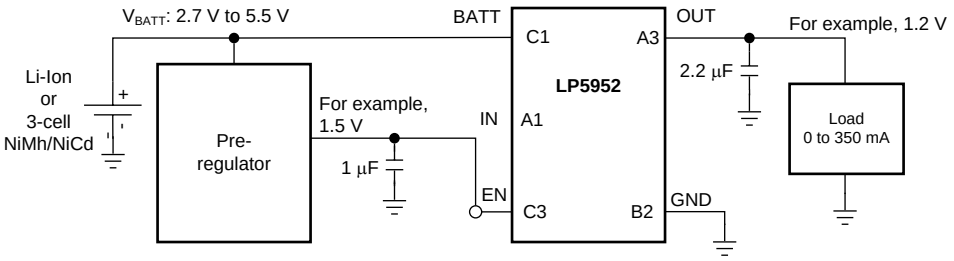
Depending upon application, only one or two tiny surface-mount external components are required; performance is specified for a –40°C to +125°C junction temperature range. The device is available in fixed output voltages from 0.5 V to 2 V. For availability, please contact your local Texas Instruments sales office.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LP5952	DSBGA (5)	1.326 mm × 0.96 mm
	USON (6)	2.00 mm × 2.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Circuit



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (May 2013) to Revision F — **Page**

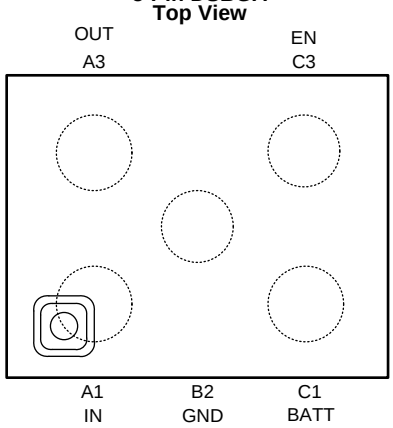
- Added *Device Information* and *Pin Configuration and Functions* sections, *ESD Ratings* and *Thermal Information* tables, *Feature Description*, *Device Functional Modes*, *Application and Implementation*, *Power Supply Recommendations*, *Layout*, *Device and Documentation Support*, and *Mechanical, Packaging, and Orderable Information* sections; update pin names to TI nomenclature ... 1
- Deleted lead temp spec - it is in POA ... 4
- Updated thermal information ... 5
- Changed values for thermal specifications in *Power Dissipation* section per updated thermal information ... 14

Changes from Revision D (April 2013) to Revision E — **Page**

- Changed layout of National Data Sheet to TI format ... 18

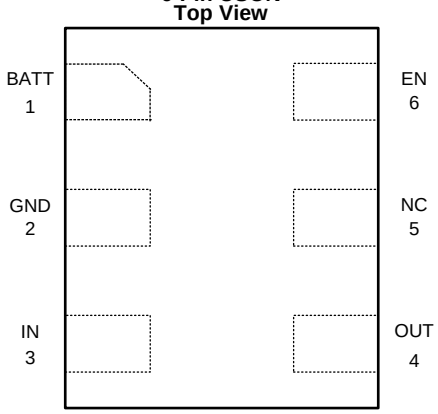
5 Pin Configuration and Functions

YZR Package
5-Pin DSBGA
Top View



NC - No internal connection

NKH Package
6-Pin USON
Top View



Pin Functions

PIN			TYPE	DESCRIPTION
NAME	USON	DSGBA		
BATT	1	C1	Input	Bias input voltage; input range: 2.5 V to 5.5 V
EN	6	C3	Input	Enable pin logic input: low = shutdown, high = active, normal operation. This pin should not be left floating. Tie to BATT if this function is not used.
GND	2	B2	Ground	Ground
IN	3	A1	Input	Power input voltage; input range: 0.7 V to 4.5 V, $V_{IN} \leq V_{BATT}$
NC	5	—	—	Do not make connections to this pin.
OUT	4	A3	Output	Regulated output voltage

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)(3)

	MIN	MAX	UNIT
IN, BATT pins: Voltage to GND, $V_{IN} \le V_{BATT}$	–0.2		V
BATT pin to IN pin		0.2	V
EN pin, voltage to GND	–0.2		V
Continuous power dissipation(4)	Internally limited		
Junction Temperature ($T_{J\text{-}MAX}$)		150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to the potential at the GND pin.
(3) If Military or Aerospace specified devices are required, contact Texas Instruments Sales Office or Distributors for availability and specifications.
(4) Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J = 165°C (typical) and disengages at T_J = 145°C (typical).

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Machine model	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Input voltage, V_{IN}	0.7	4.5	V
Input voltage, V_{BATT}	2.5	5.5	V
Input voltage, V_{EN}	0	V_{BATT}	V
Recommended load current	0	350	mA
Junction temperature, T_J	–40	125	°C
Ambient temperature, T_A(1)	–40	85	°C

(1) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature ($T_{A\text{-}MAX}$) is dependent on the maximum operating junction temperature ($T_{J\text{-}MAX\text{-}OP}$ = 125°C), the maximum power dissipation of the device in the application ($P_{D\text{-}MAX}$), and the junction-to ambient thermal resistance of the part/package in the application ($R_{\theta JA}$), as given by: $T_{A\text{-}MAX} = T_{J\text{-}MAX\text{-}OP} – (R_{\theta JA} \times P_{D\text{-}MAX})$.

6.4 Thermal Information

THERMAL METRIC[1]		LP5952		UNIT
		YZR (DSBGA)	NKH (USON)	
		5 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance[2]	181.0	181.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	0.9	93.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	110.3	116.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	7.4	8.0	°C/W
ψ_{JB}	Junction-to-board characterization parameter	110.3	116.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) Junction-to-ambient thermal resistance is highly application and board-layout dependent. In applications where high maximum power dissipation exists, special attention must be paid to thermal dissipation issues in board design.

6.5 Electrical Characteristics

Unless otherwise noted, typical values are for T_A = 25°C, and minimum and maximum limits apply over the full operating temperature range: –40°C ≤ T_J ≤ +125°C; specifications apply to the *Typical Application Circuit* with $V_{IN} = V_{OUT(NOM)} + 1$ V, $V_{BATT} = V_{OUT(NOM)} + 1.5$ V or 2.5 V (whichever is higher), I_{OUT} = 1 mA, C_{VIN} = 1 µF, C_{OUT} = 2.2 µF, $V_{EN} = V_{BATT}$.[1][2][3]

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$\Delta V_{OUT} / V_{OUT}$	Output voltage tolerance	$V_{IN} = V_{OUT(NOM)} + 0.3$ V, T_A = 25°C		–1.5		1.5	
		$V_{IN} = V_{OUT(NOM)} + 0.3$ V		2		2	
$\Delta V_{OUT} / \Delta V_{IN}$	Line regulation error	$V_{IN} = V_{OUT(NOM)} + 0.3$ V to 4.5 V, V_{BATT} = 4.5 V		1	0.3	1	mV/V
$\Delta V_{OUT} / \Delta V_{BATT}$		$V_{BATT} = V_{OUT(NOM)} + 1.5$ V (≥ 2.5 V) to 5.5 V		2.2	0.5	2.2	
$\Delta V_{OUT} / \Delta mA$	Load regulation error	I_{OUT} = 1 mA to 350 mA	DSBGA package	30	15	30	µV/mA
		I_{OUT} = 1 mA to 350 mA	USON package	60	43	60	µV/mA
I_{SC}	Output current (short circuit)	V_{OUT} = 0 V, $V_{EN} = V_{IN} = V_{BATT} = V_{OUT(NOM)} + 1.5$ V		350	500		mA
V_{DO_VBATT}[4]	Output voltage dropout V_{BATT}[5]	I_{OUT} = 350 mA, $V_{IN} = V_{OUT(NOM)} + 0.3$ V	DSBGA package		1.07	1.5	V
		I_{OUT} = 350 mA $V_{IN} = V_{OUT(NOM)} + 0.3$ V	USON package		1.08	1.5	V
		I_{OUT} = 150 mA $V_{IN} = V_{OUT(NOM)} + 0.3$ V	DSBGA package		0.96	1.3	V
		I_{OUT} = 150 mA $V_{IN} = V_{OUT(NOM)} + 0.3$ V	USON package		0.97	1.3	V
V_{DO_VIN}	Output voltage dropout V_{IN}	I_{OUT} = 350 mA $V_{BATT} = V_{OUT(NOM)} + 1.5$ V or 2.5 V	DSBGA package		88	200	mV
		I_{OUT} = 350 mA $V_{BATT} = V_{OUT(NOM)} + 1.5$ V or 2.5 V	USON package		128	250	mV
E_N	Output noise	10 Hz to 100 kHz			100		μV_{RMS}

(1) All voltages are with respect to the potential at the GND pin.
(2) Minimum and maximum limits are ensured by design, test, or statistical analysis. Typical numbers are not ensured, but do represent the most likely norm. Unless otherwise specified, conditions for typical specifications are: $V_{IN} = V_{OUT(NOM)} + 1$ V, $V_{BATT} = V_{OUT(NOM)} + 1.5$ V or 2.5 V, whichever is higher, T_A = 25°C.
(3) $V_{OUT(NOM)}$ is the stated output voltage option
(4) This specification does not apply if the battery voltage V_{BATT} needs to be decreased below the minimum operating limit of 2.5 V during this test.
(5) Dropout voltage is defined as the input to output voltage differential at which the output voltage falls to 100mV below the nominal output voltage.

Electrical Characteristics (continued)

Unless otherwise noted, typical values are for T_A = 25°C, and minimum and maximum limits apply over the full operating temperature range: –40°C ≤ T_J ≤ +125°C; specifications apply to the *Typical Application Circuit* with V_{IN} = $V_{OUT(NOM)}$ + 1 V, V_{BATT} = $V_{OUT(NOM)}$ + 1.5 V or 2.5 V (whichever is higher), I_{OUT} = 1 mA, C_{VIN} = 1 µF, C_{OUT} = 2.2 µF, V_{EN} = V_{BATT}.(1)(2)(3)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PSRR	Power Supply Rejection Ratio	Sine modulated V_{BATT}, f = 10 Hz		70		dB
		Sine modulated V_{BATT}, f = 100 Hz		65		
		Sine modulated V_{BATT}, f = 1 kHz		45		
PSRR	Power Supply Rejection Ratio	Sine modulated V_{IN}, f = 10 Hz		80		dB
		Sine modulated V_{IN}, f = 100 Hz		90		
		Sine modulated V_{IN}, f = 1 kHz		95		
		Sine modulated V_{IN}, f = 10 kHz		85		
		Sine modulated V_{IN}, f = 100 kHz		64		

6.6 Electrical Characteristics: Quiescent Currents

Unless otherwise noted, typical values are for T_A = 25°C, and minimum and maximum limits apply over the full operating temperature range: –40°C ≤ T_J ≤ +125°C.(1)(2)(3)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{Q_VBATT}	Current into V_{BATT}	I_{LOAD} = 0 mA to 350mA		50	100	µA
I_{Q_VIN}	Current into V_{IN}	I_{LOAD} = 0		11	28	µA

(1) All voltages are with respect to the potential at the GND pin.
(2) Minimum and maximum limits are ensured by design, test, or statistical analysis. Typical numbers are not ensured, but do represent the most likely norm. Unless otherwise specified, conditions for typical specifications are: V_{IN} = $V_{OUT(NOM)}$ + 1 V, V_{BATT} = $V_{OUT(NOM)}$ + 1.5 V or 2.5 V, whichever is higher, T_A = 25°C.
(3) $V_{OUT(NOM)}$ is the stated output voltage option

6.7 Electrical Characteristics: Shutdown Currents

Unless otherwise noted, typical values are for T_A = 25°C, and minimum and maximum limits apply over the full operating temperature range: –40°C ≤ T_J ≤ +125°C.(1)(2)(3)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{Q_VBATT}	Current into V_{BATT}	V_{EN} = 0 V		0.1	1	µA
I_{Q_VIN}	Current into V_{IN}	V_{EN} = 0 V		0.1	1	µA

(1) All voltages are with respect to the potential at the GND pin.
(2) Minimum and maximum limits are ensured by design, test, or statistical analysis. Typical numbers are not ensured, but do represent the most likely norm. Unless otherwise specified, conditions for typical specifications are: V_{IN} = $V_{OUT(NOM)}$ + 1 V, V_{BATT} = $V_{OUT(NOM)}$ + 1.5 V or 2.5 V, whichever is higher, T_A = 25°C.
(3) $V_{OUT(NOM)}$ is the stated output voltage option.

6.8 Electrical Characteristics: Enable Control

Unless otherwise noted, typical values are for T_A = 25°C, and minimum and maximum limits apply over the full operating temperature range: –40°C ≤ T_J ≤ +125°C.(1)(2)(3)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{EN}	Maximum input current at EN input			0.01	1	µA
V_{IL}	Low input threshold (shutdown)				0.4	V
V_{IH}	High input threshold (enable)		1			V

(1) All voltages are with respect to the potential at the GND pin.
(2) Minimum and maximum limits are ensured by design, test, or statistical analysis. Typical numbers are not ensured, but do represent the most likely norm. Unless otherwise specified, conditions for typical specifications are: V_{IN} = $V_{OUT(NOM)}$ + 1 V, V_{BATT} = $V_{OUT(NOM)}$ + 1.5 V or 2.5 V, whichever is higher, T_A = 25°C.
(3) $V_{OUT(NOM)}$ is the stated output voltage option.

6.9 Electrical Characteristics: Thermal Protection

Typical values are for T_A = 25°C.(1)(2)(3)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{SHDN}	Thermal-shutdown temperature			165		°C
ΔT_{SHDN}	Thermal-shutdown hysteresis			20		°C

(1) All voltages are with respect to the potential at the GND pin.
(2) Minimum and maximum limits are ensured by design, test, or statistical analysis. Typical numbers are not ensured, but do represent the most likely norm. Unless otherwise specified, conditions for typical specifications are: V_{IN} = $V_{OUT(NOM)}$ + 1 V, V_{BATT} = $V_{OUT(NOM)}$ + 1.5 V or 2.5 V, whichever is higher, T_A = 25°C.
(3) $V_{OUT(NOM)}$ is the stated output voltage option.

6.10 Electrical Characteristics: Transient Characteristics

Unless otherwise noted, typical values are for T_A = 25°C, and minimum and maximum limits apply over the full operating temperature range: –40°C ≤ T_J ≤ +125°C.(1)(2)(3)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
ΔV_{OUT}	Dynamic line transient response V_{IN}	V_{IN} = $V_{OUT(NOM)}$ + 0.3 V to $V_{OUT(NOM)}$ + 0.9 V; tr, tf = 10 µs			±1		mV
ΔV_{OUT}	Dynamic line transient response V_{BATT}	V_{BATT} = $V_{OUT(NOM)}$ + 1.5 V to $V_{OUT(NOM)}$ + 2.1 V; tr, tf = 10 µs			±15		mV
ΔV_{OUT}	Dynamic load transient response	Pulsed load 0 ...300 mA, di/dt = 300 mA/1 µs	DSBGA package		±15		mV
		Pulsed load 0 ...300mA, di/dt = 300 mA/1 µs	USON package		–35/+15		mV
$T_{STARTUP}$	Start-up time	EN to 0.95 × V_{OUT}			70	150	µs

(1) All voltages are with respect to the potential at the GND pin.
(2) Minimum and maximum limits are ensured by design, test, or statistical analysis. Typical numbers are not ensured, but do represent the most likely norm. Unless otherwise specified, conditions for typical specifications are: V_{IN} = $V_{OUT(NOM)}$ + 1 V, V_{BATT} = $V_{OUT(NOM)}$ + 1.5 V or 2.5 V, whichever is higher, T_A = 25°C.
(3) $V_{OUT(NOM)}$ is the stated output voltage option.

6.11 Input and Output Capacitors (Recommended)

All values are for T_A = 25°C.(1)(2)(3)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{OUT}	Output capacitance	Capacitance(4)	1.5	2.2	10	µF
		ESR	3		300	mΩ
C_{VIN}	Input capacitance at V_{IN}	Capacitance(4), not needed in typical post-regulation application (see Figure 18)	0.47	1		µF
		ESR	3		300	mΩ

(1) All voltages are with respect to the potential at the GND pin.
(2) Minimum and maximum limits are ensured by design, test, or statistical analysis. Typical numbers are not ensured, but do represent the most likely norm. Unless otherwise specified, conditions for typical specifications are: V_{IN} = $V_{OUT(NOM)}$ + 1 V, V_{BATT}= $V_{OUT(NOM)}$ + 1.5 V or 2.5 V, whichever is higher, T_A = 25°C.
(3) $V_{OUT(NOM)}$ is the stated output voltage option.
(4) The capacitor tolerance should be 30% or better over temperature. The full operating conditions for the application should be considered when selecting a suitable capacitor to ensure that the minimum value of capacitance is always met. Recommended capacitor type is X7R. However, dependent on application, X5R, Y5V, and Z5U can also be used. The shown minimum limit represents real minimum capacitance, including all tolerances and must be maintained over temperature and DC bias voltage (See *Detailed Design Procedure* in *Application and Implementation*.)

6.12 Typical Characteristics

Unless otherwise specified, T_A = 25°C, C_{IN} = 1-µF ceramic, C_{OUT} = 2.2-µF ceramic, V_{IN} = $V_{OUT(NOM)}$ + 1 V, V_{BATT} = $V_{OUT(NOM)}$ + 1.5 V, EN pin is tied to V_{BATT} (DSBGA package).

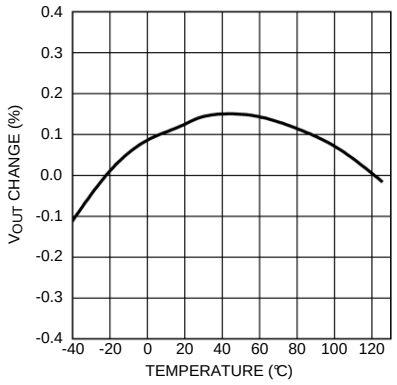
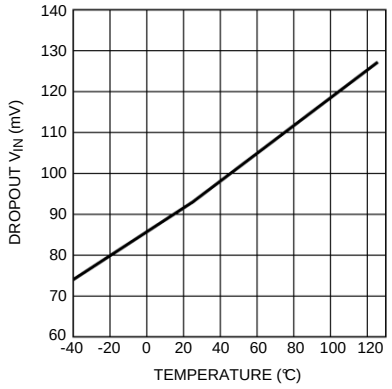
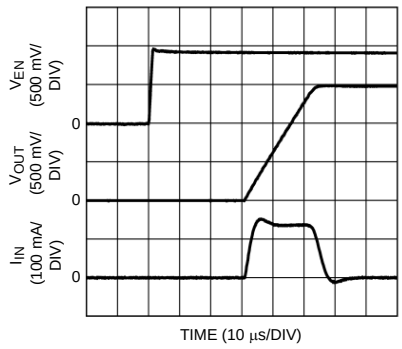


Figure 1. Output Voltage Change vs Temperature



I_{LOAD} = 350 mA

Figure 2. Dropout V_{IN} vs Temperature



1.5-V Option

Figure 3. Inrush Current V_{IN}

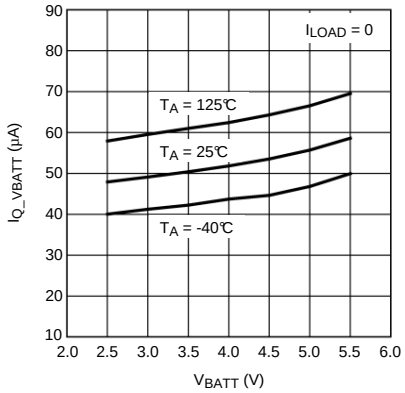


Figure 4. Quiescent Current I_{Q_VBATT} vs V_{BATT}

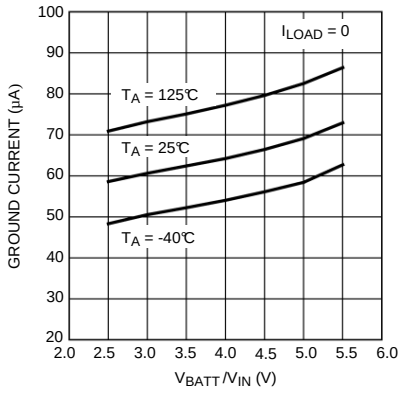


Figure 5. Ground Current vs V_{BATT} / V_{IN}

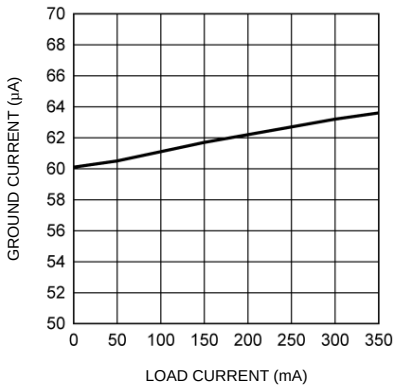
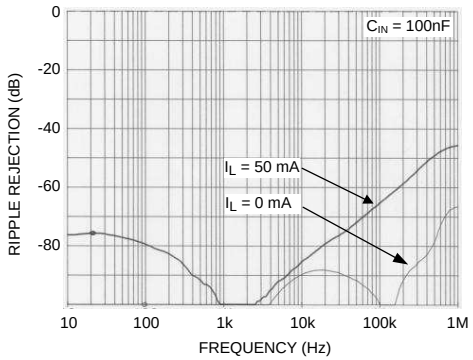


Figure 6. Ground Current vs Load Current

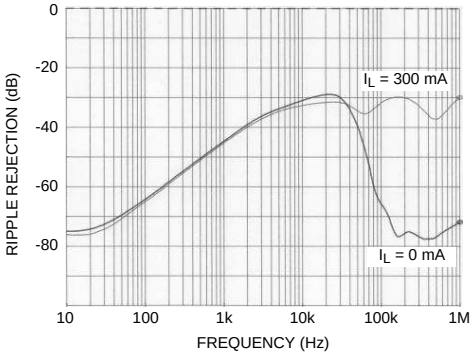
Typical Characteristics (continued)

Unless otherwise specified, T_A = 25°C, C_{IN} = 1-µF ceramic, C_{OUT} = 2.2-µF ceramic, V_{IN} = $V_{OUT(NOM)}$ + 1 V, V_{BATT} = $V_{OUT(NOM)}$ + 1.5 V, EN pin is tied to V_{BATT} (DSBGA package).



1.5-V Option

Figure 7. Power Supply Rejection Ratio V_{IN}



1.5-V Option

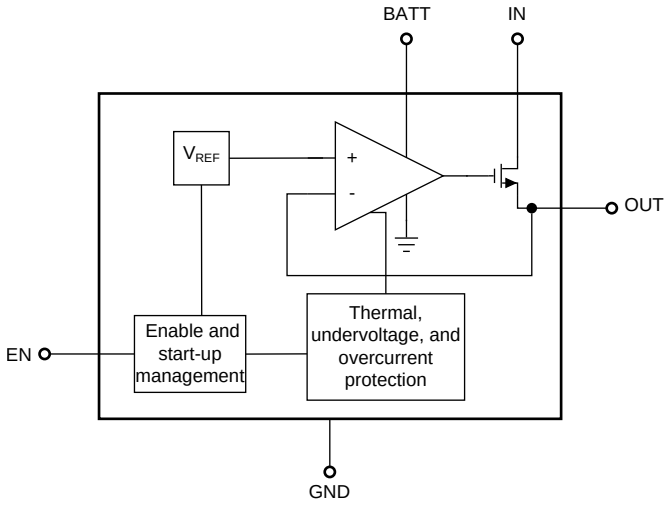
Figure 8. Power Supply Rejection Ratio V_{BATT}

7 Detailed Description

7.1 Overview

The LP5952 is a dual-supply-rail linear regulator optimized for powering ultralow-voltage circuits from a single Li-Ion cell or 3 cell NiMH/NiCd batteries. In a typical application, BATT is connected to the battery, and IN can be supplied by the output of front stage DC-DC Converter. IN does not exceed BATT at any time.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Dual-Rail Supply

The LP5952 requires two different supply voltages:

- V_{IN}, the power input voltage, is regulated to the fixed output voltage.
- V_{BATT}, the bias input voltage, supplies internal circuitry.

It is important that V_{IN} does not exceed V_{BATT} at any time. If the device is used in the typical post-regulation application as shown in Figure 18, the sequencing of the two power supplies is not an issue because V_{BATT} supplies both the DC-DC regulator and the LP5952 device. The output voltage of the DC-DC regulator takes some time to rise up and supply the input voltage of the device. In this application V_{IN} always ramps up more slowly than V_{BATT}.

If V_{IN} is shorted to V_{BATT}, the voltages at the two supply pins ramp up simultaneously causing no problems.

However, in applications with two independent supplies connected to the LP5952, special care must be taken to ensure that V_{IN} is always ≤ V_{BATT}.

7.3.2 No-Load Stability

The LP5952 remains stable and in regulation with no external load. This is an important consideration in some circuits, for example, CMOS RAM keep-alive applications.

7.3.3 Fast Turnon

Fast turnon is ensured by an optimized architecture allowing a fast ramp of the output voltage to reach the target voltage while the inrush current is controlled low at 120 mA typical (for a C_{OUT} of 2.2 µF).

Feature Description (continued)

7.3.4 Short-Circuit Protection

The LP5952 is short-circuit protected and, in the event of a peak overcurrent condition, the output current through the NFET pass device is limited.

If the overcurrent condition exists for a longer time, the average power dissipation increases depending on the input-to-output voltage difference until the thermal shutdown circuitry turns the NFET off. Refer to *Power Dissipation and Device Operation* for power dissipation calculations.

7.3.5 Thermal-Overload Protection

Thermal-overload protection limits the total power dissipation in the LP5952. When the junction temperature exceeds T_J = 165°C typical, the shutdown logic is triggered, and the NFET is turned off, allowing the device to cool down. After the junction temperature dropped by 20°C (temperature hysteresis) typical, the NFET is activated again. This results in a pulsed output voltage during continuous thermal-overload conditions.

The thermal-overload protection is designed to protect the LP5952 in the event of a fault condition. For normal continuous operation, do not exceed the absolute maximum junction temperature rating of T_J = 150°C (see *Absolute Maximum Ratings*).

7.3.6 Reverse Current Path

The internal NFET pass device in LP5952 has an inherent parasitic body diode. During normal operation, the input voltage is higher than the output voltage, and the parasitic diode is reverse biased. However, if the output is pulled above the input in an application, the current flows from the output to the input as the parasitic diode gets forward biased. The output can be pulled above the input as long as the current in the parasitic diode is limited to 50 mA. For currents above this limit an external Schottky diode must be connected from V_{OUT} to V_{IN} (cathode on V_{IN}, anode on V_{OUT}).

7.4 Device Functional Modes

7.4.1 Enable Operation

The LP5952 may be switched to an ON or OFF state by a logic input at the EN pin, V_{EN}. A logic high at this pin turns the device on. When the enable pin is low, the regulator output is off, and the device typically consumes 0.1 µA.

If the application does not require the enable switching feature, the EN pin must be tied to V_{BATT} to keep the regulator output permanently on.

To ensure proper operation, the signal source used to drive the EN input must be able to swing above and below the specified turnon and turnoff voltage thresholds shown in V_{IL} and V_{IH} in *Electrical Characteristics: Enable Control*.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LP5952 is designed to meet ultralow input-voltage application, by implementing V_{BATT} as power supply of this device. The VBATT is connected to the battery (range 2.5 V to 5.5 V), the V_{IN} range can be 0.7 V to 4.5 V. The device offers superior dropout and transient features combined with very low-quiescent currents. The LP5952 delivers this performance in standard packages DSBGA and USON with an operating junction temperature (T_J) of –40°C to +125°C.

8.2 Typical Application

8.2.1 Dual-Rail Linear Regulator

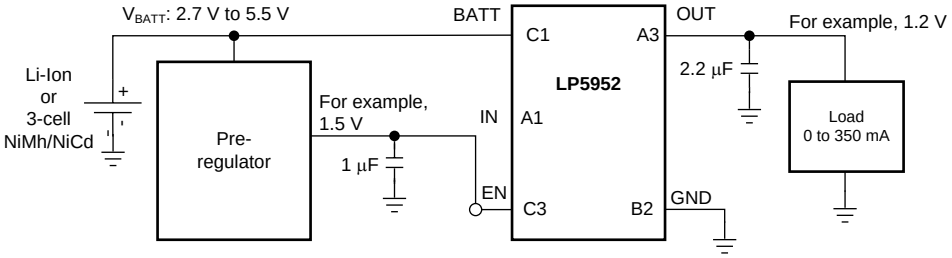


Figure 9. LP5952 Typical Application Circuit

8.2.1.1 Design Requirements

For typical dual-rail linear regulator parameters, see Table 1.

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	0.7 V to 4.5 V
V_{BATT} voltage range	2.7 V to 5.5 V
Output voltage	1.5 V
Output current	350 mA
Output capacitor range	2.2 µF
Input/output capacitor ESR range	3 mΩ to 300 mΩ

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 External Capacitors

As is common with most regulators, the LP5952 requires external capacitors to ensure stable operation. The LP5952 is specifically designed for portable applications requiring minimum board space and the smallest size components. These capacitors must be correctly selected for good performance.

8.2.1.2.2 Input Capacitor

If the LP5952 is used as a stand-alone device, an input capacitor at V_{IN} is required for stability. It is recommended that a 1-µF capacitor be connected between the LP5952 power voltage IN pin and ground. (This capacitance value may be increased without limit).

This capacitor must be located a distance of not more than 1 cm from the IN pin and returned to a clean analog ground. Any good quality ceramic, tantalum, or film capacitor may be used at the input.

A capacitor at V_{BATT} is not required if the distance to the supply does not exceed 5 cm.

If the device is used in the typical application as post regulator after a DC-DC regulator, no input capacitors are required — the capacitors of the DC-DC regulator (C_{IN} and C_{OUT}) are sufficient if both components are mounted close to each other and a proper GND plane is used. If the distance between the output capacitor of the DC-DC regulator and the IN pin of the LP5952 is larger than 5 cm, adding an input capacitor at V_{IN} is recommended.

NOTE

Important: Tantalum capacitors can suffer catastrophic failures due to surge current when connected to a low-impedance source of power (like a battery or a very large capacitor). If a tantalum capacitor is used at the input, it must be ensured by the manufacturer to have a surge current rating sufficient for the application.

The equivalent series resistance (ESR) of the input capacitor should be in the range of 3 mΩ to 300 mΩ. The tolerance and temperature coefficient must be considered when selecting the capacitor to ensure the capacitance remains ≥ 470 nF over the entire operating temperature range.

8.2.1.2.3 Output Capacitor

The LP5952 is designed specifically to work with very small ceramic output capacitors. A ceramic capacitor (dielectric types X7R, Z5U, or Y5V) in the 2.2-µF range (up to 10 µF) and with an ESR between 3 mΩ to 300 mΩ is suitable as C_{OUT} in the LP5952 application circuit.

This capacitor must be located a distance of not more than 1 cm from the OUT pin and returned to a clean analog ground.

It is also possible to use tantalum or film capacitors at the device output, V_{OUT}, but these are not as attractive for reasons of size and cost (see *Capacitor Characteristics*).

8.2.1.2.4 Capacitor Characteristics

The LP5952 is designed to work with ceramic capacitors on the output to take advantage of the benefits they offer. For capacitance values in the 1-µF to 4.7-µF range, ceramic capacitors are the smallest, least expensive and have the lowest ESR values, thus making them best for eliminating high-frequency noise. The ESR of a typical 1-µF ceramic capacitor is in the range of 3 mΩ to 40 mΩ, which easily meets the ESR requirement for stability for the LP5952.

For both input and output capacitors, careful interpretation of the capacitor specification is required to ensure correct device operation. The capacitor value can change greatly, depending on the operating conditions and capacitor type.

In particular, the output capacitor selection must take account of all the capacitor parameters, to ensure that the specification is met within the application. The capacitance can vary with DC bias conditions as well as temperature and frequency of operation. Capacitor values show some decrease over time due to aging. The capacitor parameters are also dependant on the particular case size, with smaller sizes giving poorer performance figures in general. Figure 10 shows a typical graph comparing different capacitor case sizes in a capacitance vs. DC Bias plot. As shown Figure 10, increasing the DC-bias condition can result in the capacitance value falling below the minimum value given in *Input and Output Capacitors (Recommended)* (0.47 µF or 1.5 µF in this case). The graph shows the capacitance out of specification for the 0402 case size capacitor at higher bias voltages. It is therefore recommended that the capacitor-manufacturer specifications for the nominal value capacitor are consulted for all conditions, as some capacitor sizes (such as 0402) may not be suitable in the actual application.

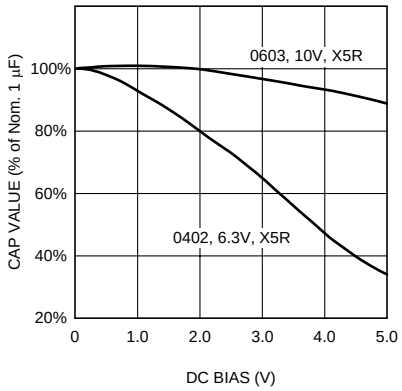


Figure 10. Typical Variation In Capacitance vs DC Bias

Capacitance of the ceramic capacitor can vary with temperature. The capacitor type X7R, which operates over a temperature range of –55°C to +125°C, only varies the capacitance to within ±15%. The capacitor type X5R has a similar tolerance over a reduced temperature range of –55°C to +85°C. Many large value ceramic capacitors, larger than 1 µF, are manufactured with Z5U or Y5V temperature characteristics. Their capacitance can drop by more than 50% as the temperature varies from 25°C to 85°C. Therefore, X7R is recommended over Z5U and Y5V in applications where the ambient temperature changes significantly above or below 25°C.

Tantalum capacitors are less desirable than ceramic for use as output capacitors because they are more expensive when comparing equivalent capacitance and voltage ratings in the 1-µF to 4.7-µF range.

Another important consideration is that tantalum capacitors have higher ESR values than equivalent size ceramics. This means that while it may be possible to find a tantalum capacitor with an ESR value within the stable range, it would have to be larger in capacitance (which means bigger and more costly) than a ceramic capacitor with the same ESR value. The ESR of a typical tantalum increases about 2:1 as the temperature goes from 25°C down to –40°C, so some guard band must be allowed.

8.2.1.2.5 Power Dissipation and Device Operation

The permissible power dissipation for any package is a measure of the capability of the device to pass heat from the power source, the junctions of the device, to the ultimate heat sink, the ambient environment. Thus the power dissipation is dependent on the ambient temperature and the thermal resistance across the various interfaces between the die and ambient air.

As stated in the *Recommended Operating Conditions*, the allowable power dissipation for the device in a given package can be calculated using Equation 1:

$$P_D = (T_{J(MAX)} – T_A) / R_{\theta JA} \quad (1)$$

With an $R_{R\theta JA}$ = 181°C/W, the device in the 5-pin DSBGA package returns a value of 552 mW with a maximum junction temperature of 125°C at T_A of 25°C or 221 mW at T_A of 85°C.

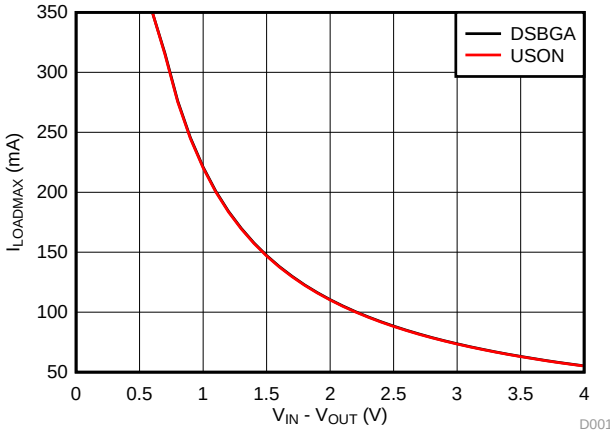
The actual power dissipation across the device can be estimated by Equation 2:

$$P_D = (V_{IN} – V_{OUT}) \times I_{OUT} \quad (2)$$

This establishes the relationship between the power dissipation allowed due to thermal consideration, the voltage drop across the device, and the continuous current capability of the device. Equation 1 and Equation 2 must be used to determine the optimum operating conditions for the device in any application. As an example, to keep full load current capability of 350 mA for a 1.5-V output voltage option at a high ambient temperature of 85°C, V_{IN} has to be kept ≤ 2.1 V (for DSBGA package):

$$V_{IN} \leq P_D / I_{OUT} + V_{OUT} = 221 \text{ mW} / 350 \text{ mA} + 1.5 \text{ V} = 2.1 \text{ V} \quad (3)$$

Figure 11 shows the output current derating due to these considerations:



T_A = 85°C V_{OUT} = 1.5 V

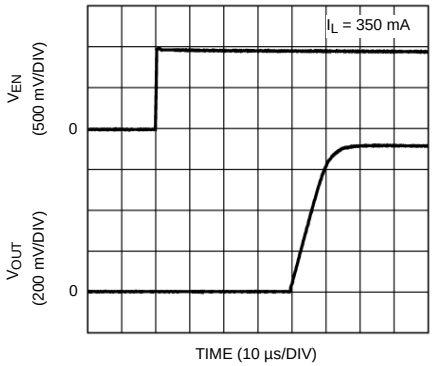
$R_{\theta JA(DSBGA)}$ = 181°C/W $R_{\theta JA(USON)}$ = 181.6°C/W

Figure 11. Maximum Load Current vs $V_{IN} - V_{OUT}$

The typical contribution of the bias input voltage supply V_{BATT} to the power dissipation can be neglected (Equation 4):

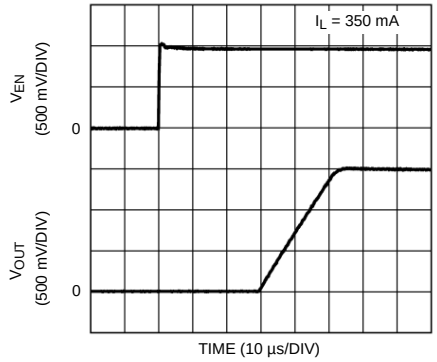
$$P_{D\_VBATT} = V_{BATT} \times I_{QVBATT} = 5.5 \text{ V} \times 50 \text{ µA} = 0.275 \text{ mW typical} \quad (4)$$

8.2.1.3 Application Curves



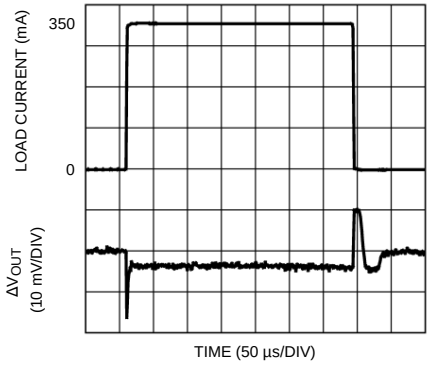
0.7-V Option

Figure 12. Enable Start-Up Time



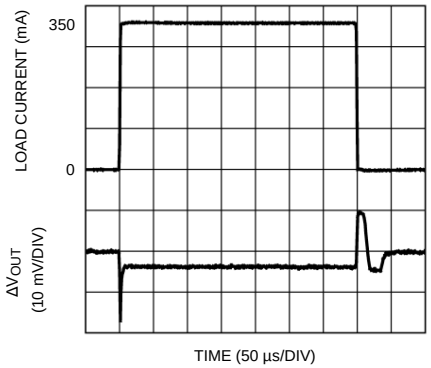
1.5-V Option

Figure 13. Enable Start-Up Time



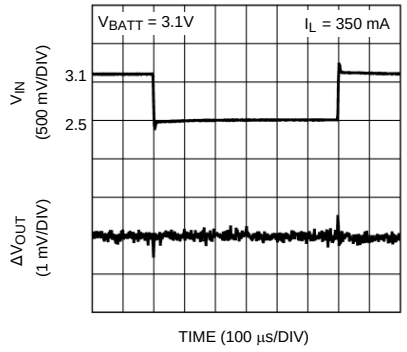
0.7-V Option

Figure 14. Load Transient Response



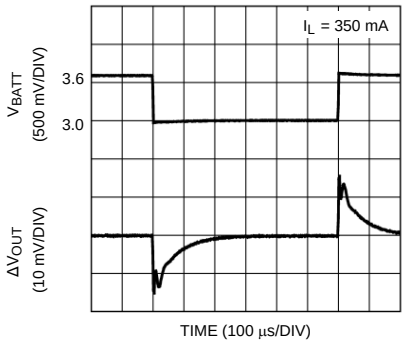
1.5-V Option

Figure 15. Load Transient Response



1.5-V Option

Figure 16. Line Transient Response V_{IN}



1.5-V Option

Figure 17. Line Transient Response V_{BATT}

8.2.2 Additional Application Circuit

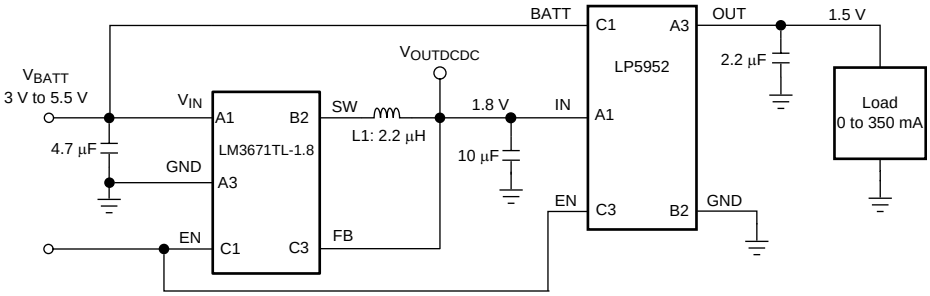


Figure 18. Typical Application Circuit With DC-DC Converter as Pre-Regulator for V_{IN}

9 Power Supply Recommendations

This device is designed to operate from an input supply voltage range of 0.7 V to 4.5 V. The input supply should be well regulated and free of spurious noise. A minimum capacitor value of 1-µF is required to be within 1 cm of the IN pin. The V_{BATT} range is 2.5 V to 5.5 V and, in the typical application, V_{BATT} is connected to batteries. In any application, V_{IN} does not exceed V_{BATT}.

10 Layout

10.1 Layout Guidelines

For best overall performance, place all circuit components on the same side of the circuit board and as near to the respective LDO pin connections as practical. Place ground return connections as close as possible to the input and output capacitor and to the LDO ground pin, connected by a wide, copper surface. The use of vias and long traces to create LDO circuit connection is strongly discouraged and negatively affect system performance.

10.2 Layout Examples

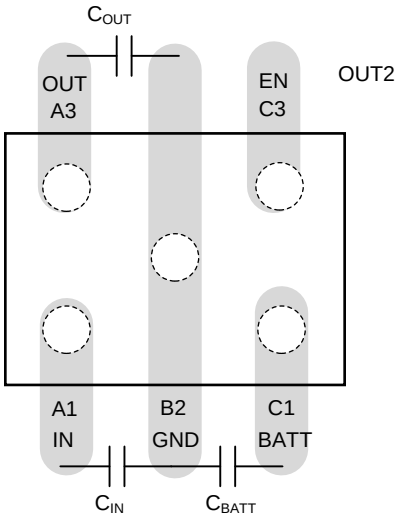


Figure 19. LP5952 DSBGA Layout Example

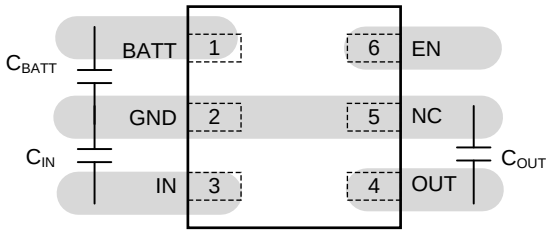


Figure 20. LP5952 WSON Layout Example

11 Device and Documentation Support

11.1 Device Support

For availability of evaluation boards, refer to the product folder of LP5952 at www.ti.com.

11.2 Documentation Support

11.2.1 Related Documentation

For information regarding evaluation boards, please refer to AN-1531 *LP5952 Evaluation Board* (SNVA188).

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP5952LC-1.2/NOPB	ACTIVE	USON	NKH	6	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	L28	Samples
LP5952LC-1.3/NOPB	ACTIVE	USON	NKH	6	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	L43	Samples
LP5952LC-1.5/NOPB	ACTIVE	USON	NKH	6	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	L25	Samples
LP5952LC-1.8/NOPB	ACTIVE	USON	NKH	6	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	L29	Samples
LP5952TL-1.0/NOPB	ACTIVE	DSBGA	YZR	5	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	L	Samples
LP5952TL-1.2/NOPB	ACTIVE	DSBGA	YZR	5	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	7	Samples
LP5952TL-1.3/NOPB	ACTIVE	DSBGA	YZR	5	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	U	Samples
LP5952TL-1.5/NOPB	ACTIVE	DSBGA	YZR	5	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	T	Samples
LP5952TL-1.6/NOPB	ACTIVE	DSBGA	YZR	5	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	B	Samples
LP5952TL-1.8/NOPB	ACTIVE	DSBGA	YZR	5	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	8	Samples
LP5952TLX-1.0/NOPB	ACTIVE	DSBGA	YZR	5	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	L	Samples
LP5952TLX-1.2/NOPB	ACTIVE	DSBGA	YZR	5	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	7	Samples
LP5952TLX-1.5/NOPB	ACTIVE	DSBGA	YZR	5	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	T	Samples
LP5952TLX-1.8/NOPB	ACTIVE	DSBGA	YZR	5	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	8	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

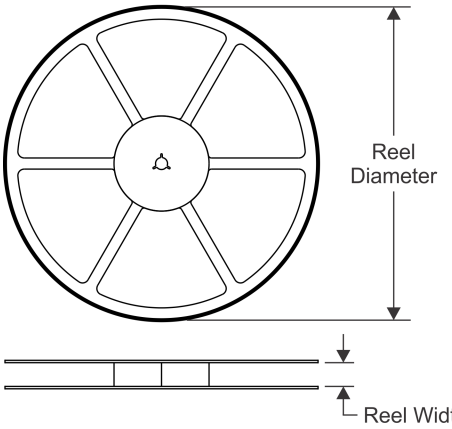
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

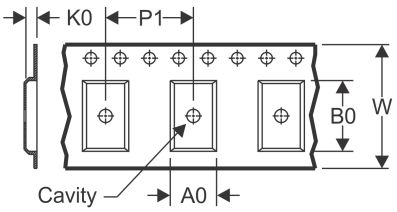
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

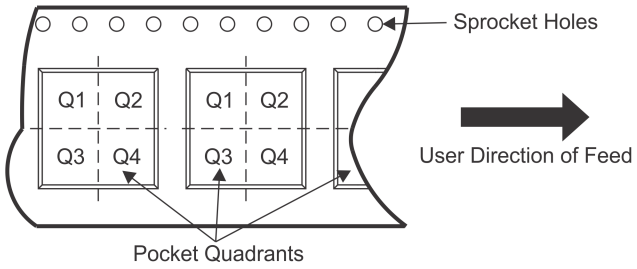


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

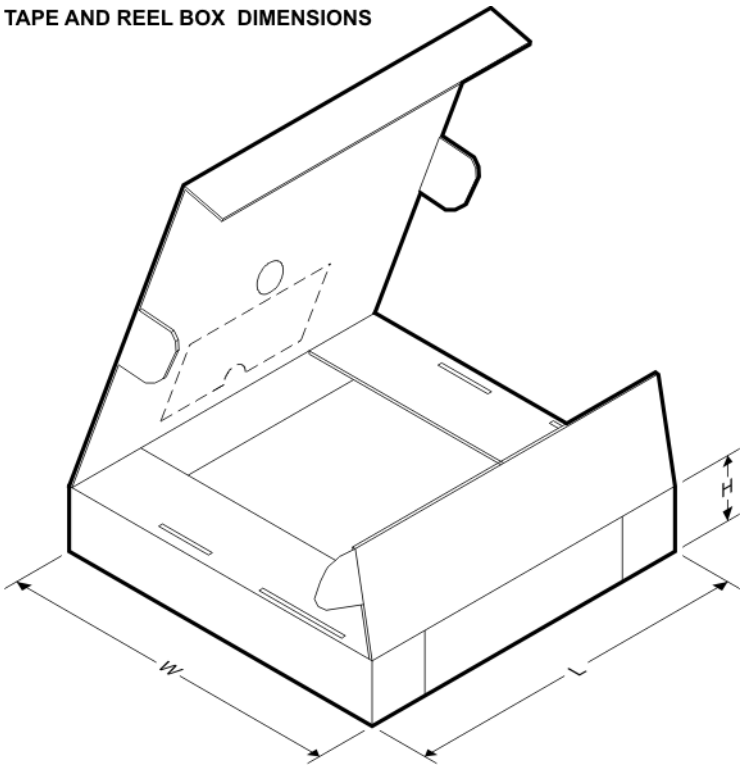
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP5952LC-1.2/NOPB	USON	NKH	6	1000	178.0	12.4	2.2	2.2	1.0	8.0	12.0	Q1
LP5952LC-1.3/NOPB	USON	NKH	6	1000	178.0	12.4	2.2	2.2	1.0	8.0	12.0	Q1
LP5952LC-1.5/NOPB	USON	NKH	6	1000	178.0	12.4	2.2	2.2	1.0	8.0	12.0	Q1
LP5952LC-1.8/NOPB	USON	NKH	6	1000	178.0	12.4	2.2	2.2	1.0	8.0	12.0	Q1
LP5952TL-1.0/NOPB	DSBGA	YZR	5	250	178.0	8.4	1.04	1.4	0.76	4.0	8.0	Q1
LP5952TL-1.2/NOPB	DSBGA	YZR	5	250	178.0	8.4	1.04	1.4	0.76	4.0	8.0	Q1
LP5952TL-1.3/NOPB	DSBGA	YZR	5	250	178.0	8.4	1.04	1.4	0.76	4.0	8.0	Q1
LP5952TL-1.5/NOPB	DSBGA	YZR	5	250	178.0	8.4	1.04	1.4	0.76	4.0	8.0	Q1
LP5952TL-1.6/NOPB	DSBGA	YZR	5	250	178.0	8.4	1.04	1.4	0.76	4.0	8.0	Q1
LP5952TL-1.8/NOPB	DSBGA	YZR	5	250	178.0	8.4	1.04	1.4	0.76	4.0	8.0	Q1
LP5952TLX-1.0/NOPB	DSBGA	YZR	5	3000	178.0	8.4	1.04	1.4	0.76	4.0	8.0	Q1
LP5952TLX-1.2/NOPB	DSBGA	YZR	5	3000	178.0	8.4	1.04	1.4	0.76	4.0	8.0	Q1
LP5952TLX-1.5/NOPB	DSBGA	YZR	5	3000	178.0	8.4	1.04	1.4	0.76	4.0	8.0	Q1
LP5952TLX-1.8/NOPB	DSBGA	YZR	5	3000	178.0	8.4	1.04	1.4	0.76	4.0	8.0	Q1

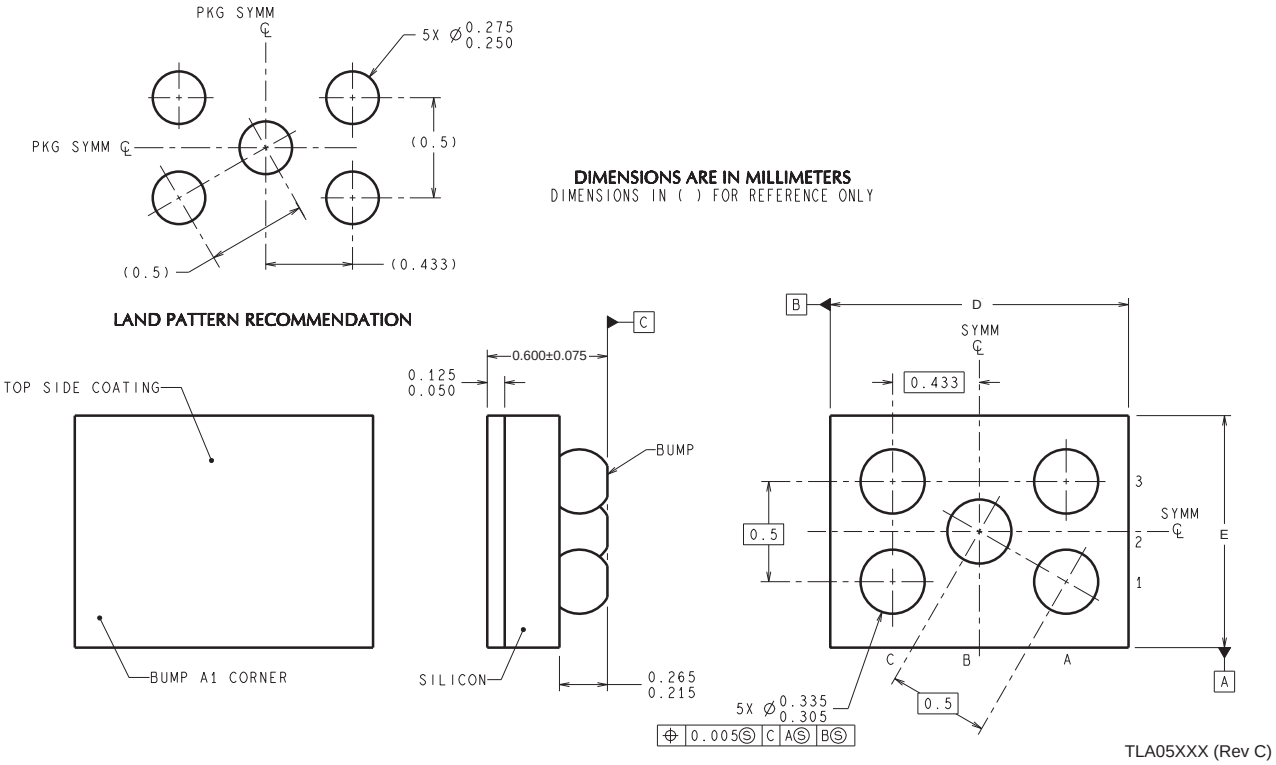
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP5952LC-1.2/NOPB	USON	NKH	6	1000	210.0	185.0	35.0
LP5952LC-1.3/NOPB	USON	NKH	6	1000	210.0	185.0	35.0
LP5952LC-1.5/NOPB	USON	NKH	6	1000	210.0	185.0	35.0
LP5952LC-1.8/NOPB	USON	NKH	6	1000	210.0	185.0	35.0
LP5952TL-1.0/NOPB	DSBGA	YZR	5	250	210.0	185.0	35.0
LP5952TL-1.2/NOPB	DSBGA	YZR	5	250	210.0	185.0	35.0
LP5952TL-1.3/NOPB	DSBGA	YZR	5	250	210.0	185.0	35.0
LP5952TL-1.5/NOPB	DSBGA	YZR	5	250	210.0	185.0	35.0
LP5952TL-1.6/NOPB	DSBGA	YZR	5	250	210.0	185.0	35.0
LP5952TL-1.8/NOPB	DSBGA	YZR	5	250	210.0	185.0	35.0
LP5952TLX-1.0/NOPB	DSBGA	YZR	5	3000	210.0	185.0	35.0
LP5952TLX-1.2/NOPB	DSBGA	YZR	5	3000	210.0	185.0	35.0
LP5952TLX-1.5/NOPB	DSBGA	YZR	5	3000	210.0	185.0	35.0
LP5952TLX-1.8/NOPB	DSBGA	YZR	5	3000	210.0	185.0	35.0

YZR0005



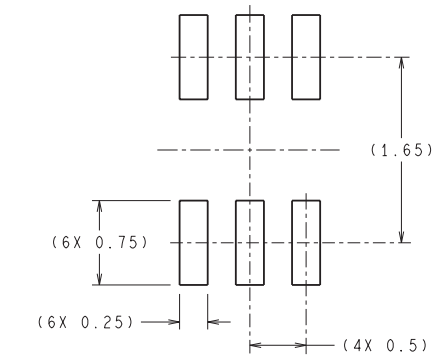
D: Max = 1.356 mm, Min =1.296 mm

E: Max = 0.99 mm, Min = 0.93 mm

4215043/A 12/12

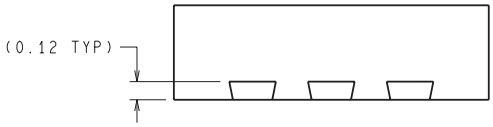
NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

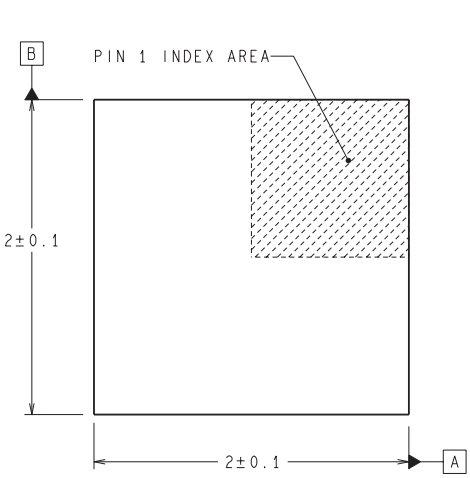
NKH0006B

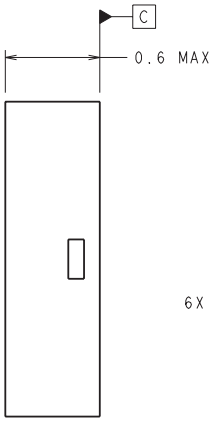


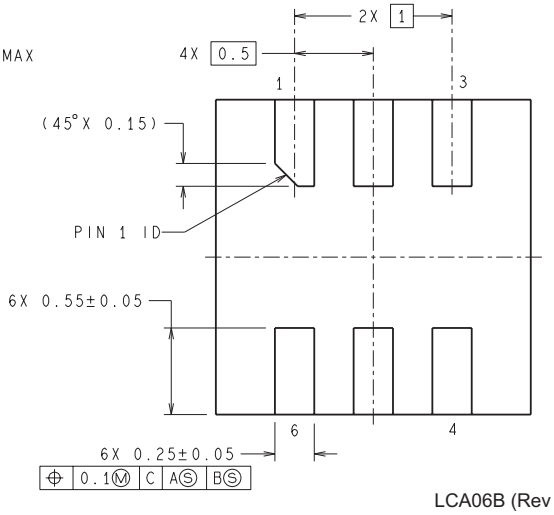
RECOMMENDED LAND PATTERN

DIMENSIONS ARE IN MILLIMETERS
DIMENSION IN ( ) FOR REFERENCE ONLY









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