
High-Input Voltage SMPS, Start-up/Linear Regulator

Features

- Accepts inputs from 15 to 450V
- Output currents: up to 3.0mA continuous, 30mA peak
- Supply current typically 50 μ A
- Line regulation typically 0.1mV/V
- Output can be trimmed from 8.0 to 12V
- Output current can be increased to 150mA with external FET

Applications

- Off-line SMPS startup circuits (pulse loads)
- Low power off-line regulators
- Regulators for noisy inputs

Description

LR645 is a high-input voltage, low-output current, linear regulator that is available in two versions. A 3-terminal, fixed-output voltage version is available in TO-92, TO-220 and SOT-89 packages, as well as an adjustable voltage version available in an 8-lead SOIC package.

The 3-terminal version of LR645 functions like any other low-voltage, 3-terminal regulator except it allows the use of much higher-input voltages. When used in a Switched-mode Power Supply (SMPS), start-up circuit, LR645 eliminates the need for large power resistors. In this application, current is drawn from the high voltage line only during start-up. Only leakage current flows after start-up, thereby reducing the continuous power dissipation to a few milliwatts.

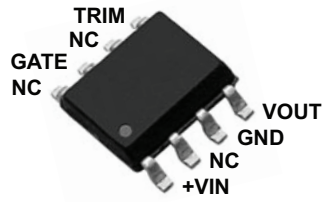
The adjustable-voltage version allows trimming of the output voltage from 8.0 to 12V. This version can also be connected to an external depletion mode metal-oxide-semiconductor field-effect transistor (MOSFET) for increased output current. When used in conjunction with depletion mode MOSFET DN2540N5, an output current of up to 150mA is achieved.

WARNING

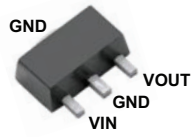
The LR645 does NOT provide galvanic isolation. When operated from an AC line, potentially lethal voltages can be present on the IC. Adequate means of protecting the end user from such voltages must be provided by the circuit developer.

LR645

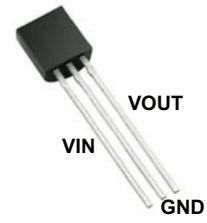
Package Type



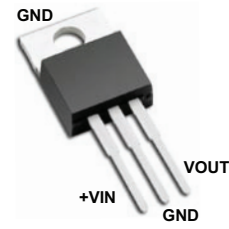
8-Lead SOIC



TO-243AA (SOT-89)



TO-92



TO-220

See [Table 2-1](#) for pin information

1.0 ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Input Voltage	450V
Output voltage.....	15.5V
Operating and storage temperature.....	-55°C to +150°C

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions, above those indicated in the operational listings of this specification, is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

1.1 ELECTRICAL SPECIFICATIONS

TABLE 1-1: ELECTRICAL CHARACTERISTICS ¹

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V _{OUT}	Output voltage	9.3	10	10.7	V	No load
	Output voltage over temperature ²	9.0	10	11.5	V	T _J = - 40 to +125°C, No load
ΔV _{OUT}	Line regulation	-	40	200	mV	V _{IN} = 15 to 400V, No load
	Load regulation	-	150	400	mV	V _{IN} = 50V, I _{OUT} = 0 to 3.0mA
V _{IN}	Operating input voltage range	15	-	450	V	
I _{INQ}	Input quiescent current	-	50	150	μA	No Load
I _{OFF}	V _{IN} off-state leakage current	-	0.1	10	μA	V _{AUX} ≥ V _{OUT} +1V applied to V _{OUT} pin
I _{AUX}	Input current to V _{OUT}	-	-	200	μA	V _{AUX} ≥ V _{OUT} +1V applied to V _{OUT} pin
ΔV _{OUT} /ΔV _{IN}	Ripple rejection ratio ²	50	60	-	dB	120 Hz, No Load
e _n	Noise voltage ²	-	25	-	μV	0.01 to 100 KHz
I _{PEAK}	Output peak current ³	-	30	-	mA	C _{OUT} = 10 μF, V _{IN} = 400V
V _{AUX}	External voltage applied to V _{OUT}	-	-	13.2	V	
8-lead, adjustable voltage version only						
V _{OUT}	Output regulation trim range ²	8	-	12	V	No load
ΔV _{OUT}	Load regulation at 8V trim ²	-	200	400	mV	V _{IN} = 15V, I _{OUT} = 0 to 1.0 mA
	Load regulation at 12V trim ²	-	100	400	mV	V _{IN} = 50V, I _{OUT} = 0 to 3.0 mA

1 Test Conditions unless otherwise specified: T_A = 25°C, V_{IN} = 15V-450V, C_{OUT} = 0.01 μF

2 Guaranteed by design

3 Pulse test duration <1.0 msec, duty cycle <2%

TABLE 1-2: THERMAL CHARACTERISTICS¹

Package	θ _{ja}	Power Dissipation @T _A =25°C
8-lead SOIC	101°C/W	0.31
TO-92	132°C/W	0.74
TO-220	29°C/W	1.8
TO-243AA (SOT-89)	133°C/W	1.6

1 Mounted on FR5 board; 25mm x 25mm x 1.57mm. Significant P_D increase possible on ceramic substrate.

LR645

2.0 PIN DESCRIPTION

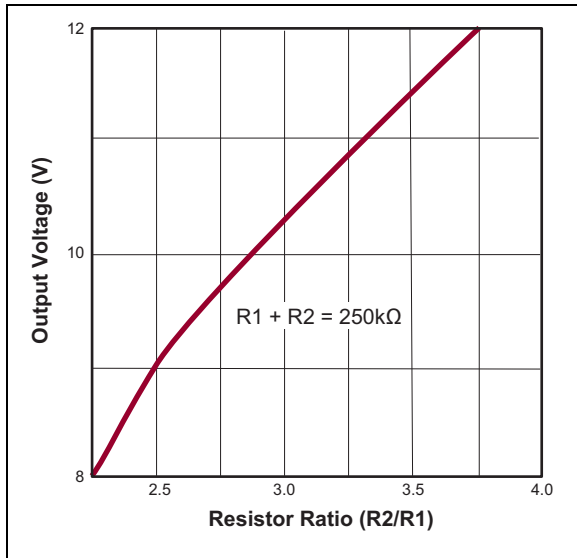
The locations of the pins are listed in [Package Type](#).

TABLE 2-1: PIN DESCRIPTION

Function	Description
VIN	Regulator input. 8 - 450V.
GND	Ground return for all internal circuitry. This pin must be electrically connected to circuit common.
GATE	Output GATE driver for an external N-channel depletion.
TRIM	A voltage divider from V_{OUT} to this pin adjusts the output voltage.
VOUT	Regulator output.
NC	No connection.

LR645

FIGURE 3-3: TYPICAL OUTPUT VOLTAGE VS RESISTOR RATIO



3.3 Off Line Linear Regulator

Circuits that require low voltages to operate logic and analog circuits benefit from LR645. The conventional use of step-down transformers can be eliminated, thereby saving space and cost. Some examples of low-voltage applications are: proximity controlled light switches, street lamp controls, and low-voltage power supplies for appliances such as washing machines, dishwashers, and refrigerators.

The wide operating-input voltage range of 15 to 450V, as well as the ripple rejection ratio of 50dB minimum, allows the use of a small, high-voltage input capacitor. The input AC line can be either full-wave or half-wave rectified. A minimum output capacitance of 0.01μF is recommended for output stability.

FIGURE 3-5: HIGH-CURRENT REGULATION

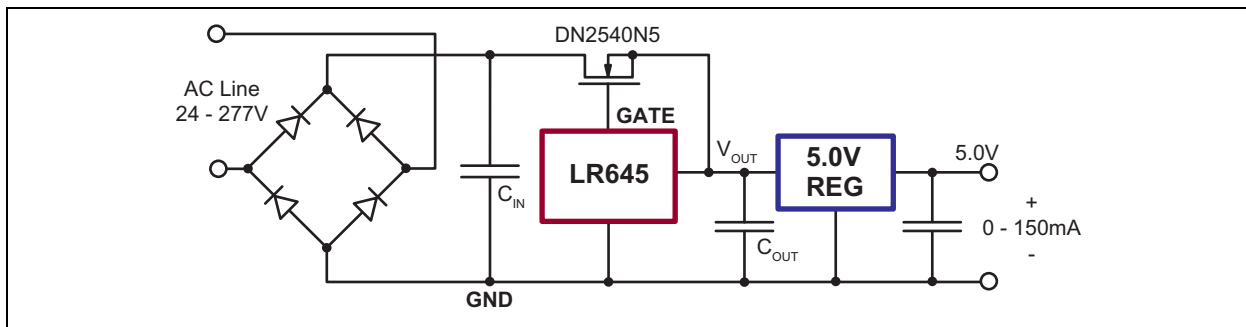
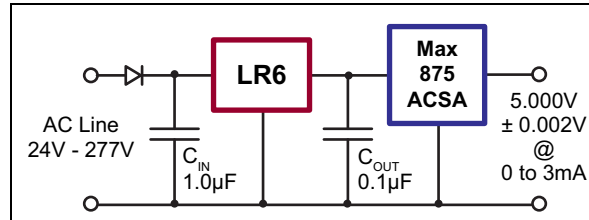


Figure 3-4 shows the LR645 as a pre-regulator to a precision regulator for high precision regulation. Higher output current is also possible by using an external depletion-mode MOSFET DN2540N5 as shown in Figure 3-5.

FIGURE 3-4: CASCADING FOR PRECISION



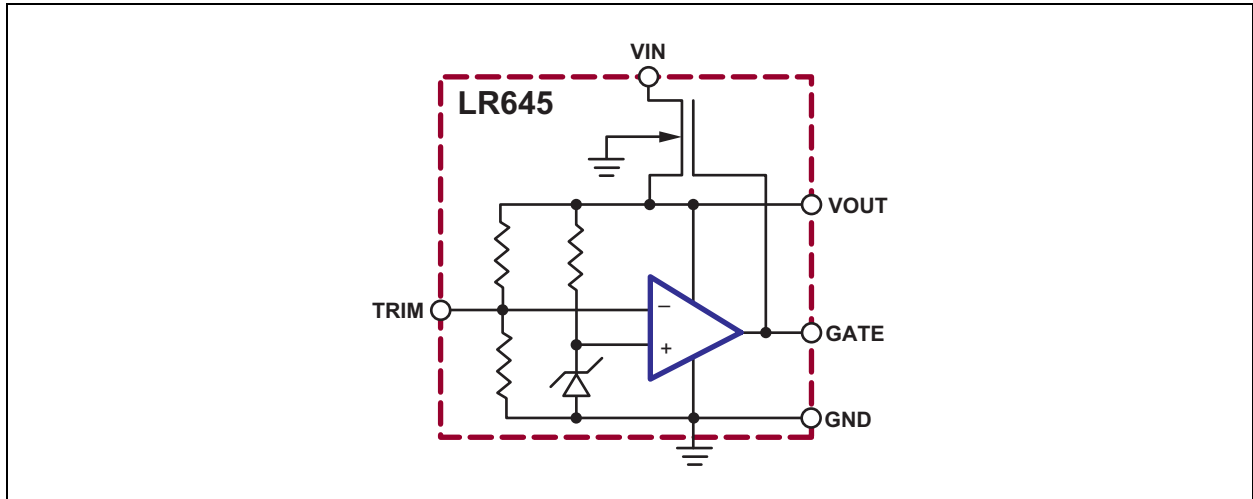
3.4 Power Dissipation Considerations

LR645 is a true linear regulator. Its power dissipation is therefore a function of input voltage and output load current. For example, if the LR645 provides a continuous load current of 3mA at 10V, while its input voltage is 400V, total dissipation in the LR645 will be:

$$\begin{aligned}
 P_{DISS} &= (V_{IN} - V_{OUT}) \times (I_{OUT} + I_{MAXQuiescent}) \\
 &= (400V - 10V) \times (3.0mA + 150\mu A) \\
 &= 1.23Watts
 \end{aligned}$$

The 1.23 watts is for continuous operation. This is within the dissipation capabilities of the TO-220 and SOT-89 packages. See Table 1-2 on Page 3 for deratings. For SMPS start-up applications, the output current is usually required only during start-up. This duration depends upon the auxiliary supply output capacitor and C_{OUT}, but is typically a few hundred milliseconds. All package types of the LR645 have been characterized for use with a C_{OUT} of at least 10μF, and an AC line of 277V.

FIGURE 3-6: BLOCK DIAGRAM

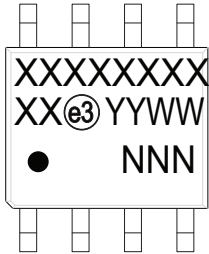


LR645

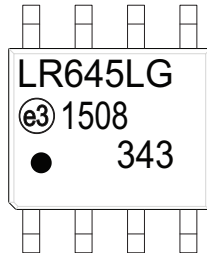
4.0 PACKAGING INFORMATION

4.1 Package Marking Information

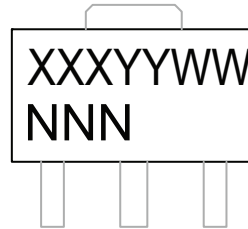
8-lead SOIC



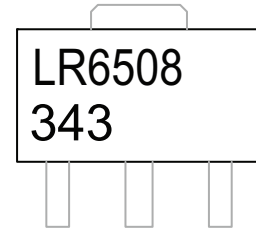
Example



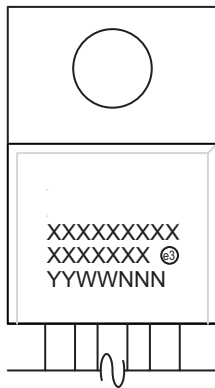
3-lead TO-243AA *
(SOT-89)



Example



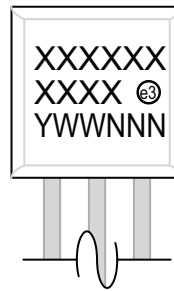
3-lead TO-220



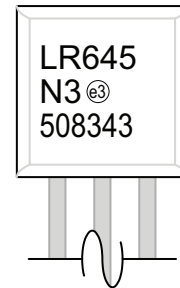
Example



3-lead TO-92



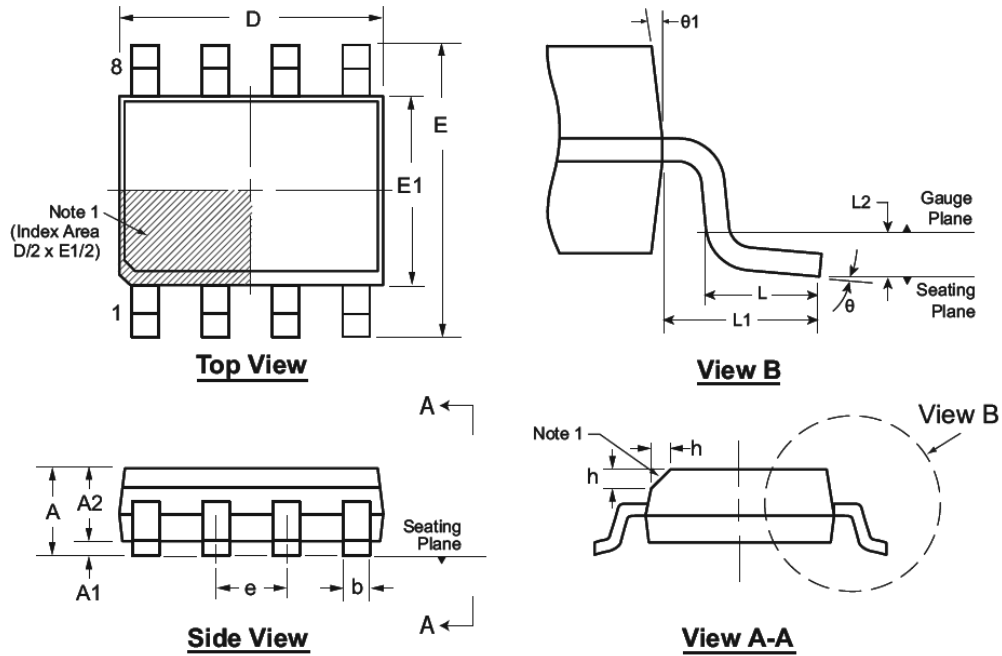
Example



Legend:	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	^(e3)	Pb-free JEDEC [®] designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (^(e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo.

8-Lead SOIC (Narrow Body) Package Outline (LG/TG) 4.90x3.90mm body, 1.75mm height (max), 1.27mm pitch



Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

Note:

1. This chamfer feature is optional. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.

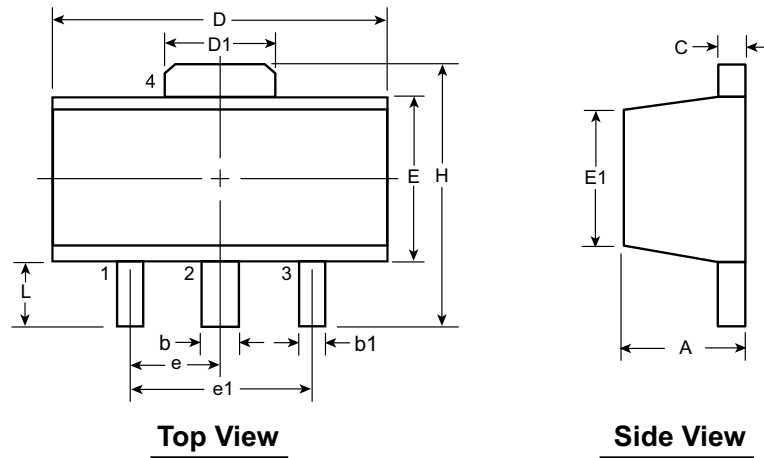
Symbol	A	A1	A2	b	D	E	E1	e	h	L	L1	L2	θ	θ_1	
Dimension (mm)	MIN	1.35*	0.10	1.25	0.31	4.80*	5.80*	3.80*	1.27 BSC	0.25	0.40	1.04 REF	0.25	0° - 8°	5° - 15°
	NOM	-	-	-	-	4.90	6.00	3.90		-	-				
	MAX	1.75	0.25	1.65*	0.51	5.00*	6.20*	4.00*		0.50	1.27				

JEDEC Registration MS-012, Variation AA, Issue E, Sept. 2005.

* This dimension is not specified in the JEDEC drawing.

Drawings are not to scale.

3-Lead TO-243AA (SOT-89) Package Outline (N8)



Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

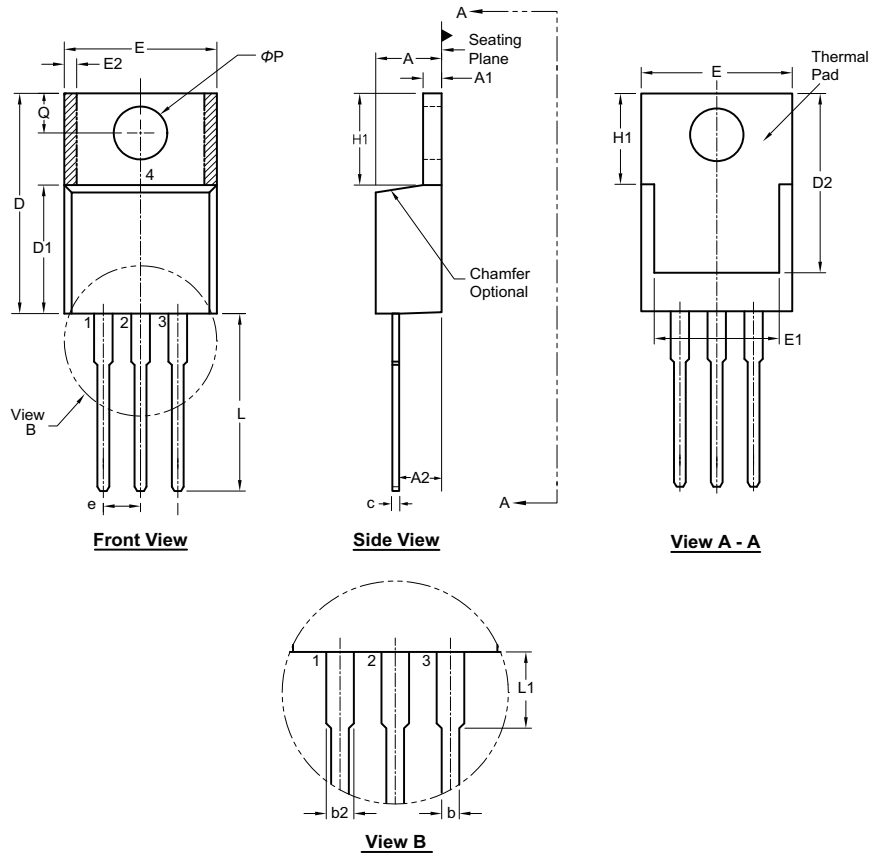
Symbol	A	b	b1	C	D	D1	E	E1	e	e1	H	L		
Dimensions (mm)	MIN	1.40	0.44	0.36	0.35	4.40	1.62	2.29	2.00 [†]	1.50 BSC	3.00 BSC	3.94	0.73 [†]	
	NOM	-	-	-	-	-	-	-	-			-	-	-
	MAX	1.60	0.56	0.48	0.44	4.60	1.83	2.60	2.29			4.25	1.20	

JEDEC Registration TO-243, Variation AA, Issue C, July 1986.

[†] This dimension differs from the JEDEC drawing

Drawings not to scale.

3-Lead TO-220 Package Outline (N5)



Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

Symbol	A	A1	A2	b	b2	c	D	D1	D2	E	E1	E2	e	H1	L	L1	Q	ΦP		
Dimension (inches)	MIN	.140	.020	.080	.015	.045	.012†	.560	.326†	.474†	.380	.270	0.20*	.100 BSC	.230	.500	.200*	.100	.139	
	NOM	-	-	-	.027	.057	-	-	-	-	-	-	-		-	-	-	-	-	-
	MAX	.190	.055	.120†	.040	.070	.024	.650	.361†	.507	.420	.350	.030		-	.270	.580	.250	.135	.161

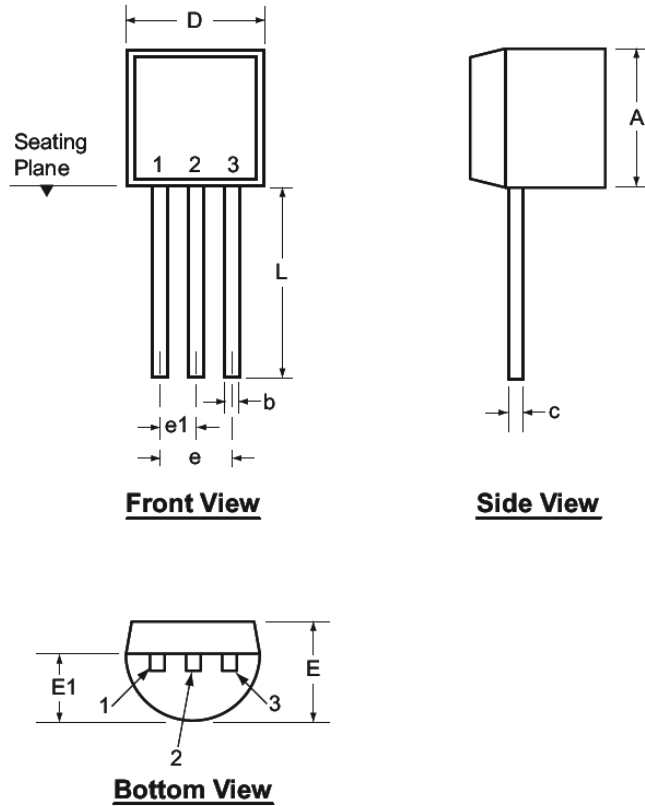
JEDEC Registration TO-220, Variation AB, Issue K, April 2002.

* This dimension is not specified in the JEDEC drawing.

† This dimension differs from the JEDEC drawing.

Drawings not to scale.

3-Lead TO-92 Package Outline (L/LL/N3)



Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

Symbol		A	b	c	D	E	E1	e	e1	L
Dimensions (inches)	MIN	.170	.014 [†]	.014 [†]	.175	.125	.080	.095	.045	.500
	NOM	-	-	-	-	-	-	-	-	-
	MAX	.210	.022 [†]	.022 [†]	.205	.165	.105	.105	.055	.610*

JEDEC Registration TO-92.

* This dimension is not specified in the JEDEC drawing.

† This dimension differs from the JEDEC drawing.

Drawings not to scale.

APPENDIX A: REVISION HISTORY

Revision A (April 2015)

- Update file to new format

LR645

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

<u>PART NO.</u>	<u>XX</u>	-	<u>X</u>	-	<u>X</u>
Device	Package Options		Environmental		Media Type
Device:	LR645	=	High-Input, Voltage SMPS, Start-up/Linear Regulator		
Package:	LG	=	8-lead SOIC (adjustable voltage)		
	N3	=	TO-92 (fixed voltage)		
	N5	=	TO-220(fixed voltage)		
	N8	=	TO-243AA (SOT-89) (fixed voltage)		
Environmental	G	=	Lead (Pb)-free/ROHS-compliant package		
Media Type:	(blank)	=	3300/Reel for LG packages		
		=	1000/Bag for N3 packages		
		=	50/Tube for TO-220 packages		
		=	2000/Reel for TO-243AA packages		
	P003	=	2000/Reel for N3 package		
	P013	=	2000/Ammo Pack for N3 package		

Examples:		
a)	LR645LG-G:	8-lead SOIC package, 3300/reel.
b)	LR645N3-G	TO-92 package, 1000/bag
c)	LR645N3-G-P003:	TO-92 package, 2000/reel.
d)	LR645N3-G-P013:	TO-92 package, 2000/ammo pack.
e)	LR645N5-G	TO-220 package, 50/tube
f)	LR645N8-G	TO-243AA package, 2000/reel

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