THE DATASHEET OF

LT3748HMS#TRPBF

100V Isolated Flyback Controller

FEATURES

- **5V to 100V Input Voltage Range**
- **1.9A Average Gate Drive Source and Sink Current**
- **Boundary Mode Operation**
- **No Transformer Third Winding or Opto-Isolator Required for Regulation**
- **Primary-Side Winding Feedback Load Regulation**
- V_{OUT} Set with Two External Resistors
- $INTV_{CC}$ Pin for Control of Gate Driver Voltage
- Programmable Soft Start
- Programmable Undervoltage Lockout
- Available in MSOP Package

APPLICATIONS

- Isolated Telecom Converters
- High Power Automotive Supplies
- Isolated Industrial Power Supplies
- Military and High Temperature Applications

DESCRIPTION

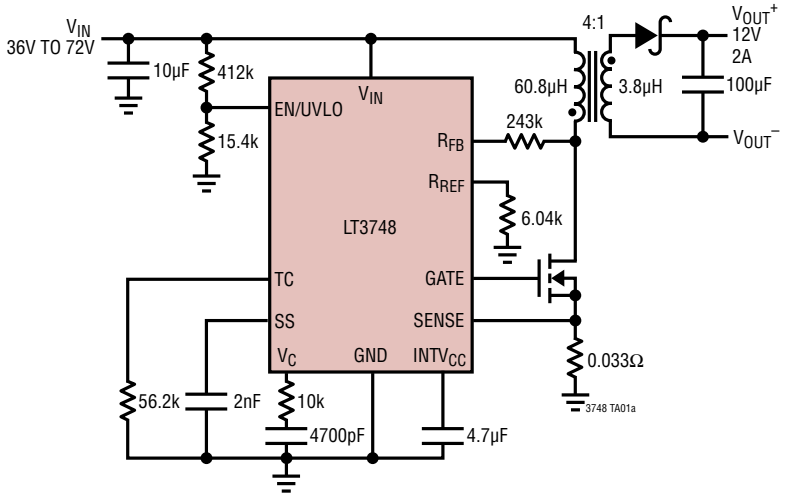
The LT®3748 is a switching regulator controller specifically designed for the isolated flyback topology and capable of high power. It drives a low side external N-channel power MOSFET from an internally regulated 7V supply. No third winding or opto-isolator is required for regulation as the part senses the isolated output voltage directly from the primary-side flyback waveform.

The LT3748 utilizes boundary mode to provide a small magnetic solution without compromising load regulation. Operating frequency is set by load current and transformer magnetizing inductance. The gate drive of the LT3748 combined with a suitable external MOSFET allow it to deliver load power up to several tens of watts from input voltages as high as 100V.

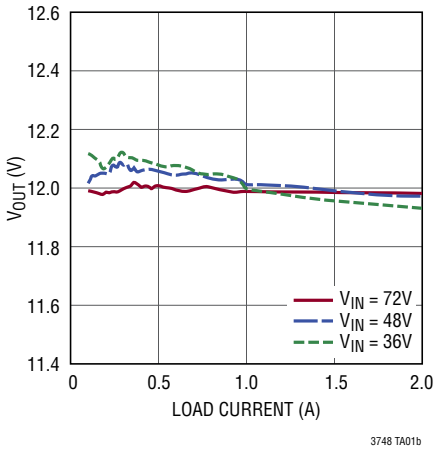
The LT3748 is available in a high voltage 16-lead MSOP package with four leads removed.

TYPICAL APPLICATION

25W, 12V Output, Isolated Telecom Supply



Output Load and Line Regulation

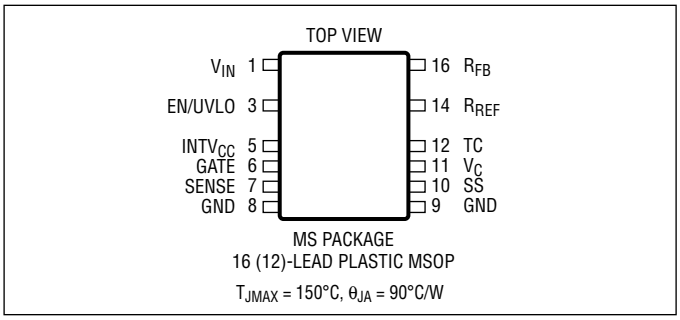


ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN}, R_{FB} 100V
V_{IN} to R_{FB} ..... ±5V
EN/UVLO ..... –0.3V, 100V
$INTV_{CC}$ ..... V_{IN} + 0.3V, 20V
SS, V_C, TC, R_{REF} 6V
SENSE 0.4V
Operating Junction Temperature Range (Note 2)
LT3748E/LT3748I ..... –40°C to 125°C
LT3748H ..... –40°C to 150°C
LT3748MP ..... –55°C to 150°C
Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT3748EMS#PBF	LT3748EMS#TRPBF	3748	16-Lead Plastic MSOP	–40°C to 125°C
LT3748IMS#PBF	LT3748IMS#TRPBF	3748	16-Lead Plastic MSOP	–40°C to 125°C
LT3748HMS#PBF	LT3748HMS#TRPBF	3748	16-Lead Plastic MSOP	–40°C to 150°C
LT3748MPMS#PBF	LT3748MPMS#TRPBF	3748	16-Lead Plastic MSOP	–55°C to 150°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 10V, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage Range		●	5		100	V
Quiescent Current	Not Switching $V_{EN/UVLO}$ = 0.2V			1.3 0	1.75 1	mA µA
V_{IN} Quiescent Current, $INTV_{CC}$ Overdriven	V_{INTVCC} = 10V			300	450	µA
$INTV_{CC}$ Voltage Range		●	4.5		20	V
$INTV_{CC}$ Pin Regulation Voltage			6.8	7	7.2	V
$INTV_{CC}$ Dropout	(V_{IN} – V_{INTVCC}), I_{INTVCC} = 10mA, V_{IN} = 5V			0.7		V
$INTV_{CC}$ Undervoltage Lockout	Falling Threshold	●	3.45	3.6	3.75	V
EN/UVLO Pin Threshold	EN/UVLO Pin Voltage Rising	●	1.19	1.223	1.25	V
EN/UVLO Pin Hysteresis Current	EN/UVLO = 1V		1.9	2.4	2.9	µA
Soft-Start Current	V_{SS} = 0.4V (Note 3)			5		µA
Soft-Start Threshold				0.65		V
Soft-Start Reset Current				3		mA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 10V, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Maximum SENSE Current Limit Threshold	V_C = 2.2V	 ●	95 90	100 100	105 110	mV mV
Minimum SENSE Current Limit Threshold	V_C = 0V			15		mV
Maximum to Minimum SENSE Threshold Ratio		●	5.2	6.6	8.2	mV/mV
SENSE Overcurrent Threshold	V_C = 2.2V		115	130	145	mV
SENSE Input Bias Current	V_{SENSE} = 10mV (Note 3)		10	15	20	µA
R_{REF} Voltage	V_C = 1.1V	 ●	1.20 1.195	1.223	1.24 1.245	V V
R_{REF} Voltage Line Regulation	5V < V_{IN} < 100V			0.005	0.025	%/V
R_{REF} Pin Bias Current	(Note 3)	●		35	500	nA
TC Current into R_{REF}	R_{TC} = 20k			27.5		µA
Error Amplifier Voltage Gain				115		V/V
Error Amplifier Transconductance	ΔI = 10µA			155		µmhos
V_C Source Current	V_C = 1.1V, V_{RREF} = 0.5V			–45		µA
V_C Sink Current	V_C = 1.1V, V_{RREF} = 2V			48		µA
Flyback Comparator Trip Current	Current into R_{FB} Pin, R_{REF} = 6.04k			10		µA
Minimum GATE Off-Time				700		ns
Minimum GATE On-Time				250		ns
Maximum Discontinuous Off-Time	V_C = 0V			24		µs
Maximum GATE Off-Time	V_{RREF} = 0.5V			55		µs
Maximum GATE On-Time	V_{SENSE} = 0V			55		µs
GATE Output Rise Time	C_L = 3300pF, 10% to 90%			16		ns
GATE Output Fall Time	C_L = 3300pF, 10% to 90%			16		ns
GATE Output Low (V_{OL})					0.05	V
GATE Output High (V_{OH})			V_{INTVCC} – 0.05			V

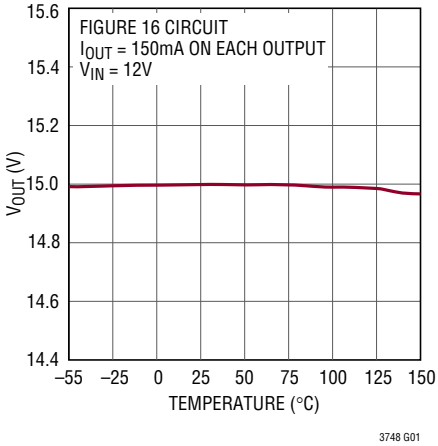
Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LT3748E is guaranteed to meet performance specifications from 0°C to 125°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design characterization and correlation with statistical process controls. The LT3748I is guaranteed over the full –40°C to 125°C operating junction temperature range. The LT3748H is guaranteed over the full –40°C to 150°C operating junction temperature range. The LT3748MP is guaranteed over the full –55°C to 150°C operating junction temperature range. High junction temperatures degrade operating lifetimes. Operating lifetime is derated at junction temperatures greater than 125°C.

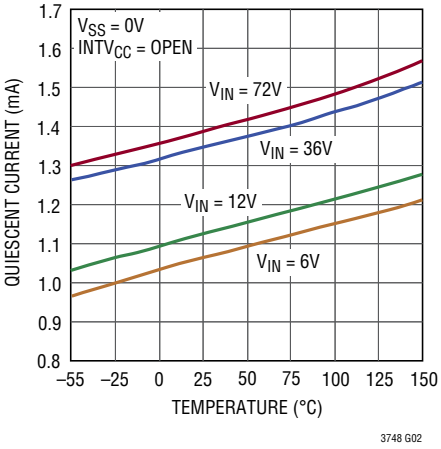
Note 3: Current flows out of the pin.

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

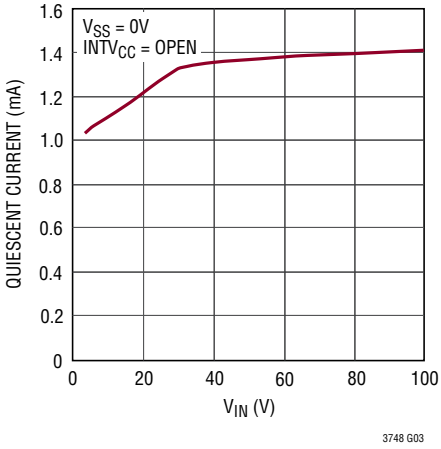
Output Regulation vs Temperature



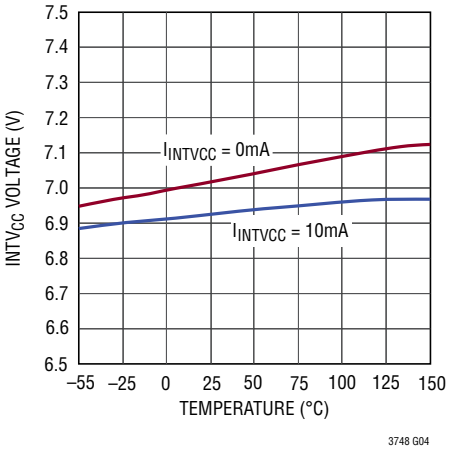
Quiescent Current vs Temperature



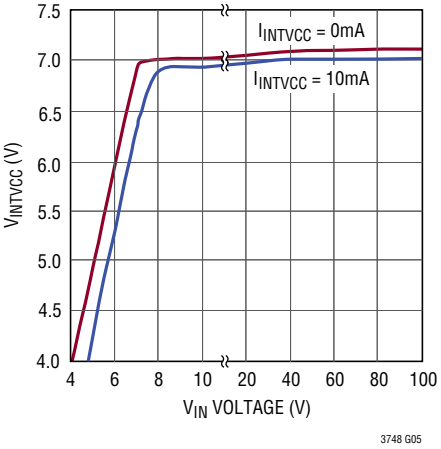
Quiescent Current vs V_{IN} Voltage



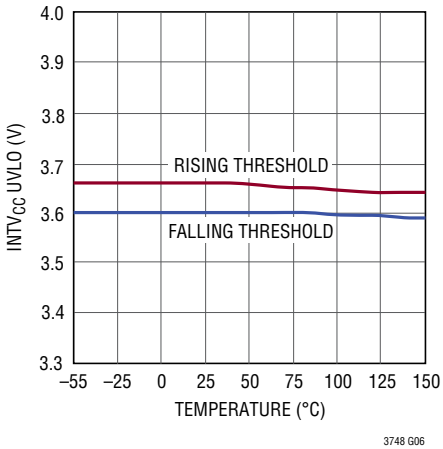
$INTV_{CC}$ Voltage vs Temperature



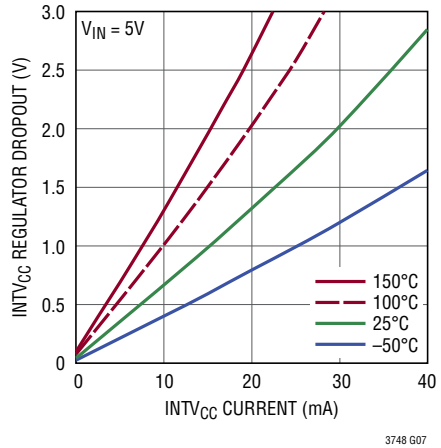
$INTV_{CC}$ Voltage vs V_{IN} Voltage



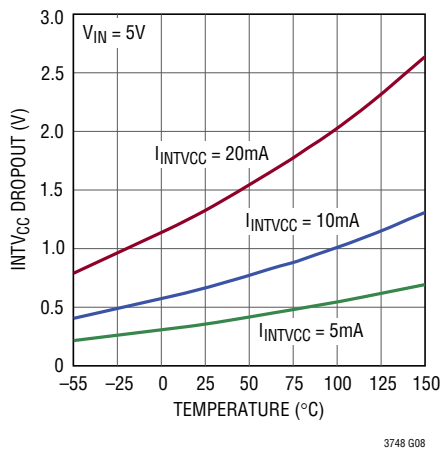
$INTV_{CC}$ Undervoltage Lockout vs Temperature



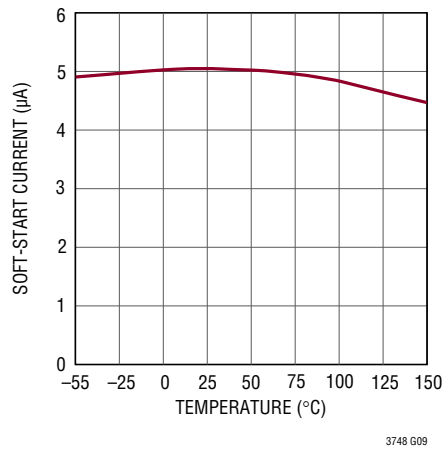
$INTV_{CC}$ Regulator Dropout vs $INTV_{CC}$ Current



$INTV_{CC}$ Dropout vs Temperature

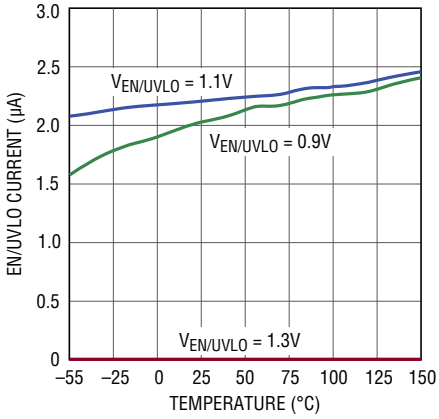


Soft-Start Current vs Temperature

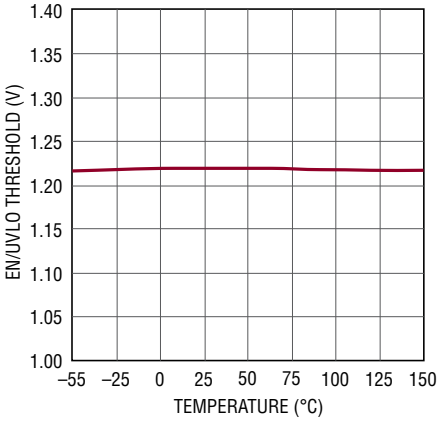


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

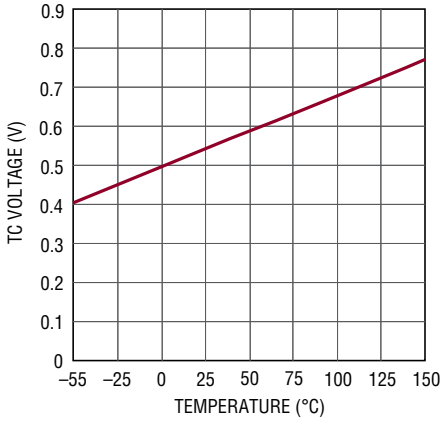
EN/UVLO Current vs Temperature



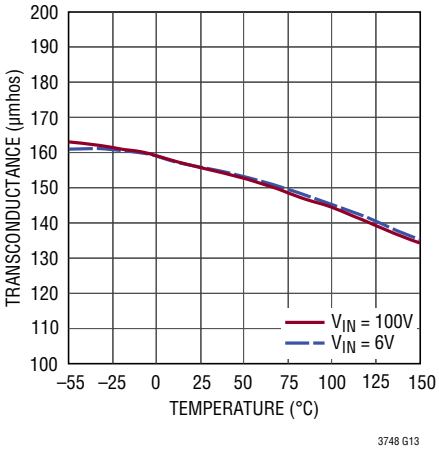
EN/UVLO Threshold vs Temperature



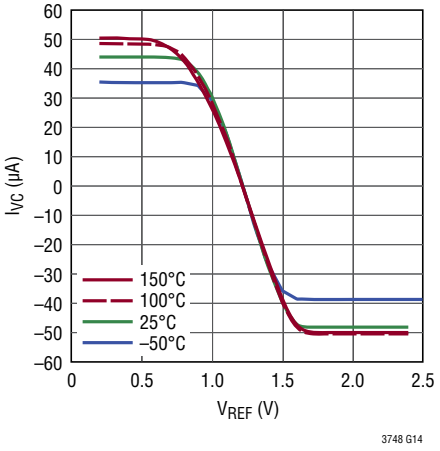
TC Pin Voltage vs Temperature



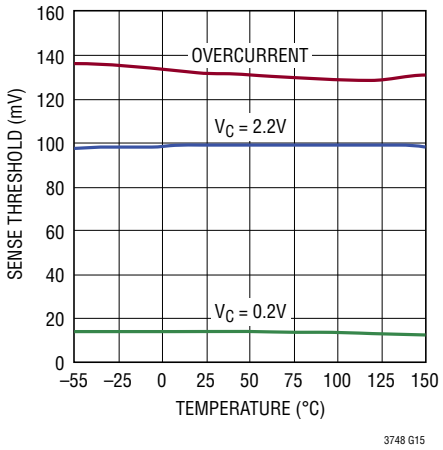
Error Amplifier Transconductance vs Temperature



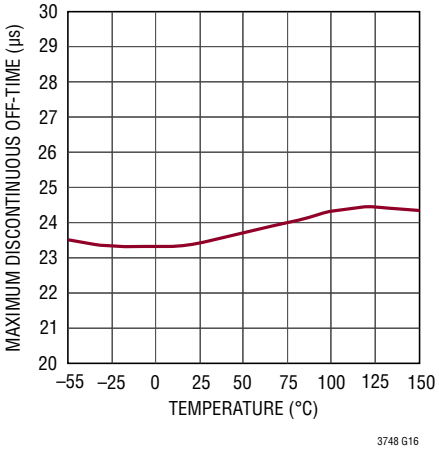
Error Amplifier Output Current vs R_{REF} Pin Voltage



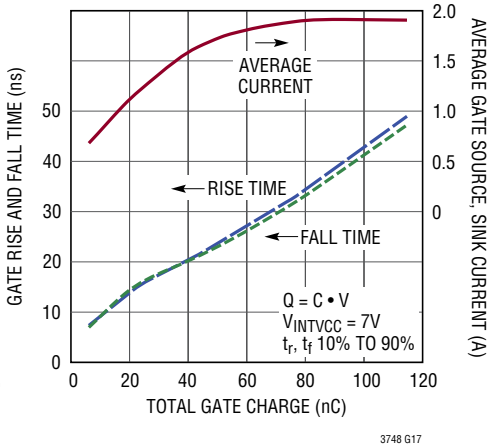
SENSE Pin Threshold vs Temperature



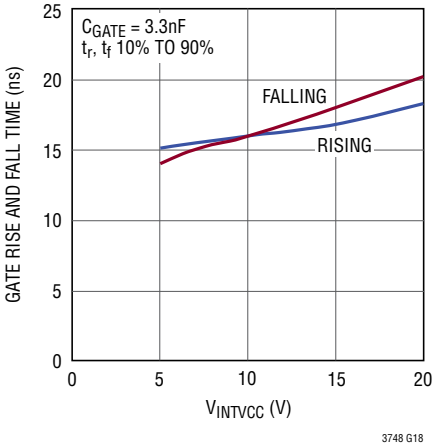
Maximum Discontinuous Off-Time vs Temperature



GATE Rise and Fall Time vs Charge



GATE Rise and Fall Time vs $INTV_{CC}$ Voltage



PIN FUNCTIONS

V_{IN} (Pin 1) Input Voltage. This pin supplies current to the internal start-up circuitry and is the reference voltage for the feedback circuitry connected to the R_{FB} pin. This pin must be locally bypassed with a capacitor.

EN/UVLO (Pin 3): Enable/Undervoltage Lockout. A resistor divider connected to V_{IN} is tied to this pin to program the minimum input voltage at which the LT3748 will operate. At a voltage below ~0.5V, the part draws less than 1µA quiescent current. When below 1.223V but above ~0.5V, the part will draw quiescent current but will not regulate the $INTV_{CC}$ supply or power the gate drive circuitry. Above 1.223V, all internal circuitry will start and the SS pin will source 5µA. When EN/UVLO falls below 1.223V, 2.4µA is sunk from the pin to provide programmable hysteresis for undervoltage lockout.

$INTV_{CC}$ (Pin 5): Gate Driver Bias Voltage. This pin supplies current to the internal gate driver circuitry of the LT3748. The $INTV_{CC}$ pin must be locally bypassed with a capacitor. This pin may also be connected to V_{IN} if a third winding is not used and if $V_{IN} \leq 20V$. If a third winding is used, the $INTV_{CC}$ voltage should be lower than the input voltage for proper operation.

GATE (Pin 6): N-Channel MOSFET Gate Driver Output. Switches between $INTV_{CC}$ and GND.

SENSE (Pin 7): The Current Sense Input for the Control Loop. Kelvin connect this pin to the positive terminal of the switch current sense resistor, R_{SENSE}, in the source of the N-channel MOSFET. The negative terminal of the current sense resistor should be connected to the GND plane close to the IC.

GND (Pins 8, 9): Ground.

SS (Pin 10): Soft-Start Pin. This pin delays start-up and clamps V_C pin voltage. Soft-start timing is set by the size of the external capacitor at the pin. Switching starts when V_{SS} reaches ~0.65V.

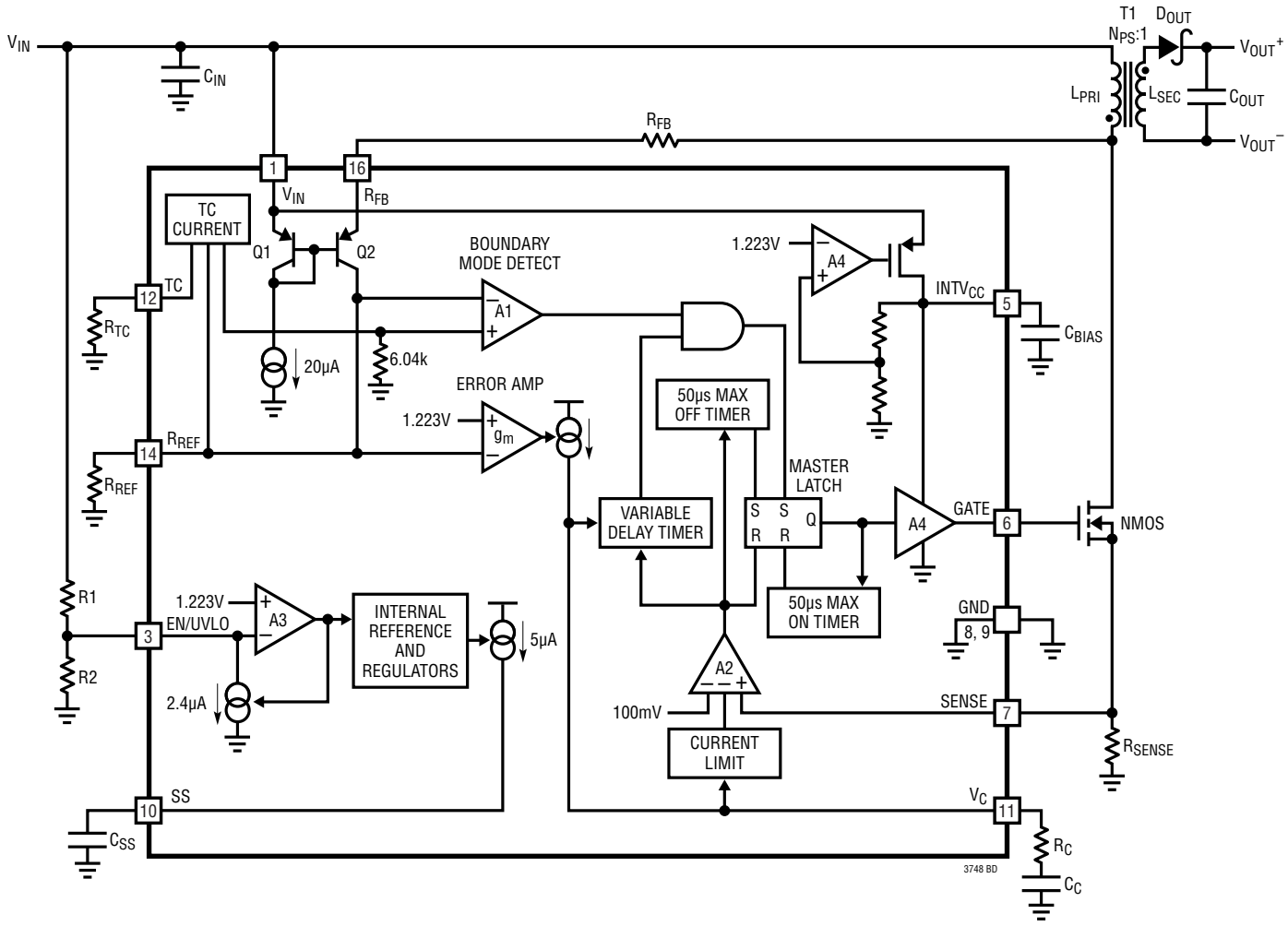
V_C (Pin 11): Compensation Pin for the Internal Error Amplifier. Connect a series RC from this pin to ground to compensate the switching regulator. A 100pF capacitor in parallel helps eliminate noise.

TC (Pin 12): Output Voltage Temperature Compensation. Connect a resistor to ground to produce a current proportional to absolute temperature to be sourced into the RREF node. $I_{TC} = 0.55V/R_{TC}$.

R_{REF} (Pin 14): Input Pin for the External Ground-Referred Reference Resistor. The resistor at this pin should be 6.04k, but for convenience in selecting a resistor divider ratio, the value may range from 5.76k to 6.34k. **The resistor should be as close to the LT3748 as possible**.

R_{FB} (Pin 16): Input Pin for the External Feedback Resistor. This pin is connected to the transformer primary at the external MOSFET power switch. The ratio of this resistor to the R_{REF} resistor, times the internal bandgap reference, determines the output voltage (plus the effect of any non-unity transformer turns ratio). The average current through this resistor during the flyback period should be approximately 200µA. **The resistor should be as close to the LT3748 as possible**.

BLOCK DIAGRAM



OPERATION

The LT3748 is a current mode switching regulator controller designed specifically for the isolated flyback topology. The special problem normally encountered in such circuits is that information relating to the output voltage on the isolated secondary side of the transformer must be communicated to the primary side in order to maintain regulation. Historically, this has been done with opto-isolators or extra transformer windings. Opto-isolator circuits waste output power and the extra components increase the cost and physical size of the power supply. Opto-isolators can also exhibit trouble due to limited dynamic response, nonlinearity, unit-to-unit variation and aging over life. Circuits employing extra transformer windings also exhibit deficiencies. Using an extra winding adds to the transformer's physical size and cost, and dynamic response is often mediocre.

The LT3748 derives its information about the isolated output voltage by examining the primary-side flyback pulse waveform. In this manner, no opto-isolator nor extra transformer winding is required for regulation. The output voltage is easily programmed with two resistors. The LT3748 features a boundary mode control method, (also called critical conduction mode) where the part operates at the boundary between continuous conduction mode and discontinuous conduction mode. Due to the boundary control mode operation, the output voltage can be calculated from the transformer primary voltage when the secondary current is almost zero. This method improves load regulation without external resistors and capacitors.

The Block Diagram shows an overall view of the system. Many of the blocks are similar to those found in traditional switching regulators, including current comparators, internal reference and regulators, logic, timers and an N-channel MOSFET gate driver. The novel sections include a special sampling error amplifier and a temperature compensation circuit.

Boundary Mode Operation

Boundary mode is a variable frequency, current mode switching scheme. The external N-channel MOSFET turns on and the inductor current increases until it reaches the V_C pin-controlled current limit. After the external MOSFET is turned off, the voltage on the drain of the MOSFET rises to the output voltage multiplied by the primary-to-secondary transformer turns ratio plus the input voltage. When the secondary current through the output diode falls to zero, the voltage on the drain of the MOSFET falls below V_{IN}. A boundary mode detection comparator detects this event and turns the external MOSFET back on.

Boundary mode returns the secondary current to zero every cycle, so the parasitic resistive voltage drops do not cause load regulation errors. Boundary mode also allows the use of a smaller transformer compared to continuous conduction mode and does not exhibit subharmonic oscillation.

At low output currents the LT3748 delays turning on the external MOSFET and thus operates in discontinuous mode. Unlike traditional flyback converters, the external MOSFET has to turn on to update the output voltage information. Below 0.6V on the V_C pin, the current comparator level decreases to its minimum value and a variable delay timer waits to reset before turning on the external MOSFET. With the addition of delay before turning the MOSFET back on, the part starts to operate in discontinuous mode. The average output current is able to decrease while still allowing a minimum off-time for the error amplifier sampling circuitry. The typical maximum discontinuous off-time with V_C equal to 0V is 24µs.

APPLICATIONS INFORMATION

Pseudo-DC Theory of Operation

The R_{REF} and R_{FB} resistors as depicted in the Block Diagram are external resistors used to program the output voltage. The LT3748 operates much the same way as traditional current mode switchers with the exception of the unique error amplifier which derives its feedback information from the flyback pulse.

Operation is as follows: when the NMOS output switch turns off, its drain voltage rises above V_{IN}. The amplitude of this flyback pulse (i.e., the difference between it and V_{IN}) is given as:

$V_{FLBK} = (V_{OUT} + V_F + I_{SEC} \bullet ESR) \bullet N_{PS}$

V_F = D_{OUT} forward voltage

I_{SEC} = Transformer secondary current

ESR = Total impedance of secondary circuit

N_{PS} = Transformer effective primary-to-secondary turns ratio

The flyback voltage is converted to a current by R_{FB} and Q2. Nearly all of this current flows through resistor R_{REF} to form a ground-referred voltage. This voltage is fed into the flyback error amplifier. The flyback error amplifier samples this output voltage information when the secondary-side winding current reaches zero. The error amplifier uses a bandgap voltage, 1.223V, as the reference voltage.

The relatively high gain in the overall loop will then cause the voltage at the R_{REF} resistor to be nearly equal to the bandgap reference voltage, V_{BG}. The relationship between V_{FLBK} and V_{BG} may then be expressed as:

$$\left(\frac{V_{FLBK}}{R_{FB}}\right) = \frac{V_{BG}}{R_{REF}} \text{ or}$$

$$V_{FLBK} = V_{BG}\left(\frac{R_{FB}}{R_{REF}}\right)$$

V_{BG} = Internal bandgap reference

Combining with the previous V_{FLBK} expression yields an expression for V_{OUT}, in terms of the internal reference, programming resistors, transformer turns ratio and diode forward voltage drop:

$$V_{OUT} = V_{BG}\left(\frac{R_{FB}}{R_{REF}}\right)\left(\frac{1}{N_{PS}}\right) - V_F - I_{SEC}\,(ESR)$$

Additionally, it includes the effect of nonzero secondary output impedance (ESR). This term can be assumed to be zero in boundary control mode.

Temperature Compensation

The first term in the V_{OUT} equation does not have a temperature dependence, but the diode forward drop, V_F, has a significant negative temperature coefficient. To compensate for this, a positive temperature coefficient current source is internally connected to the R_{REF} pin. The current is set by resistor R_{TC} to ground connected between the TC pin and ground. To cancel the temperature coefficient, the following equation is used:

$$\frac{\delta V_F}{\delta T} = -\frac{R_{FB}}{R_{TC}} \bullet \frac{1}{N_{PS}} \bullet \frac{\delta V_{TC}}{\delta T} \quad \text{or,}$$

$$R_{TC} = \frac{-R_{FB}}{N_{PS}} \bullet \frac{1}{\delta V_F / \delta T} \bullet \frac{\delta V_{TC}}{\delta T} \approx \frac{R_{FB}}{N_{PS}}$$

$(\delta V_F/\delta_T)$ = Diode's forward voltage temperature coefficient

$(\delta V_{TC}/\delta_T)$ = 1.85mV/°C

V_{TC} = 0.55V

The resistor value given by this equation should also be verified experimentally and adjusted, if necessary, to achieve optimal regulation over temperature.

The revised output voltage is as follows:

$$V_{OUT} = V_{BG}\left(\frac{R_{FB}}{R_{REF}}\right)\left(\frac{1}{N_{PS}}\right) - V_F - \left(\frac{V_{TC}}{R_{TC}}\right) \bullet \frac{R_{FB}}{N_{PS}} - I_{SEC}\,(ESR)$$

APPLICATIONS INFORMATION

Selecting Actual R_{REF}, R_{FB} and R_{TC} Resistor Values

The preceding equations define how the LT3748 would regulate the output voltage if the system had no time delays and no error sources. However, there are a number of repeatable delays and parasitics in each application which will affect the output voltage and force a re-evaluation of the R_{FB} and R_{TC} component values. The following approach is the best method for selecting the correct values.

The expression for V_{OUT}, developed in the Operation section, can be rearranged to yield the following expression for R_{FB}:

$$R_{FB} = \frac{R_{REF} \bullet N_{PS}\left[\left(V_{OUT} + V_F\right) + V_{TC}\right]}{V_{BG}}$$

where:

V_{OUT} = Output voltage

V_F = Output diode forward voltage

N_{PS} = Effective primary-to-secondary turns ratio

V_{TC} = 0.55V

The equation assumes the temperature coefficients of the output diode and V_{TC} are equal and substitutes R_{FB}/N_{PS} for the value of R_{TC}. This is a good first order approximation but will be revisited later.

First, the value of R_{REF} should be approximately 6.04k since the LT3748 is trimmed and specified using this value. If the impedance of R_{REF} varies considerably from 6.04k, additional errors will result. However, a variation in R_{REF} of several percent is acceptable. This yields a bit of freedom in selecting standard 1% resistor values to yield nominal R_{FB}/R_{REF} ratios.

With starting values for R_{FB} and R_{TC}, an initial iteration of the application should be built with final selections of all external components (transformer, diode, MOSFET, etc.). The resulting V_{OUT} should be measured and used to re-evaluate the value of R_{FB} due to non-idealities in the sampling system:

$$R_{FB(NEW)} = \frac{V_{OUT(DESIRED)}}{V_{OUT(MEASURED)}} \bullet R_{FB(OLD)}$$

With a new value of R_{FB} selected, the temperature coefficient of the output diode in the application can be tested to verify the nominal R_{TC} value. The R_{TC} resistor should be removed from the circuit under test (this will cause V_{OUT} to increase for this step) and V_{OUT} should be measured over temperature at a desired target output load. It is very important for this evaluation that uniform temperature be applied to both the output diode and the LT3748—if freeze spray or a heat gun is used there can be a significant mismatch in temperature between the two devices that causes significant error. Attempting to extrapolate the data from a diode datasheet or assuming the nominal R_{TC} value may yield a better result if there is no method to apply uniform heat or cooling such as an oven. With at least two data points (although more data points from hot to cold are recommended), the change in V/°C can be determined by:

$$\frac{\Delta V_{OUT}}{\Delta TEMP} = \frac{V_{OUT1} - V_{OUT2}}{TEMP1 - TEMP2}$$

Using the measured V_{OUT} temperature coefficient, an exact R_{TC} value can be selected using the following equation:

$$R_{TC} = \frac{R_{FB}}{N_{PS}} \bullet \frac{1.85mV/°C}{\frac{\Delta V_{OUT}}{\Delta TEMP}}$$

If the value of R_{TC} has changed significantly, which can happen with the use of some output diodes that have a very low forward drop, the R_{FB} value may need to be changed to restore V_{OUT} to the desired value. As in the previous iteration, after measuring V_{OUT}, a new R_{FB} can once again be selected using:

$$R_{FB(NEW)} = \frac{V_{OUT(DESIRED)}}{V_{OUT(MEASURED)}} \bullet R_{FB(OLD)}$$

Once the values of R_{FB} and R_{TC} are selected, the regulation accuracy from board to board for a given application will be very consistent, typically under ±5% when including device variation of all the components in the system (assuming resistor tolerances and transformer windings matching of 1% or better). However, if the transformer, the output diode or MOSFET switch are changed or the layout is dramatically altered, there may be some change in V_{OUT}.

APPLICATIONS INFORMATION

Minimum Primary Inductance Requirements

The LT3748 obtains output voltage information from the external MOSFET drain voltage when the secondary winding conducts current. The sampling circuitry needs a minimum of 400ns to settle and sample the output voltage while the MOSFET switch is off. This required settle and sample time is controlled by external components independent of the minimum off-time of the GATE pin as specified in the Electrical Characteristics table. The electrical specification minimum off-time is based on an internal timer and acts as a maximum frequency clamp. The following equation gives the minimum value for primary-side magnetizing inductance:

$$L_{PRI} \geq \frac{\left(V_{OUT} + V_{F(DIODE)}\right) \bullet R_{SENSE} \bullet t_{SETTLE(MIN)} \bullet N_{PS}}{V_{SENSE(MIN)}}$$

$V_{SENSE(MIN)}$ = 15mV

$t_{SETTLE(MIN)}$ = 400ns

N_{PS} = Ratio of primary windings to secondary windings

In addition to the primary inductance requirement for minimum settling and sampling time, the LT3748 has internal circuit constraints that prevent it from setting the GATE node high for shorter than approximately 250ns. If the inductor current exceeds the desired current limit during that time oscillation may occur at the output as the current control loop will lose its ability to regulate. Therefore, the following equation relating to maximum input voltage must also be followed in selecting primary-side magnetizing inductance:

$$L_{PRI} \geq \frac{V_{IN(MAX)} \bullet R_{SENSE} \bullet t_{ON(MIN)}}{V_{SENSE(MIN)}}$$

$t_{ON(MIN)}$ = 250ns

The last constraint on minimum inductance value would relate to minimum full-load operating frequency, $f_{SW(MIN)}$, and is derived from $f_{SW} = 1/(t_{ON} + t_{OFF})$:

$$L_{PRI} \leq V_{IN(MIN)} \bullet (V_{OUT} + V_{F(DIODE)}) \bullet N_{PS} / (f_{SW(MIN)} \bullet I_{LIM} \bullet ((V_{OUT} + V_{F(DIODE)}) \bullet N_{PS} + V_{IN(MIN)}))$$

The minimum operating frequency may be lower than the calculated number due to delays in detecting current limit and detecting boundary mode that are specific to each application.

Output Power

Because the MOSFET power switch is located outside the LT3748, the maximum output power is primarily limited by external components. Output power limitations can be separated into three categories—voltage limitations, current limitations and thermal limitations.

The voltage limitations in a flyback design are primarily the MOSFET switch $V_{DS(MAX)}$ and the output diode reverse-bias rating. Increasing the voltage rating of either component will typically decrease application efficiency if all else is equal and the voltage requirements on each of those components will be directly related to the windings ratio of the transformer, the input and output voltages and the use of any additional snubbing components. The MOSFET $V_{DS(MAX)}$ must theoretically be higher than $V_{IN(MAX)} + (V_{OUT} \bullet N_{PS})$ and the output diode reverse bias must be higher than $V_{OUT} + (V_{IN(MAX)}/N_{PS})$, though leakage inductance spikes on both the drain of the MOSFET and the anode of the output diode may more than double that requirement (see section on leakage inductance for more details on snubbers). Figure 1 illustrates the effect on available output power for several MOSFET voltage ratings while continuously maximizing windings ratio for input voltage with a fixed MOSFET current limit and output voltage. Increasing the MOSFET rating increases the possible windings ratio and or maximum input voltage and can increase the available output power for a given application. Both figures assume no leakage inductance and high efficiency.

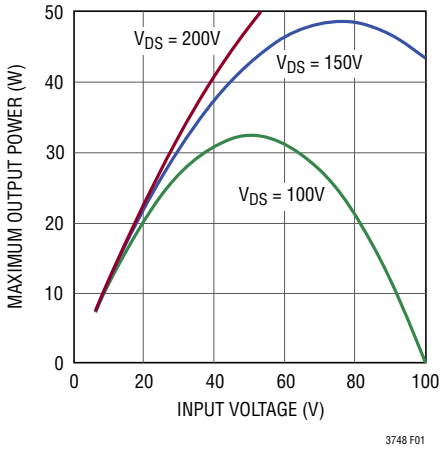


Figure 1. Maximum Output Power at $12V_{OUT}$ with a 3A I_{LIM} and Maximum V_{DS} = 100V, 150V, 200V

APPLICATIONS INFORMATION

The current limitation on output power delivery is generally constrained by transformer saturation current in higher power applications, although the MOSFET switch and output diode will need to be rated for the desired currents, as well. Increasing the peak current on the primary side of the flyback by reducing the R_{SENSE} resistor is the primary way to increase output power, and power delivered increases fairly linearly with current limit as shown in Figure 2, until parasitic losses begin to dominate. However, once the saturation current of the transformer is exceeded the energy coupling between the primary and the secondary will be reduced and incremental power will not be delivered to the output. In addition, the primary inductance will drop, the SENSE pin overcurrent threshold may trip due to a corresponding rapid rise in current, and the transformer will have to absorb the energy that is not transferred through the saturated core, leading to heating. Some manufacturers may not specify the rated saturation current but it is a necessary specification when trying to minimize transformer size and maximize output power and efficiency. Also necessary for proper design is data on saturation current over temperature—the saturation of typical power ferrites may reduce by over 20% from 25°C to 100°C.

The thermal limitation in flyback applications for lower output voltages will be dominated by losses in the output diode, with resistive and leakage losses in the transformer

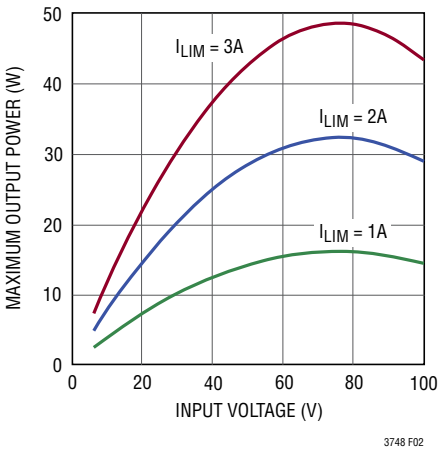


Figure 2. Maximum Output Power at $12V_{OUT}$ with 150V $V_{DS(MAX)}$ and I_{LIM} = 1A, 2A, 3A

increasing as a percentage basis of loss as the output voltage is increased. As power levels increase the output diode and transformer may exceed their rated temperature specifications. Minimizing RMS output diode current, selecting a diode with minimal forward drop at expected currents and minimizing parasitic resistances and leakage inductance in the transformer will keep those components below their maximum temperatures while maximizing efficiency. The following section discussing transformer selection will further help focus on how to minimize losses in the output diode.

While quiescent current in the LT3748 itself is low (approximately 300µA from V_{IN} and 1mA from $INTV_{CC}$), the current required to drive the external MOSFET ($f_{SW} \bullet Q_G$), if drawn from V_{IN} through the LT3748 $INTV_{CC}$ LDO, dissipates ($V_{IN} – INTV_{CC}$) • f_{SW} • Q_G. If that power is high enough to cause significant heating of the LT3748 the current may need to be drawn from a third winding. Doing so will push all thermal limitations outside of the LT3748.

Selecting a Transformer

Transformer specification and design is perhaps the most critical part of successfully applying the LT3748. In addition to the usual list of caveats dealing with high frequency isolated power supply transformer design, the following information should be carefully considered.

First and most importantly, since the voltage on the secondary side of the transformer is inferred by the voltage sampled on the primary, the transformer turns ratio must be tightly controlled to ensure a consistent output voltage. A tolerance of ±5% in turns ratio from transformer to transformer could result in a variation of more than ±5% in output regulation. Fortunately, most magnetic component manufacturers are capable of guaranteeing a turns ratio tolerance of 1% or better.

Linear Technology has worked with several leading magnetic component manufacturers to produce predesigned flyback transformers for use with the LT3748. Table 1 shows the details of several of these transformers.

APPLICATIONS INFORMATION

Table 1. Pre-Designed Transformers—Typical Specifications Unless Otherwise Noted

TRANSFORMER PART NUMBER	Size (W x L x H) mm	L_{PRI} (µH)	L_{LEAK} (nH)	N_{PS} (N_P:N_S)	I_{SAT} (A)	R_{PRI} (mΩ)	R_{SEC} (mΩ)	MANUFACTURER	TARGET APPLICATION† INPUT (V)	TARGET APPLICATION† OUTPUT
750311424	17.7 × 14.0 × 12.7	100	844	3:1	3	180	29	Würth Electronics	40 to 75	12V/1A
750311456*	17.7 × 14.0 × 12.7	100	900	3:1	2.4	225	31	Würth Electronics	40 to 75	12V/1A
750311439	17.7 × 14.0 × 12.7	37	750	2:1	2.8	89	28	Würth Electronics	30 to 75	12V/1A
750311423	17.7 × 14.0 × 12.7	50	570	4:1	4	90	12	Würth Electronics	30 to 75	5V/3A
750311457	17.7 × 14.0 × 12.7	50	600	4:1	3.7	115	12	Würth Electronics	30 to 75	5V/3A
750311689	17.7 × 14.0 × 12.7	50	600	4:1	3.7	115	12	Würth Electronics	30 to 75	5V/3A
750311458*	17.7 × 14.0 × 12.7	15	175	3:1	5	35	6	Würth Electronics	10 to 40	5V/2.5A
750311564	17.7 × 14.0 × 12.7	9	120	3:1	8	36	7	Würth Electronics	10 to 40	5V/3A
750311624	17.7 × 14.0 × 12.7	9	150	1.5:1	8	34	21	Würth Electronics	10 to 40	15V/1A
750311604	29.08 × 23.11 × 11.43	8	300	1:1	9.5	30	12	Würth Electronics	10 to 40	24V/1.3A
750311599	29.08 × 23.11 × 11.43	8	500	1.5:1	12	30	12	Würth Electronics	10 to 40	15V/2A
750311600	29.08 × 23.11 × 11.43	12	500	3:1	11	30	40	Würth Electronics	20 to 75	15V/2A
750311608	29.08 × 23.11 × 11.43	12	500	1.5:1	9	30	20	Würth Electronics	20 to 75	24V/1.3A
750311607	29.08 × 23.11 × 11.43	14	500	2.5:1	9.5	40	10	Würth Electronics	20 to 75	12V/2.5A
750311590	32.31 × 27.03 × 13.69	8	200	2:1	18	15	8	Würth Electronics	10 to 40	12V/3.8A
750311591	32.31 × 27.03 × 13.69	8	200	1.5:1	20	15	12	Würth Electronics	10 to 40	15V/3A
750311592	32.31 × 27.03 × 13.69	8	200	1:1	18	15	20	Würth Electronics	10 to 40	24V/1.9A
750311594	32.31 × 27.03 × 13.69	15	400	2.33:1	18	35	15	Würth Electronics	20 to 75	12V/3.8A
750311595	32.31 × 27.03 × 13.69	12	200	3:1	18	15	12	Würth Electronics	20 to 70	15V/3A
750311596	32.31 × 27.03 × 13.69	12	200	1.5:1	16	30	30	Würth Electronics	20 to 70	24V/1.9A
PA2367NL	17.7 × 14.0 × 12.7	85	750	2.7:1	1.7	325	26	Pulse Engineering	20 to 75	12V/1A
PA1276NL	17.7 × 14.0 × 12.7	77.4	800	1.47:1	1.6	100	75	Pulse Engineering	20 to 75	12V/1A
PA2467NL	17.7 × 14.0 × 12.7	37	750	2:1	2.9	89	28	Pulse Engineering	20 to 75	12V/1A
PA1260NL	17.7 × 14.0 × 12.7	77.4	800	3.67:1	1.5	220	18	Pulse Engineering	20 to 75	5V/2A
PA3177NL	29.21 × 21.84 × 11.43	8.3	100	2:1	8.6	10	7	Pulse Engineering	10 to 40	10V/2.5A

*2.5k isolation, others are rated for 1.5kV isolation.
†TARGET APPLICATION, NOT GUARANTEED.

Turns Ratio and RMS Diode Current

Note that when using an R_{FB}/R_{REF} resistor ratio to set output voltage, the user has relative freedom in selecting a transformer turns ratio to suit a given application. In contrast, simpler ratios of small integers (e.g., 1:1, 2:1, 3:2, etc.) can be employed to provide more freedom in setting total turns and mutual inductance.

While the turns ratio can be selected to maximize output power for a given current limit, minimizing the turns ratio and increasing the current limit will often increase efficiency and better utilize the saturation current of a given transformer. Figure 3 shows the maximum output power using three transformers with different windings ratios that have the same output inductance and peak output current, illustrating that increasing current while decreasing turns ratio can deliver more power.

There are two significant constraints on the turns ratio. First, as described in the previous section on limitations to output power, the drain of the MOSFET switch will see a voltage equal to the maximum input supply plus

APPLICATIONS INFORMATION

the output voltage multiplied by the windings ratio plus some amount of overshoot caused by leakage inductance. Second, increasing the turns ratio will increase the peak current seen on the output diode generally increasing the RMS diode current thereby lowering the efficiency. This efficiency limitation is worse at lower output voltages when the diode forward voltage is significant compared to the output voltage. In a typical application such as the 5V, 2A output shown on the back page, the diode losses dominate all the other losses, as shown in Figure 4. To calculate RMS diode current, two equations are needed—the first for calculating duty cycle, D, and the second to calculate the RMS current of a triangle waveform:

$$D = \frac{\left(V_{OUT} + V_{F(DODE)}\right) \bullet N_{PS}}{V_{IN} + \left(V_{OUT} + V_{F(DIODE)}\right) \bullet N_{PS}}$$

$$I_{DIODE(RMS)} = \sqrt{\frac{\left(I_{LIM} \bullet N_{PS}\right)^2 \bullet (1-D)}{3}}$$

For a more general analysis, Figure 5 illustrates a sweep of windings ratio on the x-axis while comparing output power and estimated efficiency for a 5V output using a 48V input. If the desired application required 20W, the maximum power curve indicates that a winding ratio of 12:1 would be sufficient at a current limit of 2A (R_{SENSE} = 0.05Ω), while a winding ratio of 5:1 would deliver the same power at 3A. However, when examining the corresponding efficiency at max load for those two windings ratios and current limits, the 5:1, 3A selection is clearly the superior solution with an estimated efficiency of 85% compared to 78% for the 12:1, 2A application.

There are several caveats to this evaluation. First, as the diode forward voltage becomes a smaller percentage of total loss at higher output voltages (>12V) the RMS current becomes less of a concern and minimizing it will have a much smaller impact on efficiency. More significantly, if a lower turns ratio forces the use of a diode with a larger forward drop to obtain a higher reverse voltage rating, any gains from minimizing current might be lost. For low output voltages (3.3V or 5V) or high input voltages (>48V), a turns ratio greater than one can be used with multiple primary windings relative to the secondary to maximize the transformer's current gain.

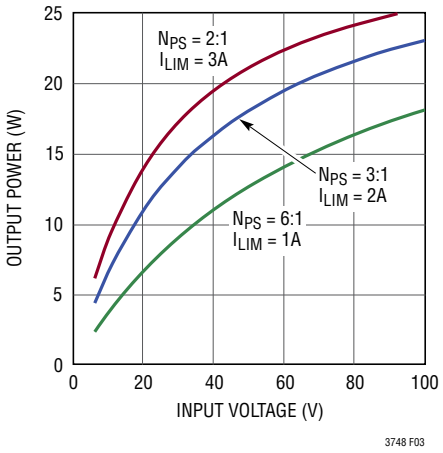


Figure 3. Maximum Output Power at 12V Out Using Three Transformers with Equal Peak Output Current and Secondary Inductance

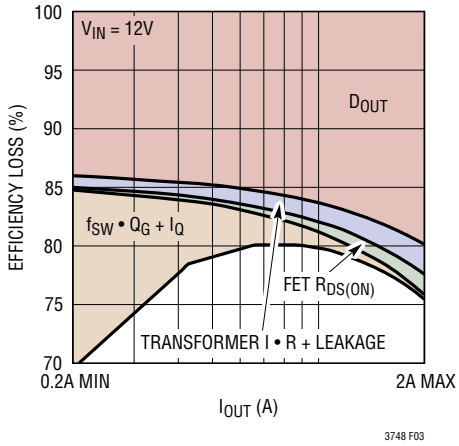


Figure 4. Sources of Loss In 5V, 2A Out Typical Application

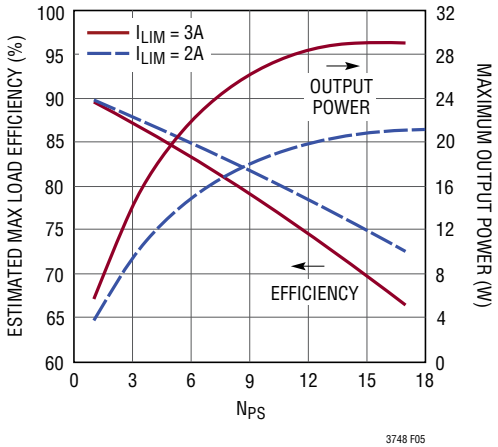


Figure 5. Estimated Efficiency and Output Power at $5V_{OUT}$ from $48V_{IN}$ vs Windings Ratio, N_{PS}, at 2A and 3A Current Limits

APPLICATIONS INFORMATION

Saturation Current

As discussed earlier in the Maximum Output Power section, because the core of the transformer is being used for energy storage in a flyback, the current in the transformer windings should not exceed their rated saturation current as energy injected once the core is saturated will not be transferred to the secondary and will instead be dissipated in the core. Information on saturation current should be provided by the transformer manufacturers and Table 1 lists the saturation current of the transformers designed for use with the LT3748.

Leakage Inductance and Snubbers

Transformer leakage inductance (on either the primary or secondary) causes a voltage spike to appear at the primary after the MOSFET switch turns off. This spike is increasingly prominent at higher load currents where more stored energy must be dissipated. Transformer leakage inductance should be minimized.

In most cases, proper selection of the external MOSFET and a well designed transformer will eliminate the need for snubber circuitry, but in some cases the optimal MOSFET may require protection from this leakage spike. An RC (resistor capacitor) snubber may be sufficient in applications where the MOSFET has significant margin beyond the predicted DC drain voltage applied in flyback while a clamp using an RCD (resistor capacitor diode) or a Zener might be a better option when using a MOSFET with very little margin for leakage inductance spiking.

The recommended approach for designing an RC snubber is to measure the period of the ringing at the MOSFET drain when the MOSFET turns off without the snubber and then add capacitance—starting with something in the range of 100pF—until the period of the ringing is 1.5 to 2 times longer. The change in period will determine the value of the parasitic capacitance, from which the parasitic inductance can be determined from the initial period, as well. Similarly, initial values can be estimating using stated switch capacitance and transformer leakage inductance. Once the value of the drain node capacitance and inductance is known, a series resistor can be added to the snubber capacitance to dissipate power and critically dampen the ringing. The equation for deriving the optimal series resistance using the observed periods (t_{PERIOD}, and $t_{PERIOD(SNUBBED)}$) and snubber capacitance ($C_{SNUBBER}$) is below, and the resultant waveforms are shown in Figure 6.

$$C_{PAR} = \frac{C_{SNUBBER}}{\left(\frac{t_{PERIOD(SNUBBED)}}{t_{PERIOD}}\right)^2 - 1}$$

$$L_{PAR} = \frac{t_{PERIOD}^2}{C_{PAR} \bullet 4\pi^2}$$

$$R_{SNUBBER} = \sqrt{\frac{L_{PAR}}{C_{PAR}}}$$

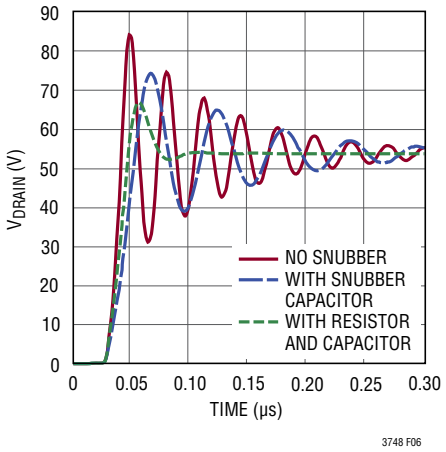


Figure 6. Observed Waveforms at MOSFET Drain when Iteratively Implementing an RC Snubber

Note that energy absorbed by a snubber will be converted to heat and will not be delivered to the load. In high voltage or high current applications, the snubber may need to be sized for thermal dissipation. To determine the power dissipated in the snubber resistor from capacitive losses, measure the drain voltage immediately before the MOSFET turns on and use the following equation relating that voltage and the MOSFET switching frequency to determine the expected power dissipation:

$$P_{SNUBBER} = f_{SW} \bullet C_{SNUBBER} \bullet V_{DRAIN}^2/2$$

Decreasing the value of the capacitor will reduce the dissipated power in the snubber at the expense of increased peak voltage on the MOSFET drain, while increasing the value of the capacitance will decrease the overshoot.

APPLICATIONS INFORMATION

Although it typically does not decrease efficiency, leakage inductance energy that would normally have been dissipated in the switch or transformer is also dissipated in the RC snubber resistor and can be calculated as:

$$P_{SNUBBER} = f_{SW} \bullet L_{LEAK} \bullet I_{LIM}^2/2$$

An RCD clamp, shown in Figure 7, also prevents the leakage inductance spike from exceeding the breakdown voltage of the MOSFET switch. In most applications, there will be a very fast voltage spike caused by a slow clamp diode. Once the diode clamps, the leakage inductance current is absorbed by the clamp capacitor. This period should not last longer than 200ns so as not to interfere with the output regulation. The clamp diode turns off after the leakage inductance energy is absorbed and the switch voltage is then equal to:

$$V_{DS} = V_{IN} + N_{PS} \bullet (V_{OUT} + V_{F(DIODE)})$$

Schottky diodes are typically the best choice for use in a snubber, but some PN diodes can be used if they turn on fast enough to limit the leakage inductance spike. Figures 8 and 9 show the waveform at the drain of the MOSFET switch for the 48V output application shown in Figure 17 at maximum rated load and maximum input voltage with an RC snubber and RCD clamp, respectively. Both solutions limit the leakage spike to less than 190V, below the 200V $V_{DS(MAX)}$ rating of the Si7464DP MOSFET.

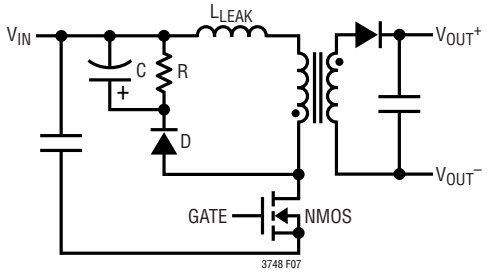


Figure 7. RCD Clamp

Leakage Inductance and Output Diode Stress

The output diode may also see increased reverse voltage stresses from leakage inductance. While it nominally sees a reverse voltage of the input voltage divided by the windings ratio plus the output voltage when the MOSFET power switch turns on, the capacitance on the output diode and the leakage inductance will cause an LC tank which may ring beyond that expected reverse voltage. An RC snubber or RCD clamp may be implemented to reduce the voltage spike if it is desirable to use a lower reverse voltage diode.

Secondary Leakage Inductance

In addition to the previously described effects of leakage inductance in general, leakage inductance on the secondary in particular exhibits an additional phenomena. It forms an inductive divider on the transformer secondary that effectively reduces the size of the primary-referred flyback pulse used for feedback. This will increase the output voltage target by a similar percentage. Note that, unlike leakage spike behavior, this phenomena is load independent. To the extent that the secondary leakage inductance is a constant percentage of mutual inductance

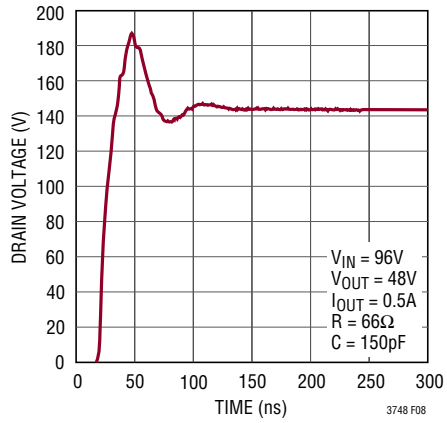


Figure 8. Waveform of MOSFET Drain During Normal Operation of Figure 19 with RC Snubber (as Drawn)

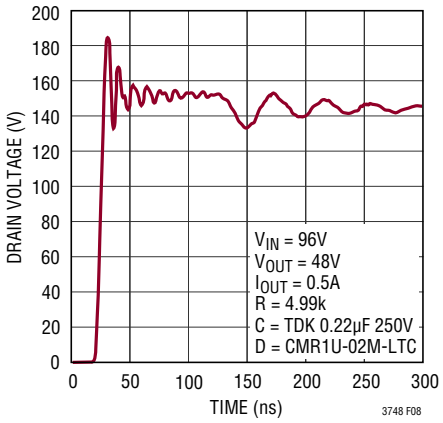


Figure 9. Waveform of MOSFET Drain During Normal Operation of Figure 19 Using RCD Clamp with Central Semiconductor CMR1U-02M-LTC Instead of RC Snubber

APPLICATIONS INFORMATION

(over manufacturing variations), this can be accommodated by adjusting the R_{FB}/R_{REF} resistor ratio.

Winding Resistance Effects

Resistance in either the primary or secondary will reduce overall efficiency (P_{OUT}/P_{IN}). Good output voltage regulation will be maintained independent of winding resistance due to the boundary mode operation of the LT3748.

Bifilar Winding

A bifilar, or similar winding technique, is a good way to minimize troublesome leakage inductances. However, remember that this will also increase primary-to-secondary capacitance and limit the primary-to-secondary breakdown voltage, so, bifilar winding is not always practical. The Linear Technology Applications group is available and extremely qualified to assist in the selection and/or design of the transformer.

Selecting a Current Sense Resistor

The external current sense resistor allows the user to optimize the current limit behavior for the particular application under consideration. As the current sense resistor is varied from several ohms down to tens of milliohms, peak switch current goes from a fraction of an ampere to tens of amperes. Care must be taken to ensure proper circuit operation, especially with small current sense resistor values.

For example, a peak MOSFET switch current of 4A requires a sense resistor of 0.025Ω. Note that the instantaneous peak power in the sense resistor is 1W, and it must be rated accordingly. The LT3748 has only a single sense line to this resistor. Therefore, any parasitic resistance in the ground side connection of the sense resistor will increase its apparent value. In the case of a 0.025Ω sense resistor, 1mΩ of parasitic resistance will cause a 4% reduction in peak switch current. Therefore, resistance of printed circuit copper traces and vias cannot necessarily be ignored.

Another issue for proper operation of the current sense circuitry is avoiding prematurely tripping the SENSE threshold while slewing the MOSFET drain when the GATE pin goes high. The LT3748 does not begin to compare the SENSE pin voltage with the target threshold until the GATE pin is near its final value, or until at least 150ns has passed, whichever occurs more slowly. This should be entirely sufficient for most applications but premature tripping of the SENSE comparator may occur in cases where a MOSFET with very high Q_G is used with a series resistor at the GATE pin.

Output Short Circuits and SENSE Pin Over Current

The LT3748 has an internal threshold to detect when primary inductor current exceeds the programmed range. This can result from an inductive output short-circuit and an output voltage below zero, reflecting a voltage back to the primary side of the transformer which, in turn, causes the LT3748 to turn the external MOSFET on before the secondary current has discharged. When the voltage at the SENSE pin exceeds approximately 130mV—equivalent to 30% higher than the programmed $I_{LIM(MAX)}$ in the R_{SENSE} resistor—the SS pin will be reset, stopping switching. Once the soft-start capacitor is recharged and the soft-start threshold is reached, switching will resume at the minimum current limit.

High Drain Capacitance and Low Current Operation

When designing applications with some combination of a low current limit ($I_{LIM} < 1A$), a high secondary-to-primary turns ratio ($N_{PS} << 1$), multiple output windings, or very capacitive output diodes, it is important to minimize the capacitance reflected onto the primary winding and on the drain of the external MOSFET. After the MOSFET turns off during each switching cycle, the primary current charges that capacitance to slew the MOSFET drain until the secondary begins to deliver power, and if the drain node does not slew and remain above V_{IN} within approximately 200ns once the GATE pin goes low and the MOSFET turns off, the LT3748 may detect that the current in the secondary is zero and turn the MOSFET back on prematurely, causing the LT3748 to switch continuously while delivering very little power to the output. The result will be droop of the output voltage at lighter loads and oscillation at the V_C node. This problem can be prevented by maximizing N_{PS} (minimizing ratio of secondary windings to primary windings), increasing the peak drain current (minimizing R_{SENSE}), and minimizing the output diode and transformer capacitance.

APPLICATIONS INFORMATION

Soft-Start

The LT3748 contains an optional soft-start function that is enabled by connecting an explicit external capacitor between the SS pin and ground. Internal circuitry prevents the control voltage at the V_C pin from exceeding that on the SS pin.

The soft-start function is engaged whenever power at V_{IN} is removed, or as a result of either undervoltage lockout, overcurrent in the sense resistor or thermal (overtemperature) shutdown. The SS node is then discharged to roughly 600mV. When this condition is removed, a nominal 5µA current acts to charge up the SS node towards roughly 2.2V. For example, a 0.1µF soft-start capacitor will place a 0.05V/ms limit on the turn-on ramp rate at the V_C node.

ENABLE and Undervoltage Lockout (UVLO)

A resistive divider from V_{IN} to the EN/UVLO pin implements undervoltage lockout (UVLO). The EN/UVLO pin threshold is set at 1.223V. In addition, the EN/UVLO pin draws 2.4µA when the voltage at the pin is below 1.223V. This current provides user programmable hysteresis based on the value of R1. The effective UVLO thresholds are:

$$V_{IN(UVLO,RISING)} = \frac{1.223V \bullet (R1+R2)}{R2} + 2.4\mu A \bullet R1$$

$$V_{IN(UVLO,FALLING)} = \frac{1.223V \bullet (R1+R2)}{R2}$$

Figure 10 shows the implementation of external shutdown control while still using the UVLO function. The NMOS grounds the EN/UVLO pin when turned on, and puts the LT3748 in shutdown with a quiescent current draw of less than 1µA.

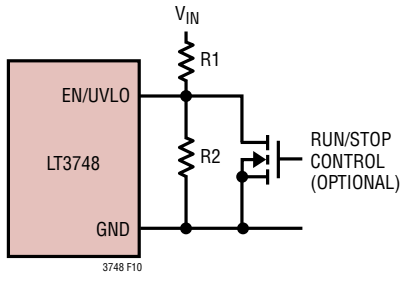


Figure 10. Undervoltage Lockout (UVLO)

Minimum Load Requirement

The LT3748 recovers output voltage information using the flyback pulse that occurs once the external MOSFET turns off and the secondary winding conducts current. In order to regulate the output voltage, the LT3748 needs to sample the flyback pulse. The LT3748 delivers a minimum amount of energy even during light load conditions to ensure accurate output voltage information. The minimum delivery of energy creates a minimum load requirement on the output of approximately 2% of maximum load. The minimum operating frequency at minimum load is approximately 42kHz.

Alternatively, a Zener diode sufficiently rated to handle the minimum load power can be used to provide a minimum load without decreasing efficiency in normal operation. In selecting a Zener diode for this purpose, the Zener voltage should be high enough that the diode does not become the load path during transient conditions but the voltage must still be low enough that the MOSFET and output voltage ratings are not exceeded when the Zener functions as the minimum load.

$INTV_{CC}$ Pin Considerations

The $INTV_{CC}$ pin powers the internal circuitry and gate driver of the LT3748. Three unique configurations exist for regulation of the $INTV_{CC}$ pin as shown in Figure 11. In the first configuration, the internal LDO drives the $INTV_{CC}$ pin internally from the V_{IN} supply. In the second configuration, the V_{IN} supply directly drives the $INTV_{CC}$ pin through a direct connection bypassing the internal LDO. Use this optional configuration for voltages lower than 20V. In the third configuration, an external supply or third winding drives the $INTV_{CC}$ pin. Use this option when a voltage supply exists lower than the input supply but higher than the regulated $INTV_{CC}$ voltage. Using a lower voltage supply provides a more efficient source of power for internal circuitry and reduces power dissipation in the LT3748.

When calculating the minimum input voltage required for a valid $INTV_{CC}$, or the power dissipated in the LT3748, it is useful to know how much current will be drawn from the $INTV_{CC}$ LDO during normal operation. The easiest way to calculate this current is to use the gate charge (Q_G) for the selected MOSFET switch at the expected V_{IN} and $INTV_{CC}$

APPLICATIONS INFORMATION

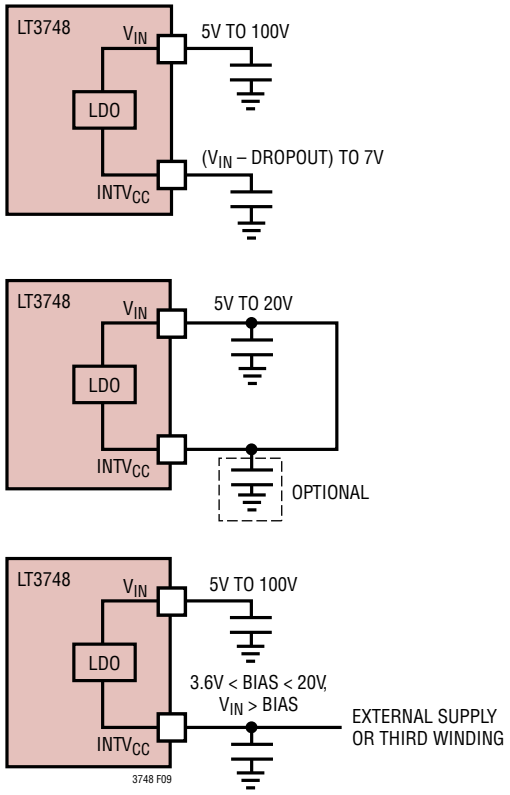


Figure 11. $INTV_{CC}$ Pin Configurations

voltages and multiply that charge required with each turn-on event by the maximum operating frequency. The maximum operating frequency in a given application can be approximated from the primary transformer inductance, the windings ratio (N_{PS}), the nominal output voltage and the maximum input voltage. Unless the part is limited by minimum on- or off-times, this maximum frequency will occur when the part is regulating in boundary mode at the minimum peak switch current, and can be derived from:

$$f_{SW(MAX)} \approx \frac{V_{IN(MAX)} \bullet \left(V_{OUT} + V_{F(DIODE)}\right) \bullet N_{PS}}{L_{PRI} \bullet I_{LIM(MIN)} \bullet \left(\left(V_{OUT} + V_{F(DIODE)}\right) \bullet N_{PS} + V_{IN(MAX)}\right)}$$

With the maximum $INTV_{CC}$ current calculated, the expected dropout when V_{IN} drops below 7V can be extracted from the curves in the Typical Performance Characteristics section. The LT3748 is tested as low as V_{IN} = 5V but the hard limit on minimum V_{IN} operation is the $INTV_{CC}$ regulator dropout and the 3.6V under voltage lockout. Figure 12 illustrates an example where operation with V_{IN} = 5V and I_{INTVCC} = 20mA might be fully functional at room

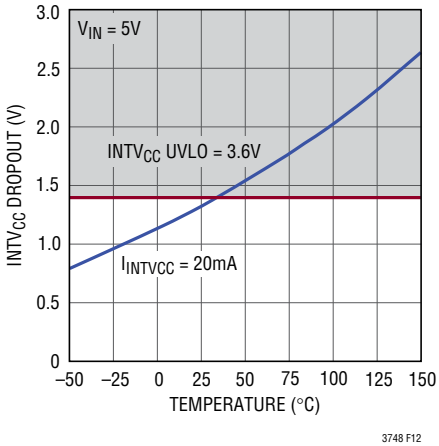


Figure 12. $INTV_{CC}$ Current at Low V_{IN} Can Cause the LT3748 to Stop Switching Due to $INTV_{CC}$ Undervoltage Lockout

temperature, but when the dropout for the same current exceeds 1.4V and trips the UVLO at higher temperatures the LT3748 will stop switching.

Overdriving $INTV_{CC}$ with a Third Winding

The LT3748 provides excellent output voltage regulation without the need for an opto-coupler or third winding, but for some applications with input voltages greater than 20V, an additional winding may improve overall system efficiency. The third winding should be designed to output a voltage between 7.2V and 20V. A resistor in series with the rectifier is recommended to absorb leakage spikes. For a typical 48V_{IN}, 10W application, overdriving the $INTV_{CC}$ pin may improve efficiency by several percent at maximum load and as much as 30% at light loads.

Loop Compensation

The LT3748 is compensated using an external resistor-capacitor network on the V_C pin. Typical values are in the range of R_C = 50k and C_C = 1nF (see the numerous schematics in the Typical Applications section for other possible values). If too large of an R_C value is used, the part will be more susceptible to high frequency noise and jitter. If too small of an R_C value is used, the transient performance will suffer. The value choice for C_C is somewhat the inverse of the R_C choice: if too small a C_C value is used, the loop may be unstable and if too large a C_C value is used, the transient performance will also suffer. Transient response plays an important role for any DC/DC converter.

APPLICATIONS INFORMATION

Synchronous Secondary Applications

Using a synchronous secondary controller such as the LT8309 with the LT3748 is an excellent method to boost converter efficiency and minimize heat, especially for lower output voltages and higher output currents. However, there are some important details to understand when designing a synchronous application. First, although the LT8309 controls a synchronous MOSFET in place of the standard output rectifier, when properly configured that synchronous MOSFET must turn off before the end of the secondary conduction time. This ensures that there is no reverse current sending power back to the primary side of the transformer and no cross conduction once the LT3748 GATE pin goes high on the next switching cycle. As a result, the forward voltage drop of the secondary MOSFET body diode is reflected back to the primary side and sampled by the LT3748. In order to guarantee an accurate sample and to maintain excellent line and load regulation, the RDRAIN resistor of the LT8309 must be optimized to allow the body diode to conduct long enough to provide an accurate reflected voltage. To ensure accurate output regulation the secondary MOSFET should turn off at least 180ns before the secondary current goes to zero. Figure 13 illustrates the expected waveform at the primary side drain node and the LT8309 GATE pin using the circuit from Figure 21 with sufficient body diode conduction time marked.

Because the body diode is conducting at the sampling point for the LT3748 when the secondary current goes to zero, the temperature coefficient of this body diode should be compensated using the TC pin using the same procedures outlined when a normal rectifier is used on the secondary. The silicon junction of the body diode has a negative temperature coefficient comparable to a standard or Schottky diode and standard values specified earlier in the applications section should be a good starting point.

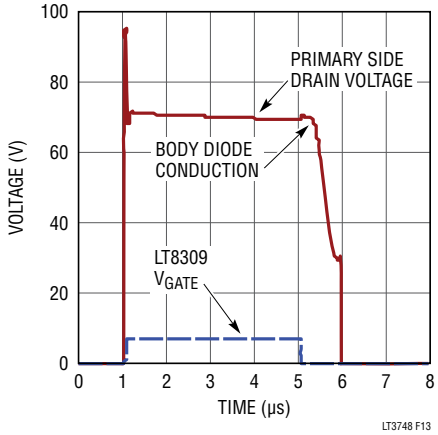


Figure 13. Waveforms at LT3748 Primary Side MOSFET Drain and LT8309 GATE Pin During Operation Illustrating Optimum Body Diode Conduction Time

APPLICATIONS INFORMATION

DESIGN EXAMPLE: 12V_{IN} TO 5V, 2A OUT

The first example is an automotive application shown on the back page of this data sheet—a nominal 12V_{IN}, 5V_{OUT} at 2A with an operating input voltage range of 6V to 45V with a design focus of maximizing efficiency.

1. Select Transformer Turns Ratio

Transformer turns ratio will affect the requirements for the MOSFET switch V_{DS} rating, the output diode reverse bias rating, the output power capability, and the efficiency of the overall converter. Because the output voltage is low compared to the forward drop on the output diode and the currents are high in this application, efficiency can be optimized by minimizing the RMS diode current. Typical efficiency in a variety of applications will be 85% to 90% and due to compromises made for the wide input voltage range and the low output voltage in this specific application, an efficiency of 85% is assumed for calculating output power. This assumption can be revised once the application is tested. Equations for evaluating each of the important criteria are:

$N_{PS} = N_P/N_S$

$V_{DS(MAX)} \geq V_{IN(MAX)} + V_{OUT} \bullet N_{PS}$

$V_{R(DIODE)} \geq V_{IN(MAX)}/N_{PS} + V_{OUT}$

$I_{OUT(MAX)} \approx 0.85 \bullet (1 - D) \bullet N_{PS} \bullet I_{LIM}/2$

$D = (V_{OUT} + V_{F(DIODE)}) \bullet N_{PS}/(V_{IN} + (V_{OUT} + V_{F(DIODE)}) \bullet N_{PS})$

$I_{DIODE(RMS)} = \sqrt{(I_{LIM} \bullet N_{PS})^2 \bullet (1 - D)/3}$

The equation for output power can be rearranged to solve for the current limit, I_{LIM}, which can be solved at the nominal or the minimum V_{IN} depending on application requirements. In this application the 2A load requirement will be set at V_{IN} = 7.5V to reduce operating stresses at higher input voltages. The results of the aforementioned equations in this application are found in Table 2.

Evaluating the results of the table, the 1:2 turns ratio looks demanding in terms of diode reverse-voltage requirements (a diode with higher reverse bias capability generally will have a larger forward drop and therefore lower application efficiency) and primary side currents and only decreases the output diode RMS current by 13% from the 1:1 case. However, on evaluating the minimum and maximum inductance requirements in Step 3, even the 1:1 case does not allow for enough on-time from maximum V_{IN} for the range of inductance that provides sufficient off-time. For that reason, a 2:1 turns ratio is selected, easing the requirement on the output diode reverse voltage rating in the process.

2. Calculate Sense Resistor Value

The sense resistor can be calculated by the following equation:

$$R_{SENSE} = \frac{100mV}{I_{LIM}}$$

The desired 5.8A current limit leads to an unusual value of 0.0172Ω, so the current limit is increased to use a more standard 0.016Ω value and I_{LIM} of 6.25A.

3. Select a Transformer Based on Inductance and Saturation Current Requirements

The transformer in this application will be selected to optimize efficiency at a 80kHz minimum switching frequency at maximum load from the nominal input voltage. In applications where transformer size is the primary requirement, reducing the current limit or increasing the switching frequency may be required. The following equations select the inductance required for a given switching frequency at max load and then verify that the inductance is large enough to satisfy the minimum on and minimum sampling times of the LT3748.

Table 2. Voltage Stresses, Output Capability and Diode Current vs Turns Ratio in 12V_{IN} to 5V, 2A Application

N_{PS}	$V_{DS(MAX)}$	$V_{R(DIODE)}$	D (V_{IN} = 12V)	D (V_{IN} = 7.5V)	I_{LIM} (2A OUT AT V_{IN} = 7.5V)	$I_{DIODE(RMS)}$ (V_{IN} = 12V)
0.5	47.5	95	0.19	0.27	12.9	3.3
1	50	50	0.31	0.42	8.2	3.9
2	55	27.5	0.48	0.59	5.8	4.8
3	60	20	0.58	0.69	5.0	5.6

APPLICATIONS INFORMATION

$$L_{PRI} \leq V_{IN(MIN)} \bullet (V_{OUT} + V_{F(DIODE)}) \bullet N_{PS}/(f_{SW(MIN)} \bullet I_{LIM} \bullet (V_{OUT} + V_{F(DIODE)}) \bullet N_{PS} + V_{IN(MIN)}))$$

$$L_{PRI} \geq (V_{OUT} + V_{F(DIODE)}) \bullet R_{SENSE} \bullet 400ns \bullet N_{PS}/15mV$$

$$L_{PRI} \geq V_{IN(MAX)} \bullet R_{SENSE} \bullet 200ns/15mV$$

For this application, the primary inductance with a 2:1 transformer and a 0.016Ω sense resistor for an 6.25A current limit is bounded by the minimum desired switching frequency and the minimum off time requirement to be between 9.6µH and 11.5µH. Looking at Table 1, there are no transformers that fit that exact requirement. For the sake of prototyping, a transformer with slightly less than the desired primary inductance is selected with the PA3177NL. The application will need to be tested thoroughly for stability at higher input voltages and when the current limit is at a minimum (in the middle of the output load range). The easiest solution to ease the requirement on minimum on-time is to reduce the maximum V_{IN} voltage although alternatively N_{PS} could be increased at the expense of efficiency (and requiring a more thorough redesign).

4. Select a MOSFET Switch

The selected 2:1 transformer requires a nominal 55V rating on the MOSFET switch, assuming no leakage inductance. However, even a small amount of leakage inductance may cause the drain to ring to double the anticipated voltage, and generally this needs to be verified in the final design. However, at currents below 10A it is fairly easy to find a MOSFET with sufficiently low $R_{DS(ON)}$ to be a very small contributor to maximum load efficiency losses while similarly having a low enough Q_G to require minimum current and minimal losses when driving the MOSFET at lighter loads. Also, while considering the efficiency gains and losses with a given MOSFET, it is important to realize that a trade-off in $R_{DS(ON)}$ for $V_{DS(MAX)}$ may backfire if a snubber needs to be added to the circuit to meet the voltage requirements and dissipates more energy than the difference in switch resistance. For that reason, a Vishay Si7738 is selected to give lots of margin with its 150V rating. The RMS current in the MOSFET can be calculated, squared and multiplied by the $R_{DS(ON)}$ to calculate losses and the current required to drive the FET at frequency can be determined, by the following equations:

$$I_{MOSFET(RMS)} = \sqrt{I_{LIM}^2 \bullet D/3}$$

$$I_{INTVCC} = f_{SW} \bullet Q_G$$

$$P_{INTVCC} = I_{INTVCC} \bullet (V_{IN} - V_{INTVCC})$$

In this application the MOSFET RMS current at maximum load is about 2.7A, which into the 0.038Ω $R_{DS(ON)}$ will be 0.28W, or on the order of 2% loss in efficiency. Assuming that the maximum operating frequency is around four times higher than the maximum load frequency (at about a quarter the output load) and reading the approximate Q_G at 7V operation from the Vishay data sheet, the approximate $INTV_{CC}$ current is likely close to 8mA, dissipating 0.04W when the load is on the order of 2.5W, or less than 2%, and much less at maximum load.

5. Select the Output Diode

The output diode reverse voltage, as calculated earlier, is the first important specification for the output diode. As with the MOSFET, choosing a diode with enough margin should preclude the use of a snubber. The second criterion is the power requirement of the diode which is more difficult to correctly ascertain—some manufacturers give direct data about power dissipation versus duty cycle, which can be used with the data from the table to determine. To avoid using a snubber, a diode with a 60V reverse-bias capability and minimal forward drop was selected—in this case, the Diodes Inc. SBR 8U60P5. In this particular application where maximizing efficiency is the goal, minimizing the maximum voltage requirement on V_{IN} may allow the use of a diode with a lower reverse bias rating and a lower forward drop which could further increase efficiency. Alternatively, if no efficient diode is available for a particular reverse bias rating, it may be more beneficial to increase the windings ratio until a diode with low forward drop can be selected and then reevaluate whether that solution with higher RMS diode current is beneficial.

APPLICATIONS INFORMATION

6. Select the Feedback Resistor for Proper Output Voltage

Using the iterative process laid out earlier in the Applications Information section, select the feedback resistor R_{FB} and program the output voltage to 5V. Adjust the R_{TC} resistor for temperature compensation of the output voltage. R_{REF} is selected as 6.04k.

7. Select the Output Capacitor

The output capacitor should be chosen to minimize the output voltage ripple while considering the increase in size and cost of a larger capacitor. The following equation calculates the output voltage ripple:

$$\Delta V_{MAX} = \frac{L_{PRI} \bullet I_{LIM}^2}{2 \bullet C_{OUT} \bullet V_{OUT}}$$

8. Add Snubber Circuitry as Necessary

With the primary components selected, the application should be constructed to evaluate ringing at the drain of the MOSFET switch and to evaluate step response to optimize the compensation network. If using an RC snubber, the equations from the Applications Information section can be used or a rough estimate of component values may come from using the published leakage inductance of the transformer and selecting a snubber capacitor ranging from 1 to 3 times larger than the published MOSFET output capacitance. In this application, the peak MOSFET drain voltage was measured at maximum load from minimum V_{IN} and exceeded the 150V rating of the Si7738. A DZ clamp was considered in order to maximize efficiency but was unable to turn on fast enough to sufficiently clamp the very fast leakage spike. The final solution is an RC snubber, implemented iteratively, that decreases efficiency by less than 1% across the majority of the output load range while reducing the worst-case drain voltage spike to just 80V. Similarly, the anode of the output diode is probed to look at potential ringing when the MOSFET switch turns on and a peak of 45V is measured across the diode. Therefore, no snubber circuitry is required.

9. Optimize the Compensation Network

To set the compensation, the application is first configured with a 22nF capacitor and 10k resistor as a starting point. A load step is applied at both light and heavy loads at the 60V maximum input voltage and the capacitance is decreased until damping decreases to the desired limit, in this case with a compensation capacitance of 2.2nF and a response implying about 60° of phase margin. After verifying stability at the minimum input voltage, as well, the compensation capacitance is doubled for safety margin. The series resistance is varied from 5k to 50k but the optimal response is observed with 24.7k. For best ripple performance, select a compensation capacitor not less than 1nF, and select a compensation resistor not greater than 50k.

10. Soft-Start Capacitor and UVLO Resistor Divider

A soft-start capacitor helps during the start-up of the flyback converter. Select the UVLO resistor divider for the intended input operation range. These equations are aforementioned.

APPLICATIONS INFORMATION

DESIGN EXAMPLE: 48V_{IN} TO 12V, 2A OUT

The second example is a telecom application shown on the front page of the datasheet. The focus of this application is a cheap, small and simple solution. Table 3 shows the results of the initial step for selecting the turns ratio.

In this example, the output diode is a much smaller efficiency loss due to the smaller voltage drop across it in ratio to V_{OUT} so minimizing output diode current is not as important. Of greater importance is minimizing the stresses on the MOSFET and output diode and the 4:1 case seems to be the best compromise for that to avoid using a snubber on either device.

20µH of primary inductance is required for minimum off-time while selecting the transformer, but in order to minimize output ripple at maximum load a 60.8µH transformer is selected. To meet the saturation current (12A, peak, on the secondary windings), a Versa-Pak VP4-0047-R provides a compact and efficient solution.

For the MOSFET switch, since the input voltage is so high, resistive losses on the primary side will be very low so minimizing $R_{DS(ON)}$ is of minimum benefit. However, since the current for the gate drive is pulled from a high V_{IN}, minimizing both Q_G and operating frequency is essential unless a third winding is added. The Vishay Si7464DP, with a 200V $V_{DS(MAX)}$ and low gate charge, keeps the $INTV_{CC}$ current to just over 3mA, worst-case, which when added to quiescent current will keep power dissipation in the LT3748 to just over 1/4W at 72V V_{IN}.

The output diode only nominally has 30V of reverse bias but a B360 diode is selected to ensure enough margin that a snubber will not be required. A more expensive diode with lower forward drop might recover several percent efficiency and if high temperature operation is required a diode rated for more average current at temperature might be needed, but the B360 is small and inexpensive.

The rest of the design and component selection is straightforward.

Suggested Layout

See Figures 14 and 15 for the DC1557A demo board layout. Note the proximity of the R_{REF} and R_{FB} resistors (R9, R5) to the LT3748 for optimal regulation. The location of these two resistors as close to the physical pins of the LT3748 is critical for accurate regulation. In addition, the high frequency current path from the V_{IN} bypass capacitor (C2) through the primary-side winding, the MOSFET switch and sense resistor (R10) is a very tight loop. Similarly, the high frequency current path for the MOSFET gate switching from the $INTV_{CC}$ capacitor through the source of the MOSFET and sense resistor is similarly small in area. For improved regulation it is recommended that the user ensure that the high current ground is kept separate or at least physically isolated from the small-signal ground used by the other ground-referenced pins.

Table 3. Voltage Stresses, Output Capability and Diode Current vs Turns Ratio in 48V_{IN} to 12V, 2A Application

N_{PS}	$V_{DS(MAX)}$	$V_{R(DIODE)}$	D (V_{IN} = 48V)	D (V_{IN} = 36V)	I_{LIM} (2A OUT AT V_{IN} = 36V)	$I_{DIODE(RMS)}$ (V_{IN} = 48V)
1	84	84	0.21	0.26	6	3.3
2	96	48	0.34	0.41	4	3.7
4	120	30	0.51	0.58	3	4.6
6	144	24	0.61	0.68	2	5.2

APPLICATIONS INFORMATION

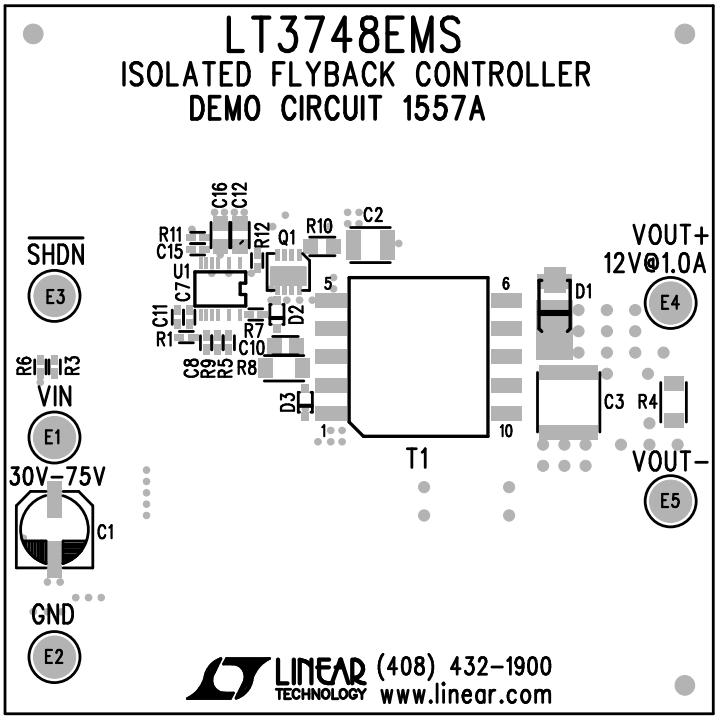


Figure 14. Demo Board Topside Silkscreen

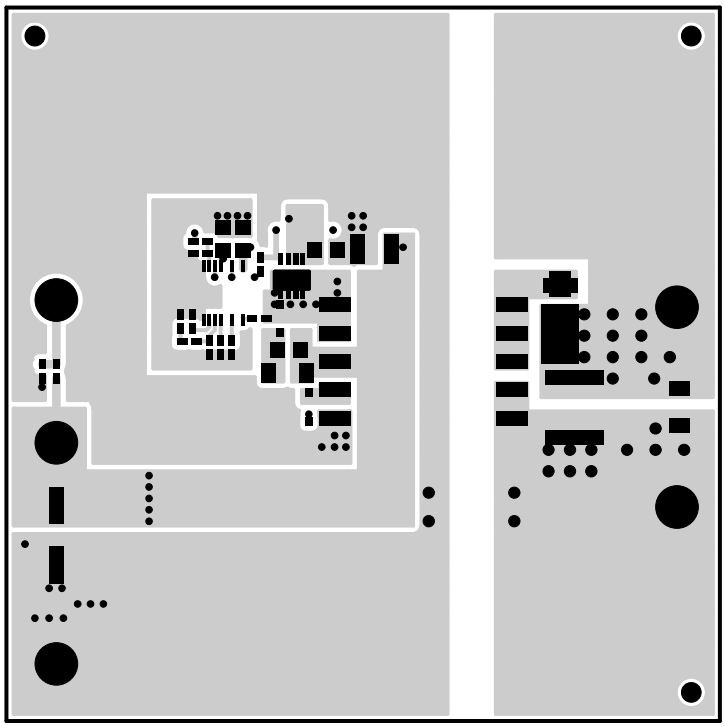


Figure 15. Demo Board Topside Metal

TYPICAL APPLICATIONS

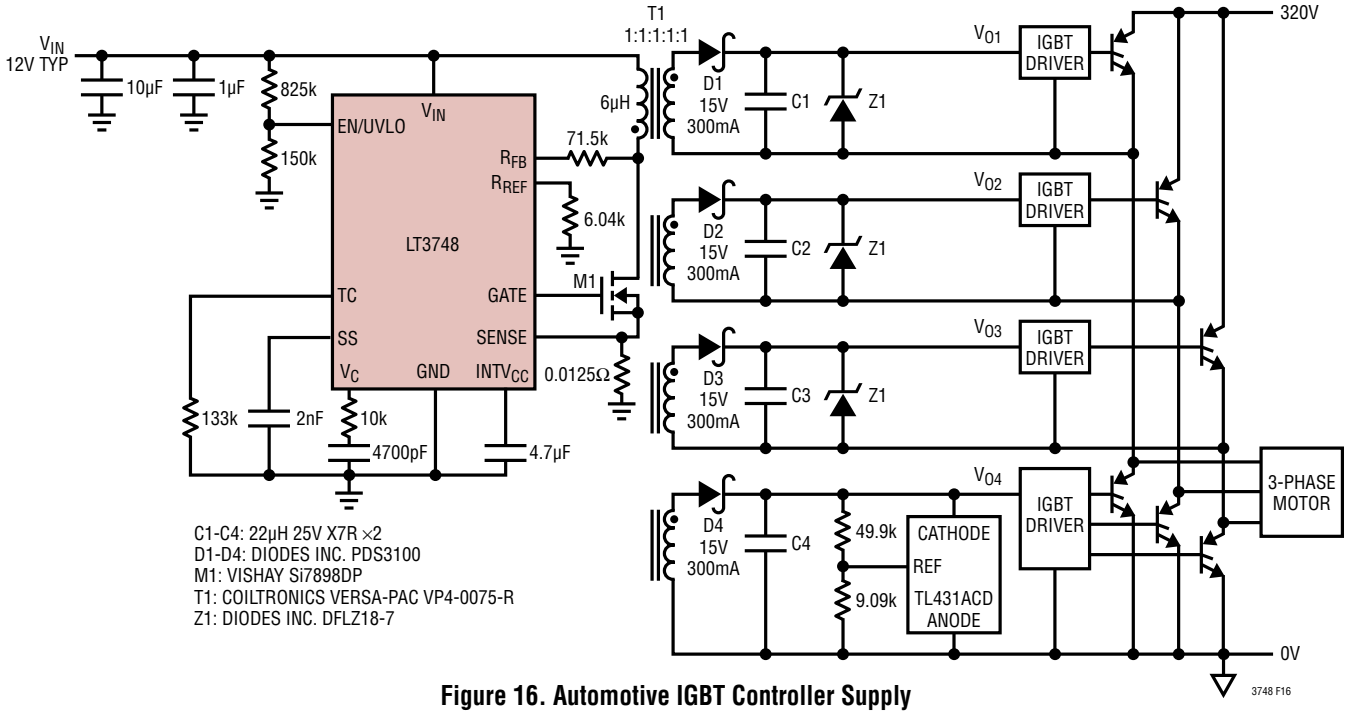


Figure 16. Automotive IGBT Controller Supply

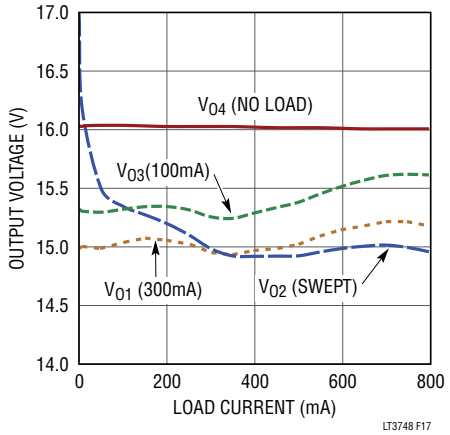
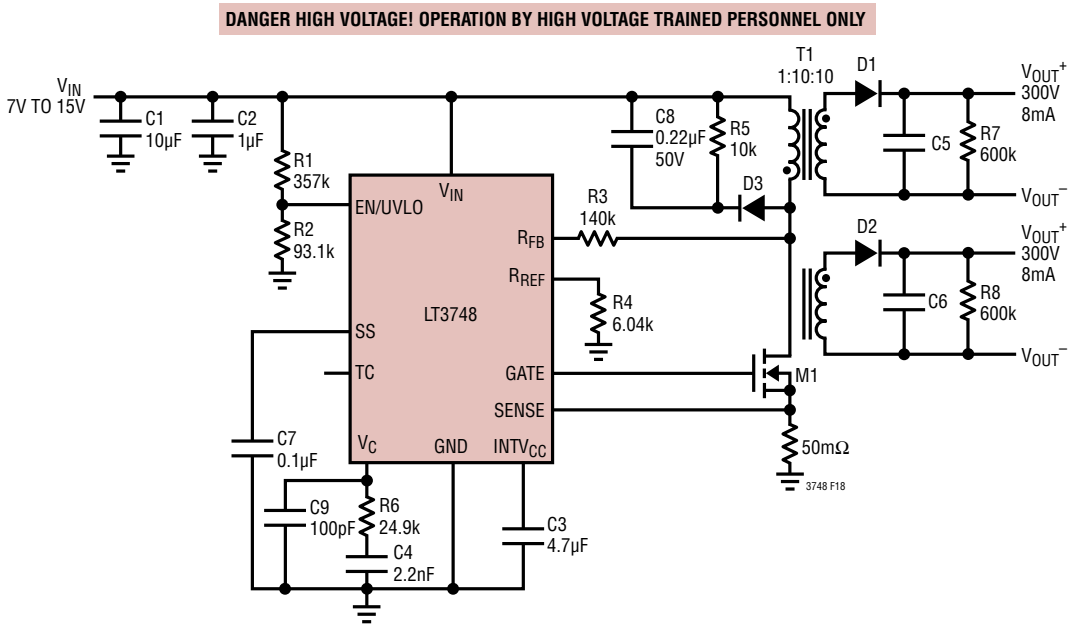


Figure 17. Cross Regulation Performance of the Supply in Figure 16 with V_{O1} and V_{O3} Loaded with V_{O2} Swept

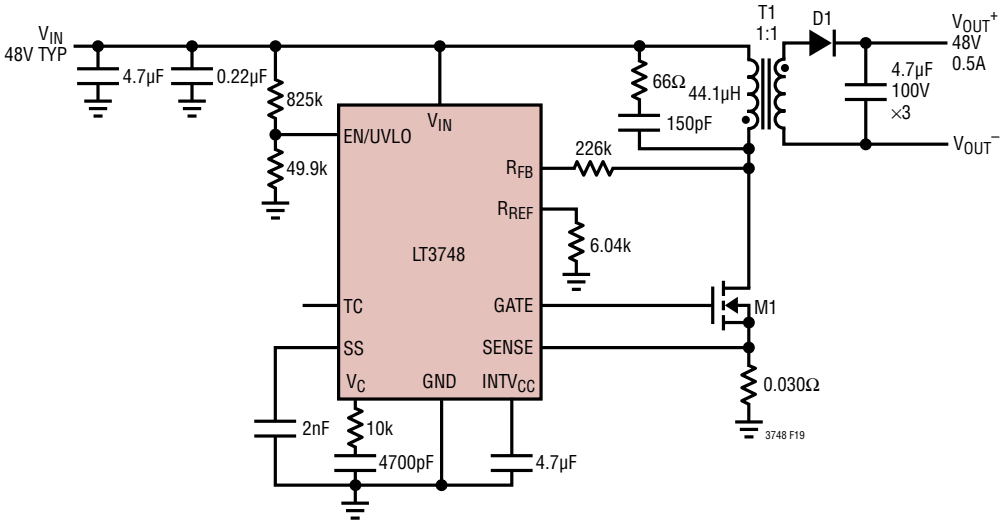
TYPICAL APPLICATIONS



C5, C6: 0.1µF 600V ×2
D1, D2: CENTRAL SEMICONDUCTOR CMR1U-06M LTC
M1: FAIRCHILD FDM3622
T1: WÜRTH ELEKTRONIK 750311486
D3: CENTRAL SEMICONDUCTOR CMMR1U-02

Figure 18. ±300V Isolated Flyback Converter

TYPICAL APPLICATIONS



D1: CENTRAL SEMICONDUCTOR CMR5U-02-LTC
M1: VISHAY Si7464DP
T1: COILTRONICS VERSA-PAC VP4-0060-R

Figure 19. 48V, 0.5A Supply from 24V to 96V Input

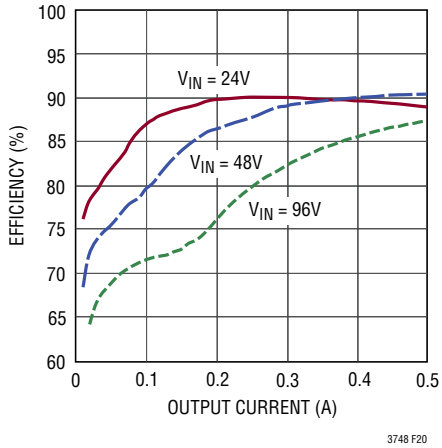


Figure 20. Efficiency of 48V Supply of Figure 17

TYPICAL APPLICATIONS

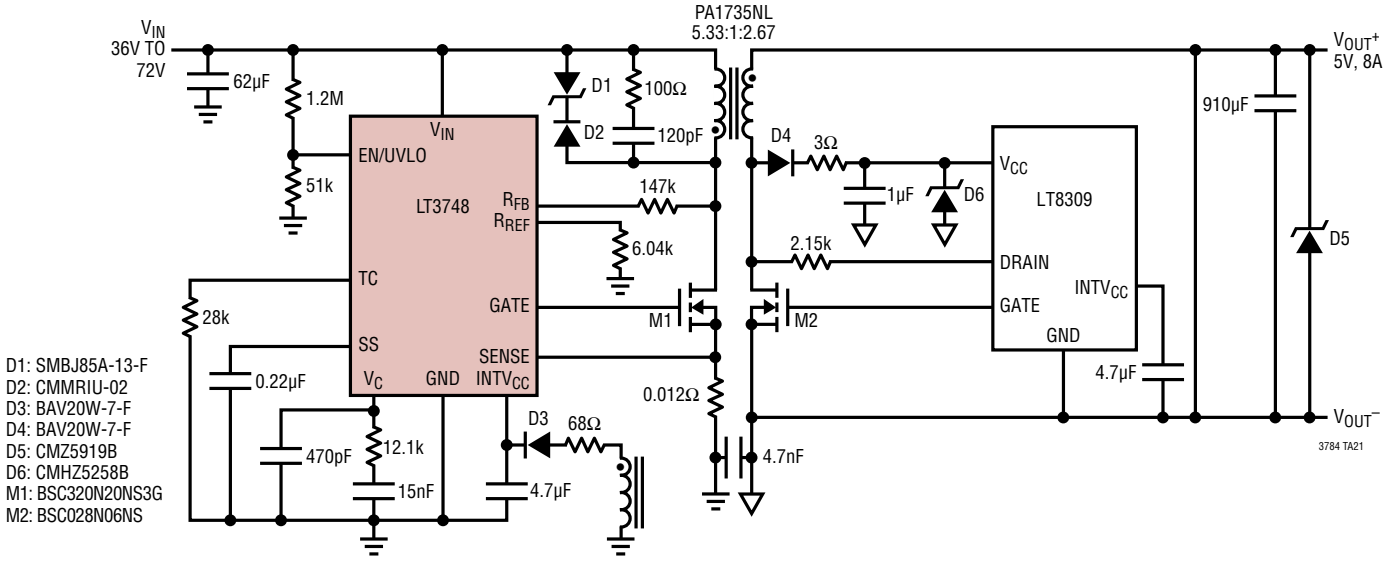


Figure 21. 5V, 8A Isolated Supply with Synchronous Secondary-Side Rectification Using LT8309

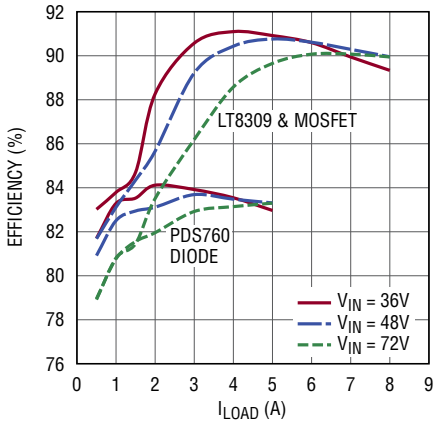


Figure 22. Efficiency of the Supply in Figure 21 as well as Performance Using a Conventional PDS760 Schottky Rectifier

TYPICAL APPLICATIONS

Figure 23 Thermal Image of the Supply in Figure 21 Using a PDS760 Instead of the LT8309 and Synchronous Switch at 5V/5A Output

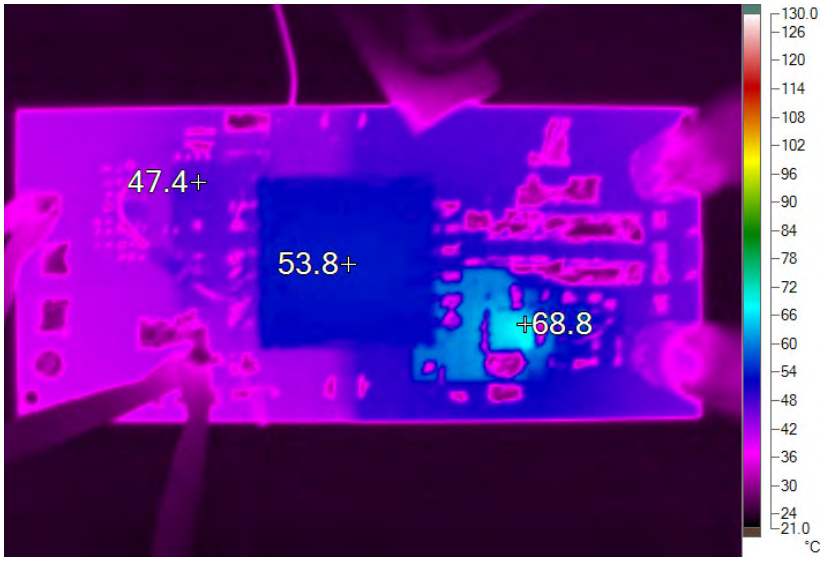


Figure 24 Thermal Image of the Supply in Figure 21 with Synchronous Secondary-Side at 5V/5A Output with Much Lower Temperatures

TYPICAL APPLICATIONS

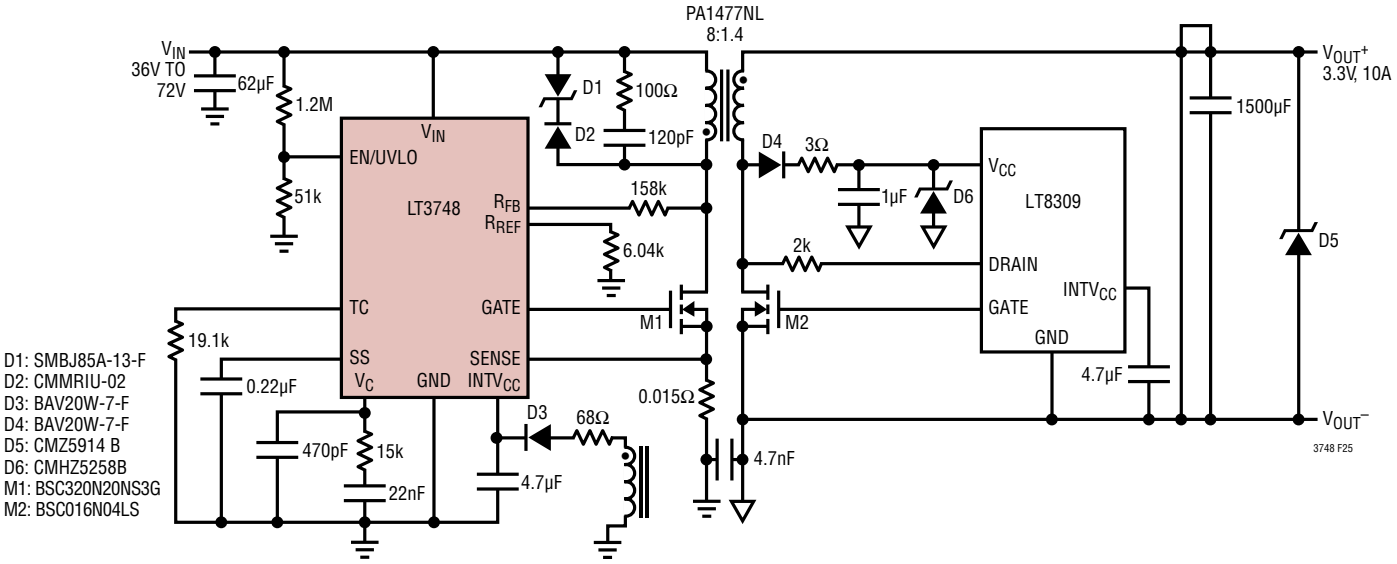


Figure 25. 3.3V, 10A Isolated, Synchronous Flyback Converter

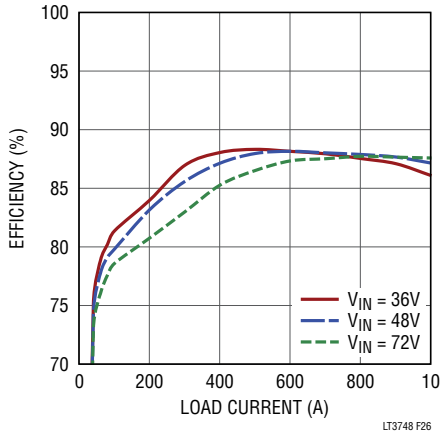
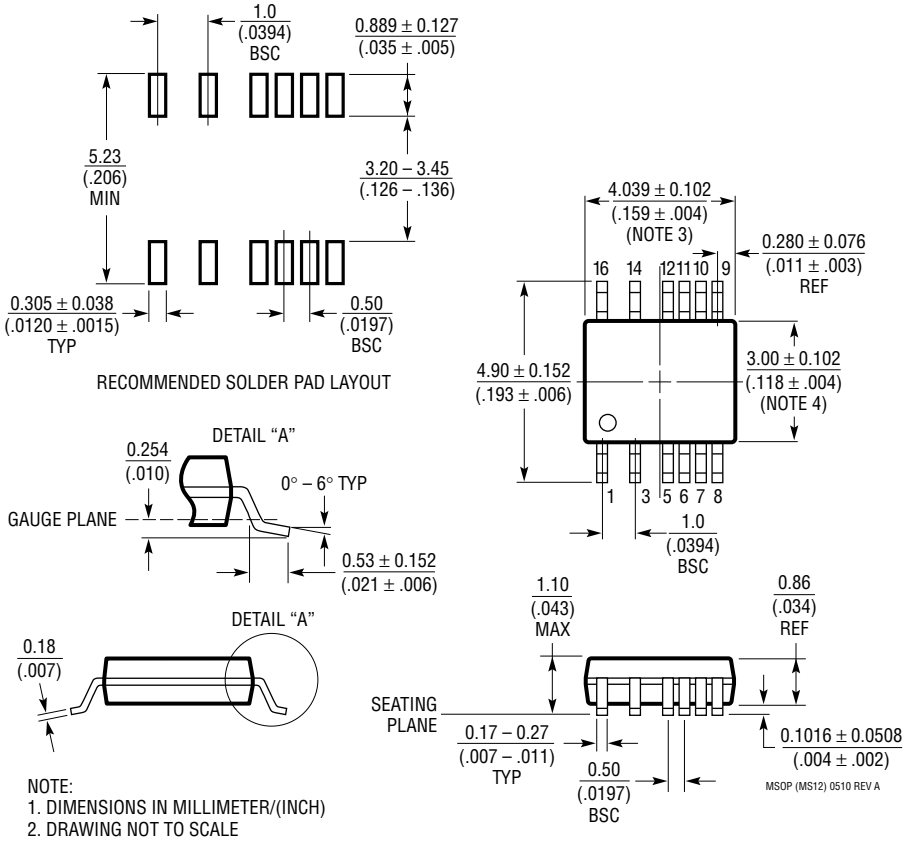


Figure 26. Efficiency of the Supply in Figure 25

PACKAGE DESCRIPTION

MS Package
Varitation: MS16 (12)
16-Lead Plastic MSOP with 4 Pins Removed
(Reference LTC DWG # 05-08-1847 Rev A)



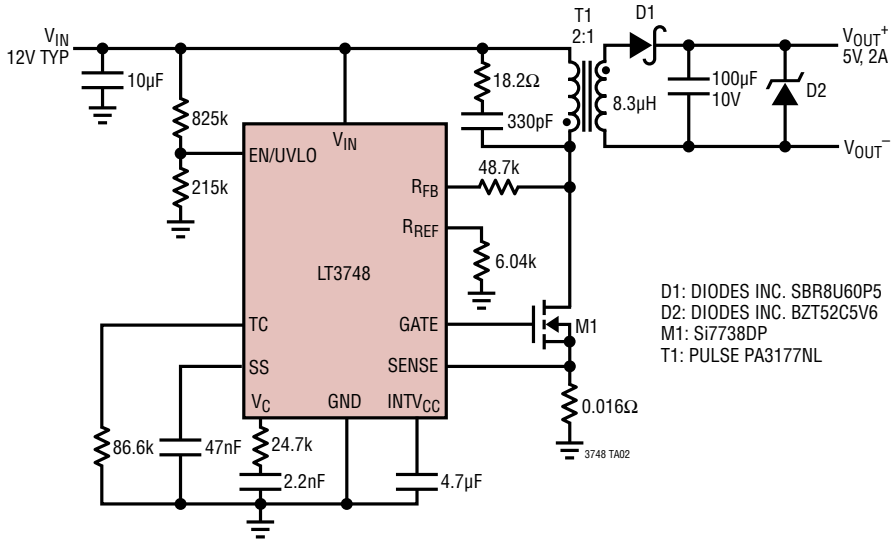
NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	10/10	Added H-grade information to Absolute Maximum Ratings, Pin Configuration, Order Information, and Electrical Characteristics sections.	2, 3
		Revised text and Table 2 in the Applications Information section.	15, 16, 20, 22
		Revised Figures 10 and 17 in the Applications Information section.	26, 27
		Revised Typical Application drawing.	30
B	2/15	Added MP-grade device.	2, 3
		Added Synchronous Secondary Applications paragraphs	20
		Added Figures 21, 22, 23, 24, 25 and 26	29, 30, 31

TYPICAL APPLICATION

5V, 2A Output from Automotive Input with Continuous Operation from 6V to 45V



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT8300	100V_{IN} Micropower Isolated Flyback Converter with 150V/260mA Switch	Low I_Q Monolithic No-Opto Flybacks, 5-Lead TSOT-23
LT8301	42V_{IN} Micropower Isolated Flyback Converter with 65V/1.2A Switch	Low I_Q Monolithic No-Opto Flybacks, 5-Lead TSOT-23
LT8302	42V_{IN} Micropower Isolated Flyback Converter with 65V/3.6A Switch	Low I_Q Monolithic No-Opto Flybacks, 8-Lead SO-8E
LT8309	Secondary-Side Synchronous Rectifier Driver	4.5V ≤ V_{CC} ≤ 40V, Fast Turn-On and Turn-Off, 5-Lead TSOT-23
LT3573	40V Isolated Flyback Converter	Monolithic No-Opto Flyback with Integrated 1.25A, 60V Switch
LT3574/LT3575	40V Isolated Flyback Converters	Monolithic No-Opto Flybacks with Integrated 0.65A / 2.5A 60V Switch
LT3757/LT3758	40V/100V Flyback, Boost Controllers	Universal Controllers with Small Package and Powerful Gate Drive
LT3957/LT3958	40V/100V Flyback, Boost Converters	Monolithic with Integrated 5A/3.3A Switch
LT1725	20V Isolated Flyback Controller	Controller with Load Compensation Circuitry
LT1737	20V Isolated Flyback Controller	No Opto-Isolator or Third Winding Required, Up to 50W Output
LTC®3803/LTC3803-3 LTC3803-5	200kHz/300kHz Flyback DC/DC Controllers	V_{IN} and V_{OUT} Limited Only by External Components
LTC3805/LTC3805-5	Adjustable Frequency Flyback Controllers	V_{IN} and V_{OUT} Limited Only by External Components

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