THE DATASHEET OF

LT8601EUJ#PBF

42V Triple Monolithic Synchronous Step-Down Regulator

FEATURES

- **Flexible Power Supply System Providing Three Outputs Over a Wide Input Voltage Range**
- **Two High Voltage Synchronous Buck Regulators**
  - **3V to 42V Input Voltage Range**
  - **Output Currents Up to 2.5A and 1.5A**
  - **High Efficiency Up to 93%**
- **One Low Voltage Synchronous Buck Regulator**
  - **2.6V to 5.5V Input Voltage Range**
  - **Output Current Up to 1.8A and 95% Efficiency**
- **Resistor Programmable and Synchronizable from 250kHz to 2.2MHz Switching Frequency**
- **Low Ripple Burst Mode® Operation**
  - **30µA I_Q at 12V_{IN} to 3.3V_{OUT2}**
  - **Output Ripple < 15mV**
- **Programmable Power-On Reset**
- Power Good Indicators
- 2-Phase Clock Reduces Input Current Ripple
- Available in Thermally Enhanced 40-Lead QFN (6mm × 6mm) Package

APPLICATIONS

- Automotive Systems
- Distributed Supply Regulation
- Industrial Controls and Power Supplies

DESCRIPTION

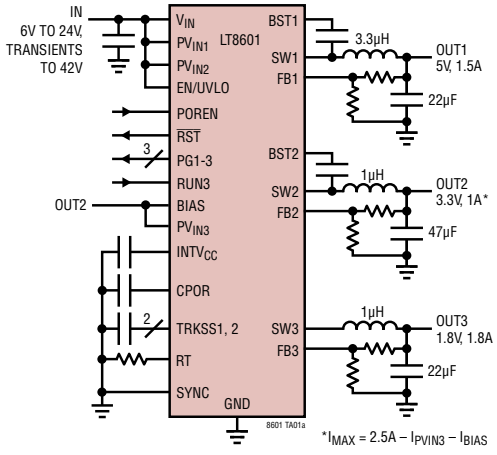
The LT®8601 is a triple channel, current mode, monolithic buck switching regulator with a programmable power-on reset. All regulators are synchronized to a single oscillator with an adjustable frequency from 250kHz to 2.2MHz. The LT8601 can be configured for micropower Burst Mode or pulse-skipping operation at light load. Micropower operation results in quiescent current of 30µA with all three regulators operating as shown in the application below with no load applied.

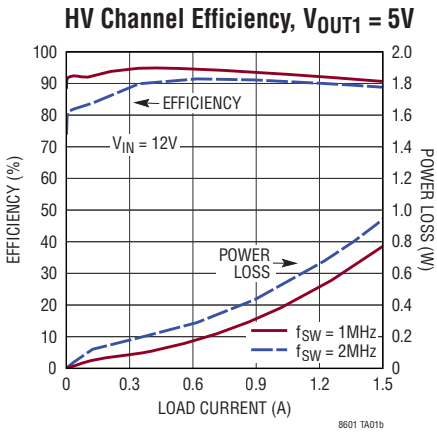
The high voltage channels are synchronous buck regulators that operate from an input of 3.0V to 42V. The output currents are up to 1.5A (OUT1) and 2.5A (OUT2). The low voltage channel operates from an input of 2.6V to 5.5V. Internal synchronous power switches provide high efficiency with output currents up to 1.8A. The LT8601 uses a 2-phase clock with channel 1 operating 180° from channels 2 and 3 to reduce input ripple current on both HV and LV inputs. All channels have cycle-by-cycle current limit, providing protection against shorted outputs. Thermal shutdown provides additional protection.

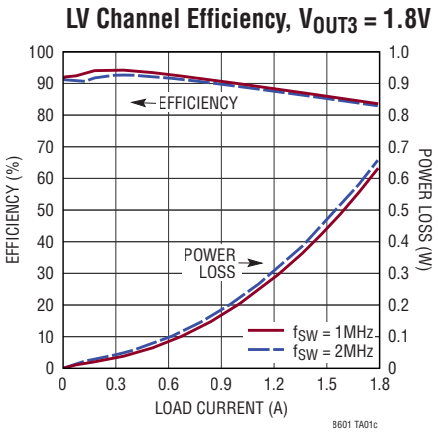
The LT8601 is available in a 40-lead 6mm × 6mm QFN package.

TYPICAL APPLICATION

Automotive Input Stepped Down to 5V, 3.3V and 1.8V Outputs at 2MHz







ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltages
- V_{IN}, $PV_{IN1,2}$ ..... –0.3V to 42V
- PV_{IN3} ..... –0.3V to 6V

PG1-3, SYNC, TRKSS1-2, RUN3, $\overline{RST}$ Voltages 6V

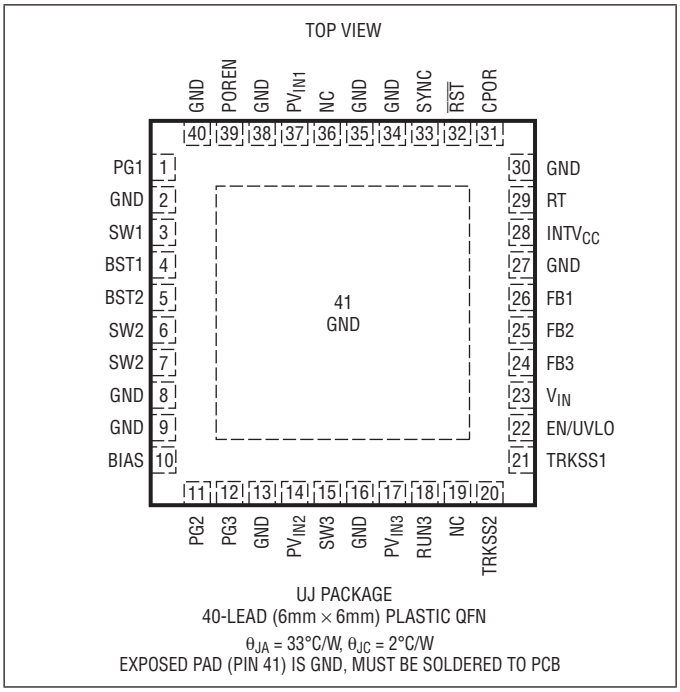
RT, FB1-3, CPOR, POREN Voltages 3.6V

EN/UVLO Voltage 42V

BIAS Voltage ..... –0.3V to 15V

Operating Junction Temperature (Notes 2 and 3)
- LT8601E ..... –40°C to 125°C
- LT8601I ..... –40°C to 125°C
- Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



UJ PACKAGE
40-LEAD (6mm × 6mm) PLASTIC QFN
θ_{JA} = 33°C/W, θ_{JC} = 2°C/W
EXPOSED PAD (PIN 41) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

http://www.linear.com/product/LT8601#orderinfo

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT8601EUJ#PBF	LT8601EUJ#TRPBF	LT8601	40-Lead (6mm × 6mm) Plastic QFN	–40°C to 125°C
LT8601IUJ#PBF	LT8601IUJ#TRPBF	LT8601	40-Lead (6mm × 6mm) Plastic QFN	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/

For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = PV_{IN1} = PV_{IN2} = 12V, EN/UVLO = 3V, PV_{IN3} = 3.3V unless otherwise noted. (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Minimum Operating Voltage		●		2.7	3	V
Minimum Operating Voltage to Start		●		3.1	3.5	V
V_{IN} Quiescent Current, Shutdown	EN/UVLO = 0.4V			0.1	1	µA
V_{IN} Quiescent Current, Operating	All Channels Active, No Load (Note 4) All Channels Active,100µA on V_{OUT2} (Note 4)			30 70		µA µA
EN/UVLO Threshold	EN/UVLO Rising EN/UVLO Falling	● ●	1.15 1.0	1.2 1.15	1.25 1.2	V V
EN/UVLO Input Current	EN/UVLO = 1.2V, V_{IN} = 42V		–40		40	nA
Oscillator						
Switching Frequency	R_T = 28.7k	●	1.8	2	2.2	MHz
	R_T = 254k	●	0.225	0.25	0.275	MHz
SYNC Input Frequency Range		●	0.25		2.2	MHz
SYNC Input Voltage Low		●			0.3	V
SYNC Input Voltage High		●	1.2			V
SYNC Input Current			–100		100	nA
Channel 1						
Feedback Voltage		●	0.988	1	1.012	V
Input Current FB1		●	–100		100	nA
FB1 Voltage Line Regulation	V_{IN} = 3V to 42V			0.002	0.01	%/V
SW1 Peak Current Limit	V_{IN} = PV_{IN1} = PV_{IN2} = 6V		2.3	2.7	3.0	A
SW1 Leakage Current				0.1	1	µA
SW1 Top On Resistance	I_{SW1} = 1A			240		mΩ
SW1 Bottom On Resistance	I_{SW1} = 1A			170		mΩ
Lower FB1 Power Good Threshold	Percentage of V_{FB1}	●	89	92	95	%
Upper FB1 Power Good Threshold	Percentage of V_{FB1}	●	105	108	111	%
PG1 Output Voltage Low	I_{PG1} = –350µA	●		0.13	0.3	V
PG1 Leakage Current	PG1 = 5V, FB1 = 1V	●			30	µA
TRKSS1 Pull-Up Current	TRKSS1 = 0.2V		1.5	2.4	3.1	µA
Minimum Switch-On Time	I_{SW1} = 1A			60		ns
Minimum Switch-Off Time	I_{SW1} = 1A			70		ns
Channel 2						
Feedback Voltage		●	0.988	1	1.012	V
Input Current FB2		●	–100		100	nA
FB2 Voltage Line Regulation	V_{IN} = 3V to 42V			0.002	0.01	%/V
SW2 Peak Current Limit	V_{IN} = PV_{IN1} = PV_{IN2} = 6V		3.5	4.0	4.5	A
SW2 Leakage Current				0.1	1	µA
SW2 Top On Resistance	I_{SW2} = 1A			150		mΩ
SW2 Bottom On Resistance	I_{SW2} = 1A			100		mΩ
Lower FB2 Power Good Threshold	Percentage of V_{FB2}	●	89	92	95	%
Upper FB2 Power Good Threshold	Percentage of V_{FB2}	●	105	108	111	%
PG2 Output Voltage Low	I_{PG2} = –350µA	●		0.13	0.3	V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = PV_{IN1} = PV_{IN2} = 12V, EN/UVLO = 3V, PV_{IN3} = 3.3V unless otherwise noted. (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
PG2 Leakage Current	PG2 = 5V, FB2 = 1V	●			30	µA
TRKSS2 Pull-Up Current	TRKSS2 = 0.2V		1.5	2.4	3.1	µA
Minimum Switch-On Time	I_{SW2} = 2A			55		ns
Minimum Switch-Off Time	I_{SW2} = 2A			70		ns
Channel 3						
Operating Voltage		●	2.6		5.5	V
Feedback Voltage		●	790	800	810	mV
Input Current FB3		●	–100		100	nA
FB3 Voltage Line Regulation	V_{IN} = 3V to 42V			0.002	0.01	%/V
SW3 Current Limit			2.6	3.2	3.8	A
SW3 Leakage	PV_{IN3} = 5.5V			0.1	1	µA
SW3 PMOS On Resistance	I_{SW3} = 1A			150		mΩ
SW3 NMOS On Resistance	I_{SW3} = 1A			120		mΩ
Lower FB3 Power Good Threshold	Percentage of V_{FB3}	●	89	92	95	%
Upper FB3 Power Good Threshold	Percentage of V_{FB3}	●	105	108	111	%
PG3 Output Voltage Low	I_{PG3} = –350µA	●		0.13	0.3	V
PG3 Leakage Current	PG3 = 5V, FB3 = 0.8V	●			30	µA
RUN3 Threshold Voltage		●	0.695	0.72	0.74	V
RUN3 Input Current	RUN3 = 3.3V	●	–100		100	nA
Soft-Start Time		●	0.7	1	1.3	ms
Minimum Switch-On Time	I_{SW3} = 1A			70		ns
Minimum Switch-Off Time	I_{SW3} = 1A			70		ns
PV_{IN3} UVLO		●		2.35	2.6	V
Power-On Reset						
CPOR Pull-Up Current	CPOR = 0V			2		µA
POR Delay Time	CPOR = 1000pF	●	31	35.2	39.4	ms
$\overline{RST}$ Output Voltage Low	$I_{\overline{RST}}$ = –100µA	●		0.1	0.2	V
$\overline{RST}$ Pull-Up Current	POR Timed Out, $\overline{RST}$ = 0V			20		µA
$\overline{RST}$ Leakage Current	$\overline{RST}$ = 6V, EN/UVLO = 0V		–40		40	nA
POREN Threshold		●	1.15	1.2	1.25	V
POREN Pull-Up Current	POREN = 0V		0.8	1.2	1.6	µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LT8601E is guaranteed to meet performance specifications from 0°C to 125°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LT8601I is guaranteed to meet performance specifications from –40°C to 125°C junction temperature. High junction temperatures degrade operating lifetimes. Operating lifetime is derated at junction temperatures above 125°C.

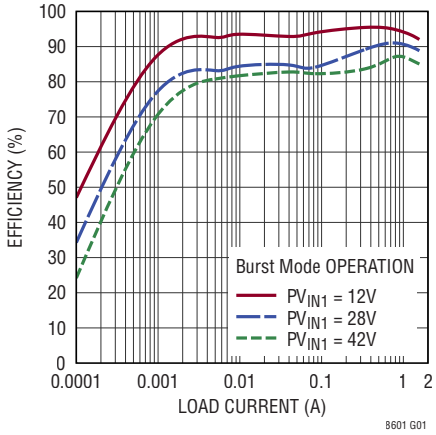
Note 3: This IC includes overtemperature protection that is intended to protect the device during overload conditions. Junction temperature will exceed 150°C when overtemperature protection is active. Continuous operation above the specified maximum junction temperature will reduce lifetime.

Note 4: All three channels enabled as shown in the application circuit titled, “Details of the Front Page Application” (using the 1MHz component values) found in the Typical Application section.

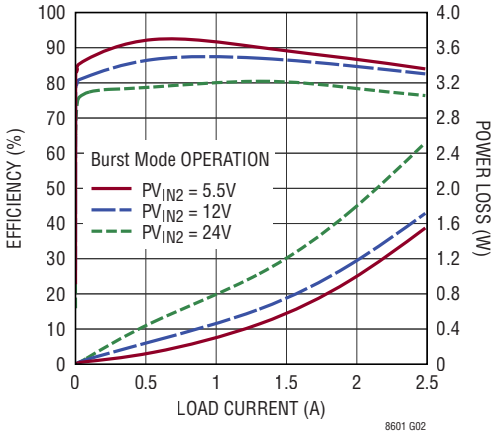
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{IN} = PV_{IN1} = PV_{IN2} = 12V, EN/UVLO = 3V and PV_{IN3} = 3.3V, unless otherwise noted.

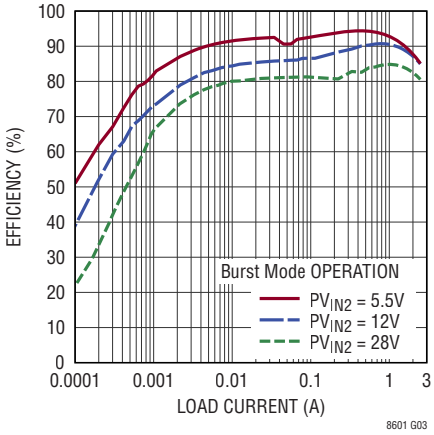
Channel 1 Efficiency vs Load
V_{OUT1} = 8V, f_{SW} = 2MHz



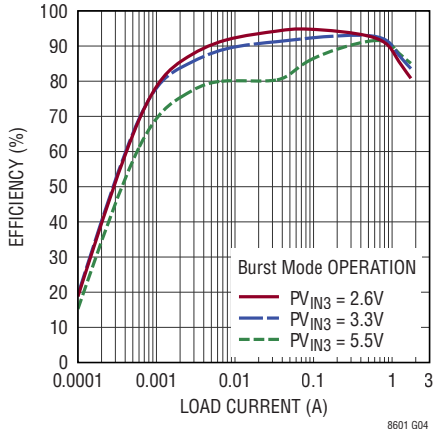
Channel 2 Efficiency vs Load
V_{OUT2} = 3.3V, f_{SW} = 2MHz



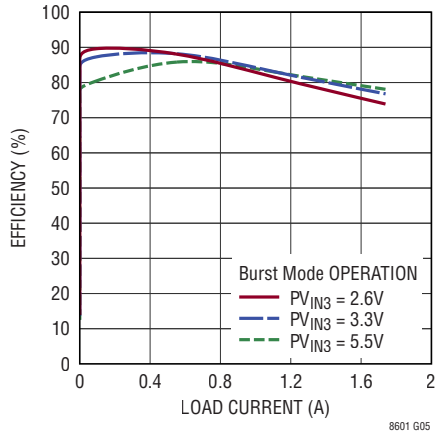
Channel 2 Efficiency vs Load
V_{OUT2} = 3.3V, f_{SW} = 1MHz



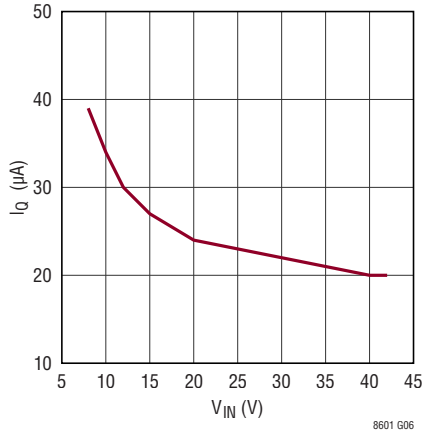
LV Channel Efficiency vs Load
V_{OUT3} = 1.8V, f_{SW} = 1MHz



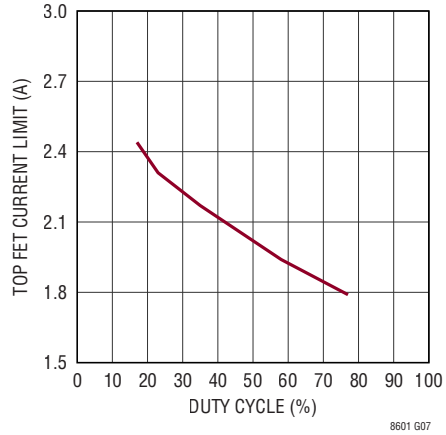
LV Channel Efficiency vs Load
V_{OUT3} = 1.2V, f_{SW} = 2MHz



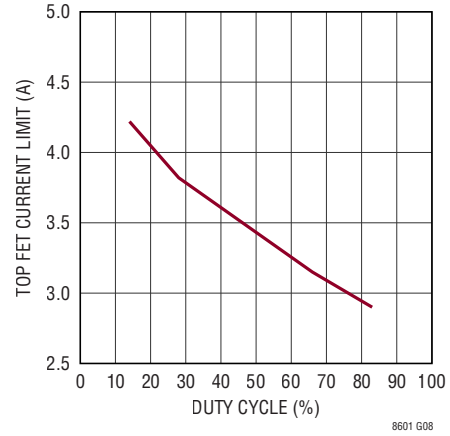
Quiescent Current vs V_{IN}



Channel 1 Peak Current Limit vs Duty Cycle



Channel 2 Peak Current Limit vs Duty Cycle

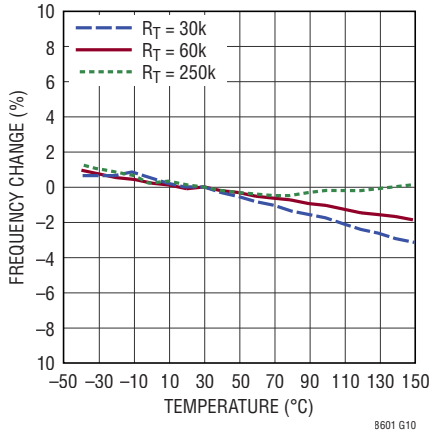


Channel 3 Peak Current Limit vs Duty Cycle

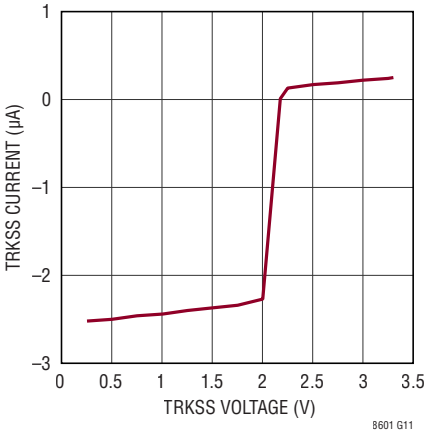
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{IN} = PV_{IN1} = PV_{IN2} = 12V, EN/UVLO = 3V and PV_{IN3} = 3.3V, unless otherwise noted.

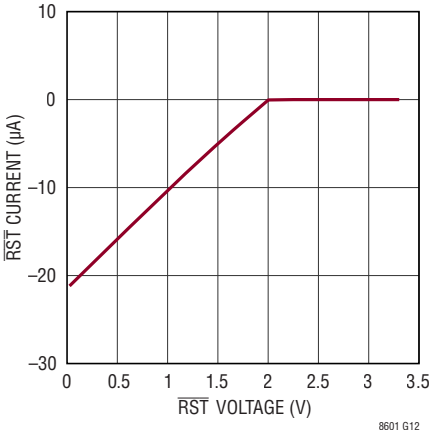
Switching Frequency vs Temperature



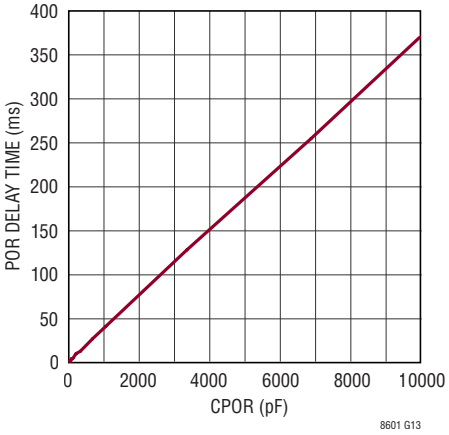
TRKSS Pull-Up Current vs Voltage



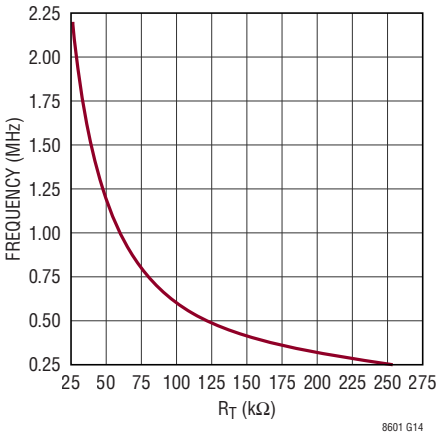
$\overline{RST}$ Pull-Up Current vs Voltage



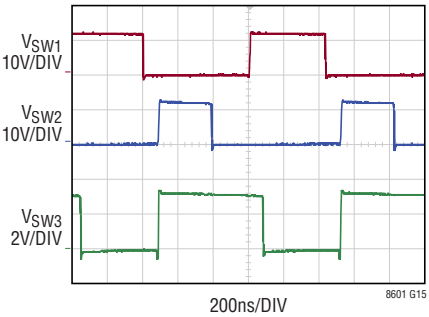
Power-On Reset Time vs CPOR



Switching Frequency vs R_T

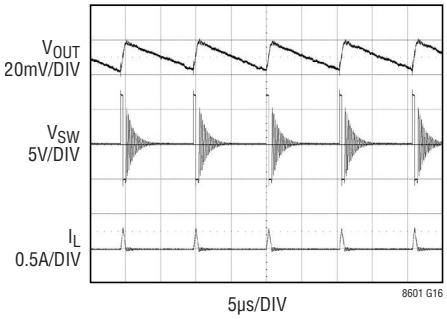


Full Frequency Waveforms



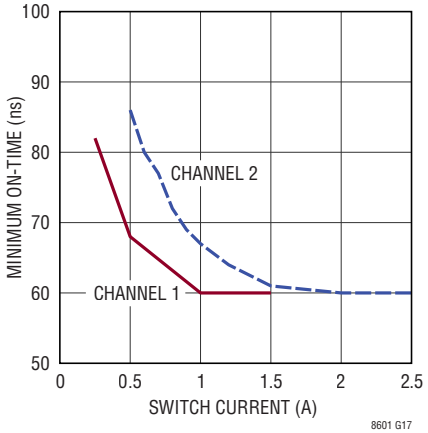
V_{OUT1} = 5V
V_{OUT2} = 3.3V
V_{OUT3} = 1.8V

Light Load Waveforms

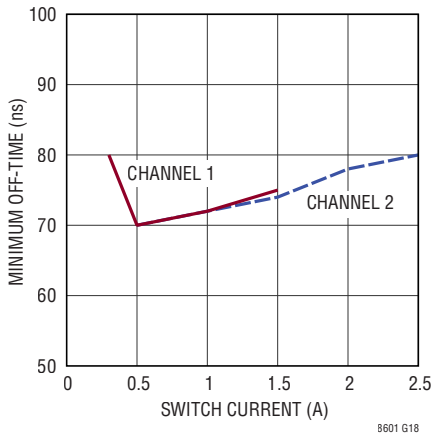


CHANNEL 1
$12V_{IN}$ TO $5V_{OUT}$ AT 10mA
V_{SYNC} = 0V

Minimum On-Time vs I_{SW}



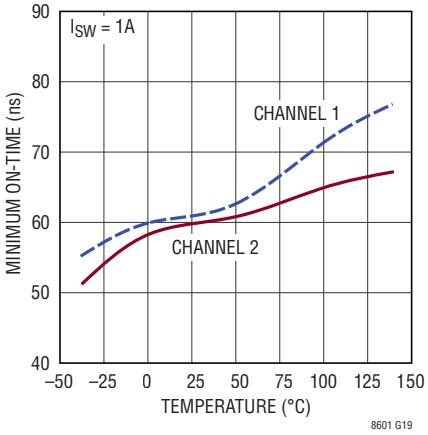
Minimum Off-Time vs I_{SW}



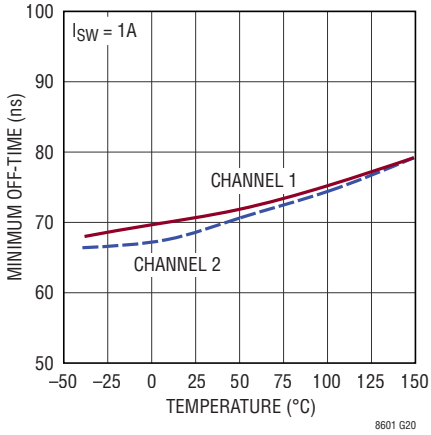
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{IN} = PV_{IN1} = PV_{IN2} = 12V, EN/UVLO = 3V and PV_{IN3} = 3.3V, unless otherwise noted.

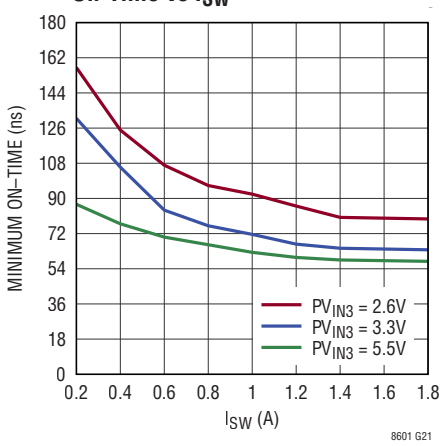
Minimum On-Time vs Temperature



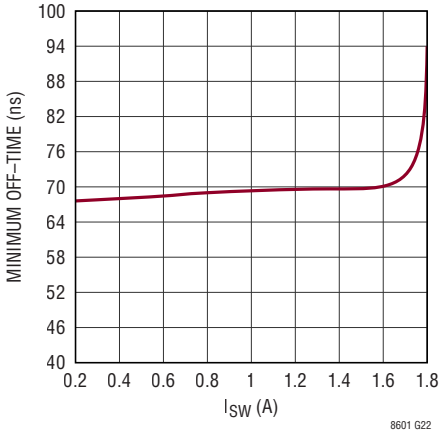
Minimum Off-Time vs Temperature



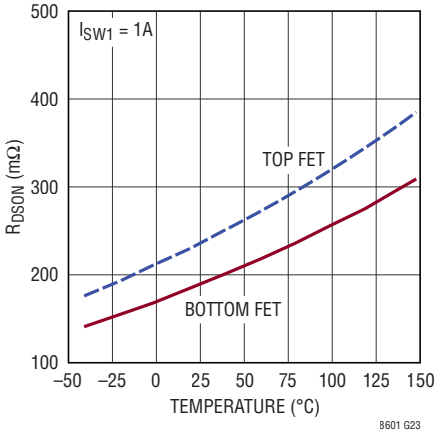
Channel 3 Minimum On-Time vs I_{SW}



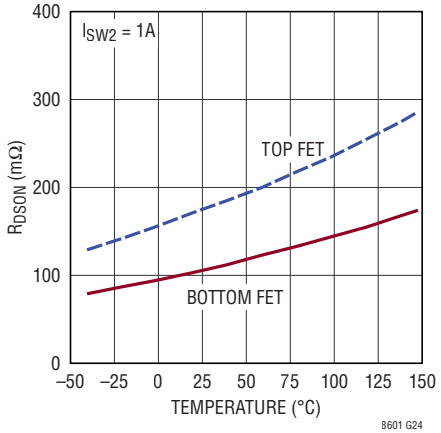
Channel 3 Minimum Off-Time vs I_{SW}



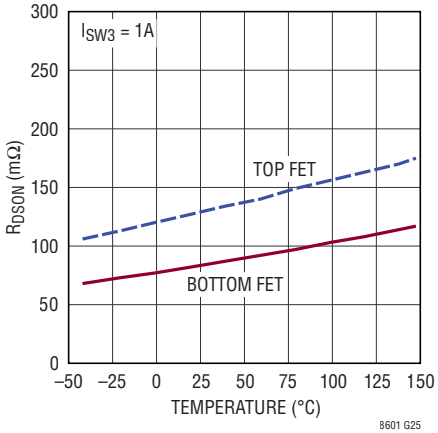
Channel 1 $R_{DS(ON)}$ vs Temperature



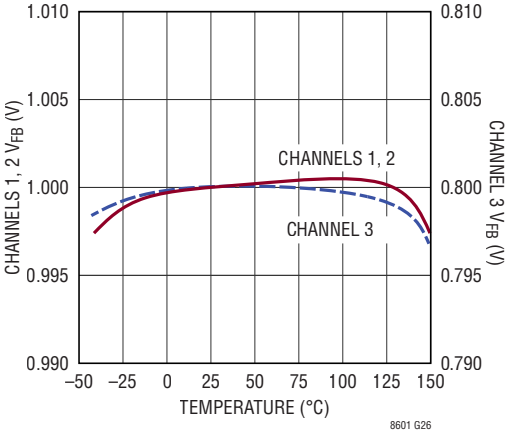
Channel 2 $R_{DS(ON)}$ vs Temperature



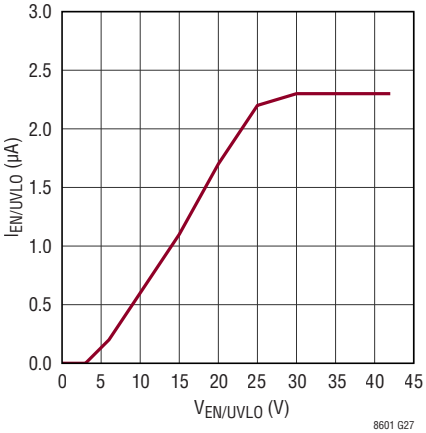
Channel 3 $R_{DS(ON)}$ vs Temperature



Feedback Voltage vs Temperature



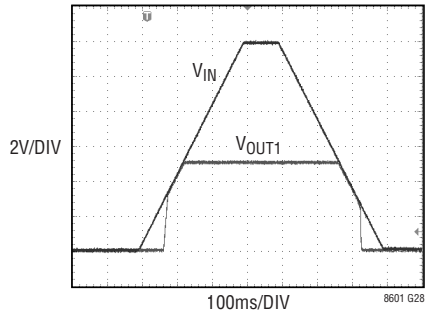
EN/UVLO Current vs Voltage



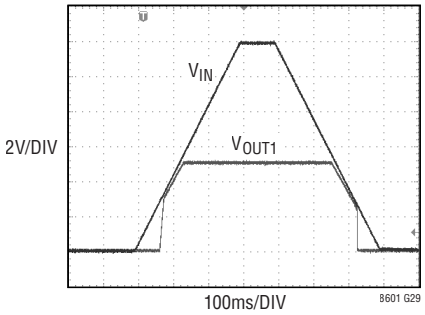
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{IN} = PV_{IN1} = PV_{IN2} = 12V, EN/UVLO = 3V and PV_{IN3} = 3.3V, unless otherwise noted.

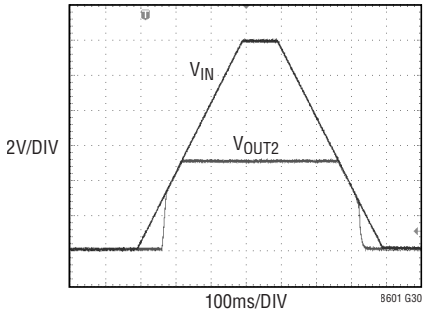
Channel 1 Start-Up and Dropout, R_L = 20Ω



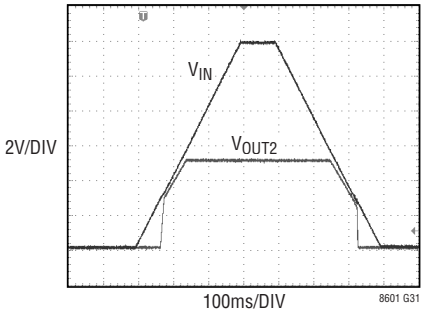
Channel 1 Start-Up and Dropout, R_L = 3.3Ω



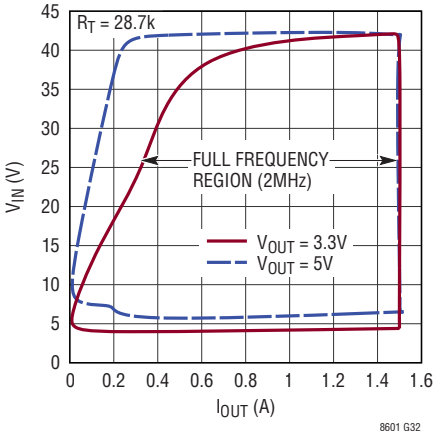
Channel 2 Start-Up and Dropout, R_L = 20Ω



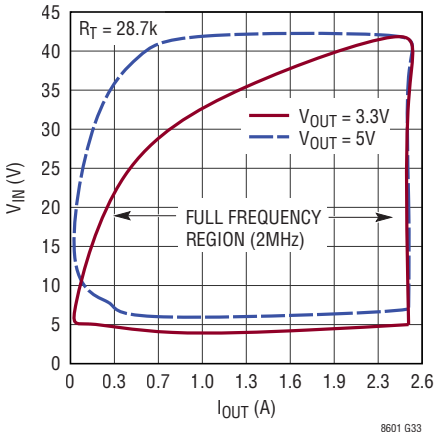
Channel 2 Start-Up and Dropout, R_L = 2Ω



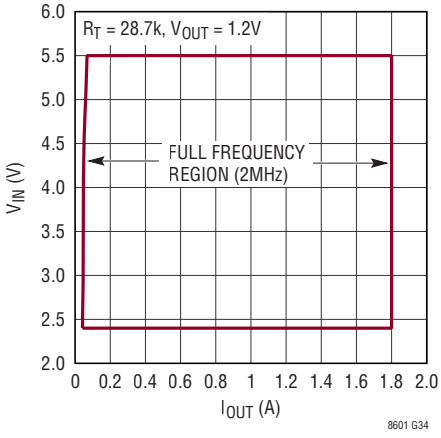
Channel 1 Full Frequency V_{IN} vs Load Current



Channel 2 Full Frequency V_{IN} vs Load Current



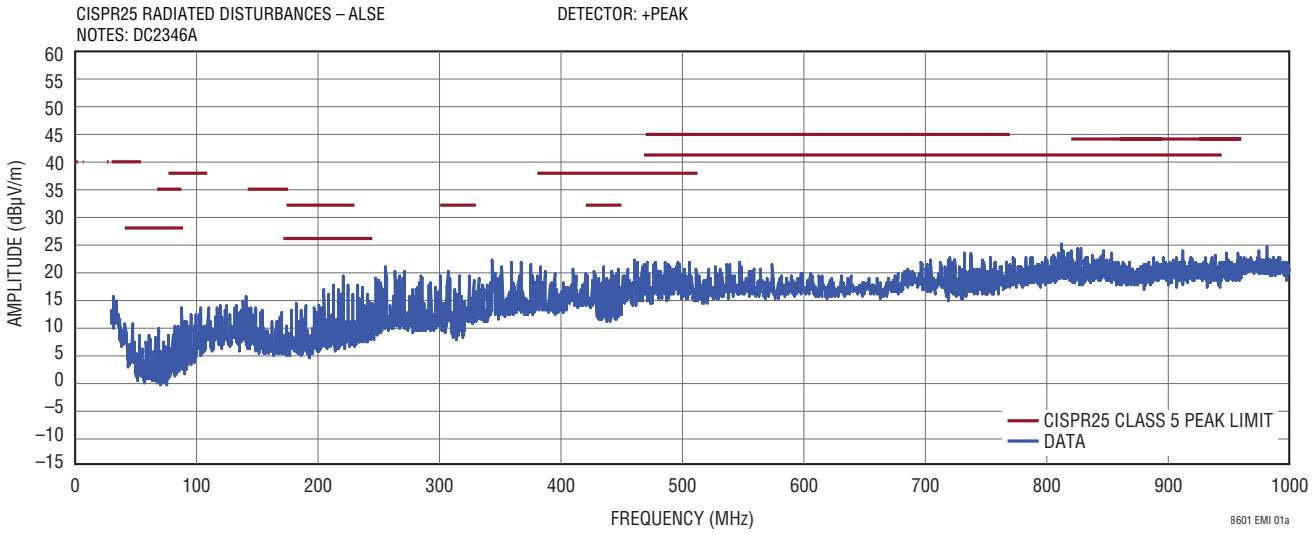
Channel 3 Full Frequency V_{IN} vs Load Current



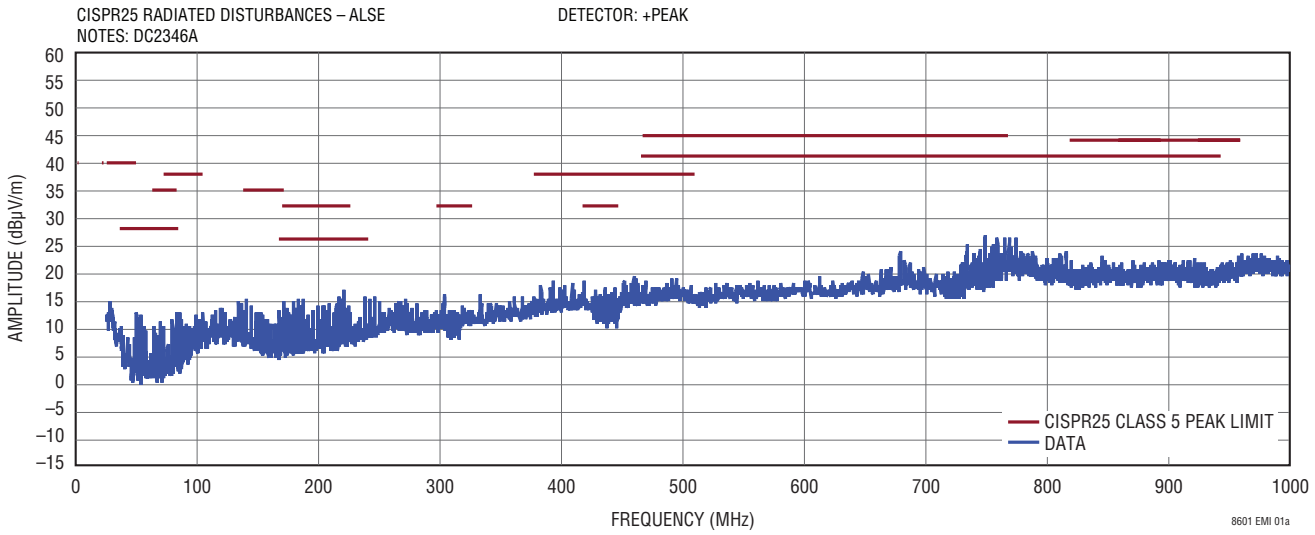
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C

Radiated EMI Performance, CISPR25 Radiated Emission Tests with Class 5 Peak Limit.

Vertical Polarization



Horizontal Polarization



Demo Board with EMI Filter Installed, 14V_{IN}, 1A on All Outputs, f_{SW} = 2MHz.

PIN FUNCTIONS

BIAS (Pin 10): Power to the Internal Regulator. Connect to an output ≥ 3.2V when available. Decouple to ground with a low ESR capacitor.

BST1, BST2 (Pins 4, 5): Boost Voltage for High Voltage Channels. The Boost Voltage provides a drive voltage higher than PV_{IN} to the gate of the NMOS top switch.

CPOR (Pin 31): Power-On Reset Timer. Connect a capacitor from this pin to ground to program the power-on reset timer. CPOR has a 2µA (typical) pull-up current.

EN/UVLO (Pin 22): Enable/Undervoltage Lockout Input. The LT8601 is in low power shutdown when this pin is ≤ 0.4V. A precision threshold at 1.20V (rising) enables the switching regulator's output switching stages. This allows the EN/UVLO pin to be used as an input undervoltage lockout by connecting to a resistor divider between V_{IN} and GND. When the EN/UVLO voltage is between 0.4V and 1.2V, the LT8601 input current will depend on the mode selected, the V_{IN} voltage, and the EN/UVLO voltage. Connect this pin to V_{IN} if the UVLO function is not needed.

FB1, FB2 (Pins 26, 25): Feedback Input Pins for the High Voltage Converters. The converters regulate the corresponding feedback pin to the lesser of 1V or the voltage on the associated TRKSS pin.

FB3 (Pin 24): Feedback Input Pin for the Low Voltage Converter. The converter regulates the corresponding feedback pin to 800mV.

GND (Pins 2, 8, 9, 13, 16, 27, 30, 34, 35, 38, 40, 41): Ground. These pins must be soldered to PCB ground. The exposed pad must also be soldered to PCB ground.

$INTV_{CC}$ (Pin 28): Internal Regulator Bypass. Do not load the $INTV_{CC}$ pin with external circuitry. $INTV_{CC}$ is 3.1V when BIAS < 3.1V, 3.4V when BIAS > 3.4V, and approximately equal to BIAS when BIAS is between 3.1V and 3.4V. Decouple to ground with a low ESR, 4.7µF capacitor.

PG1, PG2 (Pins 1, 11): Power Good Indicators for Channels 1 and 2. Open-drain logic output pulls down until the corresponding FB pin rises above 0.92V but remains below 1.08V.

PG3 (Pin 12): Power Good Indicator for Channel 3. Open-drain logic output pulls down until the corresponding FB pin rises above 0.736V but remains below 0.864V.

POREN (Pin 39): Power-On Reset Enable. This is a logic input that starts the ramp on the POR timing capacitor.

PV_{IN1}, PV_{IN2} (Pins 37, 14): Input Supply Voltage to High Voltage Channels 1 and 2, respectively. These pins are independent and can be powered from different sources if necessary. Bypass each input with a low ESR capacitor to the adjacent GND pin.

PV_{IN3} (Pin 17): Input Supply Voltage to Low Voltage Channel 3. This pin is typically connected to one of the high voltage converter outputs and should be locally bypassed with a low ESR capacitor.

$\overline{RST}$ (Pin 32): Power-On Reset Output. CMOS output with weak pull-up, this pin is held low until the POR times out.

RT (Pin 29): Frequency Programming Resistor. Connect a resistor from this pin to ground to set the internal oscillator frequency.

RUN3 (Pin 18): Run Input for the Low Voltage Converter. Channel 3 is enabled when the voltage on this pin exceeds 0.72V (typical).

SW1 (Pin 3): Channel 1 Switch Node. This is the output of the internal power switches for channel 1.

SW2 (Pins 6, 7): Channel 2 Switch Node. This is the output of the internal power switches for channel 2. These pins must be connected together.

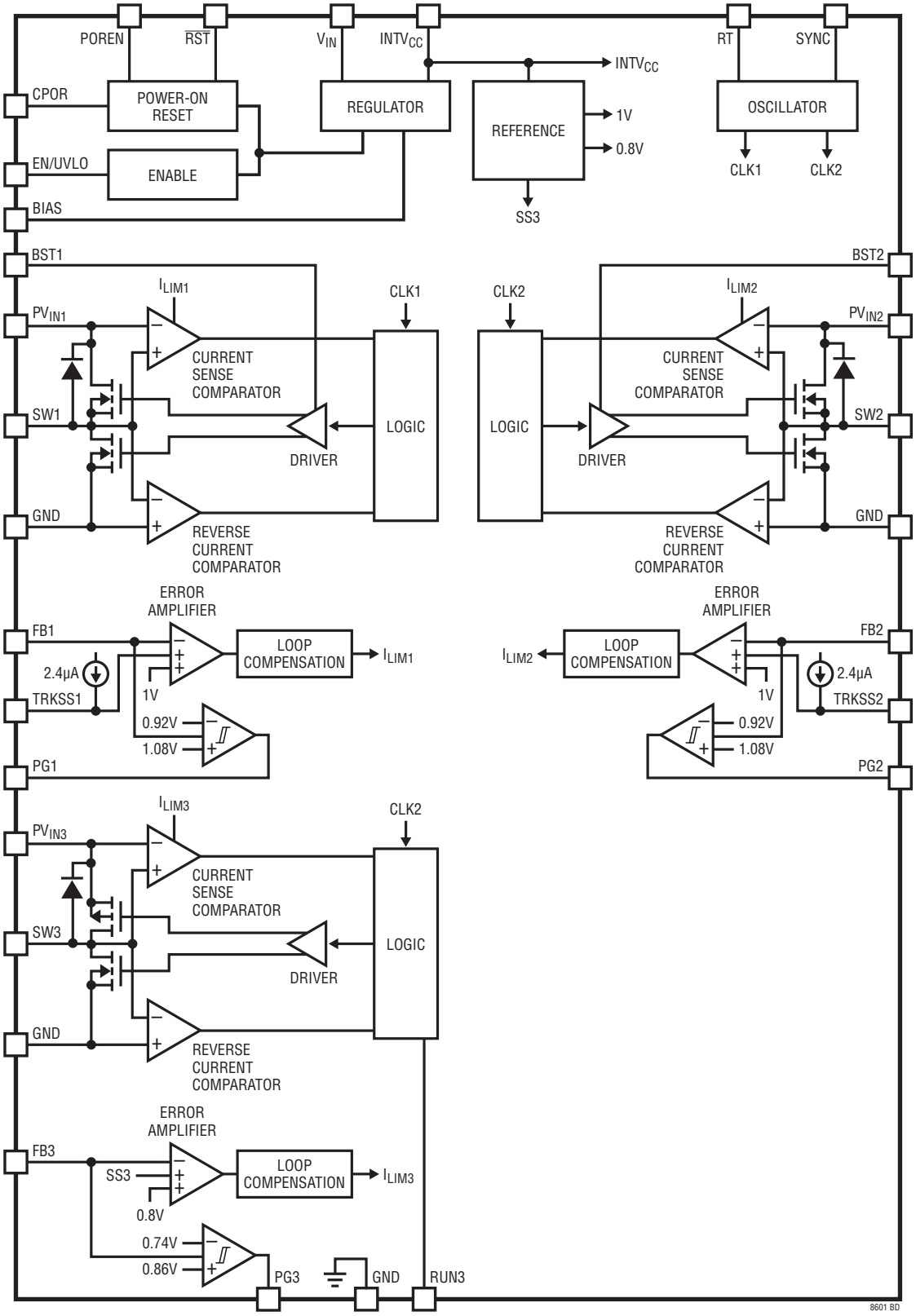
SW3 (Pin 15): Channel 3 Switch Node. This is the output of the internal power switches for channel 3.

SYNC (Pin 33): Clock Synchronization and Mode Select Input. Connect this pin to ground to enable low ripple Burst Mode operation. Connect this pin to $INTV_{CC}$ to enable pulse skip operation. Apply a digital clock input to synchronize the LT8601 switching frequency to a reference clock. When an external clock is applied, the LT8601 will operate in pulse-skipping mode.

TRKSS1, TRKSS2 (Pins 21, 20): Track/Soft-Start Inputs for the High Voltage Converters. When this pin is below 1V, the converter regulates the FB pin to the TRKSS voltage instead of the internal reference. The TRKSS pin has a 2.4µA (typical) pull-up current.

V_{IN} (Pin 23): Input Supply Voltage to Internal Functions. This pin is independent from any PV_{IN} pin and can be powered from different sources if necessary. V_{IN} must be above 3V for the part to operate.

BLOCK DIAGRAM



OPERATION

The LT8601 is a triple channel, constant frequency, current mode, monolithic buck switching regulator with power-on reset. All channels are synchronized to a single oscillator. Two of the channels are high voltage capable (up to 42V input) while the other is low voltage capable (up to 5.5V input) and is typically powered from the high voltage buck outputs.

Start-Up

When enabled by setting the EN/UVLO voltage above its threshold, the LT8601 starts charging the $INTV_{CC}$ capacitor from V_{IN}. If BIAS is higher than 3.2V, BIAS supplies current to the $INTV_{CC}$ regulator to reduce V_{IN} quiescent current.

High Voltage Buck Regulators

Each high voltage channel is a synchronous buck regulator that operates from an independent PV_{IN} pin. The internal top power MOSFET is turned on at the beginning of each oscillator cycle, and turned off when the current flowing through the top MOSFET reaches a level determined by the error amplifier. The error amplifier measures the output voltage through an external resistor divider tied to the FB pin to control the peak current in the top switch. The reference of the error amplifier is determined by the lower of the internal 1V reference and the voltage at its TRKSS pin.

While the top MOSFET is off, the bottom MOSFET is turned on for the remainder of the oscillator cycle or until the inductor current starts to reverse. If overload conditions result in more than 2A for channel 1 or 3.3A for channel 2 flowing through the bottom switch, the next clock cycle will be delayed until switch current returns to a safe level.

Low Voltage Buck Regulator

The low voltage channel is a synchronous buck regulator that operates from an independent PV_{IN} pin. The PV_{IN} pin has an undervoltage lockout set at 2.35V (typical). Each internal top power MOSFET is turned on at the beginning of each oscillator cycle, and turned off when the current flowing through the top MOSFET reaches a level determined by the error amplifier. The error amplifier measures the output voltage through an external resistor divider tied to the FB pin to control the peak current in the top switch. The reference of the error amplifier is an internal 800mV reference. The low voltage channel has a RUN pin to allow power sequencing and an internal soft-start circuit ramps the output voltage up in 1ms.

While the top MOSFET is off, the bottom MOSFET is turned on for the remainder of the oscillator cycle or until the inductor current starts to reverse. If overload conditions result in more than 2.4A flowing through the bottom switch, the next clock cycle will be delayed until switch current returns to a safe level.

Multiphase Switching

The oscillator generates two clock signals 180° out of phase. Channel 1 operates from CLK1, while channels 2 and 3 operate from CLK2. Since a buck regulator only draws input current during the top switch on-cycle, multiphase operation reduces peak input current and doubles the input current frequency. These effects reduce input current ripple and reduce the input capacitance required.

Light Load Operation

At light load, the regulators operate in low ripple Burst Mode operation. Low ripple Burst Mode operation shuts down most internal circuitry between switch on-cycles to conserve power while still retaining low ripple at the output.

Undervoltage Lockout

The EN/UVLO pin is used to put the LT8601 in shutdown, reducing the input current to less than 1µA. The accurate 1.2V (rising) threshold of the EN/UVLO pin provides a programmable V_{IN} undervoltage lockout through an external resistor divider tied to the EN/UVLO pin. A 50mV (typical) hysteresis voltage on the EN/UVLO pin prevents switching noise from inadvertently shutting down the LT8601.

Power Good Comparators

Each channel has a power good comparator that trips when the feedback pin is above or below its reference voltage by more than 8%. The PG output pins are open-drain. The PG pin for each channel is pulled low when the corresponding output is out of regulation. The PG outputs are not valid until $INTV_{CC}$ rises to 2.7V

OPERATION

Power-On Reset Timer

The LT8601 includes a power-on reset timer. The power-on reset timeout period is adjustable using an external capacitor on the CPOR pin as described in the Applications Information section. The timer is initiated when the POREN pin is higher than 1.2V (typical).

The output of the POR timer, the $\overline{RST}$ pin, is an open-drain output with a weak internal pull-up of 100kΩ (typical) to approximately 2V. $\overline{RST}$ is held low until the expiration of the POR timer. The $\overline{RST}$ pin is only valid when the LT8601 is enabled and $INTV_{CC}$ is above 2.7V.

APPLICATIONS INFORMATION

Setting the Output Voltages

The output voltages are set by the resistor dividers on the outputs as shown in Figure 1. The formula used is:

$$R1 = R2 \bullet \left(\frac{V_{OUTx}}{V_{FB}} - 1 \right)$$

where V_{OUTx} is the output voltage of regulator x and V_{FB} is the feedback reference voltage. V_{FB} is 1V for the high voltage regulators (1 and 2) and 800mV for the low voltage channel. R2 should be 200k or less to avoid noise problems.

To improve the frequency response, a feedforward capacitor C_{ff} may also be used. Typical values are 10pF to 100pF. Great care should be taken to route the FB node away from noise sources, such as an inductor or a SW line.

Switching Frequency

The LT8601 uses a constant frequency architecture that can be programmed from 250kHz to 2.2MHz by tying a resistor from the RT pin to ground. Table 1 shows the closest 1% resistor value of R_T for common switching frequencies.

Table 1. Switching Frequency vs R_T Value

SWITCHING FREQUENCY (MHz)	R_T (kΩ)
0.25	255
0.35	178
0.5	124
0.75	80.6
1.0	60.4
1.25	47.5
1.5	39.2
1.75	33.2
2.0	28.7
2.2	26.1

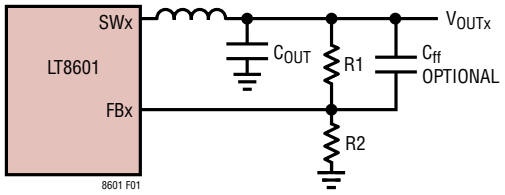


Figure 1. Feedback Resistor Divider

The following equation approximates the values shown in Table 1:

$$R_T = \frac{61.9}{f_S - 0.009} - 1.9$$

where R_T is in kΩ and f_S is in MHz.

Selection of the operating frequency is mainly a trade-off between efficiency and component size. The advantage of high frequency operation is that smaller inductor and capacitor values may be used. The advantage of low frequency operation is higher efficiency.

The high switching frequency also decreases the duty cycle range because of finite minimum on- and off-times independent of the switching frequency. The minimum and maximum duty cycles are:

$$DC_{MIN} = f_S \bullet t_{ON(MIN)}$$

$$DC_{MAX} = 1 - f_S \bullet t_{OFF(MIN)}$$

where f_S is the switching frequency, $t_{ON(MIN)}$ is the minimum switch on-time, and $t_{OFF(MIN)}$ is the minimum switch off-time. These equations illustrate how duty cycle range increases when switching frequency decreases. Information about individual channel minimum on and off times can be found in the Electrical Characteristics table and Typical Performance curves section.

APPLICATIONS INFORMATION

The internal oscillator of the LT8601 can be synchronized to an external 250kHz to 2.2MHz clock signal on the SYNC pin.

V_{IN} Voltage Range

The LT8601's minimum operating voltage is 3V. To program a higher minimum operating voltage, use a resistor divider between the V_{IN} pin and the EN/UVLO pin. The EN/UVLO threshold is 1.2V. The EN/UVLO pin has 50mV of hysteresis to prevent glitches from falsely disabling the LT8601.

The UVLO circuit is shown in Figure 3, Reverse Protection Diodes. The calculation for the lockout voltage is:

$$V_{IN(UVLO)} = \frac{R_{UV1}+R_{UV2}}{R_{UV2}} \bullet 1.2V$$

PV_{IN} Voltage Range

Each switching regulator channel operates from its own PV_{IN} pin (PV_{IN1} to PV_{IN3}). The PV_{IN} pin can be connected to either an independent voltage supply or a high voltage channel output. The PV_{IN1} and PV_{IN2} voltage range is 3.0V to 42V. The PV_{IN3} voltage range is 2.6V to 5.5V.

The minimum PV_{IN} voltage to regulate output voltage at full frequency is:

$$PV_{INx(MIN)} = \frac{V_{OUTx}}{DC_{MAX}}$$

where DC_{MAX} is the maximum duty cycle (refer to Switching Frequency section) for that channel. If PV_{IN} is below the calculated minimum voltage, the channel starts to skip switch off-cycles. At low input voltages, the part will turn on the top switch for longer than a full switch cycle in order to extend the effective duty cycle. When the part is extending the effective duty cycle, the switching frequency will drop to one half (or less) of the programmed frequency.

The maximum PV_{IN} voltage to regulate output voltage at full frequency is:

$$PV_{INx(MAX)} = \frac{V_{OUTx}}{DC_{MIN}}$$

where DC_{MIN} is the minimum duty cycle (refer to Switching Frequency section) for that channel. If PV_{IN} is above the calculated maximum voltage, the channel starts to skip switch on-cycles (pulse-skipping). In this case, the channel switching frequency will no longer be the programmed frequency. The output will continue to regulate, but the peak inductor current and output ripple will increase significantly.

Inductor Selection

Inductor selection involves inductance, saturation current, series resistance (DCR) and magnetic loss.

A good starting point for the inductance values are:

$$Lx = Kx \bullet \frac{V_{OUTx}}{PV_{INx}} \bullet \frac{PV_{INx} - V_{OUTx}}{f_S}$$

where f_S is the switching frequency in MHz, Lx is in µH, V_{OUTx} is the channel output voltage and K1 = 1.7, K2 = 1.0 and K3 = 1.4.

Once the inductance is selected, the inductor current ripple and peak current can be calculated:

$$\Delta I_{Lx} = \frac{V_{OUTx}}{Lx \bullet f_S} \bullet \left(1 - \frac{V_{OUTx}}{PV_{INx(MAX)}}\right)$$

$$I_{Lx(PEAK)} = I_{OUTx(MAX)} + \frac{\Delta I_{Lx}}{2}$$

To guarantee sufficient output current, peak inductor current must be lower than the switch current limit (I_{LIM}).

To keep the efficiency high, the inductor series resistance (DCR) should be as small as possible (must be < 0.1Ω channels 1 and 3; < 0.06 Ω channel 2), and the core material should be intended for the chosen switching frequency. Table 2 lists several vendors and suitable inductor series.

Table 2. Inductor Vendors

VENDOR	SERIES	WEBSITE
TDK	SLF, VLC, VLF	www.tdk.com
Sumida	CDRH, CDR, CDMC	www.sumida.com
Coilcraft	XAL, XFL, MSS	www.coilcraft.com
NIC	NPIM, NPIS	www.niccomp.com
Würth	TPC, SPC, PD, PDF, PD3	www.we-online.com

APPLICATIONS INFORMATION

Of course, such a simple design guide will not always result in the optimum inductors for the applications. A larger value inductor provides a slightly higher maximum load current and will reduce the output voltage ripple. A larger value inductor can result in higher efficiency if the DCR and magnetic losses are the same. However, for inductors of the same dimensions, the larger value inductor has higher DCR. The trade-off between inductance and DCR is not always obvious. Use experiments to find optimum inductors.

Low inductance may result in discontinuous mode operation, which is acceptable, but reduces maximum load current. For details of maximum output current and discontinuous mode operation, see the Linear Technology Application Note 44. For duty cycles greater than 50%, there is a minimum inductance required to avoid subharmonic oscillations.

$$L_{MINx} = \frac{1.05 \bullet \left(V_{OUTx} + V_{BOTx}\right)}{f_S}, \text{ chs 1 and 3}$$

$$L_{MINx} = \frac{0.70 \bullet \left(V_{OUTx} + V_{BOTx}\right)}{f_S}, \text{ ch 2}$$

where V_{OUTx} is the output voltage; V_{BOTx} is the voltage across the bottom switch; f_S is the switching frequency in MHz and L_{MINx} is in µH. If the frequency is synchronized over a range, use the lowest frequency to determine L_{MINx}.

Shorted Output Protection

If the bottom MOSFET current exceeds the valley current limit at the start of a clock cycle, the top MOSFET is kept off until the overcurrent situation clears. This prevents the buildup of inductor current during a shorted output. Further, during overload or short-circuit conditions, the LT8601 safely tolerates operation with a saturated inductor.

Input Capacitor Selection

Bypass each PV_{IN} pin of the LT8601 with a ceramic capacitor of X7R or X5R type.

Step-down converters draw current from the input supply in pulses with very fast rise and fall times. The input capacitor is required to reduce the resulting voltage ripple at the LT8601 input and to force this switching current into a tight local loop, minimizing EMI. The input capacitor must have low impedance at the switching frequency to do this effectively and it must have an adequate ripple current rating.

The worst case ripple current is when V_{OUT} is one half of PV_{IN}. In this case, the ripple current is:

$$I_{CIN(RMS)} = \frac{I_{OUT}}{2}$$

A reasonable value for the input capacitor is:

$$\frac{4.7\mu F}{f_S}, \text{ Chs 1 and 3}$$

$$\frac{10\mu F}{f_S}, \text{ Ch 2}$$

where f_S is the switching frequency in MHz.

Careful placement of C_{IN} is essential to get the lowest ripple and EMI. C_{IN} should be placed as close to the PV_{IN} pin as possible and on the same side of the PC board. The layer immediately below the component traces should be an unbroken ground plane. The ground side of C_{IN} should have at least 2 vias to the ground plane as close to C_{IN} as possible. This provides a high frequency return path directly under the PV_{IN} to C_{IN} trace. This minimizes loop area of the high frequency, high current path from PV_{IN} to C_{IN} and back to the GND exposed pad. See Figure 8, Recommended PCB Layout.

A word of caution is in order regarding the use of ceramic capacitors at the input. A ceramic input capacitor can combine with stray inductance to form a resonant tank circuit back to the supply. If power is applied quickly (for example by plugging the circuit into a live power source), this tank can ring, as much as doubling the input voltage. The solution is to either clamp the input voltage or dampen the tank circuit by adding a lossy capacitor in parallel with the ceramic capacitor. For details, see Linear Technology Application Note 88.

APPLICATIONS INFORMATION

Output Capacitor Selection

The output capacitor performs two functions. First, it filters the inductor current to generate an output with low voltage ripple. Second, it stores energy to minimize overshoot during transient loads. Because the LT8601 operates at a high frequency, minimal output capacitance is necessary. The control loop operates well with or without the presence of output capacitor series resistance (ESR). Ceramic capacitors, which achieve very low output ripple and small circuit size, are therefore an option.

You can estimate output ripple with the following equations:

$$V_{RIPPLE} = \frac{\Delta I_L}{8 \bullet f_S \bullet C_{OUT}}, \text{ for ceramic}$$

$$V_{RIPPLE} = \Delta I_L \bullet ESR, \text{ for aluminum or tantalum.}$$

where V_{RIPPLE} is the peak-to-peak output ripple, f_S is the switching frequency in MHz, ΔI_L is the peak-to-peak ripple current in the inductor, C_{OUT} is the output capacitor value in µF and ESR is the output capacitor series resistance.

Another constraint on the output capacitor is that it must have greater energy storage than the inductor. When the load current steps from high to low, the stored energy in the inductor transfers to the output and the resulting voltage step should be small compared to the regulation voltage. For a 5% overshoot, this requirement indicates:

$$C_{OUT} \geq 10 \bullet L \bullet \left(\frac{I_{LIM}}{V_{OUT}} \right)^2$$

where I_{LIM} is the maximum switch current limit. For applications that intend to operate near minimum on-time, larger output capacitance values may be required to minimize output voltage ripple than described by the equations in this section.

The low ESR and small size of ceramic capacitors make them the preferred type for LT8601 applications. Not all ceramic capacitors are the same, however. Many of the higher value capacitors use poor dielectrics with high temperature and voltage coefficients. In particular, Y5V and Z5U types lose a large fraction of their capacitance with applied voltage and at temperature extremes. Because loop stability and transient response depend on the value of C_{OUT}, this loss may be unacceptable. Use X7R or X5R types.

Electrolytic capacitors are also an option. The ESRs of most aluminum electrolytic capacitors are too large to deliver low output ripple. Tantalum, as well as newer, lower-ESR, organic electrolytic capacitors intended for power supply use are suitable. Chose a capacitor with a low enough ESR for the required output ripple. Because the volume of the capacitor determines its ESR, both the size and the value will be larger than a ceramic capacitor that would give similar ripple performance. One benefit is that the larger capacitance may give better transient response for large changes in load current. Table 3 lists several capacitor vendors.

Table 3. Low ESR Capacitor Vendors

VENDOR	SERIES	TYPE
Murata www.murata.com		Ceramic
TDK www.tdk.com		Ceramic
Kemet www.kemet.com	 T494, T495 T510, T520, T525, T530 A700	Ceramic Tantalum Tantalum Organic Polymer Alum. Organic Polymer
Panasonic www.panasonic.com	 SP-CAP	Ceramic Alum. Organic Polymer
AVX www.avx.com	 TPS, TES, TCH	Ceramic Tantalum

BST and SW Pin Considerations

The high voltage channels require a voltage above PV_{IN} to drive the gates of the top NFET switches. Connect an external capacitor between the BST and SW pins. An internal MOS switch connects BST to the internal $INTV_{CC}$ supply during the switch off-cycles. Then BST is boosted to approximately 3.3V above SW during the switch on-cycles. In most cases, a 0.1µF capacitor will work well.

APPLICATIONS INFORMATION

Soft-Start

The LT8601 has a soft-start pin for each high voltage channel and internal soft-start for each low voltage channel. The low voltage channel soft-start is set to 1ms.

On the high voltage channels, the feedback pin voltage is regulated to the lower of the corresponding TRKSS pin and the internal reference of 1V. A capacitor from the TRKSS pin to ground is charged by an internal 2.4µA current source resulting in an output ramping linearly from 0V to the regulated voltage. The duration of the ramp is:

$$t_{SS} = C_{TRKSS} \bullet \frac{1V}{2.4\mu A}$$

where t_{SS} is the ramping time in seconds and C_{TRKSS} is the capacitance on the TRKSS pin in F.

The TRKSS pin is pulled down through approximately 200Ω at start-up until $INTV_{CC}$ has reached operating voltage. It is also pulled down when an undervoltage condition is detected by either the internal lockout on PV_{IN} or the programmable EN/UVLO pin.

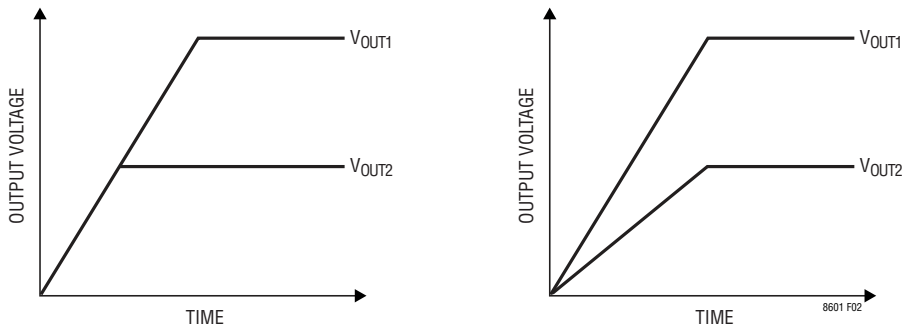
The TRKSS pin can be used to allow the output of one regulator to track the output of another regulator. To achieve coincident tracking, connect a resistor divider, R_{TR1} and R_{TR2}, from the master output to ground and tie the R_{TR1}, R_{TR2} common node to the TRKSS pin of slave regulator. To achieve ratiometric tracking, connect both TRKSS1 and TRKSS2 to a single capacitor to ground. Figure 2 shows the output waveforms for both coincident and ratiometric tracking. Note: Pulling TRKSS1 and TRKSS2 to ground does not guarantee the respective channel will never display a switching cycle.

For applications with a startup sequence that requires a PG pin be tied to a TRKSS input, a 10k or less resistor must be used as an external pull-up. The soft-start time with this configuration can be approximated by:

$$t_{SS} = 0.5 \bullet R_{PULLUP} \bullet C_{TRKSS}$$

A more exact formula, that includes the dependence on the pull-up voltage, V_{PULLUP}, is given by:

$$t_{SS} = R_{PULLUP} \bullet C_{TRKSS} \bullet Log_e \left(\frac{V_{PULLUP}}{V_{PULLUP} - 1} \right)$$



(2a) Coincident Tracking **(2b) Ratiometric Tracking**

Figure 2. Example Tracking Output Waveforms

APPLICATIONS INFORMATION

Reverse Protection

In battery charging applications or in battery backup systems, an output will be held high by the battery when the input to the LT8601 is absent. If the V_{IN} and PV_{IN} pins are floated and the LT8601 is enabled, the internal circuitry will pull its quiescent current through the SW pin of the output that is held high. This is acceptable if the system can tolerate a small current (< 100µA) in this state. If the LT8601 is disabled, the SW pin current will drop to essentially zero. However, if the V_{IN} or PV_{IN} pin is grounded while the output is held high, an external diode is required at the V_{IN}/PV_{IN} pin to prevent current being pulled out of the V_{IN}/PV_{IN} pin. An example is shown in Figure 3. In this case, both OUT1 and OUT3 are held high by batteries. PV_{IN1} and PVI_{N3} must be diode protected if they are connected to external supplies.

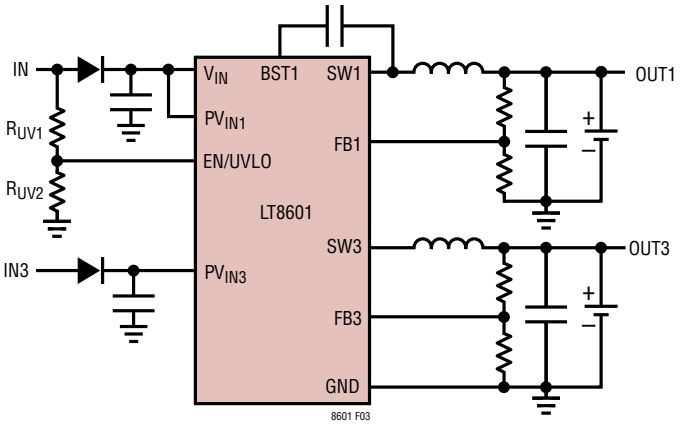


Figure 3. Reverse Protection Diodes

Burst Mode Operation

To improve efficiency at light loads, the LT8601 automatically switches to Burst Mode operation which minimizes the switching loss and keeps the output voltage ripple small. In Burst Mode operation, most of the circuits are shut down between switch-on bursts to minimize power loss. If at least one channel remains full frequency, the oscillator remains on and all bursts are synchronized to the appropriate phase of the oscillator (Figure 4). If all three channels go into Burst Mode operation, the oscillator will also shut off between bursts with a further savings in power (Figure 5). Because the channels of the LT8601 may have different loads, channels can have different switching frequencies when in Burst Mode operation.

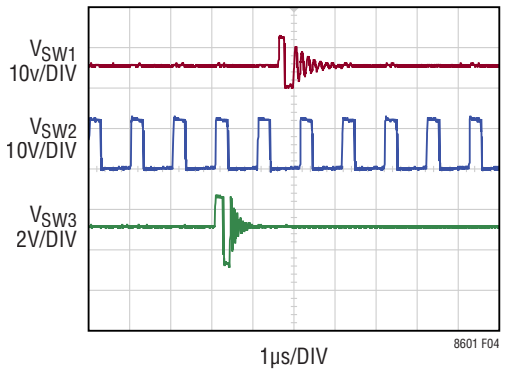


Figure 4. Burst Mode Operation SW Waveforms with Oscillator Running

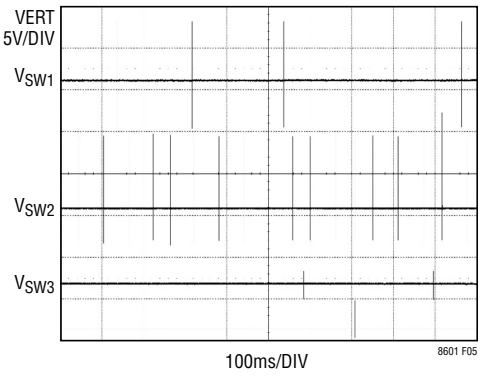


Figure 5. Burst Mode Operation SW Waveforms with All Channels in Burst Mode Operation

Mode Selection and Synchronization

To select low ripple Burst Mode operation, the SYNC pin should be connected to a voltage below 0.3V such as ground. To select pulse-skipping operation, connect the SYNC pin to an available voltage above 1.2V such as $INTV_{CC}$.

To synchronize the LT8601 to an external frequency, drive the SYNC pin with a square wave between 20% and 80% duty cycle with a high voltage above 1.2V and a low voltage below 0.3V. If the negative or positive pulse widths are less than 140ns, use a high voltage above 1.4V and a low voltage below 0.2V. The LT8601 will not enter Burst Mode operation at low output loads while synchronized to an external clock but instead will pulse skip to maintain regulation. The LT8601 may be synchronized over a 250kHz to 2.2MHz range. The R_T resistor should be chosen to set the LT8601 switching frequency equal to the synchronization input. If a range of frequencies is

APPLICATIONS INFORMATION

used, set R_T to the center of the range. For example, if the synchronization signal will be 400kHz to 600kHz, the R_T should be selected for 500kHz.

For some applications it is desirable for the LT8601 to operate in pulse-skipping mode, offering two major differences from Burst Mode operation. First, in pulse-skipping mode the clock stays awake at all times and all switching cycles are aligned to the clock. Second, full frequency switching is reached at a lower output load in pulse-skipping than Burst Mode operation. These two differences come at the expense of increased quiescent current for pulse-skipping. To enable pulse-skipping mode, the SYNC pin is tied high either to a logic output or to the $INTV_{CC}$ pin.

Do not leave the SYNC pin floating.

Power Good Comparators

Each channel of the LT8601 has a power good comparator that monitors their corresponding feedback voltage when the LT8601 is enabled. The threshold of power good comparator is 0.92V to 1.08V for the high voltage channels, and 736mV to 864mV for the low voltage channel. The PG outputs are open-drain and have a recommended external pull-up resistance value of 20k or less. An appropriate pull-up resistance value will take into consideration the specific application configuration and the leakage current of the PG pin.

Power-On Reset Timer

The power-on reset timer circuit provides a programmable reset timer. The POREN pin is the enable for the reset timer and includes a 1µA (typical) internal pull-up. Once enabled, the reset timer begins an internal clock counter that terminates after 64 cycles. Upon counter termination, the $\overline{RST}$ open-drain output releases allowing the pin to transition high. The $\overline{RST}$ output includes a weak, 100kΩ, internal pull-up resistor to approximately 2V.

The power-on reset timeout period, $t_{\overline{RST}}$, can be programmed by connecting a capacitor, C_{POR}, between the CPOR pin and ground. The value of $t_{\overline{RST}}$ is calculated by:

$$t_{\overline{RST}} = 35.2 \bullet C_{POR}$$

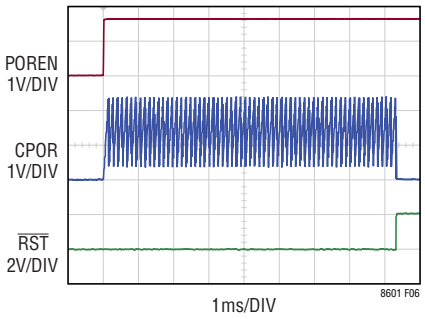


Figure 6. Power-On Reset Timing

where C_{POR} is in pF and $t_{\overline{RST}}$ is in microseconds. For example, using a capacitor value of 8.2nF gives a 289ms reset timeout period. The accuracy of $t_{\overline{RST}}$ will be determined by several factors including the accuracy and temperature coefficient of the capacitor CPOR, parasitic capacitance on the CPOR pin and board trace, and system noise. It is not recommended to use capacitor values greater than 10nF for best accuracy. Figure 6 shows the power-on reset timing.

Sequencing

The LT8601 provides great flexibility in sequencing the 3 channels and the power-on reset timer. Each channel has a power good output (PG1 to PG3) and a controlling input (TRKSS1, TRKSS2 and RUN3). The POR has a control input (POREN) and a reset output ($\overline{RST}$). All 4 outputs (PG1-PG3, $\overline{RST}$) are open-drain, and all 4 inputs (TRKSS1/2, RUN3, POREN) have internal pull-up currents to reduce external component counts when not driven by a PG pin. The soft-start function on the TRKSS pins will

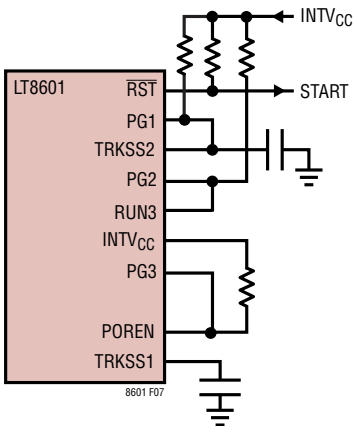


Figure 7. Sequencing the Outputs and POR

APPLICATIONS INFORMATION

work when using sequencing; simply connect the capacitor to the TRKSS pin as usual, connect an external pull-up resistor of value 10k or less, and use the desired PG output to short the cap. A sequencing example is shown in Figure 7.

In this example, channel 1 starts first, and soft-starts according to the cap on TRKSS1. Once OUT1 has reached regulation, channel 2 soft-starts. When OUT2 is good, channel 3 starts up. When OUT3 is in regulation, then the POR timer is started. One caution when connecting RUN pins to TRKSS pins: the TRKSS channel will start ramping immediately, but the RUN channel will not start until the voltage reaches the RUN threshold.

The EN/UVLO has two thresholds enabling three regions of operation. When EN/UVLO is below the shutdown threshold, the LT8601 is in low power shutdown and draws less than 1µA from V_{IN}. The shutdown threshold is typically between 0.4V and 1.1V. When the EN/UVLO is above the shutdown threshold but below the undervoltage threshold, the internal bias circuitry starts but the regulators' output switches are disabled. The input current in this region typically ranges between 1µA and 400µA depending on several factors including the mode selected and the voltage at V_{IN}. When the EN/UVLO is above the undervoltage threshold, normal operation is active.

PCB Layout

For proper operation and minimum EMI, care must be taken during printed circuit board layout. Figure 8 shows the recommended component placement with trace, ground plane and via locations. Note that large, switched currents flow in the LT8601's PV_{IN} pins, GND pins, and the input capacitors. The loop formed by the input capacitor should be as small as possible by placing the capacitor close to the PV_{IN} pin and the adjacent GND pin. When using a physically large input capacitor, the resulting loop may become too large in which case using a small case/value capacitor placed close to the PV_{IN} and GND pins plus a larger capacitor further away is preferred. These components, along with the inductor and output capacitor, should be placed on the same side of the circuit board, and their connections should be made on that layer. Place a local, unbroken ground plane under the application circuit on the layer closest to the surface layer. The SW and BOOST nodes should be as small as possible. Finally, keep the FB and R_T nodes small so that the ground traces will shield them from the SW and BOOST nodes. The exposed pad on the bottom of the package must be soldered to ground to provide a good electrical connection as well as a good thermal connection so that the PCB can act as a heat sink. To keep thermal resistance low, extend the ground plane as much as possible, and add thermal vias under and near the LT8601 to additional ground planes within the circuit board and on the bottom side.

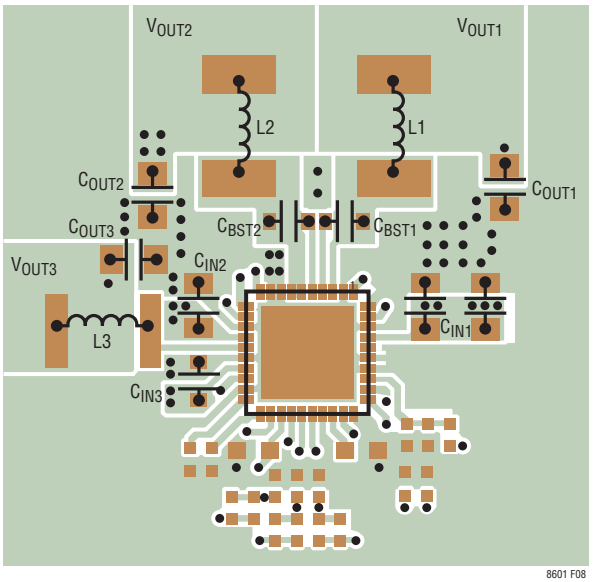


Figure 8. Recommended PCB Layout

APPLICATIONS INFORMATION

Thermal Considerations

Care should be taken in the layout of the PCB to ensure good heat sinking of the LT8601. The exposed pad on the bottom of the package must be soldered to a ground plane. This ground should be tied to large copper layers below with thermal vias; these layers will spread heat dissipated by the LT8601. Recommended layer use for a 4-layer board is:

Layer 1 (Components): use 2oz copper; unbroken high frequency/high current routing (C_{IN} loop, SW node, BST node, inductor, C_{OUT}), high current DC routing, ground plane on remainder

Layer 2 (Internal): Unbroken ground plane

Layer 3 (Internal): Signal routing, ground plane on remainder

Layer 4 (Bottom): Use 2oz copper; high current DC routing (V_{IN}, V_{OUT}), ground plane on remainder

Placing additional vias can reduce thermal resistance further. Many small thermal vias are better than a few large ones. Following these PCB design guidelines can reduce θ_{JA} to 22°C/W.

Power dissipation within the LT8601 can be estimated by adding the power dissipated in each channel. Calculate each channel's power loss from an efficiency measurement and subtract the inductor loss. The die temperature is calculated by multiplying the total LT8601 power dissipation by the thermal resistance from junction to ambient θ_{JA}, and adding the ambient temperature. The maximum load current should be derated as the die temperature approaches the maximum junction rating. The LT8601 will stop switching if the internal temperature rises too high. This thermal protection is above the maximum operating temperature and is intended as a failsafe only.

Even with the best thermal practices, the LT8601 must be derated at high ambient temperature. The thermal derating curves in Figure 9 show the front page application (Ch1: 5V, Ch2: 3.3V, Ch3: 1.8V). The PCB layout is as described above and the θ_{JA} is 22°C/W. The output currents are decreased uniformly as a percentage of maximum. Although derating is application dependent, this set of curves is representative of typical applications with a range of frequencies and input voltages.

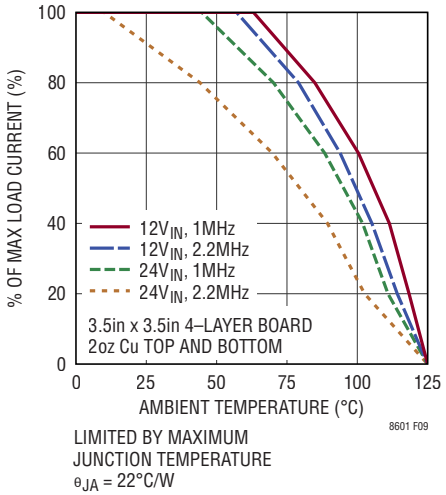
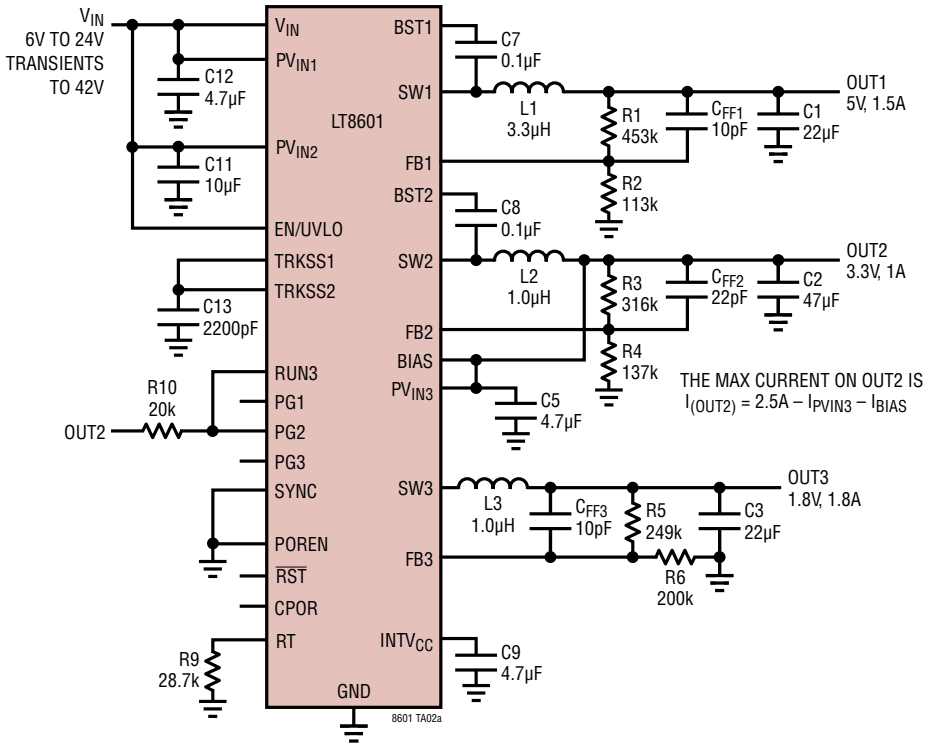


Figure 9. Thermal Derating, E- and I-Grade

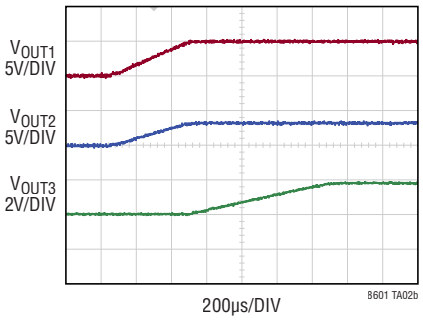
TYPICAL APPLICATIONS

Details of Front Page Application



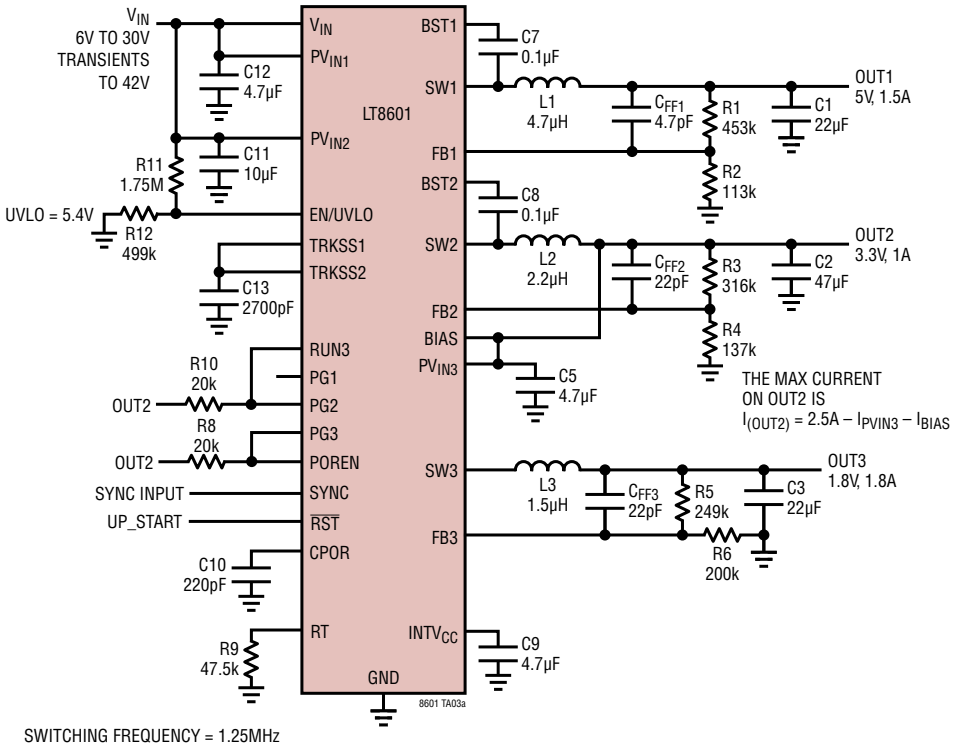
THE VALUES SHOWN ARE FOR 2MHz OPERATION. FOR 1MHz OPERATION, MAKE THE FOLLOWING CHANGES:
L1 = 6.2µH, CFF1 = 4.7pF, L2 = 2.7µH, L3 = 2.2µH, R9 = 60.4k.
AT 1MHz OPERATION, THE INPUT VOLTAGE RANGE IS 6V TO 42V.

Start-Up Sequence



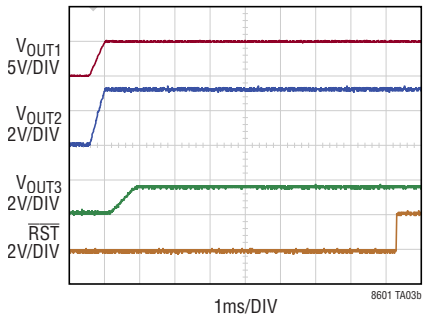
TYPICAL APPLICATIONS

Automotive Input Steps Down to 5V, 3.3V, 1.8V



SWITCHING FREQUENCY = 1.25MHz

Start-Up Sequence

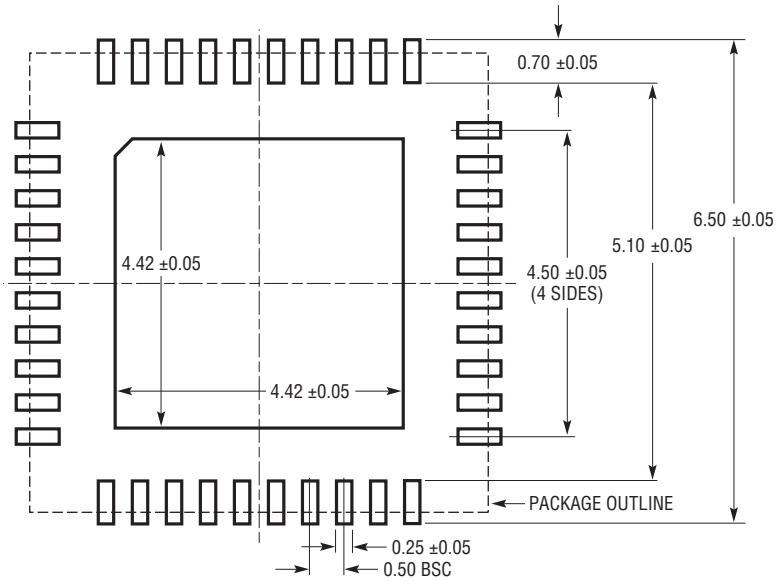


START-UP SEQUENCE:
CH1 AND CH2 SOFT-START
RATIOMETRICALLY;
THEN CH3 TURNS ON;
THEN POR TIMER STARTS.

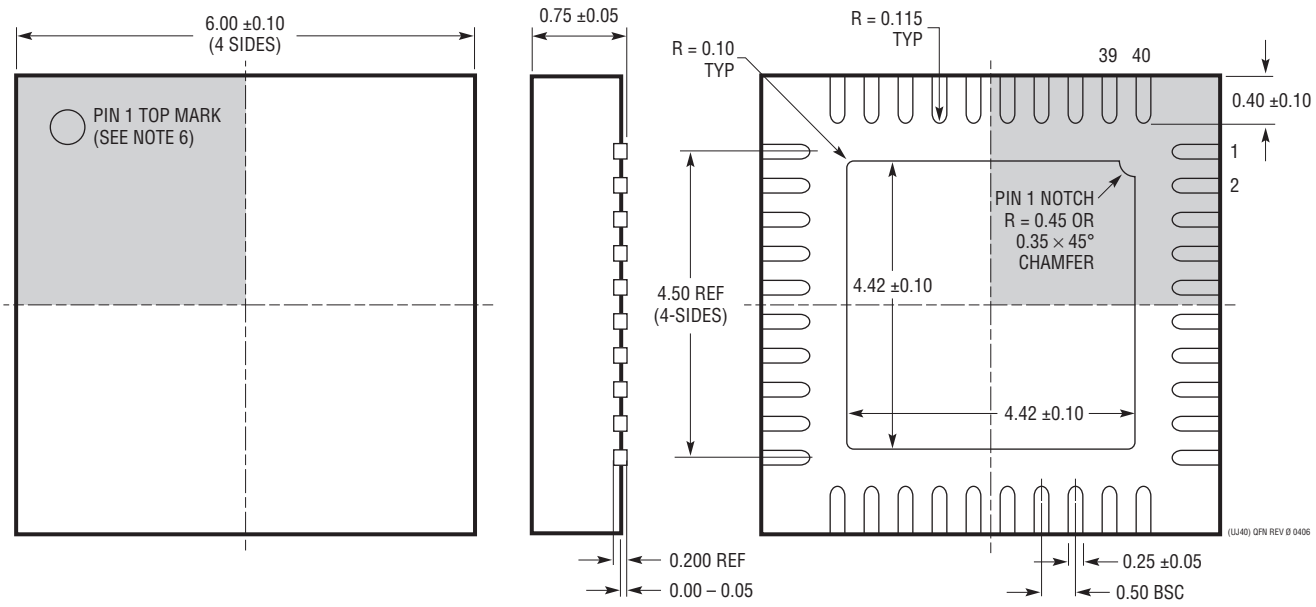
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LT8601#packaging for the most recent package drawings.

UJ Package
40-Lead Plastic QFN (6mm × 6mm)
(Reference LTC DWG # 05-08-1728 Rev Ø)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



BOTTOM VIEW—EXPOSED PAD

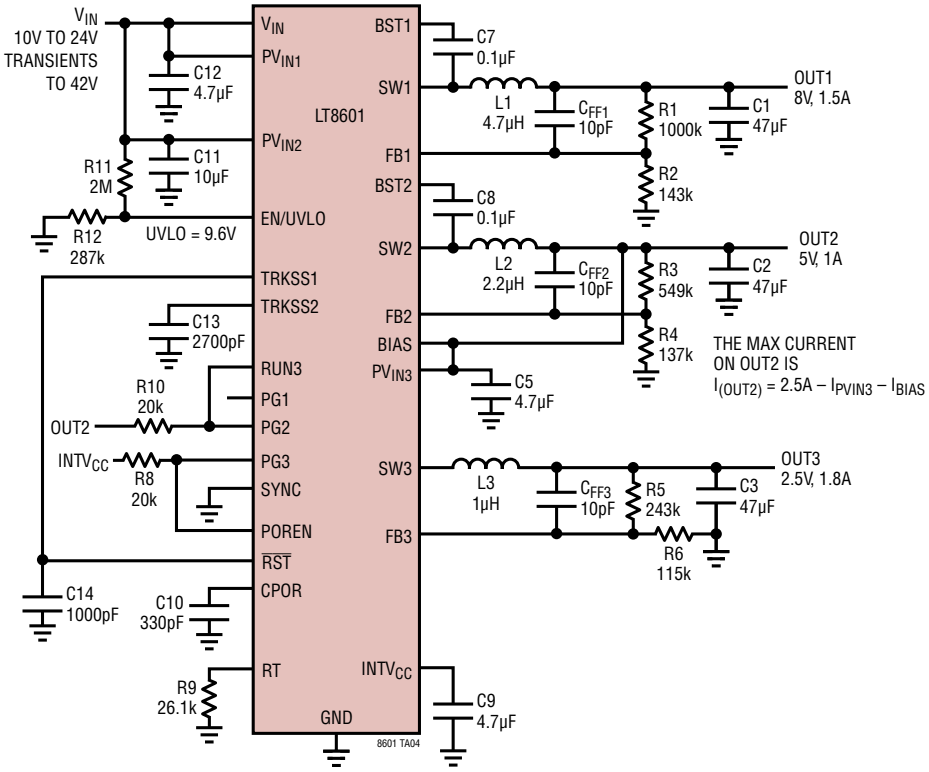
NOTE:
1. DRAWING IS A JEDEC PACKAGE OUTLINE VARIATION OF (WJJD-2)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE
   MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE, IF PRESENT
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	06/17	Clarified Resitor Value for 2MHz Switching.	3
		Clarified Channels 1, 2, 3 Feedback Voltage Limits.	3, 4
		Clarified RUN3 Threshold Upper Limits.	4
		Clarified $\overline{RST}$ Pull-Up Current.	4
		Clarified R_T Value on Bottom Graphs.	8
		Clarified Conditions for EMI Performance Graphs.	9
		Clarified $INTV_{CC}$ (Pin 28) Description.	10
		Clarified BST and SW Pin Considerations Paragraph.	16
		Clarified Mode Selection and Synchronization Paragraph.	18
		Clarified Values in Power-On Reset Timer Paragraph.	19
		Clarified Sequencing Paragraph.	20

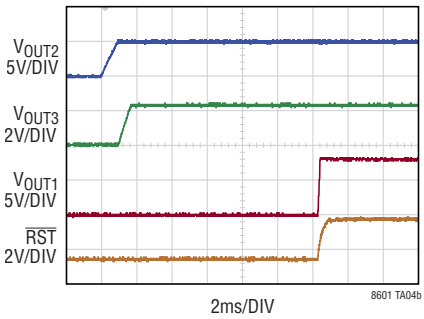
TYPICAL APPLICATION

Wide Range Input Stepped Down to 5V, 2.5V and 8V (Delayed)



SWITCHING FREQUENCY = 2.2MHz

Start-Up Sequence



START-UP SEQUENCE:
CH2 SOFT-STARTS;
THEN CH3 TURNS ON;
THEN POR TIMER STARTS;
AFTER POR TIMES OUT, THEN
CH1 STARTS.

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT8602	42V, Quad Output (2.5A+1.5A+1.8A+1.8A) 95% Efficiency, 2.2MHz Synchronous Micropower Step-Down DC/DC Converter with I_Q = 25µA	V_{IN} = 3V to 42V, $V_{OUT(MIN)}$= 0.8V, I_Q = 25µA, I_{SD} < 1µA, 6mm × 6mm QFN-40 Package
LT3507/LT3507A	36V, 2.7A + 1.8A + 1.8A + LDO Controller, 2.5MHz, High Efficiency, Triple Output Step-Down DC/DC Converter	V_{IN} = 4V to 36V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 7mA, I_{SD} < 1µA, 5mm × 7mm QFN
LT8640	42V, 6A, 96% Efficiency, 2.2MHz Synchronous Micropower Step-Down DC/DC Converter with I_Q = 2.5µA	V_{IN} = 3.4V to 42V, $V_{OUT(MIN)}$ = 0.985V, I_Q = 2.5µA, I_{SD} < 1µA, 3mm × 4mm QFN
LT8614	42V, 4A, 96% Efficiency, 2.2MHz Synchronous Micropower Step-Down DC/DC Converter with I_Q = 2.5µA	V_{IN} = 3.4V to 42V, $V_{OUT(MIN)}$ = 0.985V, I_Q = 2.5µA, I_{SD} < 1µA, 3mm × 4mm QFN
LT8612	42V, 6A, 96% Efficiency, 2.2MHz Synchronous Micropower Step-Down DC/DC Converter with I_Q = 2.5µA	V_{IN} = 3.4V to 42V, $V_{OUT(MIN)}$ = 0.985V, I_Q = 2.5µA, I_{SD} < 1µA, 3mm × 6mm QFN
LT8610/LT8610A/ LT8610AB/LT8610AC	42V, 2.5A, 96% Efficiency, 2.2MHz Synchronous Micropower Step-Down DC/DC Converter with I_Q = 2.5µA	V_{IN} = 3.4V to 42V, $V_{OUT(MIN)}$ = 0.985V, I_Q = 2.5µA, I_{SD} < 1µA, MSOP-16E
LT8611	42V, 2.5A, 96% Efficiency, 2.2MHz Synchronous Micropower Step-Down DC/DC Converter with I_Q = 2.5µA and Input/Output Current Limit/Monitor	V_{IN} = 3.4V to 42V, $V_{OUT(MIN)}$ = 0.985V , I_Q = 2.5µA, I_{SD} < 1µA, 3mm × 5mm QFN-24

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