THE DATASHEET OF

LTC2242CUP-10#PBF

10-Bit, 250Msps ADC

FEATURES

- **Sample Rate: 250Msps**
- **60.5dB SNR**
- **78dB SFDR**
- **1.2GHz Full Power Bandwidth S/H**
- **Single 2.5V Supply**
- **Low Power Dissipation: 740mW**
- LVDS, CMOS, or Demultiplexed CMOS Outputs
- Selectable Input Ranges: ±0.5V or ±1V
- No Missing Codes
- Optional Clock Duty Cycle Stabilizer
- Shutdown and Nap Modes
- Data Ready Output Clock
- Pin Compatible Family
  250Msps: LTC2242-12 (12-Bit), LTC2242-10 (10-Bit)
  210Msps: LTC2241-12 (12-Bit), LTC2241-10 (10-Bit)
  170Msps: LTC2240-12 (12-Bit), LTC2240-10 (10-Bit)
  185Msps: LTC2220-1 (12-Bit)*
  170Msps: LTC2220 (12-Bit), LTC2230 (10-Bit)*
  135Msps: LTC2221 (12-Bit), LTC2231 (10-Bit)*
- 64-Pin 9mm × 9mm QFN Package

APPLICATIONS

- Wireless and Wired Broadband Communication
- Cable Head-End Systems
- Power Amplifier Linearization
- Communications Test Equipment

DESCRIPTION

The LTC®2242-10 is a 250Msps, sampling 10-bit A/D converter designed for digitizing high frequency, wide dynamic range signals. The LTC2240-10 is perfect for demanding communications applications with AC performance that includes 60.5dB SNR and 78dB SFDR. Ultralow jitter of $95fs_{RMS}$ allows IF undersampling with excellent noise performance.

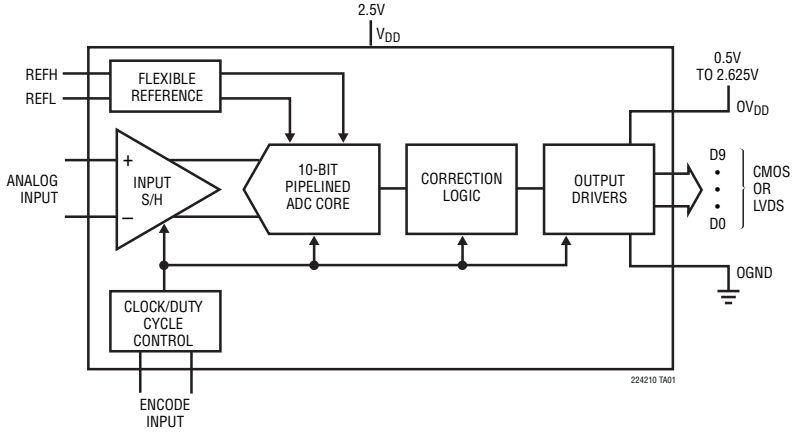
DC specs include ±0.4LSB INL (typ), ±0.2LSB DNL (typ) and no missing codes over temperature.

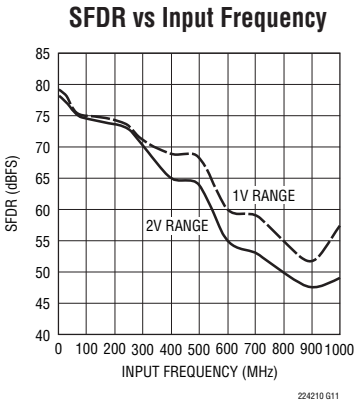
The digital outputs can be either differential LVDS, or single-ended CMOS. There are three format options for the CMOS outputs: a single bus running at the full data rate or two demultiplexed buses running at half data rate with either interleaved or simultaneous update. A separate output power supply allows the CMOS output swing to range from 0.5V to 2.625V.

The ENC$^+$ and ENC$^-$ inputs may be driven differentially or single ended with a sine wave, PECL, LVDS, TTL, or CMOS inputs. An optional clock duty cycle stabilizer allows high performance over a wide range of clock duty cycles.

*LTC2220-1, LTC2220, LTC2221, LTC2230, LTC2231 are 3.3V parts.

TYPICAL APPLICATION



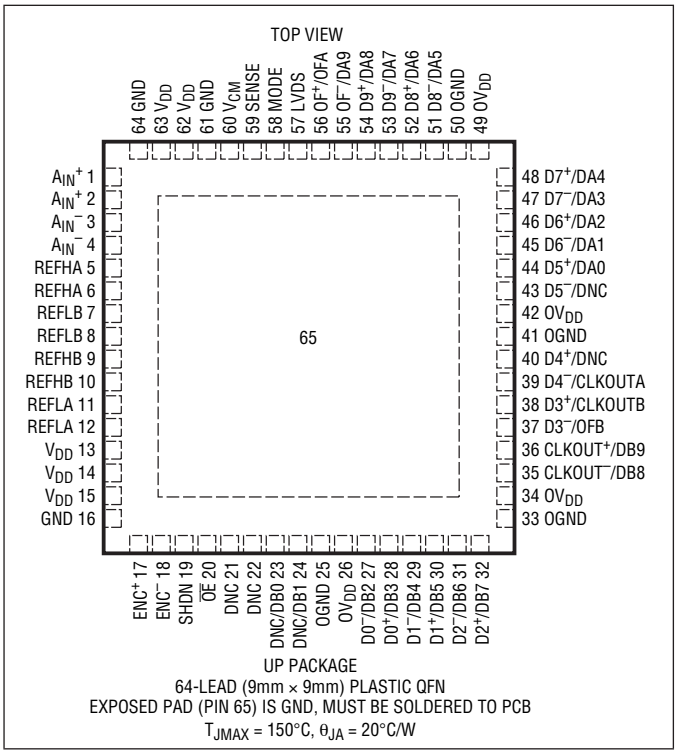


ABSOLUTE MAXIMUM RATINGS

OV_{DD} = V_{DD} (Notes 1, 2)

Supply Voltage (V_{DD}) 2.8V
Digital Output Ground Voltage (OGND) ..... –0.3V to 1V
Analog Input Voltage (Note 3) ..... –0.3V to (V_{DD} + 0.3V)
Digital Input Voltage ..... –0.3V to (V_{DD} + 0.3V)
Digital Output Voltage ..... –0.3V to (OV_{DD} + 0.3V)
Power Dissipation 1500mW
Operating Temperature Range
LTC2242C-10 ..... 0°C to 70°C
LTC2242I-10 ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



UP PACKAGE
64-LEAD (9mm × 9mm) PLASTIC QFN
EXPOSED PAD (PIN 65) IS GND, MUST BE SOLDERED TO PCB
T_{JMAX} = 150°C, θ_{JA} = 20°C/W

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC2242CUP-10#PBF	LTC2242CUP-10#TRPBF	LTC2242UP-10	64-Lead (9mm × 9mm) Plastic QFN	0°C to 70°C
LTC2242IUP-10#PBF	LTC2242IUP-10#TRPBF	LTC2242UP-10	64-Lead (9mm × 9mm) Plastic QFN	–40°C to 85°C
LEAD BASED FINISH	**TAPE AND REEL**	**PART MARKING***	**PACKAGE DESCRIPTION**	**TEMPERATURE RANGE**
LTC2242CUP-10#PBF	LTC2242CUP-10#TR	LTC2242UP-10	64-Lead (9mm × 9mm) Plastic QFN	0°C to 70°C
LTC2242IUP-10#PBF	LTC2242IUP-10#TR	LTC2242UP-10	64-Lead (9mm × 9mm) Plastic QFN	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *Temperature grades are identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

CONVERTER CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Resolution (No Missing Codes)		●	10			Bits
Integral Linearity Error	Differential Analog Input (Note 5)	●	–1	±0.4	1	LSB
Differential Linearity Error	Differential Analog Input	●	–0.7	±0.2	0.7	LSB
Offset Error	(Note 6)	●	–17	±5	17	mV
Gain Error	External Reference	●	–3.5	±0.7	3.5	%FS

CONVERTER CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Offset Drift				±10		µV/C
Full-Scale Drift	Internal Reference External Reference			±60 ±45		ppm/C ppm/C
Transition Noise	SENSE = 1V			0.18		LSB_{RMS}

ANALOG INPUT

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Analog Input Range ($A_{IN}^+ - A_{IN}^-$)	2.375V < V_{DD} < 2.625V (Note 7)	●		±0.5 to ±1		V
$V_{IN, CM}$	Analog Input Common Mode ($A_{IN}^+ + A_{IN}^-$)/2	Differential Input (Note 7)	●	1.2	1.25	1.3	V
I_{IN}	Analog Input Leakage Current	0 < A_{IN}^+, A_{IN}^- < V_{DD}	●	–1		1	µA
I_{SENSE}	SENSE Input Leakage	0V < SENSE < 1V	●	–1		1	µA
I_{MODE}	MODE Pin Pull-Down Current to GND				7		µA
I_{LVDS}	LVDS Pin Pull-Down Current to GND				7		µA
t_{AP}	Sample and Hold Acquisition Delay Time				0.4		ns
t_{JITTER}	Sample and Hold Acquisition Delay Time Jitter				95		fs_{RMS}
	Full Power Bandwidth	Figure 8 Test Circuit			1200		MHz

DYNAMIC ACCURACY

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. A_{IN} = –1dBFS. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
SNR	Signal-to-Noise Ratio (Note 10)	10MHz Input			60.6		dB
		70MHz Input	●	59.2	60.5		dB
		140MHz Input			60.5		dB
		240MHz Input			60.4		dB
SFDR	Spurious Free Dynamic Range 2nd or 3rd Harmonic (Note 11)	10MHz Input			78		dB
		70MHz Input	●	63	75		dB
		140MHz Input			74		dB
		240MHz Input			73		dB
	Spurious Free Dynamic Range 4th Harmonic or Higher (Note 11)	10MHz Input			85		dB
		70MHz Input	●	71	85		dB
		140MHz Input			85		dB
		240MHz Input			85		dB
S/(N+D)	Signal-to-Noise Plus Distortion Ratio (Note 12)	10MHz Input			60.4		dB
		70MHz Input	●	58.2	60.4		dB
		140MHz Input			60.3		dB
		240MHz Input			60.2		dB
IMD	Intermodulation Distortion	f_{IN1} = 135MHz, f_{IN2} = 140MHz			81		dBc

INTERNAL REFERENCE CHARACTERISTICS (Note 4)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CM} Output Voltage	I_{OUT} = 0	1.225	1.25	1.275	V
V_{CM} Output Tempco			±35		ppm/°C
V_{CM} Line Regulation	2.375V < V_{DD} < 2.625V		3		mV/V
V_{CM} Output Resistance	–1mA < I_{OUT} < 1mA		2		Ω

DIGITAL INPUTS AND DIGITAL OUTPUTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
ENCODE INPUTS (ENC+, ENC–)							
V_{ID}	Differential Input Voltage	(Note 7)	●	0.2			V
V_{ICM}	Common Mode Input Voltage	Internally Set Externally Set (Note 7)	 ●	 1.2	1.5 1.5	 2.0	V V
R_{IN}	Input Resistance				4.8		kΩ
C_{IN}	Input Capacitance	(Note 7)			2		pF
LOGIC INPUTS ($\overline{OE}$, SHDN)							
V_{IH}	High Level Input Voltage	V_{DD} = 2.5V	●	1.7			V
V_{IL}	Low Level Input Voltage	V_{DD} = 2.5V	●			0.7	V
I_{IN}	Input Current	V_{IN} = 0V to V_{DD}	●	–10		10	µA
C_{IN}	Input Capacitance	(Note 7)			3		pF
LOGIC OUTPUTS (CMOS MODE)							
OV_{DD} = 2.5V							
C_{OZ}	Hi-Z Output Capacitance	$\overline{OE}$ = High (Note 7)			3		pF
I_{SOURCE}	Output Source Current	V_{OUT} = 0V			37		mA
I_{SINK}	Output Sink Current	V_{OUT} = 2.5V			23		mA
V_{OH}	High Level Output Voltage	I_O = –10µA I_O = –500µA			2.495 2.45		V V
V_{OL}	Low Level Output Voltage	I_O = 10µA I_O = 500µA			0.005 0.07		V V
OV_{DD} = 1.8V							
V_{OH}	High Level Output Voltage	I_O = –500µA			1.75		V
V_{OL}	Low Level Output Voltage	I_O = 500µA			0.07		V
LOGIC OUTPUTS (LVDS MODE)							
V_{OD}	Differential Output Voltage	100Ω Differential Load	●	247	350	454	mV
V_{OS}	Output Common Mode Voltage	100Ω Differential Load	●	1.125	1.250	1.375	V

POWER REQUIREMENTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 9)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{DD}	Analog Supply Voltage	(Note 8)	●	2.375	2.5	2.625	V
P_{SLEEP}	Sleep Mode Power	SHDN = High, $\overline{OE}$ = High, No CLK			1		mW
P_{NAP}	Nap Mode Power	SHDN = High, $\overline{OE}$ = Low, No CLK			28		mW
LVDS OUTPUT MODE							
OV_{DD}	Output Supply Voltage	(Note 8)	●	2.375	2.5	2.625	V
I_{VDD}	Analog Supply Current		●		285	320	mA
I_{OVDD}	Output Supply Current		●		58	70	mA
P_{DISS}	Power Dissipation		●		858	975	mW
CMOS OUTPUT MODE							
OV_{DD}	Output Supply Voltage	(Note 8)	●	0.5	2.5	2.625	V
I_{VDD}	Analog Supply Current	(Note 7)	●		285	320	mA
P_{DISS}	Power Dissipation				740		mW

TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_S	Sampling Frequency	(Note 8)	●	1		250	MHz
t_L	ENC Low Time (Note 7)	Duty Cycle Stabilizer Off Duty Cycle Stabilizer On	● ●	1.9 1.5	2 2	500 500	ns ns
t_H	ENC High Time (Note 7)	Duty Cycle Stabilizer Off Duty Cycle Stabilizer On	● ●	1.9 1.5	2 2	500 500	ns ns
t_{AP}	Sample-and-Hold Aperture Delay				0.4		ns
$t_{\overline{OE}}$	Output Enable Delay	(Note 7)	●		5	10	ns
LVDS OUTPUT MODE							
t_D	ENC to DATA Delay	(Note 7)	●	1	1.7	2.8	ns
t_C	ENC to CLKOUT Delay	(Note 7)	●	1	1.7	2.8	ns
	DATA to CLKOUT Skew	(t_C – t_D) (Note 7)	●	–0.6	0	0.6	ns
	Rise Time				0.5		ns
	Fall Time				0.5		ns
	Pipeline Latency				5		Cycles
CMOS OUTPUT MODE							
t_D	ENC to DATA Delay	(Note 7)	●	1	1.7	2.8	ns
t_C	ENC to CLKOUT Delay	(Note 7)	●	1	1.7	2.8	ns
	DATA to CLKOUT Skew	(t_C – t_D) (Note 7)	●	–0.6	0	0.6	ns
Pipeline Latency	Full Rate CMOS				5		Cycles
	Demuxed Interleaved				5		Cycles
	Demuxed Simultaneous				5 and 6		Cycles

ELECTRICAL CHARACTERISTICS

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All voltage values are with respect to ground with GND and OGND wired together (unless otherwise noted).

Note 3: When these pin voltages are taken below GND or above V_{DD}, they will be clamped by internal diodes. This product can handle input currents of greater than 100mA below GND or above V_{DD} without latchup.

Note 4: V_{DD} = 2.5V, f_{SAMPLE} = 250MHz, LVDS outputs, differential ENC^+/ENC^- = $2V_{P-P}$ sine wave, input range = $2V_{P-P}$ with differential drive, unless otherwise noted.

Note 5: Integral nonlinearity is defined as the deviation of a code from a "best straight line" fit to the transfer curve. The deviation is measured from the center of the quantization band.

Note 6: Offset error is the offset voltage measured from –0.5 LSB when the output code flickers between 00 0000 0000 and 11 1111 1111 in 2's complement output mode.

Note 7: Guaranteed by design, not subject to test.

Note 8: Recommended operating conditions.

Note 9: V_{DD} = 2.5V, f_{SAMPLE} = 250MHz, differential ENC^+/ENC^- = $2V_{P-P}$ sine wave, input range = $1V_{P-P}$ with differential drive, output C_{LOAD} = 5pF.

Note 10: SNR minimum and typical values are for LVDS mode. Typical values for CMOS mode are typically 0.2dB lower.

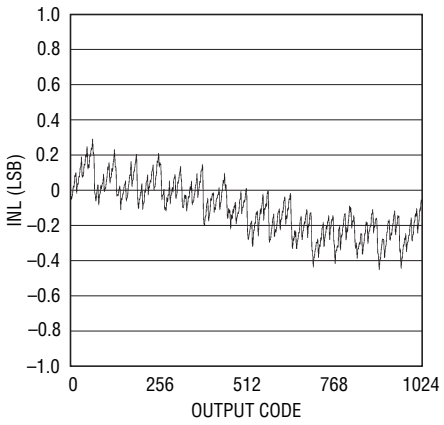
Note 11: SFDR minimum values are for LVDS mode. Typical values are for both LVDS and CMOS modes.

Note 12: SINAD minimum and typical values are for LVDS mode. Typical values for CMOS mode are typically 0.2dB lower.

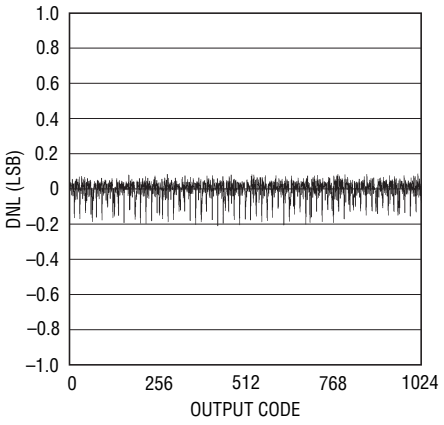
TYPICAL PERFORMANCE CHARACTERISTICS

(T_A = 25°C unless otherwise noted, Note 4)

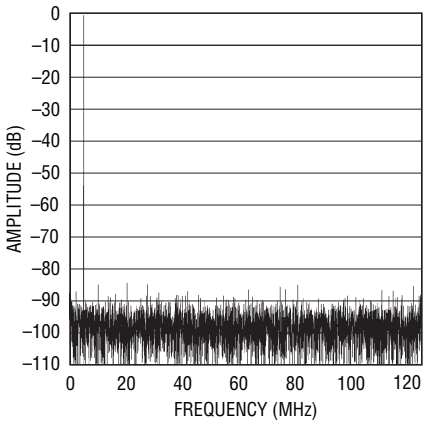
Integral Nonlinearity



Differential Nonlinearity



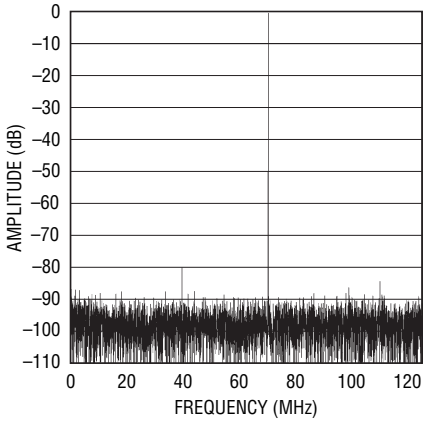
8192 Point FFT, f_{IN} = 5MHz, –1dB, 2V Range, LVDS Mode



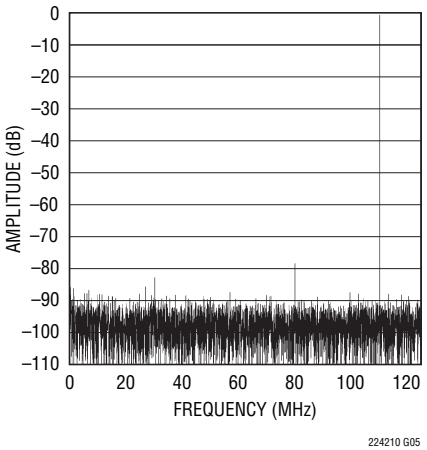
TYPICAL PERFORMANCE CHARACTERISTICS

(T_A = 25°C unless otherwise noted, Note 4)

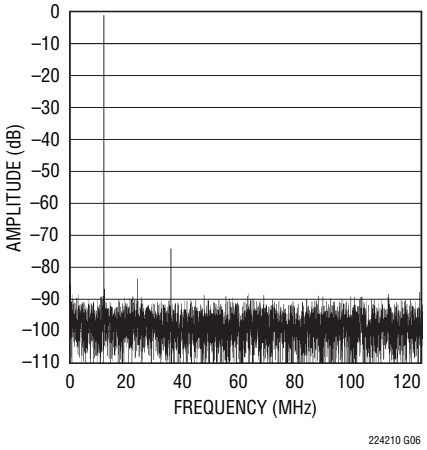
8192 Point FFT, f_{IN} = 70MHz, –1dB, 2V Range, LVDS Mode



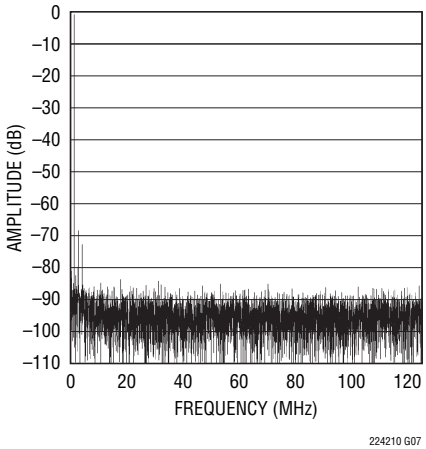
8192 Point FFT, f_{IN} = 140MHz, –1dB, 2V Range, LVDS Mode



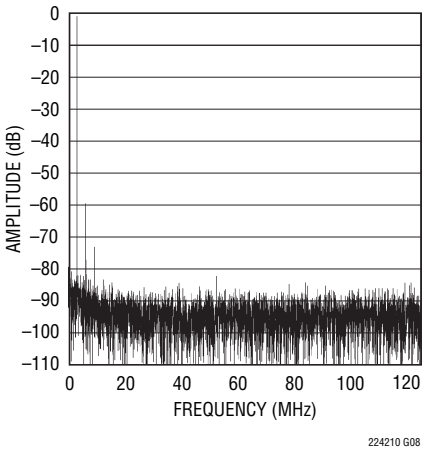
8192 Point FFT, f_{IN} = 240MHz, –1dB, 2V Range, LVDS Mode



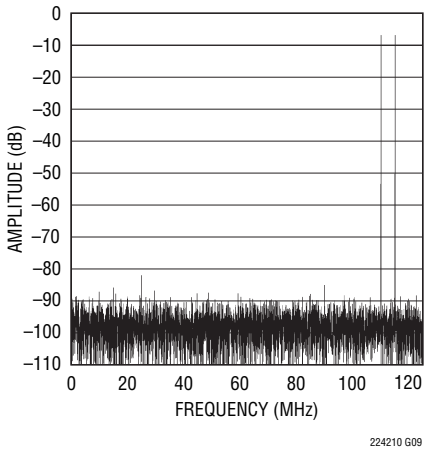
8192 Point FFT, f_{IN} = 500MHz, –1dB, 1V Range, LVDS Mode



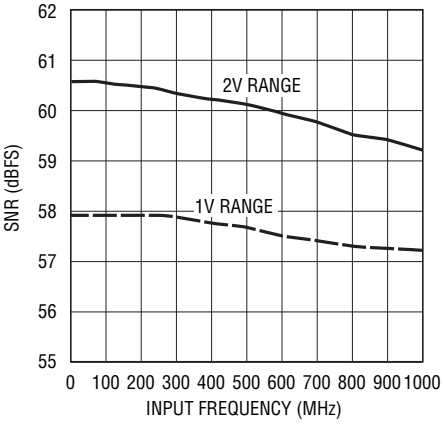
8192 Point FFT, f_{IN} = 1GHz, –1dB, 1V Range, LVDS Mode



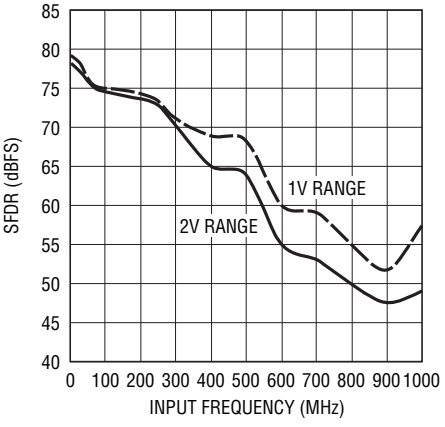
8192 Point 2-Tone FFT, f_{IN} = 135MHz and 140MHz, –1dB, 2V Range, LVDS Mode



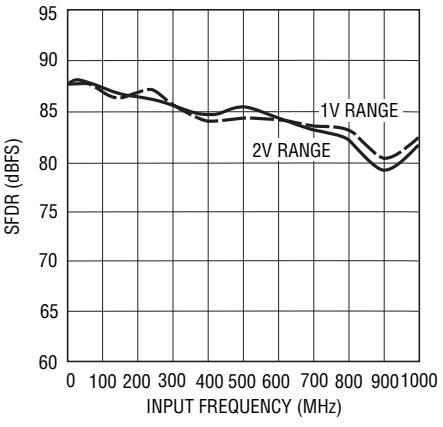
SNR vs Input Frequency, –1dB, LVDS Mode



SFDR (HD2 and HD3) vs Input Frequency, –1dB, LVDS Mode



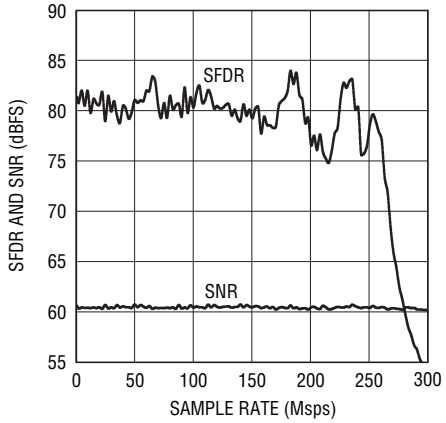
SFDR (HD4+) vs Input Frequency, –1dB, LVDS Mode



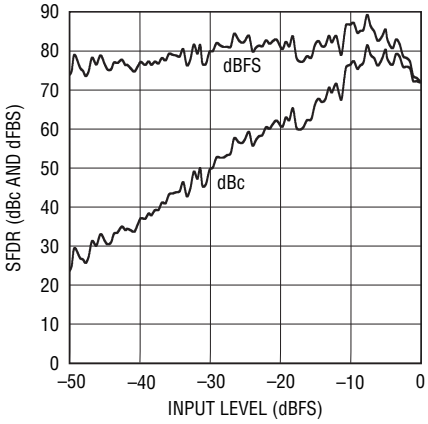
TYPICAL PERFORMANCE CHARACTERISTICS

(T_A = 25°C unless otherwise noted, Note 4)

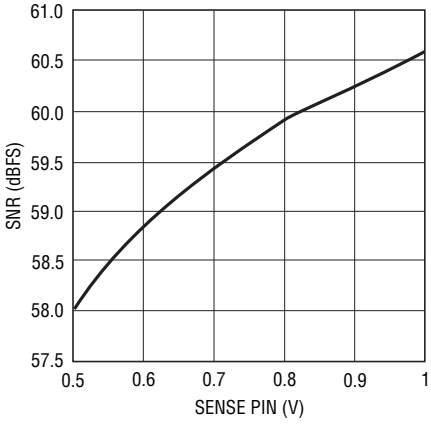
SFDR and SNR vs Sample Rate, 2V Range, f_{IN} = 30MHz, –1dB, LVDS Mode



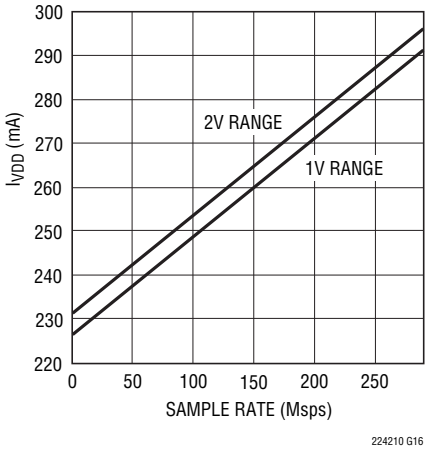
SFDR vs Input Level, f_{IN} = 70MHz, 2V Range



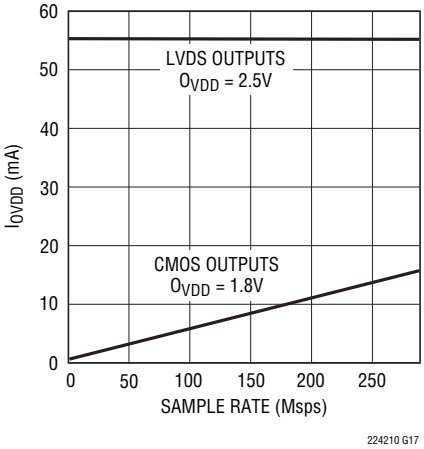
SNR vs SENSE, f_{IN} = 5MHz, –1dB



I_{VDD} vs Sample Rate, 5MHz Sine Wave Input, –1dB



I_{OVDD} vs Sample Rate, 5MHz Sine Wave Input, –1dB



PIN FUNCTIONS (CMOS Mode)

A_{IN}^+ (Pins 1, 2): Positive Differential Analog Input.

A_{IN}^- (Pins 3, 4): Negative Differential Analog Input.

REFHA (Pins 5, 6): ADC High Reference. Bypass to Pins 7, 8 with 0.1µF ceramic chip capacitor, to Pins 11, 12 with a 2.2µF ceramic capacitor and to ground with 1µF ceramic capacitor.

REFLB (Pins 7, 8): ADC Low Reference. Bypass to Pins 5, 6 with 0.1µF ceramic chip capacitor. Do not connect to Pins 11, 12.

REFHB (Pins 9, 10): ADC High Reference. Bypass to Pins 11, 12 with 0.1µF ceramic chip capacitor. Do not connect to Pins 5, 6.

REFLA (Pins 11, 12): ADC Low Reference. Bypass to Pins 9, 10 with 0.1µF ceramic chip capacitor, to Pins 5, 6 with a 2.2µF ceramic capacitor and to ground with 1µF ceramic capacitor.

V_{DD} (Pins 13, 14, 15, 62, 63): 2.5V Supply. Bypass to GND with 0.1µF ceramic chip capacitors.

GND (Pins 16, 61, 64): ADC Power Ground.

ENC^+ (Pin 17): Encode Input. Conversion starts on the positive edge.

ENC^- (Pin 18): Encode Complement Input. Conversion starts on the negative edge. Bypass to ground with 0.1µF ceramic for single-ended encode signal.

SHDN (Pin 19): Shutdown Mode Selection Pin. Connecting SHDN to GND and $\overline{OE}$ to GND results in normal operation with the outputs enabled. Connecting SHDN to GND and $\overline{OE}$ to V_{DD} results in normal operation with the outputs at high impedance. Connecting SHDN to V_{DD} and $\overline{OE}$ to GND results in nap mode with the outputs at high impedance. Connecting SHDN to V_{DD} and $\overline{OE}$ to V_{DD} results in sleep mode with the outputs at high impedance.

$\overline{OE}$ (Pin 20): Output Enable Pin. Refer to SHDN pin function.

DNC (Pins 21, 22, 40, 43): Do not connect these pins.

DB0-DB9 (Pins 23, 24, 27, 28, 29, 30, 31, 32, 35, 36): Digital Outputs, B Bus. DB9 is the MSB. At high impedance in full rate CMOS mode.

OGND (Pins 25, 33, 41, 50): Output Driver Ground.

OV_{DD} (Pins 26, 34, 42, 49): Positive Supply for the Output Drivers. Bypass to ground with 0.1µF ceramic chip capacitor.

OFB (Pin 37): Over/Under Flow Output for B Bus. High when an over or under flow has occurred. At high impedance in full rate CMOS mode.

CLKOUTB (Pin 38): Data Valid Output for B Bus. In demux mode with interleaved update, latch B bus data on the falling edge of CLKOUTB. In demux mode with simultaneous update, latch B bus data on the rising edge of CLKOUTB. This pin does not become high impedance in full rate CMOS mode.

CLKOUTA (Pin 39): Data Valid Output for A Bus. Latch A bus data on the falling edge of CLKOUTA.

DA0-DA9 (Pins 44, 45, 46, 47, 48, 51, 52, 53, 54, 55): Digital Outputs, A Bus. DA9 is the MSB.

OFA (Pin 56): Over/Under Flow Output for A Bus. High when an over or under flow has occurred.

LVDS (Pin 57): Output Mode Selection Pin. Connecting LVDS to 0V selects full rate CMOS mode. Connecting LVDS to $1/3V_{DD}$ selects demux CMOS mode with simultaneous update. Connecting LVDS to $2/3V_{DD}$ selects demux CMOS mode with interleaved update. Connecting LVDS to V_{DD} selects LVDS mode.

MODE (Pin 58): Output Format and Clock Duty Cycle Stabilizer Selection Pin. Connecting MODE to 0V selects offset binary output format and turns the clock duty cycle stabilizer off. Connecting MODE to $1/3V_{DD}$ selects offset binary output format and turns the clock duty cycle stabilizer on. Connecting MODE to $2/3V_{DD}$ selects 2's complement output format and turns the clock duty cycle stabilizer on. Connecting MODE to V_{DD} selects 2's complement output format and turns the clock duty cycle stabilizer off.

SENSE (Pin 59): Reference Programming Pin. Connecting SENSE to V_{CM} selects the internal reference and a ±0.5V input range. Connecting SENSE to V_{DD} selects the internal reference and a ±1V input range. An external reference greater than 0.5V and less than 1V applied to SENSE selects an input range of $\pm V_{SENSE}$. ±1V is the largest valid input range.

V_{CM} (Pin 60): 1.25V Output and Input Common Mode Bias. Bypass to ground with 2.2µF ceramic chip capacitor.

GND (Exposed Pad) (Pin 65): ADC Power Ground. The exposed pad on the bottom of the package needs to be soldered to ground.

PIN FUNCTIONS (LVDS Mode)

AIN+ (Pins 1, 2): Positive Differential Analog Input.

AIN– (Pins 3, 4): Negative Differential Analog Input.

REFHA (Pins 5, 6): ADC High Reference. Bypass to Pins 7, 8 with 0.1µF ceramic chip capacitor, to Pins 11, 12 with a 2.2µF ceramic capacitor and to ground with 1µF ceramic capacitor.

REFLB (Pins 7, 8): ADC Low Reference. Bypass to Pins 5, 6 with 0.1µF ceramic chip capacitor. Do not connect to Pins 11, 12.

REFHB (Pins 9, 10): ADC High Reference. Bypass to Pins 11, 12 with 0.1µF ceramic chip capacitor. Do not connect to Pins 5, 6.

REFLA (Pins 11, 12): ADC Low Reference. Bypass to Pins 9, 10 with 0.1µF ceramic chip capacitor, to Pins 5, 6 with a 2.2µF ceramic capacitor and to ground with 1µF ceramic capacitor.

V_{DD} (Pins 13, 14, 15, 62, 63): 2.5V Supply. Bypass to GND with 0.1µF ceramic chip capacitors.

GND (Pins 16, 61, 64): ADC Power Ground.

ENC+ (Pin 17): Encode Input. Conversion starts on the positive edge.

ENC– (Pin 18): Encode Complement Input. Conversion starts on the negative edge. Bypass to ground with 0.1µF ceramic for single-ended encode signal.

SHDN (Pin 19): Shutdown Mode Selection Pin. Connecting SHDN to GND and $\overline{OE}$ to GND results in normal operation with the outputs enabled. Connecting SHDN to GND and $\overline{OE}$ to V_{DD} results in normal operation with the outputs at high impedance. Connecting SHDN to V_{DD} and $\overline{OE}$ to GND results in nap mode with the outputs at high impedance. Connecting SHDN to V_{DD} and $\overline{OE}$ to V_{DD} results in sleep mode with the outputs at high impedance.

$\overline{OE}$ (Pin 20): Output Enable Pin. Refer to SHDN pin function.

DNC (Pins 21, 22, 23, 24): Do not connect these pins.

D0–/D0+ to D9–/D9+ (Pins 27, 28, 29, 30, 31, 32, 37, 38, 39, 40, 43, 44, 45, 46, 47, 48, 51, 52, 53, 54): LVDS Digital Outputs. All LVDS outputs require differential 100Ω termination resistors at the LVDS receiver. D9–/D9+ is the MSB.

OGND (Pins 25, 33, 41, 50): Output Driver Ground.

OV_{DD} (Pins 26, 34, 42, 49): Positive Supply for the Output Drivers. Bypass to ground with 0.1µF ceramic chip capacitor.

CLKOUT–/CLKOUT+ (Pins 35 to 36): LVDS Data Valid Output. Latch data on rising edge of CLKOUT–, falling edge of CLKOUT+.

OF–/OF+ (Pins 55 to 56): LVDS Over/Under Flow Output. High when an over or under flow has occurred.

LVDS (Pin 57): Output Mode Selection Pin. Connecting LVDS to 0V selects full rate CMOS mode. Connecting LVDS to $1/3V_{DD}$ selects demux CMOS mode with simultaneous update. Connecting LVDS to $2/3V_{DD}$ selects demux CMOS mode with interleaved update. Connecting LVDS to V_{DD} selects LVDS mode.

MODE (Pin 58): Output Format and Clock Duty Cycle Stabilizer Selection Pin. Connecting MODE to 0V selects offset binary output format and turns the clock duty cycle stabilizer off. Connecting MODE to $1/3V_{DD}$ selects offset binary output format and turns the clock duty cycle stabilizer on. Connecting MODE to $2/3V_{DD}$ selects 2's complement output format and turns the clock duty cycle stabilizer on. Connecting MODE to V_{DD} selects 2's complement output format and turns the clock duty cycle stabilizer off.

SENSE (Pin 59): Reference Programming Pin. Connecting SENSE to V_{CM} selects the internal reference and a ±0.5V input range. Connecting SENSE to V_{DD} selects the internal reference and a ±1V input range. An external reference greater than 0.5V and less than 1V applied to SENSE selects an input range of $\pm V_{SENSE}$. ±1V is the largest valid input range.

V_{CM} (Pin 60): 1.25V Output and Input Common Mode Bias. Bypass to ground with 2.2µF ceramic chip capacitor.

GND (Exposed Pad) (Pin 65): ADC Power Ground. The exposed pad on the bottom of the package needs to be soldered to ground.

FUNCTIONAL BLOCK DIAGRAM

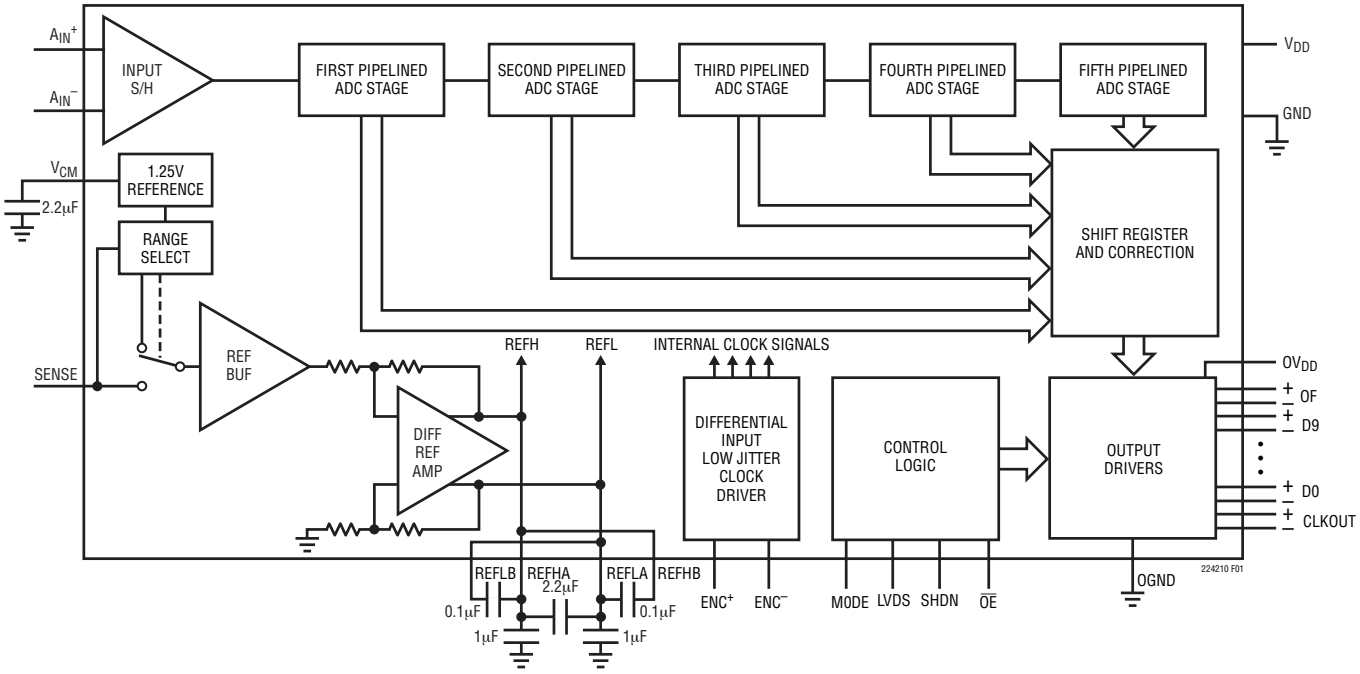
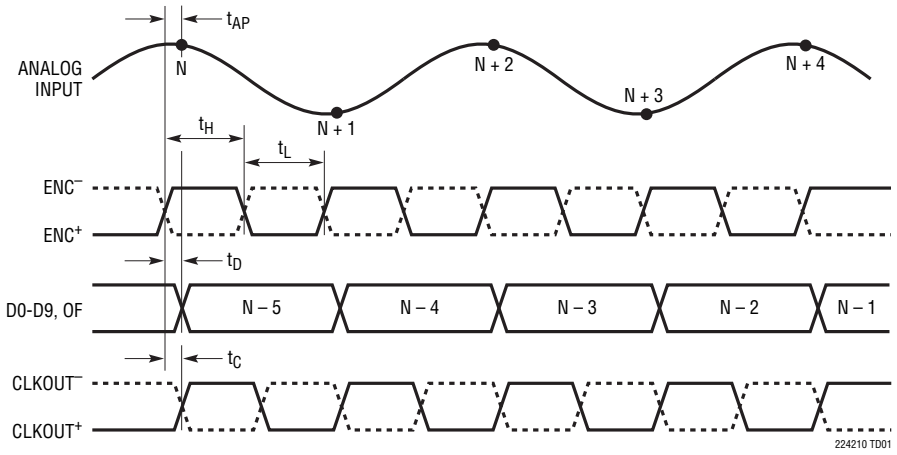


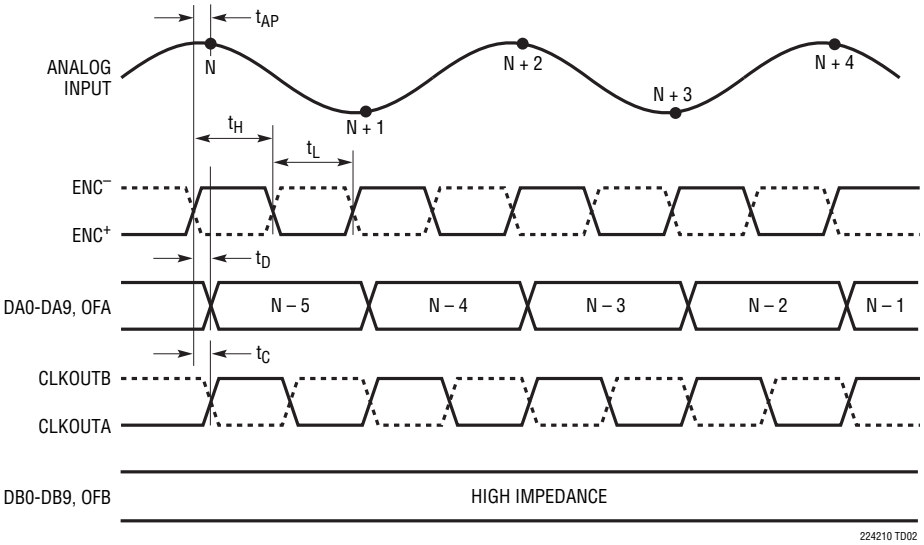
Figure 1. Functional Block Diagram

TIMING DIAGRAMS

LVDS Output Mode Timing
All Outputs Are Differential and Have LVDS Levels

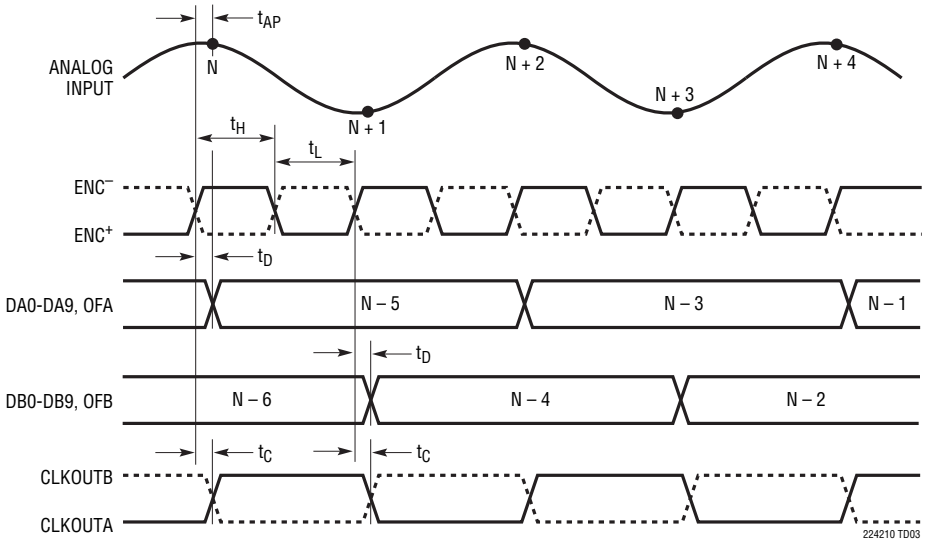


Full-Rate CMOS Output Mode Timing
All Outputs Are Single-Ended and Have CMOS Levels

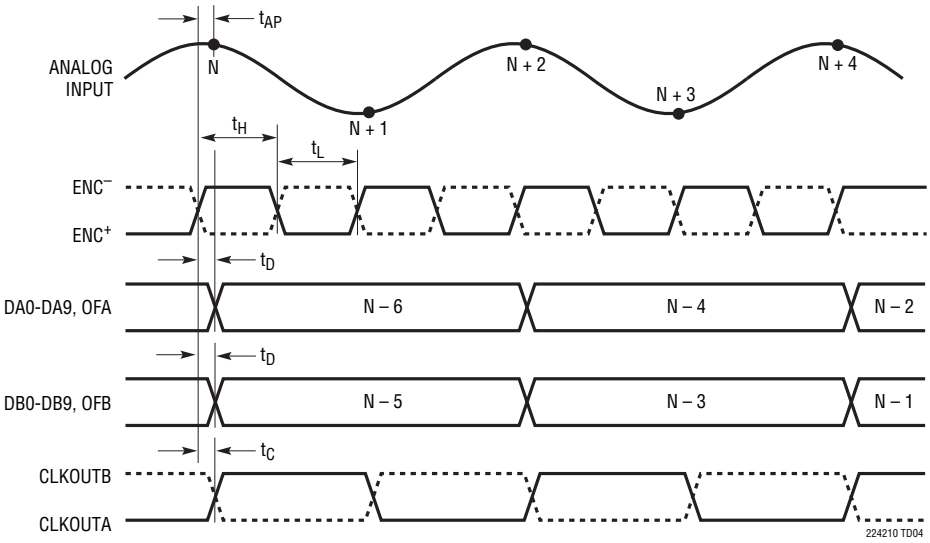


TIMING DIAGRAMS

Demultiplexed CMOS Outputs with Interleaved Update
All Outputs Are Single-Ended and Have CMOS Levels



Demultiplexed CMOS Outputs with Simultaneous Update
All Outputs Are Single-Ended and Have CMOS Levels



APPLICATIONS INFORMATION

DYNAMIC PERFORMANCE

Signal-to-Noise Plus Distortion Ratio

The signal-to-noise plus distortion ratio [S/(N + D)] is the ratio between the RMS amplitude of the fundamental input frequency and the RMS amplitude of all other frequency components at the ADC output. The output is band limited to frequencies above DC to below half the sampling frequency.

Signal-to-Noise Ratio

The signal-to-noise ratio (SNR) is the ratio between the RMS amplitude of the fundamental input frequency and the RMS amplitude of all other frequency components except the first five harmonics and DC.

Total Harmonic Distortion

Total harmonic distortion is the ratio of the RMS sum of all harmonics of the input signal to the fundamental itself. The out-of-band harmonics alias into the frequency band between DC and half the sampling frequency. THD is expressed as:

$$THD = 20Log\left(\sqrt{\left(V2^2 + V3^2 + V4^2 + ...Vn^2\right)}/V1\right)$$

where V1 is the RMS amplitude of the fundamental frequency and V2 through Vn are the amplitudes of the second through nth harmonics. The THD calculated in this data sheet uses all the harmonics up to the fifth.

Intermodulation Distortion

If the ADC input signal consists of more than one spectral component, the ADC transfer function nonlinearity can produce intermodulation distortion (IMD) in addition to THD. IMD is the change in one sinusoidal input caused by the presence of another sinusoidal input at a different frequency.

If two pure sine waves of frequencies fa and fb are applied to the ADC input, nonlinearities in the ADC transfer function can create distortion products at the sum and difference frequencies of mfa ± nfb, where m and n = 0, 1, 2, 3, etc. The 3rd order intermodulation products are 2fa + fb, 2fb + fa, 2fa – fb and 2fb – fa. The intermodulation distortion is defined as the ratio of the RMS value of either input tone to the RMS value of the largest 3rd order intermodulation product.

Spurious Free Dynamic Range (SFDR)

Spurious free dynamic range is the peak harmonic or spurious noise that is the largest spectral component excluding the input signal and DC. This value is expressed in decibels relative to the RMS value of a full scale input signal.

Full Power Bandwidth

The full power bandwidth is that input frequency at which the amplitude of the reconstructed fundamental is reduced by 3dB for a full scale input signal.

Aperture Delay Time

The time from when a rising ENC^+ equals the ENC^- voltage to the instant that the input signal is held by the sample and hold circuit.

Aperture Delay Jitter

The variation in the aperture delay time from conversion to conversion. This random variation will result in noise when sampling an AC input. The signal to noise ratio due to the jitter alone will be:

$$SNR_{JITTER} = -20\log\left(2\pi \bullet f_{IN} \bullet t_{JITTER}\right)$$

CONVERTER OPERATION

As shown in Figure 1, the LTC2242-10 is a CMOS pipelined multi-step converter. The converter has five pipelined ADC stages; a sampled analog input will result in a digitized value five cycles later (see the Timing Diagram section). For optimal performance the analog inputs should be driven differentially. The encode input is differential for improved common mode noise immunity. The LTC2242-10 has two phases of operation, determined by the state of the differential ENC^+/ENC^- input pins. For brevity, the text will refer to ENC^+ greater than ENC^- as ENC high and ENC^+ less than ENC^- as ENC low.

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Each pipelined stage shown in Figure 1 contains an ADC, a reconstruction DAC and an interstage residue amplifier. In operation, the ADC quantizes the input to the stage and the quantized value is subtracted from the input by the DAC to produce a residue. The residue is amplified and output by the residue amplifier. Successive stages operate out of phase so that when the odd stages are outputting their residue, the even stages are acquiring that residue and vice versa.

When ENC is low, the analog input is sampled differentially directly onto the input sample-and-hold capacitors, inside the "Input S/H" shown in the block diagram. At the instant that ENC transitions from low to high, the sampled input is held. While ENC is high, the held input voltage is buffered by the S/H amplifier which drives the first pipelined ADC stage. The first stage acquires the output of the S/H during this high phase of ENC. When ENC goes back low, the first stage produces its residue which is acquired by the second stage. At the same time, the input S/H goes back to acquiring the analog input. When ENC goes back high, the second stage produces its residue which is acquired by the third stage. An identical process is repeated for the third and fourth stages, resulting in a fourth stage residue that is sent to the fifth stage ADC for final evaluation.

Each ADC stage following the first has additional range to accommodate flash and amplifier offset errors. Results from all of the ADC stages are digitally synchronized such that the results can be properly combined in the correction logic before being sent to the output buffer.

SAMPLE/HOLD OPERATION AND INPUT DRIVE

Sample/Hold Operation

Figure 2 shows an equivalent circuit for the LTC2242-10 CMOS differential sample-and-hold. The analog inputs are connected to the sampling capacitors (C_{SAMPLE}) through NMOS transistors. The capacitors shown attached to each input ($C_{PARASITIC}$) are the summation of all other capacitance associated with each input.

During the sample phase when ENC is low, the transistors connect the analog inputs to the sampling capacitors and they charge to, and track the differential input voltage. When ENC transitions from low to high, the sampled input

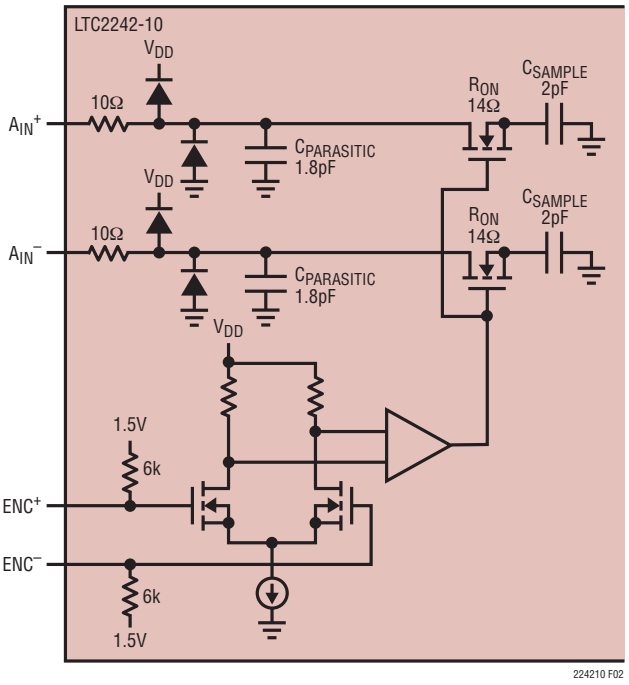

Figure 2. Equivalent Input Circuit

voltage is held on the sampling capacitors. During the hold phase when ENC is high, the sampling capacitors are disconnected from the input and the held voltage is passed to the ADC core for processing. As ENC transitions from high to low, the inputs are reconnected to the sampling capacitors to acquire a new sample. Since the sampling capacitors still hold the previous sample, a charging glitch proportional to the change in voltage between samples will be seen at this time. If the change between the last sample and the new sample is small, the charging glitch seen at the input will be small. If the input change is large, such as the change seen with input frequencies near Nyquist, then a larger charging glitch will be seen.

Common Mode Bias

For optimal performance the analog inputs should be driven differentially. Each input should swing ±0.5V for the 2V range or ±0.25V for the 1V range, around a common mode voltage of 1.25V. The V_{CM} output pin (Pin 60) may be used to provide the common mode bias level. V_{CM} can be tied directly to the center tap of a transformer to set the DC input level or as a reference level to an op amp

APPLICATIONS INFORMATION

differential driver circuit. The V_{CM} pin must be bypassed to ground close to the ADC with a 2.2µF or greater capacitor.

Input Drive Impedance

As with all high performance, high speed ADCs, the dynamic performance of the LTC2242-10 can be influenced by the input drive circuitry, particularly the second and third harmonics. Source impedance and input reactance can influence SFDR. At the falling edge of ENC, the sample-and-hold circuit will connect the 2pF sampling capacitor to the input pin and start the sampling period. The sampling period ends when ENC rises, holding the sampled input on the sampling capacitor. Ideally the input circuitry should be fast enough to fully charge the sampling capacitor during the sampling period $1/(2f_S)$; however, this is not always possible and the incomplete settling may degrade the SFDR. The sampling glitch has been designed to be as linear as possible to minimize the effects of incomplete settling.

For the best performance, it is recommended to have a source impedance of 100Ω or less for each input. The source impedance should be matched for the differential inputs. Poor matching will result in higher even order harmonics, especially the second.

Input Drive Circuits

Figure 3 shows the LTC2242-10 being driven by an RF transformer with a center tapped secondary. The secondary center tap is DC biased with V_{CM}, setting the ADC input signal at its optimum DC level. Terminating on the transformer secondary is desirable, as this provides a common mode path for charging glitches caused by the sample and hold. Figure 3 shows a 1:1 turns ratio transformer. Other turns ratios can be used if the source impedance seen by the ADC does not exceed 100Ω for each ADC input. A disadvantage of using a transformer is the loss of low frequency response. Most small RF transformers have poor performance at frequencies below 1MHz.

Figure 4 demonstrates the use of a differential amplifier to convert a single ended input signal into a differential input signal. The advantage of this method is that it provides low frequency input response; however, the limited gain bandwidth of most op amps will limit the SFDR at high input frequencies.

Figure 5 shows a capacitively-coupled input circuit. The impedance seen by the analog inputs should be matched.

The 25Ω resistors and 12pF capacitor on the analog inputs serve two purposes: isolating the drive circuitry from

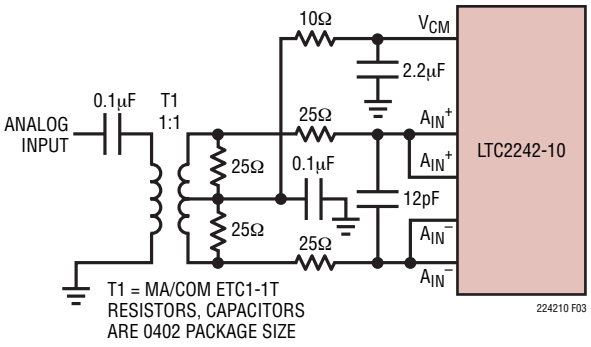

Figure 3. Single-Ended to Differential Conversion Using a Transformer

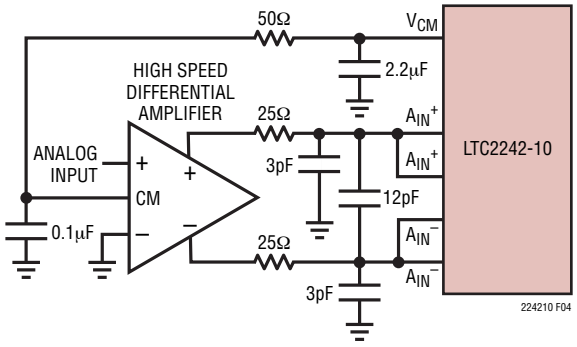

Figure 4. Differential Drive with an Amplifier

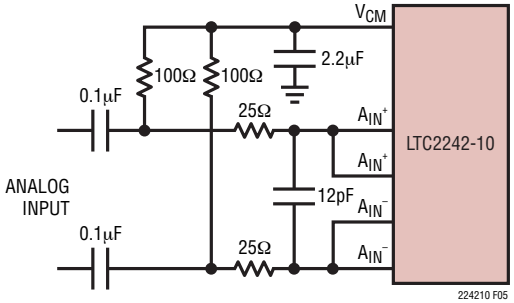

Figure 5. Capacitively-Coupled Drive

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the sample-and-hold charging glitches and limiting the wideband noise at the converter input. For input frequencies higher than 100MHz, the capacitor may need to be decreased to prevent excessive signal loss.

The A_{IN}^+ and A_{IN}^- inputs each have two pins to reduce package inductance. The two A_{IN}^+ and the two A_{IN}^- pins should be shorted together.

For input frequencies above 100MHz the input circuits of Figure 6, 7 and 8 are recommended. The balun transformer gives better high frequency response than a flux coupled center tapped transformer. The coupling capacitors allow the analog inputs to be DC biased at 1.25V. In Figure 8 the series inductors are impedance matching elements that maximize the ADC bandwidth.

Reference Operation

Figure 9 shows the LTC2242-10 reference circuitry consisting of a 1.25V bandgap reference, a difference amplifier and switching and control circuit. The internal voltage reference can be configured for two pin selectable input ranges of 2V (±1V differential) or 1V (±0.5V differential). Tying the SENSE pin to V_{DD} selects the 2V range; typing the SENSE pin to V_{CM} selects the 1V range.

The 1.25V bandgap reference serves two functions: its output provides a DC bias point for setting the common mode voltage of any external input circuitry; additionally, the reference is used with a difference amplifier to generate the differential reference levels needed by the internal ADC circuitry. An external bypass capacitor is required for the 1.25V reference output, V_{CM}. This provides a high frequency low impedance path to ground for internal and external circuitry.

The difference amplifier generates the high and low reference for the ADC. High speed switching circuits are connected to these outputs and they must be externally bypassed. Each output has four pins: two each of REFHA and REFHB for the high reference and two each of REFLA and REFLB for the low reference. The multiple output pins are needed to reduce package inductance. Bypass capacitors must be connected as shown in Figure 9.

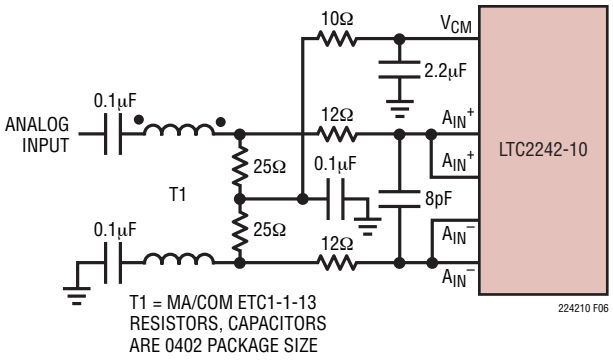

Figure 6. Recommended Front End Circuit for Input Frequencies Between 100MHz and 250MHz

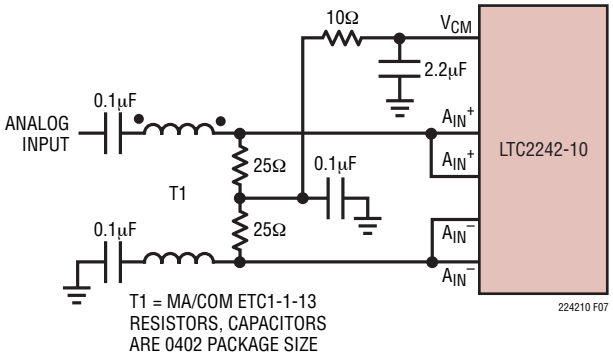

Figure 7. Recommended Front End Circuit for Input Frequencies Between 250MHz and 500MHz

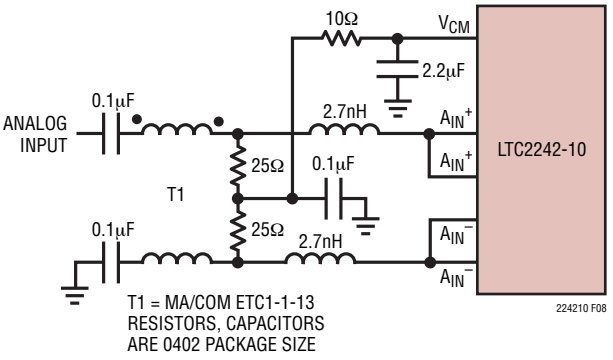

Figure 8. Recommended Front End Circuit for Input Frequencies Above 500MHz

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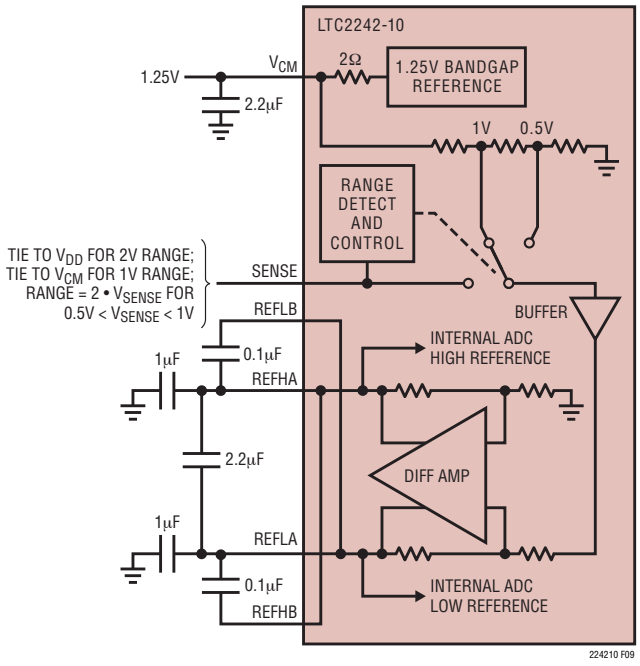

Figure 9. Equivalent Reference Circuit

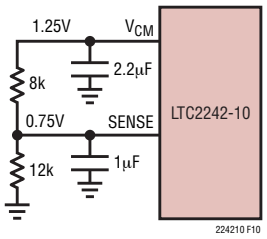

Figure 10. 1.5V Range ADC

Other voltage ranges in between the pin selectable ranges can be programmed with two external resistors as shown in Figure 10. An external reference can be used by applying its output directly or through a resistor divider to SENSE. It is not recommended to drive the SENSE pin with a logic device. The SENSE pin should be tied to the appropriate level as close to the converter as possible. If the SENSE pin is driven externally, it should be bypassed to ground as close to the device as possible with a 1µF ceramic capacitor.

Input Range

The input range can be set based on the application. The 2V input range will provide the best signal-to-noise performance while maintaining excellent SFDR. The 1V input range will have better SFDR performance, but the SNR will degrade by 1.7dB. See the Typical Performance Characteristics section.

Driving the Encode Inputs

The noise performance of the LTC2242-10 can depend on the encode signal quality as much as on the analog input. The ENC^+/ENC^- inputs are intended to be driven differentially, primarily for noise immunity from common mode noise sources. Each input is biased through a 4.8k resistor to a 1.5V bias. The bias resistors set the DC operating point for transformer coupled drive circuits and can set the logic threshold for single-ended drive circuits.

Any noise present on the encode signal will result in additional aperture jitter that will be RMS summed with the inherent ADC aperture jitter.

In applications where jitter is critical (high input frequencies) take the following into consideration:

1. Differential drive should be used.

2. Use as large an amplitude as possible; if transformer coupled use a higher turns ratio to increase the amplitude.

3. If the ADC is clocked with a sinusoidal signal, filter the encode signal to reduce wideband noise.

4. Balance the capacitance and series resistance at both encode inputs so that any coupled noise will appear at both inputs as common mode noise. The encode inputs have a common mode range of 1.2V to 2.0V. Each input may be driven from ground to V_{DD} for single-ended drive.

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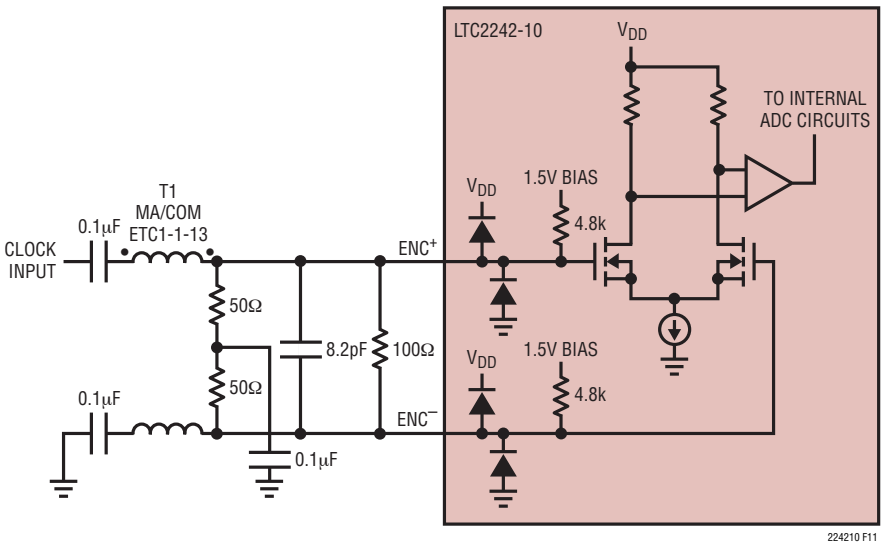

Figure 11. Transformer Driven ENC+/ENC–

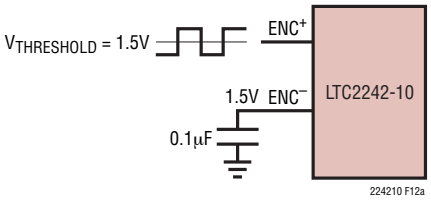

Figure 12a. Single-Ended ENC Drive, Not Recommended for Low Jitter

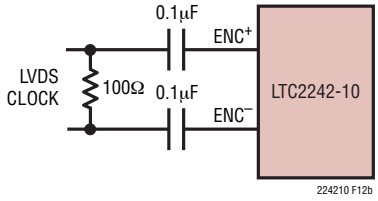

Figure 12b. ENC Drive Using LVDS

Maximum and Minimum Encode Rates

The maximum encode rate for the LTC2242-10 is 250Msps. For the ADC to operate properly, the encode signal should have a 50% (±5%) duty cycle. Each half cycle must have at least 1.9ns for the ADC internal circuitry to have enough settling time for proper operation. Achieving a precise 50% duty cycle is easy with differential sinusoidal drive using a transformer or using symmetric differential logic such as PECL or LVDS.

An optional clock duty cycle stabilizer circuit can be used if the input clock has a non 50% duty cycle. This circuit uses the rising edge of the ENC+ pin to sample the analog input. The falling edge of ENC+ is ignored and the internal falling edge is generated by a phase-locked loop. The input clock duty cycle can vary from 40% to 60% and the clock duty cycle stabilizer will maintain a constant 50% internal duty cycle. If the clock is turned off for a long period of time, the duty cycle stabilizer circuit will require one hundred clock cycles for the PLL to lock onto the input clock. To use the clock duty cycle stabilizer, the MODE pin should be connected to $1/3V_{DD}$ or $2/3V_{DD}$ using external resistors.

The lower limit of the LTC2242-10 sample rate is determined by droop of the sample-and-hold circuits. The pipelined architecture of this ADC relies on storing analog signals on small valued capacitors. Junction leakage will discharge the capacitors. The specified minimum operating frequency for the LTC2242-10 is 1Msps.

DIGITAL OUTPUTS

Table 1 shows the relationship between the analog input voltage, the digital data bits, and the overflow bit.

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Table 1. Output Codes vs Input Voltage

$A_{IN}^+ - A_{IN}^-$ (2V Range)	OF	D9 – D0 (Offset Binary)	D9 – D0 (2's Complement)
>+1.000000V	1	11 1111 1111	01 1111 1111
+0.998047V	0	11 1111 1111	01 1111 1111
+0.996094V	0	11 1111 1110	01 1111 1110
+0.001953V	0	10 0000 0001	00 0000 0001
0.000000V	0	10 0000 0000	00 0000 0000
–0.001953V	0	01 1111 1111	11 1111 1111
–0.003906V	0	01 1111 1110	11 1111 1110
–0.998047V	0	00 0000 0001	10 0000 0001
–1.000000V	0	00 0000 0000	10 0000 0000
<–1.000000V	1	00 0000 0000	10 0000 0000

Digital Output Modes

The LTC2242-10 can operate in several digital output modes: LVDS, CMOS running at full speed, and CMOS demultiplexed onto two buses, each of which runs at half speed. In the demultiplexed CMOS modes the two buses (referred to as bus A and bus B) can either be updated on alternate clock cycles (interleaved mode) or simultaneously (simultaneous mode). For details on the clock timing, refer to the timing diagrams.

The LVDS pin selects which digital output mode the part uses. This pin has a four-level logic input which should be connected to GND, $1/3V_{DD}$, $2/3V_{DD}$ or V_{DD}. An external resistor divider can be used to set the $1/3V_{DD}$ or $2/3V_{DD}$ logic values. Table 2 shows the logic states for the LVDS pin.

Table 2. LVDS Pin Function

LVDS	DIGITAL OUTPUT MODE
GND	Full-Rate CMOS
$1/3V_{DD}$	Demultiplexed CMOS, Simultaneous Update
$2/3V_{DD}$	Demultiplexed CMOS, Interleaved Update
V_{DD}	LVDS

Digital Output Buffers (CMOS Modes)

Figure 13a shows an equivalent circuit for a single output buffer in the CMOS output mode. Each buffer is powered by OV_{DD} and OGND, which are isolated from the ADC power and ground. The additional N-channel transistor in the output driver allows operation down to voltages as low as 0.5V. The internal resistor in series with the output makes the output appear as 50Ω to external circuitry and may eliminate the need for external damping resistors.

As with all high speed/high resolution converters, the digital output loading can affect the performance. The digital outputs of the LTC2242-10 should drive a minimal capacitive load to avoid possible interaction between the digital outputs and sensitive input circuitry. The output should be buffered with a device such as an 74VCX245 CMOS latch. For full speed operation the capacitive load should be kept under 10pF.

Lower OV_{DD} voltages will also help reduce interference from the digital outputs.

Digital Output Buffers (LVDS Mode)

Figure 13b shows an equivalent circuit for a differential output pair in the LVDS output mode. A 3.5mA current is steered from OUT^+ to OUT^- or vice versa which creates a ±350mV differential voltage across the 100Ω termination resistor at the LVDS receiver. A feedback loop regulates the common mode output voltage to 1.25V. For proper operation each LVDS output pair needs an external 100Ω termination resistor, even if the signal is not used (such as OF^+/OF^- or $CLKOUT^+/CLKOUT^-$). To minimize noise the PC board traces for each LVDS output pair should be routed close together. To minimize clock skew all LVDS PC board traces should have about the same length.

APPLICATIONS INFORMATION

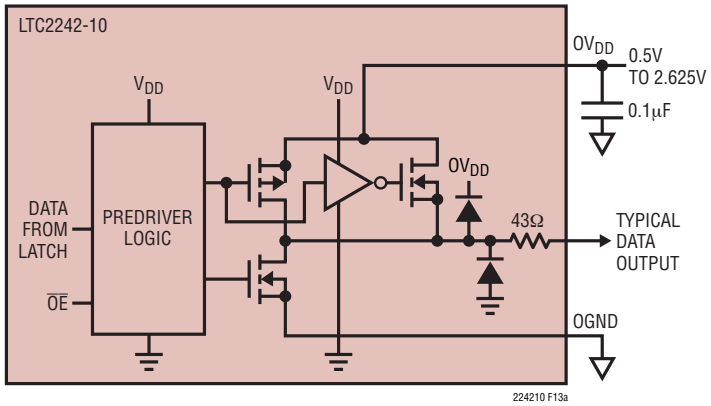


Figure 13a. Digital Output Buffer in CMOS Mode

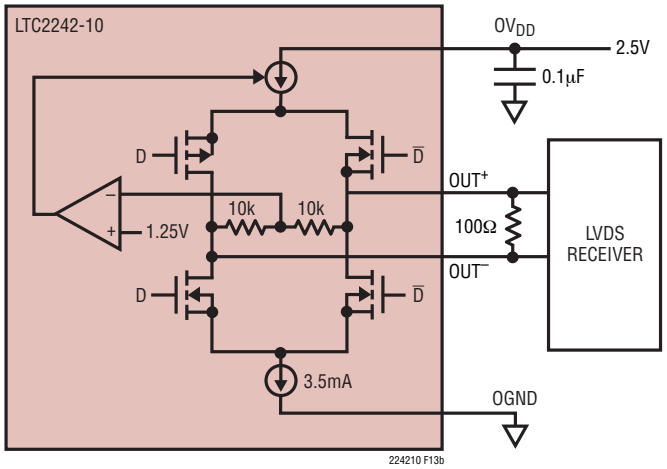


Figure 13b. Digital Output in LVDS Mode

Data Format

The LTC2242-10 parallel digital output can be selected for offset binary or 2's complement format. The format is selected with the MODE pin. Connecting MODE to GND or $1/3V_{DD}$ selects offset binary output format. Connecting MODE to $2/3V_{DD}$ or V_{DD} selects 2's complement output format. An external resistor divider can be used to set the $1/3V_{DD}$ or $2/3V_{DD}$ logic values. Table 3 shows the logic states for the MODE pin.

Table 3. MODE Pin Function

MODE PIN	OUTPUT FORMAT	CLOCK DUTY CYCLE STABILIZER
0	Offset Binary	Off
$1/3V_{DD}$	Offset Binary	On
$2/3V_{DD}$	2's Complement	On
V_{DD}	2's Complement	Off

Overflow Bit

An overflow output bit indicates when the converter is overranged or underranged. In CMOS mode, a logic high on the OFA pin indicates an overflow or underflow on the A data bus, while a logic high on the OFB pin indicates an overflow or underflow on the B data bus. In LVDS mode, a differential logic high on the OF^+/OF^- pins indicates an overflow or underflow.

Output Clock

The ADC has a delayed version of the ENC^+ input available as a digital output, CLKOUT. The CLKOUT pin can be used to synchronize the converter data to the digital system. This is necessary when using a sinusoidal encode. In all CMOS modes, A bus data will be updated just after CLKOUTA rises and can be latched on the falling edge of CLKOUTA. In demux CMOS mode with interleaved update, B bus data will be updated just after CLKOUTB rises and can be latched on the falling edge of CLKOUTB. In demux CMOS mode with simultaneous update, B bus data will be updated just after CLKOUTB falls and can be latched on the rising edge of CLKOUTB. In LVDS mode, data will be updated just after $CLKOUT^+/CLKOUT^-$ rises and can be latched on the falling edge of $CLKOUT^+/CLKOUT^-$.

Output Driver Power

Separate output power and ground pins allow the output drivers to be isolated from the analog circuitry. The power supply for the digital output buffers, OV_{DD}, should be tied to the same power supply as for the logic being driven. For example if the converter is driving a DSP powered by a 1.8V supply then OV_{DD} should be tied to that same 1.8V supply.

In the CMOS output mode, OV_{DD} can be powered with any voltage up to 2.625V. OGND can be powered with any voltage from GND up to 1V and must be less than OV_{DD}. The logic outputs will swing between OGND and OV_{DD}.

In the LVDS output mode, OV_{DD} should be connected to a 2.5V supply and OGND should be connected to GND.

APPLICATIONS INFORMATION

Output Enable

The outputs may be disabled with the output enable pin, $\overline{OE}$. In CMOS or LVDS output modes $\overline{OE}$ high disables all data outputs including OF and CLKOUT. The data access and bus relinquish times are too slow to allow the outputs to be enabled and disabled during full speed operation. The output Hi-Z state is intended for use during long periods of inactivity.

The Hi-Z state is not a truly open circuit; the output pins that make an LVDS output pair have a 20k resistance between them. Therefore in the CMOS output mode, adjacent data bits will have 20k resistance in between them, even in the Hi-Z state.

Sleep and Nap Modes

The converter may be placed in shutdown or nap modes to conserve power. Connecting SHDN to GND results in normal operation. Connecting SHDN to V_{DD} and $\overline{OE}$ to V_{DD} results in sleep mode, which powers down all circuitry including the reference and typically dissipates 1mW. When exiting sleep mode it will take milliseconds for the output data to become valid because the reference capacitors have to recharge and stabilize. Connecting SHDN to V_{DD} and $\overline{OE}$ to GND results in nap mode, which typically dissipates 28mW. In nap mode, the on-chip reference circuit is kept on, so that recovery from nap mode is faster than that from sleep mode, typically taking 100 clock cycles. In both sleep and nap mode all digital outputs are disabled and enter the Hi-Z state.

GROUNDING AND BYPASSING

The LTC2242-10 requires a printed circuit board with a clean unbroken ground plane. A multilayer board with an internal ground plane is recommended. Layout for the printed circuit board should ensure that digital and analog signal lines are separated as much as possible. In particular, care should be taken not to run any digital signal alongside an analog signal or underneath the ADC.

High quality ceramic bypass capacitors should be used at the V_{DD}, OV_{DD}, V_{CM}, REFHA, REFHB, REFLA and REFLB pins. Bypass capacitors must be located as close to the pins as possible. Of particular importance are the capacitors between REFHA and REFLB and between REFHB and REFLA. These capacitors should be as close to the device as possible (1.5mm or less). Size 0402 ceramic capacitors are recommended. The 2.2µF capacitor between REFHA and REFLA can be somewhat further away. The traces connecting the pins and bypass capacitors must be kept short and should be made as wide as possible.

The LTC2242-10 differential inputs should run parallel and close to each other. The input traces should be as short as possible to minimize capacitance and to minimize noise pickup.

HEAT TRANSFER

Most of the heat generated by the LTC2242-10 is transferred from the die through the bottom-side exposed pad and package leads onto the printed circuit board. For good electrical and thermal performance, the exposed pad should be soldered to a large grounded pad on the PC board. It is critical that all ground pins are connected to a ground plane of sufficient area.

Clock Sources for Undersampling

Undersampling is especially demanding on the clock source and the higher the input frequency, the greater the sensitivity to clock jitter or phase noise. A clock source that degrades SNR of a full-scale signal by 1dB at 70MHz will degrade SNR by 3dB at 140MHz, and 4.5dB at 190MHz.

In cases where absolute clock frequency accuracy is relatively unimportant and only a single ADC is required, a canned oscillator from vendors such as Saronix or Vectron can be placed close to the ADC and simply connected directly to the ADC. If there is any distance to the ADC, some source termination to reduce ringing that may occur even over a fraction of an inch is advisable. You must not allow the clock to overshoot the supplies or performance will suffer. Do not filter the clock signal with a narrow band filter unless you have a sinusoidal clock source, as the rise and fall time artifacts present in typical digital clock signals will be translated into phase noise.

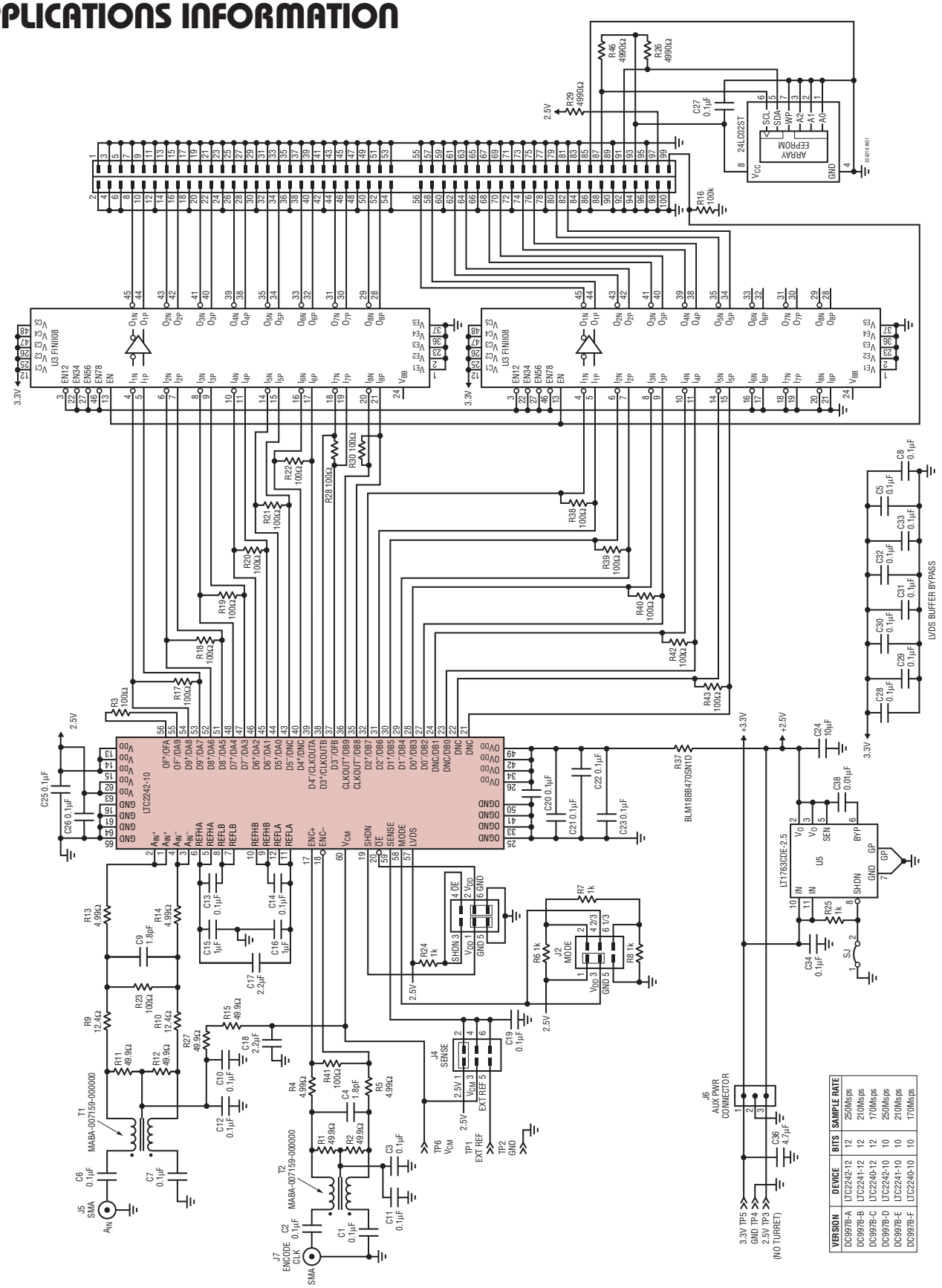
APPLICATIONS INFORMATION

The lowest phase noise oscillators have single-ended sinusoidal outputs, and for these devices the use of a filter close to the ADC may be beneficial. This filter should be close to the ADC to both reduce roundtrip reflection times, as well as reduce the susceptibility of the traces between the filter and the ADC. If the circuit is sensitive to close-in phase noise, the power supply for oscillators and any buffers must be very stable, or propagation delay variation with supply will translate into phase noise. Even though these clock sources may be regarded as digital devices, do not operate them on a digital supply. If your clock is also used to drive digital devices such as an FPGA, you should locate the oscillator, and any clock fan-out devices close to the ADC, and give the routing to the ADC precedence. The clock signals to the FPGA should have series termination at the driver to prevent high frequency noise from the FPGA disturbing the substrate of the clock fan-out device. If you use an FPGA as a programmable divider, you must re-time the signal using the original oscillator, and the re-timing flip-flop as well as the oscillator should be close to the ADC, and powered with a very quiet supply.

For cases where there are multiple ADCs, or where the clock source originates some distance away, differential clock distribution is advisable. This is advisable both from the perspective of EMI, but also to avoid receiving noise from digital sources both radiated, as well as propagated in the waveguides that exist between the layers of multilayer PCBs. The differential pairs must be close together and distanced from other signals. The differential pair should be guarded on both sides with copper distanced at least 3x the distance between the traces, and grounded with vias no more than 1/4 inch apart.

APPLICATIONS INFORMATION

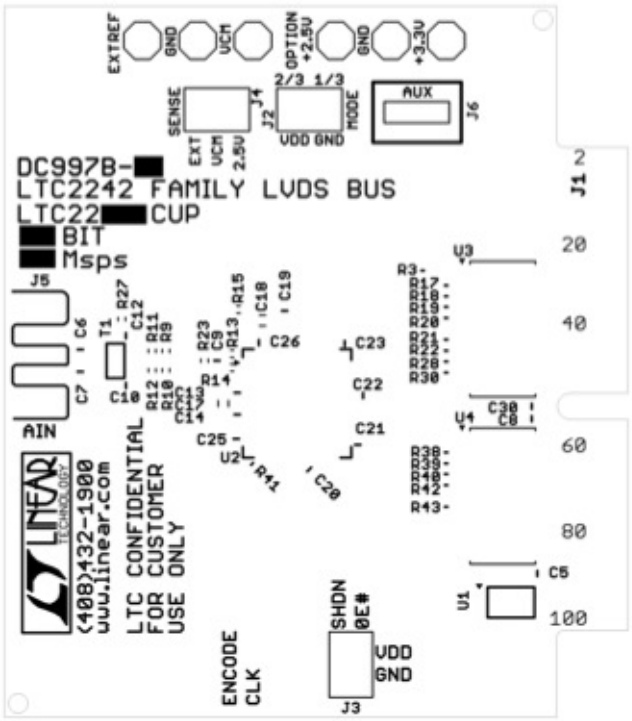
Evaluation Circuit Schematic of the LTC2242-10



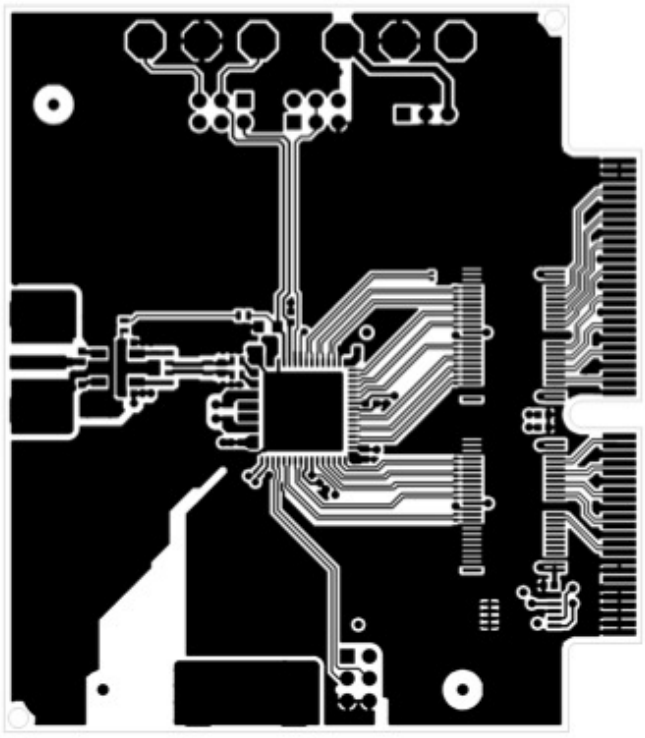
VERSION	DEVICE	BITS	SAMPLE RATE
DC997B-A	LTC2242-12	12	250Msps
DC997B-B	LTC2241-12	12	210Msps
DC997B-C	LTC2240-12	12	170Msps
DC997B-D	LTC2242-10	10	250Msps
DC997B-E	LTC2241-10	10	210Msps
DC997B-F	LTC2240-10	10	170Msps

APPLICATIONS INFORMATION

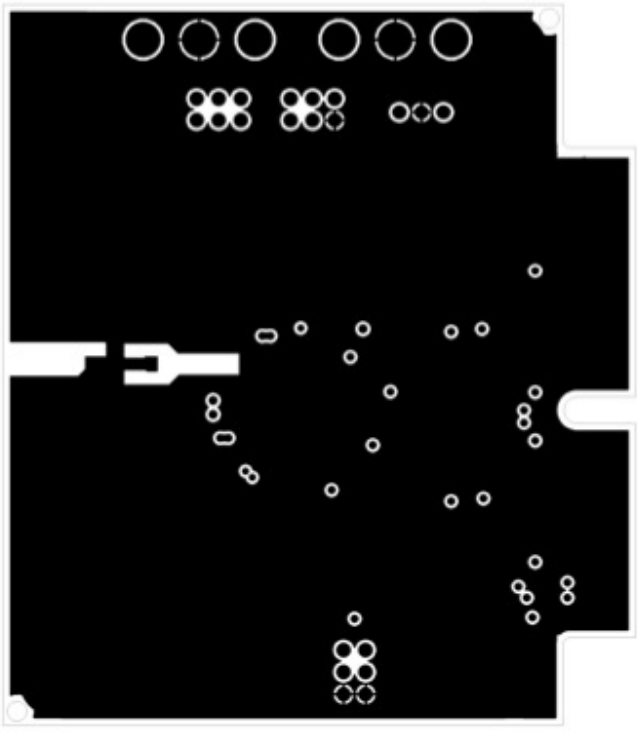
Silkscreen Top



Layer 1 Component Side

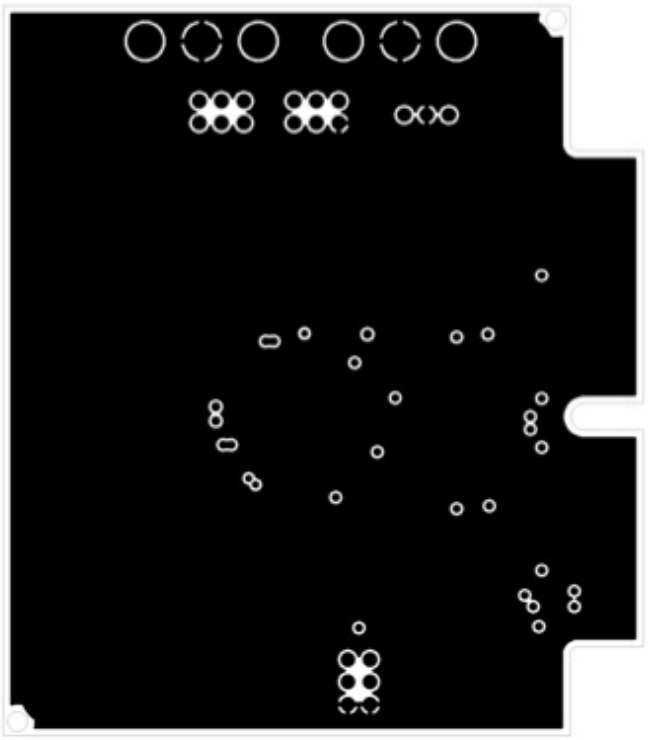


Layer 2 GND Plane

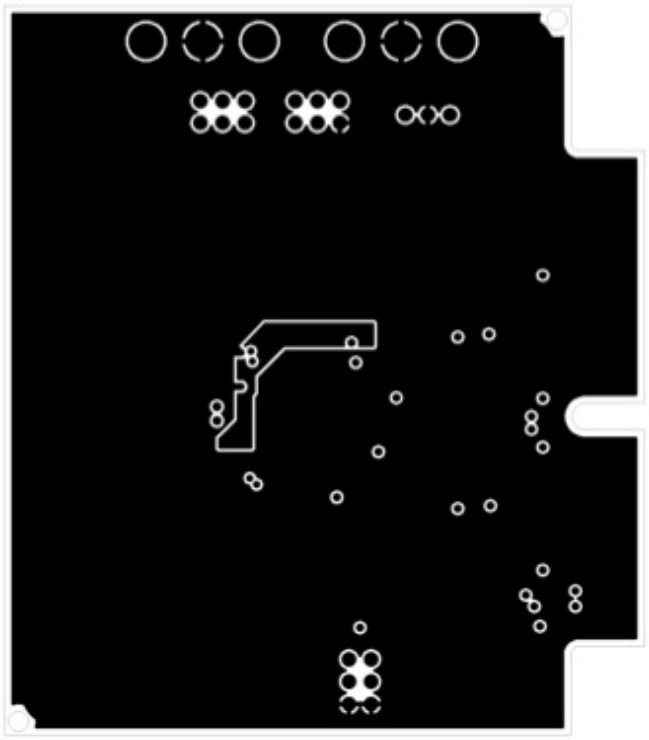


APPLICATIONS INFORMATION

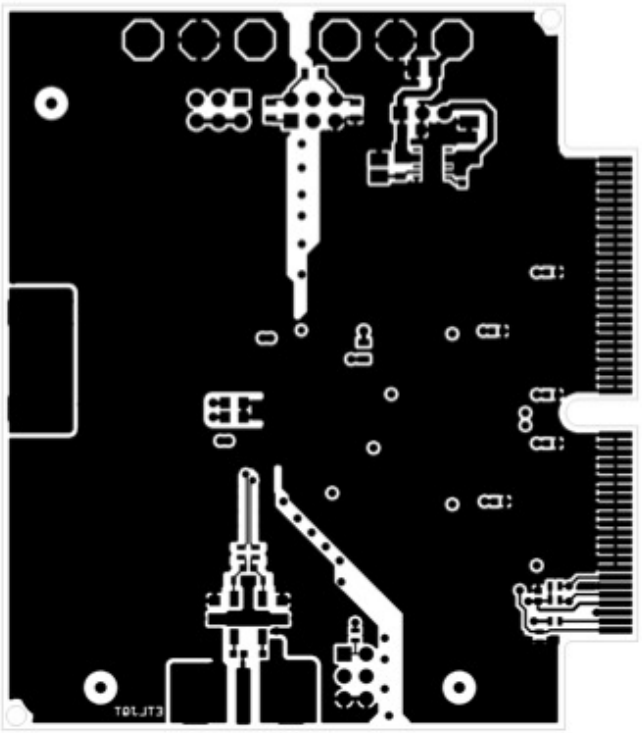
Layer 3 Power/Ground Plane



Layer 4 Power/Ground Planes

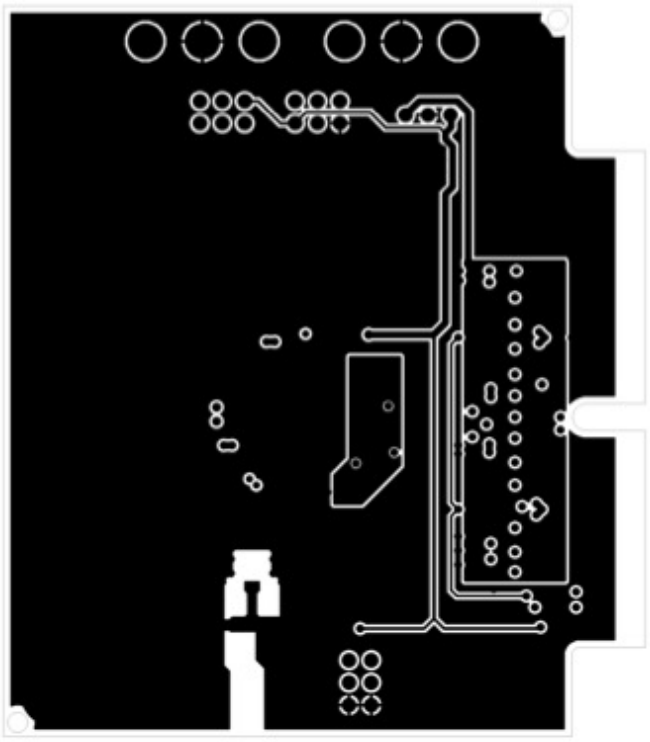


Layer 5 Power/Ground Planes



APPLICATIONS INFORMATION

Layer Back Solder Side

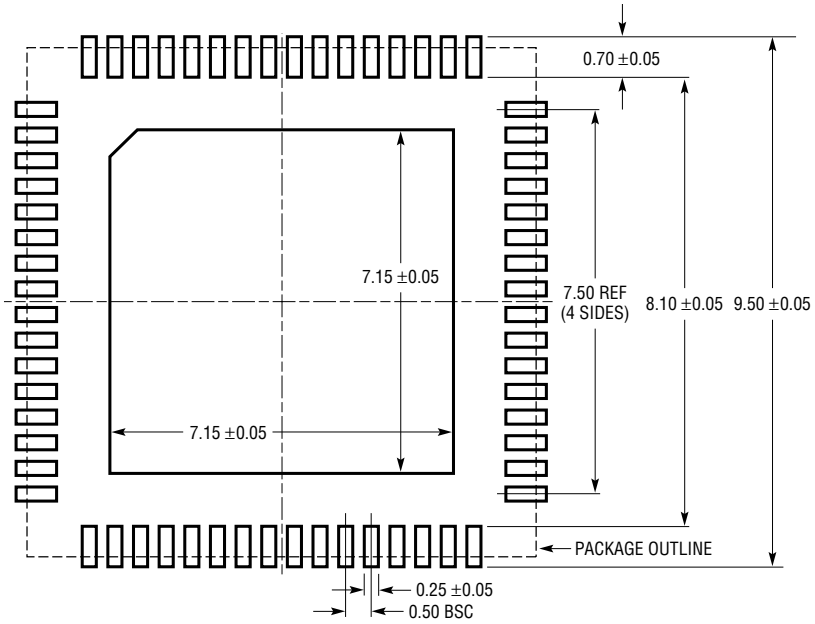


Silk Screen Back, Solder Side

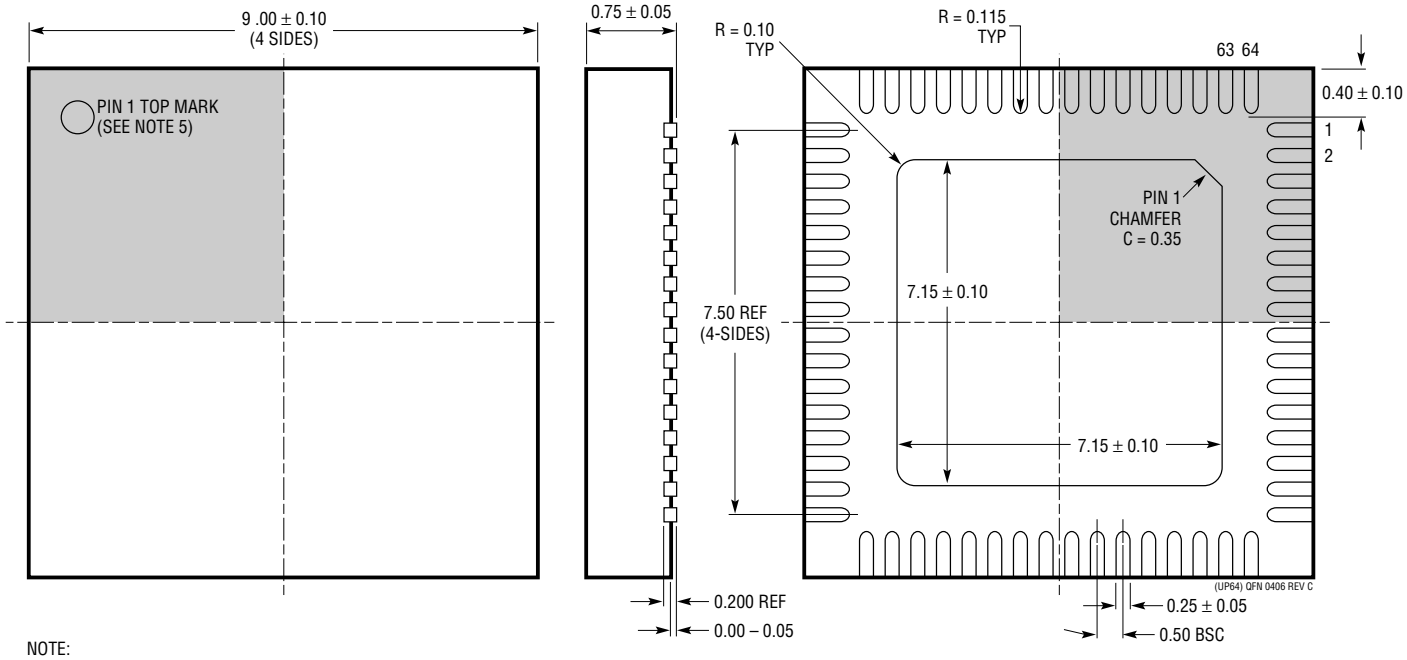
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

UP Package
64-Lead Plastic QFN (9mm × 9mm)
(Reference LTC DWG # 05-08-1705 Rev C)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING CONFORMS TO JEDEC PACKAGE OUTLINE MO-220 VARIATION WNJR-5
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE
   MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE, IF PRESENT
4. EXPOSED PAD SHALL BE SOLDER PLATED
5. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE
6. DRAWING NOT TO SCALE

REVISION HISTORY (Revision history begins at Rev D)

REV	DATE	DESCRIPTION	PAGE NUMBER
D	10/11	Corrected part number on schematic drawing in Applications Information.	24
		Reordered board layers in Applications Information.	25 - 27

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1748	14-Bit, 80Msps, 5V ADC	76.3dB SNR, 90dB SFDR, 48-Pin TSSOP
LTC1750	14-Bit, 80Msps, 5V Wideband ADC	Up to 500MHz IF Undersampling, 90dB SFDR
LT®1993-2	High Speed Differential Op Amp	800MHz BW, 70dBc Distortion at 70MHz, 6dB Gain
LT1994	Low Noise, Low Distortion Fully Differential Input/Output Amplifier/Driver	Low Distortion: –94dBc at 1MHz
LTC2202	16-Bit, 10Msps, 3.3V ADC, Lowest Noise	150mW, 81.6dB SNR, 100dB SFDR, 48-Pin QFN
LTC2208	16-Bit, 130Msps, 3.3V ADC, LVDS Outputs	1250mW, 78dB SNR, 100dB SFDR, 48-Pin QFN
LTC2220	12-Bit, 170Msps, 3.3V ADC, LVDS Outputs	890mW, 67.7dB SNR, 84dB SFDR, 64-Pin QFN
LTC2220-1	12-Bit, 185Msps, 3.3V ADC, LVDS Outputs	910mW, 67.7dB SNR, 80dB SFDR, 64-Pin QFN
LTC2221	12-Bit, 135Msps, 3.3V ADC, LVDS Outputs	660mW, 67.8dB SNR, 84dB SFDR, 64-Pin QFN
LTC2224	12-Bit, 135Msps, 3.3V ADC, High IF Sampling	630mW, 67.6dB SNR, 84dB SFDR, 48-Pin QFN
LTC2230	10-Bit, 170Msps, 3.3V ADC, LVDS Outputs	890mW, 61.2dB SNR, 78dB SFDR, 64-Pin QFN
LTC2231	10-Bit, 135Msps, 3.3V ADC, LVDS Outputs	660mW, 61.2dB SNR, 78dB SFDR, 64-Pin QFN
LTC2240-10	10-Bit, 170Msps, 2.5V ADC, LVDS Outputs	445mW, 60.6dB SNR, 78dB SFDR, 64-Pin QFN
LTC2240-12	12-Bit, 170Msps, 2.5V ADC, LVDS Outputs	445mW, 65.5dB SNR, 78dB SFDR, 64-Pin QFN
LTC2241-10	10-Bit, 210Msps, 2.5V ADC, LVDS Outputs	585mW, 60.6dB SNR, 78dB SFDR, 64-Pin QFN
LTC2242-12	12-Bit, 210Msps, 2.5V ADC, LVDS Outputs	585mW, 65.5dB SNR, 78dB SFDR, 64-Pin QFN
LTC2242-12	12-Bit, 250Msps, 2.5V ADC, LVDS Outputs	740mW, 65.5dB SNR, 78dB SFDR, 64-Pin QFN
LTC2255	14-Bit, 125Msps, 3V ADC, Lowest Power	395mW, 72.5dB SNR, 88dB SFDR, 32-Pin QFN
LTC2284	14-Bit, Dual, 105Msps, 3V ADC, Low Crosstalk	540mW, 72.4dB SNR, 88dB SFDR, 64-Pin QFN
LT5512	DC to 3GHz High Signal Level Downconverting Mixer	DC to 3GHz, 21dBm IIP3, Integrated LO Buffer
LT5514	Ultralow Distortion IF Amplifier/ADC Driver with Digitally Controlled Gain	450MHz to 1dB BW, 47dB OIP3, Digital Gain Control 10.5dB to 33dB in 1.5dB/Step
LT5515	1.5GHz to 2.5GHz Direct Conversion Quadrature Demodulator	High IIP3: 20dBm at 1.9GHz, Integrated LO Quadrature Generator
LT5516	800MHz to 1.5GHz Direct Conversion Quadrature Demodulator	High IIP3: 21.5dBm at 900MHz, Integrated LO Quadrature Generator
LT5517	40MHz to 900MHz Direct Conversion Quadrature Demodulator	High IIP3: 21dBm at 800MHz, Integrated LO Quadrature Generator
LT5522	600MHz to 2.7GHz High Linearity Downconverting Mixer	4.5V to 5.25V Supply, 25dBm IIP3 at 900MHz, NF = 12.5dB, 50Ω Single-Ended RF and LO Ports

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