# THE DATASHEET OF

# LTC3624IMSE-2#PBF

www.win-source.net 0086-755-83957316

# 17V, 2A Synchronous Step-Down Regulator with 3.5µA Quiescent Current

## FEATURES

- **Wide $V_{IN}$ Range: 2.7V to 17V**
- **Wide $V_{OUT}$ Range: 0.6V to $V_{IN}$**
- **95% Max Efficiency**
- **Low $I_Q$: 3.5µA, Zero-Current Shutdown**
- **Constant Frequency (1MHz/2.25MHz)**
- **Fixed $V_{OUT}$ Options Available**
- Low Dropout Operation (100% Duty Cycle) with Ultralow $I_Q$
- 2A Rated Output Current
- ±1% Output Voltage Accuracy
- Current Mode Operation for Excellent Line and Load Transient Response
- Synchronizable to External Clock
- Pulse-Skipping, Forced Continuous, Burst Mode® Operation
- Internal Compensation and Soft-Start
- Overtemperature Protection
- Compact 8-Lead DFN (3mm × 3mm) Package

## APPLICATIONS

- Battery Powered Equipment
- Portable Instrumentation
- Emergency Radios
- General Purpose Step-Down Supplies

## DESCRIPTION

The LTC®3624/LTC3624-2 is a high efficiency 17V, 2A synchronous monolithic step-down regulator. The switching frequency is fixed to 1MHz (LTC3624) or 2.25MHz (LTC3624-2) with a ±40% synchronization range. The regulator features ultralow quiescent current and high efficiency over a wide $V_{OUT}$ range.

The step-down regulator operates from an input voltage range of 2.7V to 17V and provides an adjustable output range from 0.6V to $V_{IN}$ while delivering up to 2A of output current. A user-selectable mode input is provided to allow the user to trade off ripple noise for light load efficiency; Burst Mode operation provides the highest efficiency at light loads, while pulse-skipping mode provides the lowest voltage ripple. The MODE pin can also be used to sync the switching frequency to an external clock.

**LTC3624/LTC3624-2 Options**

| PART NAME | FREQUENCY | $V_{OUT}$ |
|---|---|---|
| LTC3624 | 1MHz | Adjustable |
| LTC3624-3.3 | 1MHz | 3.3V |
| LTC3624-5 | 1MHz | 5V |
| LTC3624-2 | 2.25MHz | Adjustable |
| LTC3624-23.3 | 2.25MHz | 3.3V |
| LTC3624-25 | 2.25MHz | 5V |

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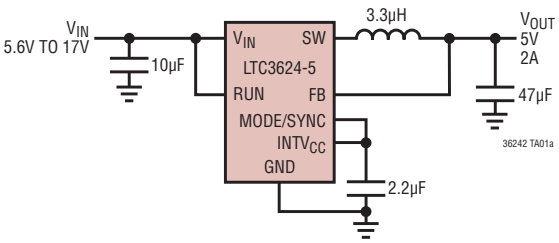
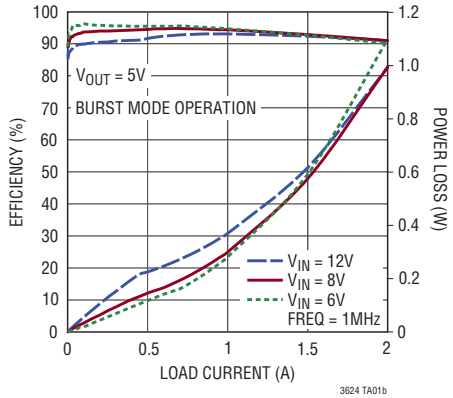
## TYPICAL APPLICATION

**5V $V_{OUT}$ with 800mA Burst Clamp, $f_{SW}$ = 1MHz**




**Efficiency and Power Loss vs Load**

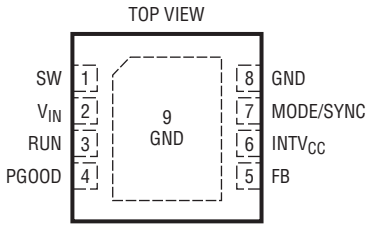


## ABSOLUTE MAXIMUM RATINGS (Note 1)

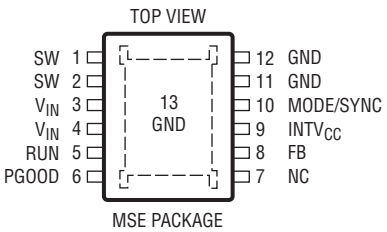
$V_{IN}$ Voltage ..... –0.3V to 17V
RUN Voltage ..... –0.3V to 17V
MODE/SYNC, FB Voltages ..... –0.3V to 6V
$INTV_{CC}$, PGOOD Voltages ..... –0.3V to 6V

Operating Junction Temperature Range
(Notes 2, 5) ..... –40°C to 150°C
Storage Temperature Range ..... –65°C to 150°C

## PIN CONFIGURATION




DD PACKAGE
8-LEAD (3mm × 3mm) PLASTIC DFN
$T_{JMAX}$ = 125°C, $\theta_{JA}$ = 43°C/W, $\theta_{JC}$ = 5.5°C/W
EXPOSED PAD (PIN 13) IS GND, MUST BE SOLDERED TO PCB




MSE PACKAGE
12-LEAD PLASTIC MSOP
$T_{JMAX}$ = 150°C, $\theta_{JA}$ = 40°C/W, $\theta_{JC}$ = 10°C/W
EXPOSED PAD (PIN 13) IS GND, MUST BE SOLDERED TO PCB FOR OPTIMAL THERMAL PERFORMANCE

## ORDER INFORMATION http://www.linear.com/product/LTC3624#orderinfo

| LEAD FREE FINISH | TAPE AND REEL | PART MARKING* | PACKAGE DESCRIPTION | TEMPERATURE RANGE |
|---|---|---|---|---|
| LTC3624EDD#PBF | LTC3624EDD#TRPBF | LGJF | 8-Lead (3mm × 3mm) Plastic DFN | –40°C to 125°C |
| LTC3624IDD#PBF | LTC3624IDD#TRPBF | LGJF | 8-Lead (3mm × 3mm) Plastic DFN | –40°C to 125°C |
| LTC3624EMSE#PBF | LTC3624EMSE#TRPBF | 3624 | 12-Lead Plastic MSOP | –40°C to 125°C |
| LTC3624IMSE#PBF | LTC3624IMSE#TRPBF | 3624 | 12-Lead Plastic MSOP | –40°C to 125°C |
| LTC3624HMSE#PBF | LTC3624HMSE#TRPBF | 3624 | 12-Lead Plastic MSOP | –40°C to 150°C |
| LTC3624EDD-3.3#PBF | LTC3624EDD-3.3#TRPBF | LGRG | 8-Lead (3mm × 3mm) Plastic DFN | –40°C to 125°C |
| LTC3624IDD-3.3#PBF | LTC3624IDD-3.3#TRPBF | LGRG | 8-Lead (3mm × 3mm) Plastic DFN | –40°C to 125°C |
| LTC3624EMSE-3.3#PBF | LTC3624EMSE-3.3#TRPBF | 362433 | 12-Lead Plastic MSOP | –40°C to 125°C |
| LTC3624IMSE-3.3#PBF | LTC3624IMSE-3.3#TRPBF | 362433 | 12-Lead Plastic MSOP | –40°C to 125°C |
| LTC3624HMSE-3.3#PBF | LTC3624HMSE-3.3#TRPBF | 362433 | 12-Lead Plastic MSOP | –40°C to 150°C |
| LTC3624EDD-5#PBF | LTC3624EDD-5#TRPBF | LGRD | 8-Lead (3mm × 3mm) Plastic DFN | –40°C to 125°C |
| LTC3624IDD-5#PBF | LTC3624IDD-5#TRPBF | LGRD | 8-Lead (3mm × 3mm) Plastic DFN | –40°C to 125°C |
| LTC3624EMSE-5#PBF | LTC3624EMSE-5#TRPBF | 36245 | 12-Lead Plastic MSOP | –40°C to 125°C |
| LTC3624IMSE-5#PBF | LTC3624IMSE-5#TRPBF | 36245 | 12-Lead Plastic MSOP | –40°C to 125°C |
| LTC3624HMSE-5#PBF | LTC3624HMSE-5#TRPBF | 36245 | 12-Lead Plastic MSOP | –40°C to 150°C |
| LTC3624EDD-2#PBF | LTC3624EDD-2#TRPBF | LGMN | 8-Lead (3mm × 3mm) Plastic DFN | –40°C to 125°C |
| LTC3624IDD-2#PBF | LTC3624IDD-2#TRPBF | LGMN | 8-Lead (3mm × 3mm) Plastic DFN | –40°C to 125°C |
| LTC3624EMSE-2#PBF | LTC3624EMSE-2#TRPBF | 36242 | 12-Lead Plastic MSOP | –40°C to 125°C |
| LTC3624IMSE-2#PBF | LTC3624IMSE-2#TRPBF | 36242 | 12-Lead Plastic MSOP | –40°C to 125°C |

## ORDER INFORMATION

http://www.linear.com/product/LTC3624#orderinfo

| LEAD FREE FINISH | TAPE AND REEL | PART MARKING* | PACKAGE DESCRIPTION | TEMPERATURE RANGE |
|---|---|---|---|---|
| LTC3624HMSE-2#PBF | LTC3624HMSE-2#TRPBF | 36242 | 12-Lead Plastic MSOP | –40°C to 150°C |
| LTC3624EDD-23.3#PBF | LTC3624EDD-23.3#TRPBF | LGRH | 8-Lead (3mm × 3mm) Plastic DFN | –40°C to 125°C |
| LTC3624IDD-23.3#PBF | LTC3624IDD-23.3#TRPBF | LGRH | 8-Lead (3mm × 3mm) Plastic DFN | –40°C to 125°C |
| LTC3624EMSE-23.3#PBF | LTC3624EMSE-23.3#TRPBF | 362423 | 12-Lead Plastic MSOP | –40°C to 125°C |
| LTC3624IMSE-23.3#PBF | LTC3624IMSE-23.3#TRPBF | 362423 | 12-Lead Plastic MSOP | –40°C to 125°C |
| LTC3624HMSE-23.3#PBF | LTC3624HMSE-23.3#TRPBF | 362423 | 12-Lead Plastic MSOP | –40°C to 150°C |
| LTC3624EDD-25#PBF | LTC3624EDD-25#TRPBF | LGRF | 8-Lead (3mm × 3mm) Plastic DFN | –40°C to 125°C |
| LTC3624IDD-25#PBF | LTC3624IDD-25#TRPBF | LGRF | 8-Lead (3mm × 3mm) Plastic DFN | –40°C to 125°C |
| LTC3624EMSE-25#PBF | LTC3624EMSE-25#TRPBF | 362425 | 12-Lead Plastic MSOP | –40°C to 125°C |
| LTC3624IMSE-25#PBF | LTC3624IMSE-25#TRPBF | 362425 | 12-Lead Plastic MSOP | –40°C to 125°C |
| LTC3624HMSE-25#PBF | LTC3624HMSE-25#TRPBF | 362425 | 12-Lead Plastic MSOP | –40°C to 150°C |

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/

For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

## ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at $T_J$ = 25°C. (Note 2) $V_{IN}$ = 12V, unless otherwise noted.**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $V_{IN}$ | Operating Voltage | | | 2.7 | | 17 | V |
| $V_{OUT}$ | Output Voltage Range | | | 0.6 | | $V_{IN}$ | V |
| $I_{VIN}$ | Input Quiescent Current | Shutdown Mode, $V_{RUN}$ = 0V<br>Burst Mode Operation<br>Forced Continuous Mode (Note 3) | | | 0.1<br>3.5<br>1.8 | 1.0<br>7 | µA<br>µA<br>mA |
| $V_{FB}$ | Regulated Feedback Voltage | (Note 4) | <br>● | 0.594<br>0.591 | 0.6<br>0.6 | 0.606<br>0.609 | V<br>V |
| $V_{OUT}$ | Regulated Fixed Output Voltage | LTC3624-3.3/LTC3624-23.3 (Note 4) | <br>● | 3.267<br>3.250 | 3.3<br>3.3 | 3.333<br>3.350 | V<br>V |
| | | LTC3624-5/LTC3624-25 (Note 4) | <br>● | 4.950<br>4.925 | 5.0<br>5.0 | 5.050<br>5.075 | V<br>V |
| $\Delta V_{LINE(REG)}$ | Reference Voltage Line Regulation | $V_{IN}$ = 2.7V to 17V (Note 4) | | | 0.01 | 0.015 | %/V |
| $\Delta V_{LOAD(REG)}$ | Output Voltage Load Regulation | (Note 4) | | | 0.1 | | % |
| $I_{LSW}$ | NMOS Switch Leakage<br>PMOS Switch Leakage | | | | 0.1<br>0.1 | 1<br>1 | µA<br>µA |
| $R_{DS(ON)}$ | NMOS On-Resistance | | | | 115 | | mΩ |
| | PMOS On-Resistance | $V_{IN}$ = 5V | | | 200 | | mΩ |
| $D_{MAX}$ | Maximum Duty Cycle | $V_{FB}$ = 0.5V, $V_{MODE/SYNC}$ = 1.5V | ● | | 100 | | % |
| $t_{ON(MIN)}$ | Minimum On-Time | | | | 60 | | ns |
| $V_{RUN}$ | RUN Input High<br>RUN Input Low | | | <br>0.35 | | 1.0 | V<br>V |
| $I_{RUN}$ | RUN Input Current | $V_{RUN}$ = 12V | | | 0 | 100 | nA |

## ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at $T_J$ = 25°C. (Note 2) $V_{IN}$ = 12V, unless otherwise noted.**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $V_{MODE/SYNC}$ | Pulse-Skipping Mode<br>Burst Mode Operation<br>Forced Continuous Mode | | | <br>$V_{INTVCC}$ – 0.4<br>1.0 | | 0.3<br><br>$V_{INTVCC}$ – 1.2 | V<br>V<br>V |
| $I_{MODE/SYNC}$ | MODE/SYNC Input Current | | | | 0 | 100 | nA |
| $t_{SS}$ | Internal Soft-Start Time | | | | 1 | | ms |
| $I_{LIM}$ | Peak Current Limit | $V_{IN}$ > 5V (E-, I-Grade)<br>$V_{IN}$ > 5V (H-Grade) | ●<br>● | 2.4<br>2.3 | 3 | 3.6 | A<br>A |
| $I_{FB}$ | FB Input Current | | | | | 10 | nA |
| $I_{FB(VOUT)}$ | Feedback Input Leakage Current | Fixed Output Versions | | | 2 | 10 | µA |
| $V_{UVLO}$ | $V_{INTVCC}$ Undervoltage Lockout | $V_{IN}$ Ramping Up | | 2.4 | 2.6 | 2.7 | V |
| $V_{UVLO(HYS)}$ | $V_{INTVCC}$ Undervoltage Lockout Hysteresis | | | | 175 | | mV |
| $V_{OVLO}$ | $V_{IN}$ Overvoltage Lockout Rising | | ● | 18 | 19 | 20 | V |
| $V_{OVLO(HYS)}$ | $V_{IN}$ Overvoltage Lockout Hysteresis | | | | 500 | | mV |
| $f_{OSC}$ | Oscillator Frequency | LTC3624/LTC3624-3.3/LTC3624-5<br>(E-, I-Grade)<br>(H-Grade) | <br>●<br>● | 0.92<br>0.82<br>0.78 | <br>1.00 | 1.08<br>1.16 | MHz<br>MHz<br>MHz |
| | | LTC3624-2/LTC3624-23.3/LTC3624-25<br>(E-, I-Grade)<br>(H-Grade) | <br>●<br>● | 2.05<br>1.8<br>1.7 | <br>2.25 | 2.45<br>2.6 | MHz<br>MHz<br>MHz |
| $f_{SYNC}$ | SYNC Capture Range | LTC3624/LTC3624-3.3/LTC3624-5 | | 50 | | 150 | % |
| | | LTC3624-2/LTC3624-23.3/LTC3624-25 | | 50 | | 140 | % |
| $V_{INTVCC}$ | $V_{INTVCC}$ LDO Output Voltage | $V_{IN}$ > 4V | | 3.2 | 3.6 | 4.0 | V |
| $\Delta V_{PGOOD}$ | Power Good Range | LTC3624/LTC3624-2 | | | ±7.5 | ±11.5 | % |
| | | LTC3624-3.3/LTC3624-5/LTC3624-23.3/<br>LTC3624-25 | | | ±7.5 | ±13 | % |
| $R_{PGOOD}$ | Power Good Resistance | | | | 280 | 350 | Ω |
| $t_{PGOOD}$ | PGOOD Delay | PGOOD Low to High<br>PGOOD High to Low | | | 0<br>32 | | Cycles<br>Cycles |

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** The LTC3624/LTC3624-2 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC3624E/LTC3624E-2 is guaranteed to meet specifications from 0°C to 85°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3624I/LTC3624I-2 is guaranteed over the –40°C to 125°C operating junction temperature range and the LTC3624H is guaranteed over the –40°C to 150°C operating junction temperature range. High junction temperatures degrade operating lifetimes; operation lifetime is decreased for junction temperatures greater than 125°C. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors. $T_J$ is calculated from the ambient, $T_A$, and power dissipation, $P_D$, according to the following formula:

$$T_J = T_A + (P_D \bullet \theta_{JA})$$

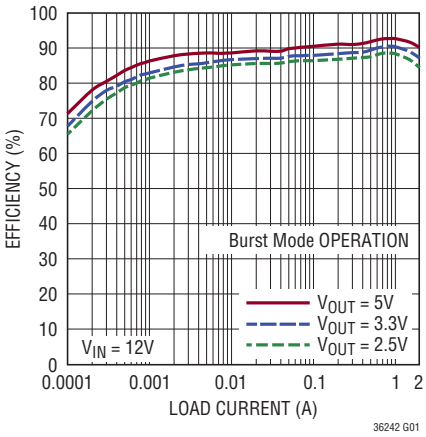
**Note 3:** The quiescent current in forced continuous mode does not include switching loss of the power FETs.

**Note 4:** The LTC3624 is tested in a proprietary test mode that servos FB to the output of the error amplifier.

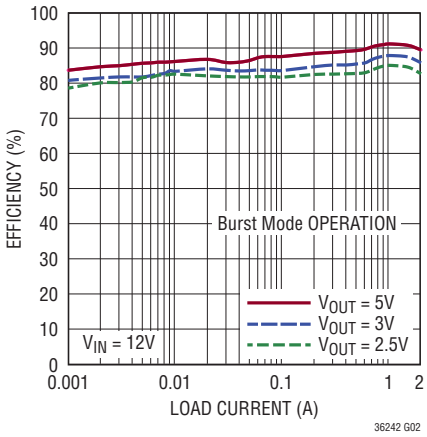
**Note 5:** This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. The maximum rated junction temperature will be exceeded when overtemperature protection is active Continuous operation above the specified maximum operating junction temperature may impair device reliability. The overtemperature protection level is not production tested but guaranteed by design.

## TYPICAL PERFORMANCE CHARACTERISTICS $T_J$ = 25°C, unless otherwise noted.

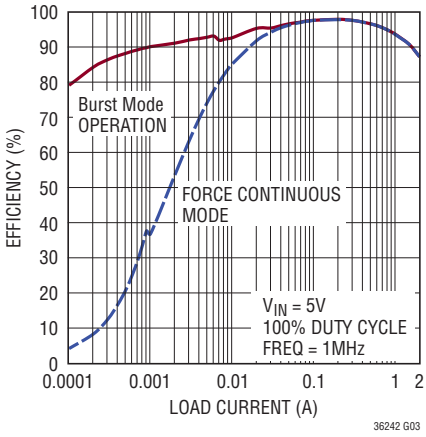
### Efficiency vs Load Current at 1MHz



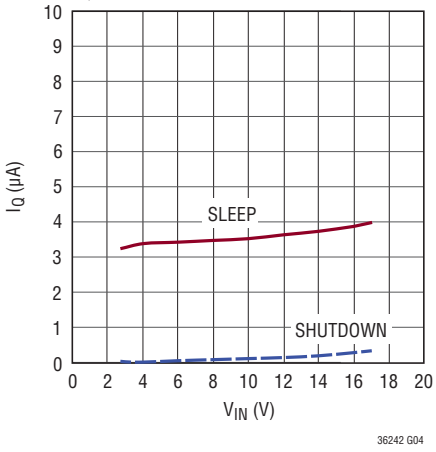

### Efficiency vs Load Current in Burst Mode Operation at 2.25MHz



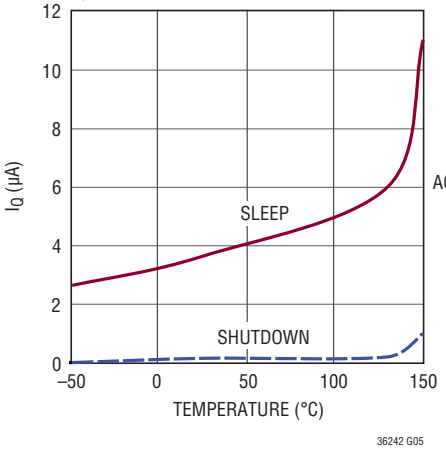

### Efficiency vs Load Current in Dropout



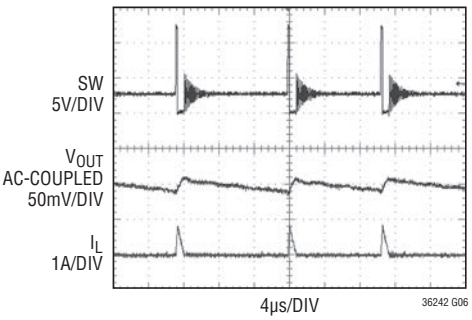

### $I_Q$ vs $V_{IN}$




### $I_Q$ vs Temperature

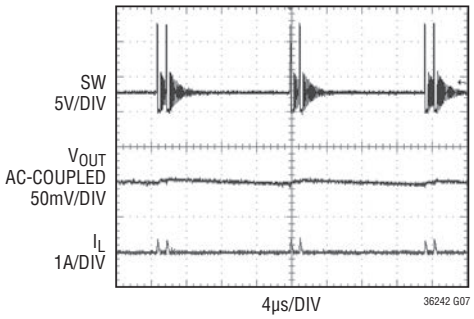



### Burst Mode Operation



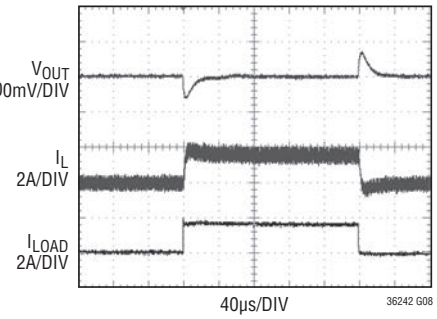

$V_{IN}$ = 12V
$V_{OUT}$ = 2.5V
Burst Mode OPERATION
$I_{OUT}$ = 30mA
L = 2.2µH

### Pulse-Skipping Mode Operation



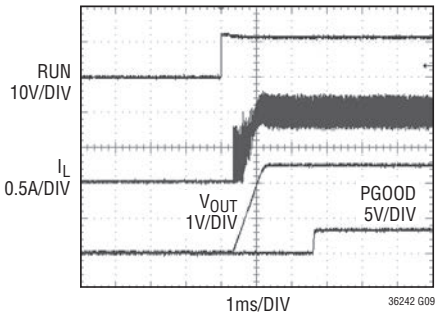

$V_{IN}$ = 12V
$V_{OUT}$ = 2.5V
PULSE-SKIPPING MODE
$I_{OUT}$ = 10mA
L = 2.2µH

### Load Transient Response




$V_{IN}$ = 12V
$V_{OUT}$ = 2.5V
$I_{LOAD}$ = 0A to 1.8A
FORCED CONTINUOUS MODE

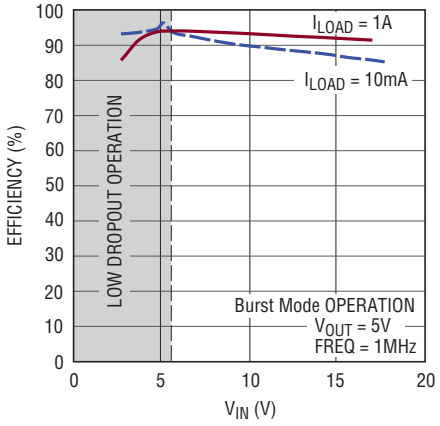
### Soft-Start Operation



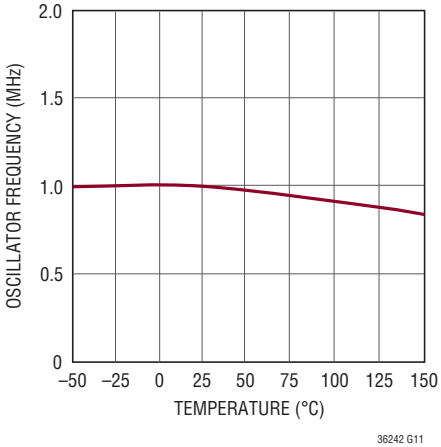

$V_{IN}$ = 12V
$V_{OUT}$ = 2.5V
$I_{LOAD}$ = 1A

## TYPICAL PERFORMANCE CHARACTERISTICS $T_J$ = 25°C, unless otherwise noted.

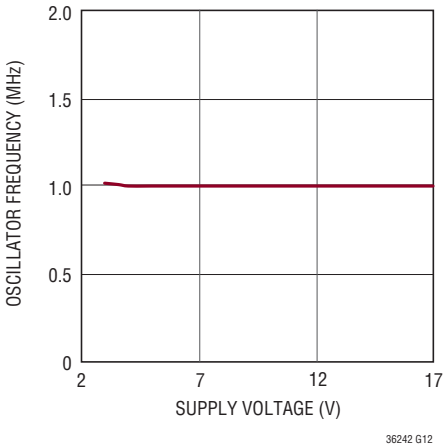
### Efficiency vs Input Voltage



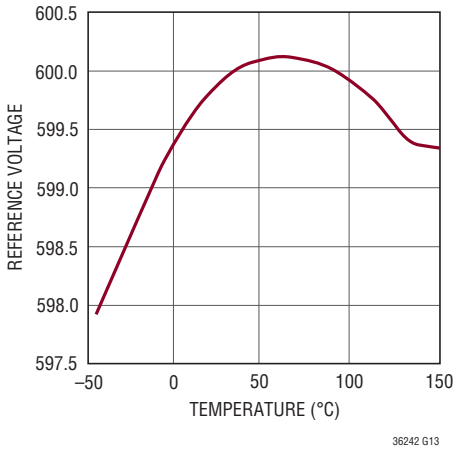

### Oscillator Frequency vs Temperature



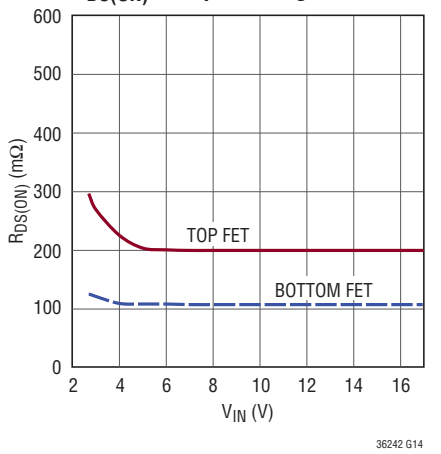

### Oscillator Frequency vs Supply Voltage



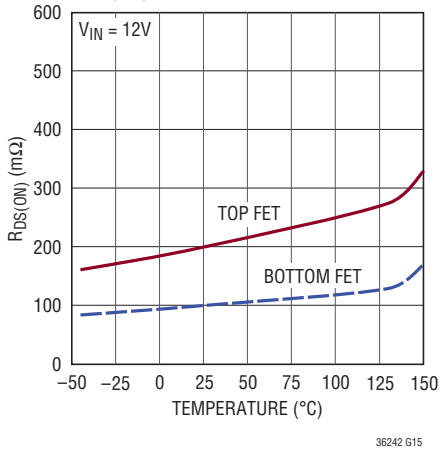

### Reference Voltage vs Temperature



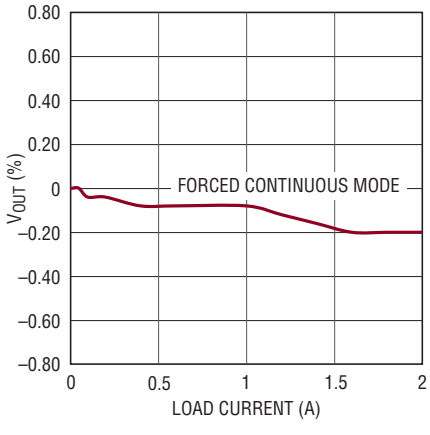

### $R_{DS(ON)}$ vs Input Voltage



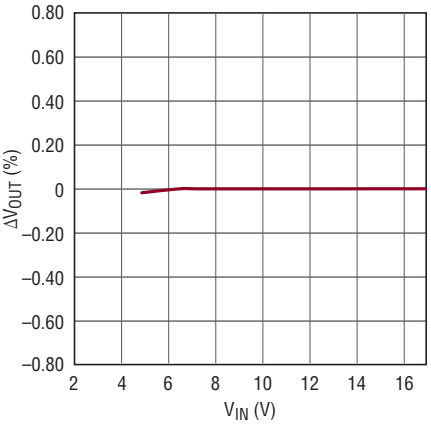

### $R_{DS(ON)}$ vs Temperature



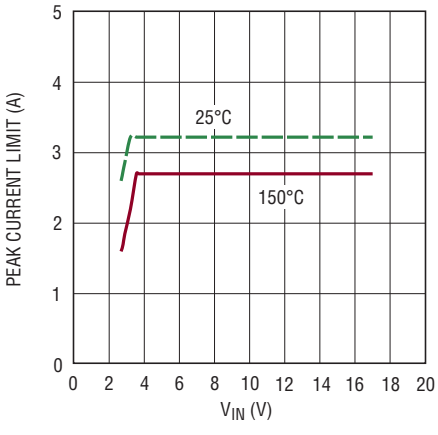

### Load Regulation




### Line Regulation




### $V_{IN}$ vs Peak Current Limit



## PIN FUNCTIONS (DFN/MSOP)

**SW (Pin 1/Pins 1, 2):** Switch Node Connection to the Inductor of the Step-Down Regulator.

**$V_{IN}$ (Pin 2/Pins 3, 4):** Input Voltage of the Step-Down Regulator.

**RUN (Pin 3/Pin 5):** Logic Controlled RUN Input. Do not leave this pin floating. Logic high activates the step-down regulator.

**PGOOD (Pin 4/Pin 6):** $V_{OUT}$ within Regulation Indicator.

**FB (Pin 5/Pin 8):** Feedback Input to the Error Amplifier of the Step-Down Regulator. Connect a resistor divider tap to this pin. The output voltage can be adjusted from 0.6V to $V_{IN}$ by:

$$V_{OUT} = 0.6V \bullet [1 + (R2/R1)]$$

See Figure 1.

For fixed $V_{OUT}$ options, connect the FB pin directly to $V_{OUT}$.

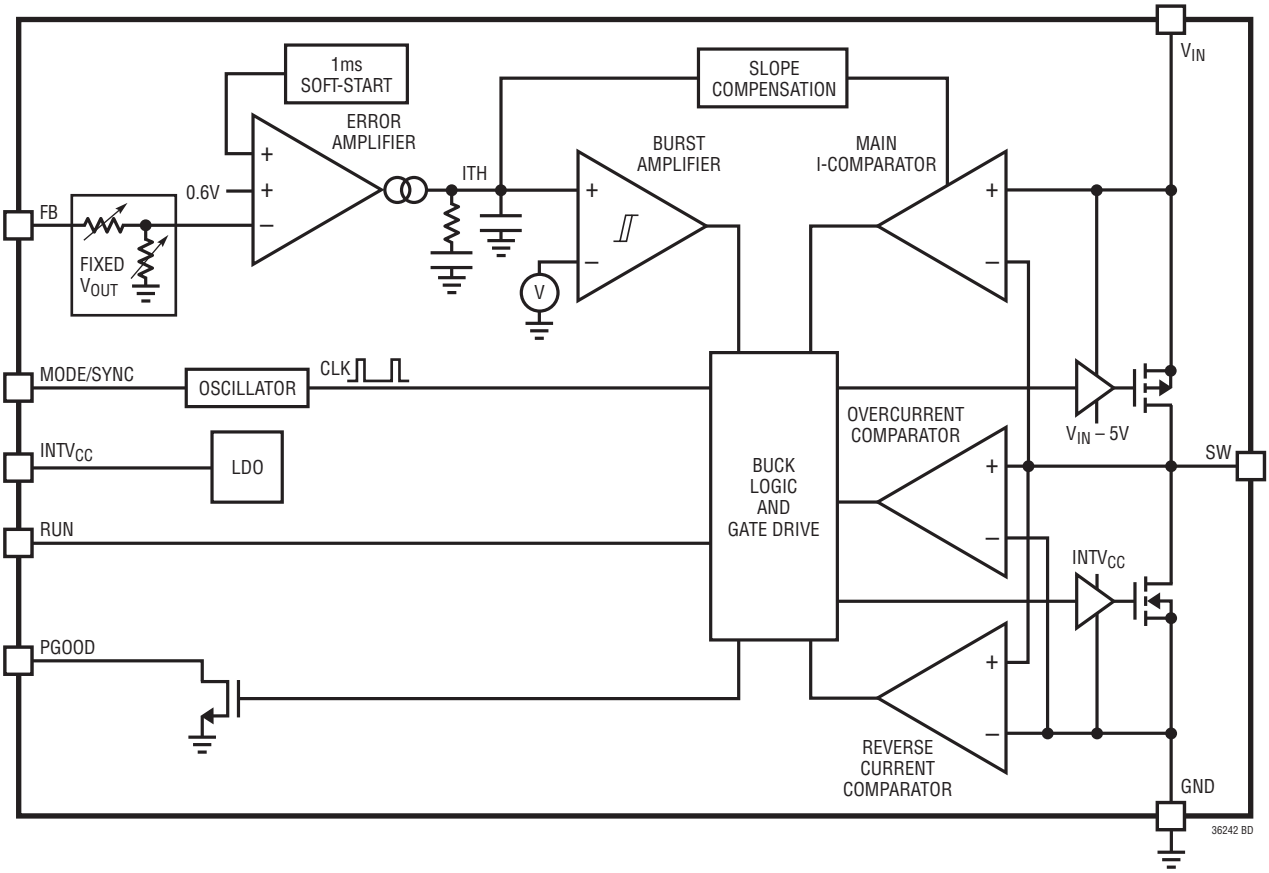
**$INTV_{CC}$ (Pin 6/Pin 9):** Low Dropout Regulator. Bypass with at least 2.2µF to Ground.

**MODE/SYNC (Pin 7/Pin 10):** Burst Mode Select and External Clock Synchronization of the Step-Down Regulator. Tie MODE/SYNC to $INTV_{CC}$ for Burst Mode operation with a 800mA peak current clamp, tie MODE/SYNC to GND for pulse skipping operation, and tie MODE/SYNC to a voltage between 1V and $V_{INTVCC}$ – 1.2V for forced continuous mode. Furthermore, connecting MODE/SYNC to an external clock will sync the system clock to the external clock and put the part in forced continuous mode.

**GND (Pin 8, Exposed Pad Pin 9/Pins 11, 12, Exposed Pad Pin 13):** Power and Signal Ground. The exposed pad must be soldered to PCB ground for electrical and rated thermal performance.

**NC (Pin 7, MSOP Only):** No Connect. There is no electrical connection to this pin inside the package.

## BLOCK DIAGRAM



## OPERATION

The LTC3624/LTC3624-2 uses a constant-frequency, peak current mode architecture. It operates through a wide $V_{IN}$ range and regulates with ultralow quiescent current. The operation frequency is set at either 1MHz or 2.25MHz and can be synchronized to an external oscillator ±40% of the inherent frequency. To suit a variety of applications, the selectable MODE/SYNC pin allows the user to trade off output ripple for efficiency.

The output voltage is set by an external divider returned to the FB pin. An error amplifier compares the divided output voltage with a reference voltage of 0.6V and adjusts the peak inductor current accordingly. Overvoltage and undervoltage comparators will pull the PGOOD output low if the output voltage is not within ±7.5% of the programmed value. The PGOOD output will go low 32 clock cycles after falling out of regulation and will go high immediately after achieving regulation.

### Main Control Loop

During normal operation, the top power switch (P-channel MOSFET) is turned on at the beginning of a clock cycle. The inductor current is allowed to ramp up to a peak level. Once that level is reached, the top power switch is turned off and the bottom switch (N-channel MOSFET) is turned on until the next clock cycle. The peak current level is controlled by the internally compensated ITH voltage, which is the output of the error amplifier. This amplifier compares the FB voltage to the 0.6V internal reference. When the load current increases, the FB voltage decreases slightly below the reference, which causes the error amplifier to increase the ITH voltage until the average inductor current matches the new load current.

The main control loop is shut down by pulling the RUN pin to ground.

### Low Current Operation

Two discontinuous-conduction modes (DCMs) are available to control the operation of the LTC3624/LTC3624-2 at low currents. Both modes, Burst Mode operation and pulse-skipping, automatically switch from continuous operation to the selected mode when the load current is low.

To optimize efficiency, Burst Mode operation can be selected by tying the MODE/SYNC pin to $INTV_{CC}$. In Burst Mode operation, the peak inductor current is set to be at least 800mA, even if the output of the error amplifier demands less. Thus, when the switcher is on at relatively light output loads, FB voltage will rise and cause the ITH voltage to drop. Once the ITH voltage goes below 0.2V, the switcher goes into its sleep mode with both power switches off. The switcher remains in this sleep state until the external load pulls the output voltage below its regulation point. During sleep mode, the part draws an ultralow 3.5µA of quiescent current from $V_{IN}$.

To minimize $V_{OUT}$ ripple, pulse-skipping mode can be selected by grounding the MODE/SYNC pin. In the LTC3624/LTC3624-2, pulse-skipping mode is implemented similarly to Burst Mode operation with the peak inductor current set to be at least 132mA. This results in lower ripple than in Burst Mode operation with the trade-off being slightly lower efficiency.

### Forced Continuous Mode Operation

Aside from the two discontinuous-conduction modes, the LTC3624/LTC3624-2 also has the ability to operate in the forced continuous mode by setting the MODE/SYNC voltage between 1V and $V_{INTVCC}$ – 1.2V. In forced continuous mode, the switcher will switch cycle by cycle regardless of what the output load current is. If forced continuous mode is selected, the minimum peak current is set to be –266mA in order to ensure that the part can operate continuously at zero output load.

### High Duty Cycle/Dropout Operation

When the input supply voltage decreases towards the output voltage, the duty cycle increases and slope compensation is required to maintain the fixed switching frequency. The LTC3624/LTC3624-2 has internal circuitry to accurately maintain the peak current limit ($I_{LIM}$) of 3A even at high duty cycles.

As the duty cycle approaches 100%, the LTC3624/LTC3624-2 enters dropout operation. During dropout, if force continuous mode is selected, the top PMOS switch is turned on continuously, and all active circuitry is kept

## OPERATION

alive. However, if Burst Mode operation or pulse-skipping mode is selected, the part will transition in and out of sleep mode depending on the output load current. This significantly reduces the quiescent current, thus prolonging the use of the input supply.

### $V_{IN}$ Overvoltage Protection

In order to protect the internal power MOSFET devices against transient voltage spikes, the LTC3624/LTC3624-2 constantly monitors the $V_{IN}$ pin for an overvoltage condition. When $V_{IN}$ rises above 19V, the regulator suspends operation by shutting off both power MOSFETs. Once $V_{IN}$ drops below 18.5V, the regulator immediately resumes normal operation. The regulator executes its soft-start function when exiting an overvoltage condition.

### Minimum On-Time

The minimum on-time is the smallest duration of the time the top power switch is allowed to be in its on state. This time is typically 60ns. In forced continuous mode operation, the minimum on-time limit imposes a minimum duty cycle of 6% for the LTC3624 ($F_{SW}$ = 1MHz) and 13.5% for the LTC3624-2 ($F_{SW}$ = 2.25MHz). In the rare cases that this minimum on-time is violated, the output voltage may lose regulation. In such situation, the user must choose either Burst Mode or pulse-skipping mode operation, or apply a slower external clock to force a slower switching frequency in order to adhere to the minimum on-time limitation.

### Low Supply Operation

The LTC3624 incorporates an undervoltage lockout circuit which shuts down the part when the input voltage drops below 2.7V. As the input voltage rises slightly above the undervoltage threshold, the switcher will begin its basic operation. However, the $R_{DS(ON)}$ of the top and bottom switch will be slightly higher than that specified in the electrical characteristics due to lack of gate drive. Refer to graph of $R_{DS(ON)}$ versus $V_{IN}$ for more details.

### Soft-Start

The LTC3624/LTC3624-2 has an internal 1ms soft-start ramp. During start-up soft-start operation, the switcher will operate in pulse-skipping mode.

## APPLICATIONS INFORMATION

### Output Voltage Programming

The output voltage is set by external resistive divider according to the following equation for adjustable output versions:

$$V_{OUT} = 0.6V \bullet \left(1 + \frac{R2}{R1}\right)$$

The resistive divider allows the FB pin to sense a fraction of the output voltage as shown in Figure 1.

For fixed $V_{OUT}$ options, connect FB pin directly to $V_{OUT}$.

### Input Capacitor ($C_{IN}$) Selection

The input capacitance, $C_{IN}$, is needed to filter the square wave current at the drain of the top power MOSFET. To

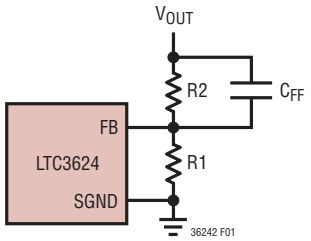



**Figure 1. Setting the Output Voltage (Adjustable Version)**

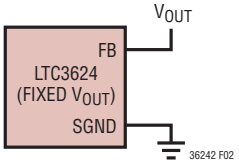



**Figure 2. Setting the Output Voltage (Fixed $V_{OUT}$ Option)**

## APPLICATIONS INFORMATION

prevent large voltage transients from occurring, a low ESR input capacitor sized for the maximum RMS current should be used. The maximum RMS current is given by:

$$I_{RMS} \cong I_{OUT(MAX)} \frac{V_{OUT}}{V_{IN}} \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where:

$$I_{RMS} \cong \frac{I_{OUT}}{2}$$

This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that ripple current ratings from capacitor manufacturers are often based on only 2000 hours of life which makes it advisable to further derate the capacitor, or choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design. For low input voltage applications, sufficient bulk input capacitance is needed to minimize transient effects during output load changes.

### Output Capacitor ($C_{OUT}$) Selection

The selection of $C_{OUT}$ is determined by the effective series resistance (ESR) that is required to minimize voltage ripple and load step transients as well as the amount of bulk capacitance that is necessary to ensure that the control loop is stable. Loop stability can be checked by viewing the load transient response. The output ripple, $\Delta V_{OUT}$, is determined by:

$$\Delta V_{OUT} < \Delta I_L \left( \frac{1}{8 \bullet f \bullet C_{OUT}} + ESR \right)$$

The output ripple is highest at maximum input voltage since $\Delta I_L$ increases with input voltage. Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements. Dry tantalum, special polymer, aluminum electrolytic, and ceramic capacitors are all available in surface mount packages. Special polymer capacitors are very low ESR but have lower capacitance density than other types. Tantalum capacitors have the highest capacitance density but it is important to only use types that have been surge tested for use in switching power supplies. Aluminum electrolytic capacitors have significantly higher ESR, but can be used in cost-sensitive applications provided that consideration is given to ripple current ratings and long-term reliability. Ceramic capacitors have excellent low ESR characteristics and small footprints.

### Using Ceramic Input and Output Capacitors

Higher values, lower cost ceramic capacitors are now becoming available in smaller case sizes. Their high ripple current, high voltage rating and low ESR make them ideal for switching regulator applications. However, care must be taken when these capacitors are used at the input and output. When a ceramic capacitor is used at the input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the $V_{IN}$ input. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at $V_{IN}$ large enough to damage the part.

When choosing the input and output ceramic capacitors, choose the X5R and X7R dielectric formulations. These dielectrics have the best temperature and voltage characteristics of all the ceramics for a given value and size.

Since the ESR of a ceramic capacitor is so low, the input and output capacitor must instead fulfill a charge storage requirement. During a load step, the output capacitor must instantaneously supply the current to support the load until the feedback loop raises the switch current enough to support the load. Typically, five cycles are required to respond to a load step, but only in the first cycle does the output voltage drop linearly. The output droop, $V_{DROOP}$, is

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usually about three times the linear drop of the first cycle. Thus, a good place to start with the output capacitor value is approximately:

$$C_{OUT} = 3\frac{\Delta I_{OUT}}{f \bullet V_{DROOP}}$$

More capacitance may be required depending on the duty cycle and load-step requirements. In most applications, the input capacitor is merely required to supply high frequency bypassing, since the impedance to the supply is very low. A 10µF ceramic capacitor is usually enough for these conditions. Place this input capacitor as close to the $V_{IN}$ pin as possible.

### Output Power Good

When the LTC3624/LTC3624-2's output voltage is within the ±7.5% window of the regulation point, the output voltage is good and the PGOOD pin is pulled high with an external resistor. Otherwise, an internal open-drain pull-down device (280Ω) will pull the PGOOD pin low. To prevent unwanted PGOOD glitches during transients or dynamic $V_{OUT}$ changes, the LTC3624/LTC3624-2's PGOOD falling edge includes a blanking delay of approximately 32 switching cycles.

### Frequency Sync Capability

The LTC3624/LTC3624-2 has the capability to sync to a ±40% range of the internal programmed frequency. It takes 2 to 3 cycles of external clock to engage the sync mode, and roughly 2µs of no clocks for the part to realize that the sync signal is gone. Once engaged in sync, the LTC3624/LTC3624-2 immediately runs at the external clock frequency.

### Inductor Selection

Given the desired input and output voltages, the inductor value and operating frequency determine the ripple current:

$$\Delta I_L = \frac{V_{OUT}}{f \bullet L}\left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right)$$

Lower ripple current reduces power losses in the inductor, ESR losses in the output capacitors and output voltage ripple. Highest efficiency operation is obtained at low frequency with small ripple current. However, achieving this requires a large inductor. There is a trade-off between component size, efficiency and operating frequency.

A reasonable starting point is to choose a ripple current that is about 40% of $I_{OUT(MAX)}$. To guarantee that ripple current does not exceed a specified maximum, the inductance should be chosen according to:

$$L = \frac{V_{OUT}}{f \bullet \Delta I_{L(MAX)}}\left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right)$$

Once the value for L is known, the type of inductor must be selected. Actual core loss is independent of core size for a fixed inductor value, but is very dependent on the inductance selected. As the inductance or frequency increases, core losses decrease. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase.

Ferrite designs have very low core losses and are preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates "hard", which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequent output voltage ripple. Do not allow the core to saturate!

Different core materials and shapes will change the size/current and price/current relationship of an inductor. Toroid or shielded pot cores in ferrite or permalloy materials are small and don't radiate much energy, but generally cost more than powdered iron core inductors with similar characteristics. The choice of which style inductor to use mainly depends on the price versus size requirements and any radiated field/EMI requirements. New designs for surface mount inductors are available from Toko, Vishay, Coilcraft, NEC/Tokin, Cooper, TDK and Würth Elektronik. Refer to Table 1 for more details.

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**Table 1. Inductor Selection Table**

| INDUCTOR | INDUCTANCE (µH) | DCR (mΩ) | MAX CURRENT (A) | DIMENSIONS (mm) | HEIGHT (mm) | MANUFACTURER |
|---|---|---|---|---|---|---|
| XAL4020 Series | 1.0 | 13.25 | 8.7 | 4.3 × 4.3 | 2.1 | Coilcraft |
| | 1.5 | 21.45 | 7.1 | 4.3 × 4.3 | 2.1 | www.coilcraft.com |
| | 2.2 | 35.20 | 5.6 | 4.3 × 4.3 | 2.1 | |
| XAL4030 Series | 3.3 | 26.0 | 5.5 | 4.3 × 4.3 | 3.1 | |
| | 4.7 | 40.1 | 4.5 | 4.3 × 4.3 | 3.1 | |
| | 6.8 | 67.4 | 3.6 | 4.3 × 4.3 | 3.1 | |
| IHLP-1616BZ-11 Series | 1.0 | 24 | 4.5 | 4.3 × 4.7 | 2 | Vishay |
| | 2.2 | 61 | 3.25 | 4.3 × 4.7 | 2 | www.vishay.com |
| IHLP-2020BZ-01 Series | 1 | 18.9 | 7 | 5.4 × 5.7 | 2 | |
| | 2.2 | 45.6 | 4.2 | 5.4 × 5.7 | 2 | |
| | 3.3 | 79.2 | 3.3 | 5.4 × 5.7 | 2 | |
| | 4.7 | 108 | 2.8 | 5.4 × 5.7 | 2 | |
| | 5.6 | 113 | 2.5 | 5.4 × 5.7 | 2 | |
| | 6.8 | 139 | 2.4 | 5.4 × 5.7 | 2 | |
| FDV0620 Series | 1 | 18 | 5.7 | 6.7 × 7.4 | 2 | Toko |
| | 2.2 | 37 | 4 | 6.7 × 7.4 | 2 | www.toko.com |
| | 3.3 | 51 | 3.2 | 6.7 × 7.4 | 2 | |
| | 4.7 | 68 | 2.8 | 6.7 × 7.4 | 2 | |
| MPLC0525L Series | 1 | 16 | 6.4 | 6.2 × 5.4 | 2.5 | NEC/Tokin |
| | 1.5 | 24 | 5.2 | 6.2 × 5.4 | 2.5 | www.nec-tokin.com |
| | 2.2 | 40 | 4.1 | 6.2 × 5.4 | 2.5 | |
| HCP0703 Series | 1 | 9 | 11 | 7 × 7.3 | 3 | Cooper Bussmann |
| | 1.5 | 14 | 9 | 7 × 7.3 | 3 | www.cooperbussmann.com |
| | 2.2 | 18 | 8 | 7 × 7.3 | 3 | |
| | 3.3 | 28 | 6 | 7 × 7.3 | 3 | |
| | 4.7 | 37 | 5.5 | 7 × 7.3 | 3 | |
| | 6.8 | 54 | 4.5 | 7 × 7.3 | 3 | |
| | 8.2 | 64 | 4 | 7 × 7.3 | 3 | |
| RLF7030 Series | 1 | 8.8 | 6.4 | 6.9 × 7.3 | 3.2 | TDK |
| | 1.5 | 9.6 | 6.1 | 6.9 × 7.3 | 3.2 | www.tdk.com |
| | 2.2 | 12 | 5.4 | 6.9 × 7.3 | 3.2 | |
| | 3.3 | 20 | 4.1 | 6.9 × 7.3 | 3.2 | |
| | 4.7 | 31 | 3.4 | 6.9 × 7.3 | 3.2 | |
| | 6.8 | 45 | 2.8 | 6.9 × 7.3 | 3.2 | |
| WE-TPC 4828 Series | 1.2 | 17 | 3.1 | 4.8 × 4.8 | 2.8 | Würth Elektronik |
| | 1.8 | 20 | 2.7 | 4.8 × 4.8 | 2.8 | www.we-online.com |
| | 2.2 | 23 | 2.5 | 4.8 × 4.8 | 2.8 | |
| | 2.7 | 27 | 2.35 | 4.8 × 4.8 | 2.8 | |
| | 3.3 | 30 | 2.15 | 4.8 × 4.8 | 2.8 | |

### Checking Transient Response

The regular loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in load current. When a load step occurs, $V_{OUT}$ immediately shifts by an amount equal to the $\Delta I_{LOAD}$ • ESR, where ESR is the effective series resistance of $C_{OUT}$. $\Delta I_{LOAD}$ also begins to charge or discharge $C_{OUT}$ generating a feedback error signal used by the regulator to return $V_{OUT}$ to its steady-state value. During this recovery time, $V_{OUT}$ can be monitored for overshoot or ringing that would indicate a stability problem.

The initial output voltage step may not be within the bandwidth of the feedback loop, so the standard second order overshoot/DC ratio cannot be used to determine phase margin. In addition, a feedforward capacitor can be added to improve the high frequency response, as

## APPLICATIONS INFORMATION

shown in Figure 1. Capacitor $C_{FF}$ provides phase lead by creating a high frequency zero with R2, which improves the phase margin.

The output voltage settling behavior is related to the stability of the closed-loop system and will demonstrate the actual overall supply performance. For a detailed explanation of optimizing the compensation components, including a review of control loop theory, refer to application Note 76.

In some applications, a more severe transient can be caused by switching in loads with large (>1µF) input capacitors. The discharge input capacitors are effectively put in parallel with $C_{OUT}$, causing a rapid drop in $V_{OUT}$. No regulator can deliver enough current to prevent this problem if the switch connecting the load has low resistance and is driven quickly. The solution is to limit the turn-on speed of the load switch driver. A Hot Swap™ controller is designed specifically for this purpose and usually incorporates current limiting, short-circuit protection and soft-starting.

### Efficiency Considerations

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Percent efficiency can be expressed as:

$$\% \text{ Efficiency} = 100\% - (L1 + L2 + L3 + \ldots)$$

where L1, L2, etc. are the individual losses as a percentage of input power. Although all dissipative elements in the circuit produce losses, three main sources usually account for most of the losses in LTC3624/LTC3624-2 circuits: 1) $I^2R$ losses, 2) switching and biasing losses, 3) other losses.

1. $I^2R$ losses are calculated from the DC resistances of the internal switches, $R_{SW}$, and external inductor, $R_L$. In continuous mode, the average output current flows through inductor L but is "chopped" between the internal top and bottom power MOSFETs. Thus, the series resistance looking into the SW pin is a function of both top and bottom MOSFET $R_{DS(ON)}$ and the duty cycle (DC) as follows:

   $$R_{SW} = (R_{DS(ON)TOP})(DC) + (R_{DS(ON)BOT})(1 - DC)$$

   The $R_{DS(ON)}$ for both the top and bottom MOSFETs can be obtained from the Typical Performance Characteristics curves. Thus to obtain $I^2R$ losses:

   $$I^2R \text{ losses} = I_{OUT}^2(R_{SW} + R_L)$$

2. The switching current is the sum of the MOSFET driver and control currents. The power MOSFET driver current results from switching the gate capacitance of the power MOSFETs. Each time a power MOSFET gate is switched from low to high to low again, a packet of charge dQ moves from IN to ground. The resulting dQ/dt is a current out of IN that is typically much larger than the DC control bias current. In continuous mode, $I_{GATECHG} = f(Q_T + Q_B)$, where $Q_T$ and $Q_B$ are the gate charges of the internal top and bottom power MOSFETs and f is the switching frequency. The power loss is thus:

   $$\text{Switching Loss} = I_{GATECHG} \bullet V_{IN}$$

   The gate charge loss is proportional to $V_{IN}$ and f and thus their effects will be more pronounced at higher supply voltages and higher frequencies.

3. Other "hidden" losses such as transition loss and copper trace and internal load resistances can account for additional efficiency degradations in the overall power system. It is very important to include these "system" level losses in the design of a system. Transition loss arises from the brief amount of time the top power MOSFET spends in the saturated region during switch node transitions. The LTC3624/LTC3624-2 internal power devices switch quickly enough that these losses are not significant compared to other sources. These losses plus other losses, including diode conduction losses during dead-time and inductor core losses, generally account for less than 2% total additional loss.

### Thermal Conditions

In a majority of applications, the LTC3624/LTC3624-2 does not dissipate much heat due to its high efficiency and low thermal resistance of its exposed pad DFN package. However, in applications where the LTC3624/LTC3624-2 is running at high ambient temperature, high $V_{IN}$, high switching frequency, and maximum output current load,

## APPLICATIONS INFORMATION

the heat dissipated may exceed the maximum junction temperature of the part. If the junction temperature reaches approximately 160°C, both power switches will be turned off until the temperature drops about 15°C cooler.

To avoid the LTC3624/LTC3624-2 from exceeding the maximum junction temperature, the user will need to do some thermal analysis. The goal of the thermal analysis is to determine whether the power dissipated exceeds the maximum junction temperature of the part. The temperature rise is given by:

$$T_{RISE} = P_D \bullet \theta_{JA}$$

As an example, consider the case when the LTC3624/LTC3624-2 is used in applications where $V_{IN}$ = 12V, $I_{OUT}$ = 2A, f = 1MHz, $V_{OUT}$ = 1.8V. The equivalent power MOSFET resistance $R_{SW}$ is:

$$R_{SW} = R_{DS(ON)TOP} \bullet \frac{V_{OUT}}{V_{IN}} + R_{DS(ON)BOT} \bullet \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

$$= 200m\Omega \bullet \frac{1.8V}{12V} + 100m\Omega \bullet \left(1 - \frac{1.8V}{12V}\right)$$

$$= 115m\Omega$$

The $V_{IN}$ current during 1MHz force continuous operation with no load is about 8mA, which includes switching and internal biasing current loss, transition loss, inductor core loss and other losses in the application. Therefore, the total power dissipated by the part is:

$$P_D = I_{OUT}^2 \bullet R_{SW} + V_{IN} \bullet I_{IN(Q)}$$

$$= 2A^2 \bullet 115m\Omega + 12V \bullet 8mA$$

$$= 556mW$$

The DFN 3mm × 3mm package junction-to-ambient thermal resistance, $\theta_{JA}$, is around 43°C/W. Therefore, the junction temperature of the regulator operating in a 25°C ambient temperature is approximately:

$$T_J = T_A + T_{rise} = 25°C + 0.556W \bullet 43°C/W = 49°C$$

Remembering that the above junction temperature is obtained from an $R_{DS(ON)}$ at 25°C, we might recalculate the junction temperature based on a higher $R_{DS(ON)}$ since it increases with temperature. Redoing the calculation assuming that $R_{SW}$ increased 5% at 49°C yields a new junction temperature of 50°C. If the application calls for a higher ambient temperature and/or higher switching frequency, care should be taken to reduce the temperature rise of the part by using a heat sink or forced air flow.

### Board Layout Considerations

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC3624/LTC3624-2 (refer to Figure 3). Check the following in your layout:

1. Do the capacitors $C_{IN}$ connect to the $V_{IN}$ and GND as close as possible? These capacitors provide the AC current to the internal power MOSFETs and their drivers.
2. Are $C_{OUT}$ and L closely connected? The (–) plate of $C_{OUT}$ returns current to GND and the (–) plate of $C_{IN}$.
3. The resistive divider, R1 and R2, must be connected between the (+) plate of $C_{OUT}$ and a ground line terminated near GND. The feedback signal $V_{FB}$ should be routed away from noisy components and traces, such as the SW line, and its trace length should be minimized. Keep R1 and R2 close to the IC.
4. Solder the exposed pad (Pin 9) on the bottom of the package to the GND plane. Connect this GND plane to other layers with thermal vias to help dissipate heat from the LTC3624/LTC3624-2.
5. Keep sensitive components away from the SW pin. The input capacitor, $C_{IN}$, feedback resistors, and $INTV_{CC}$ bypass capacitors should be routed away from the SW trace and the inductor.
6. A ground plane is preferred.
7. Flood all unused areas on all layers with copper, which reduces the temperature rise of power components. These copper areas should be connected to GND.

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### Design Example

As a design example, consider using the LTC3624/LTC3624-2 in an application with the following specifications:

$V_{IN}$ = 10.8V to 13.2V

$V_{OUT}$ = 3.3V

$I_{OUT(MAX)}$ = 2A

$I_{OUT(MIN)}$ = 0A

$f_{SW}$ = 2.25MHz

Because efficiency and quiescent current are important at both 500mA and 0A current states, Burst Mode operation will be utilized.

Given the internal oscillator of 2.25MHz, we can calculate the inductor value for about 40% ripple current at maximum $V_{IN}$:

$$L = \left(\frac{3.3V}{2.25MHz \bullet 0.8A}\right)\left(1-\frac{3.3V}{13.2V}\right) = 1.38\mu H$$

Given this, a 1.5µH inductor would suffice.

$C_{OUT}$ will be selected based on the ESR that is required to satisfy the output voltage ripple requirement and the bulk capacitance needed for loop stability. For this design, a 47µF ceramic capacitor will be used.

$C_{IN}$ should be sized for a maximum current rating of:

$$I_{RMS} = 2A\left(\frac{3.3V}{13.2V}\right)\left(\frac{13.2V}{3.3V}-1\right)^{1/2} = 0.86A$$

Bypassing the $V_{IN}$ pin to ground with 10µF ceramic capacitors is adequate for most applications.

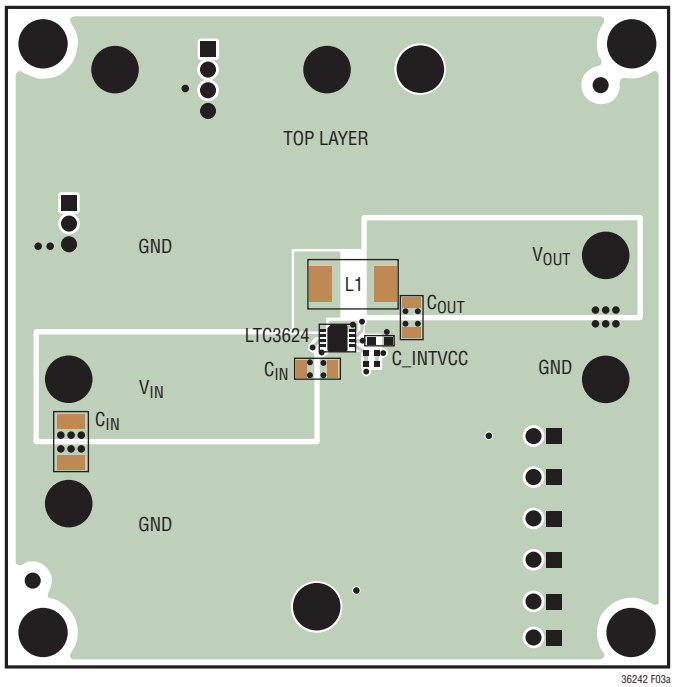



Figure 3a. Sample PCB Layout-Top Side

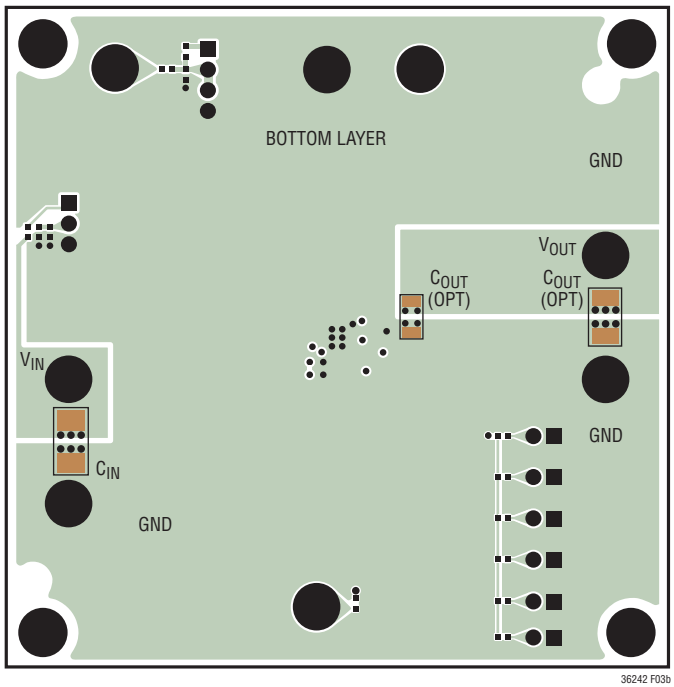
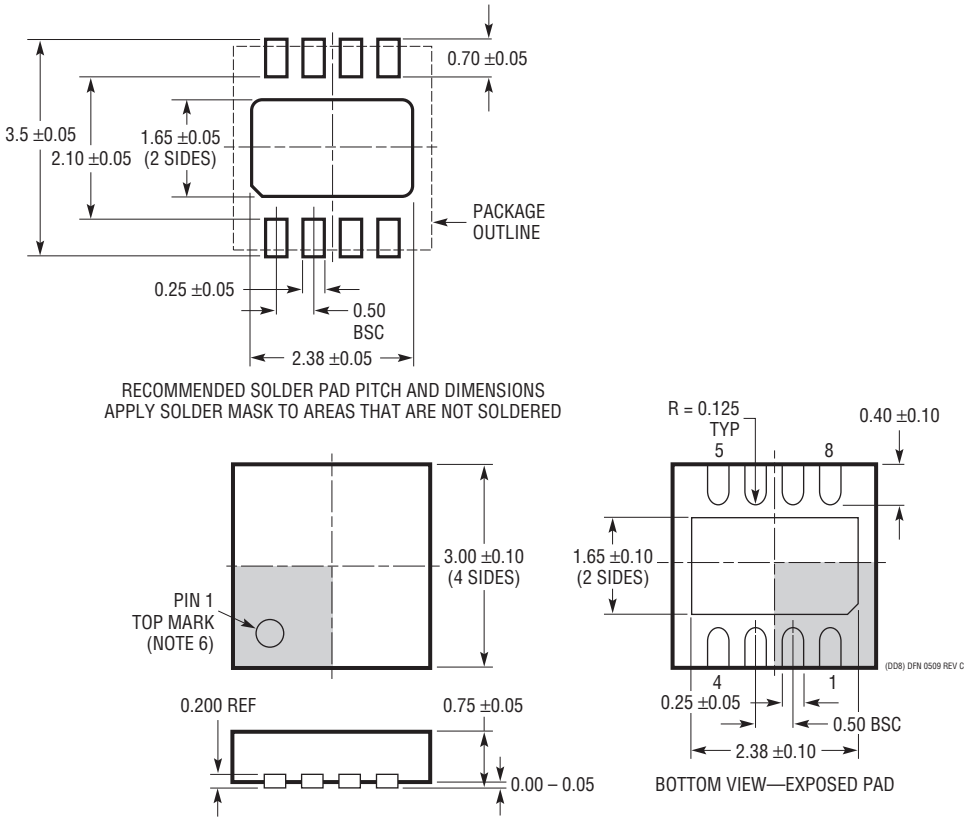



Figure 3b. Sample PCB Layout-Bottom Side

# PACKAGE DESCRIPTION

**Please refer to http://www.linear.com/product/LTC3624#packaging for the most recent package drawings.**

**DD Package**
**8-Lead Plastic DFN (3mm × 3mm)**
(Reference LTC DWG # 05-08-1698 Rev C)

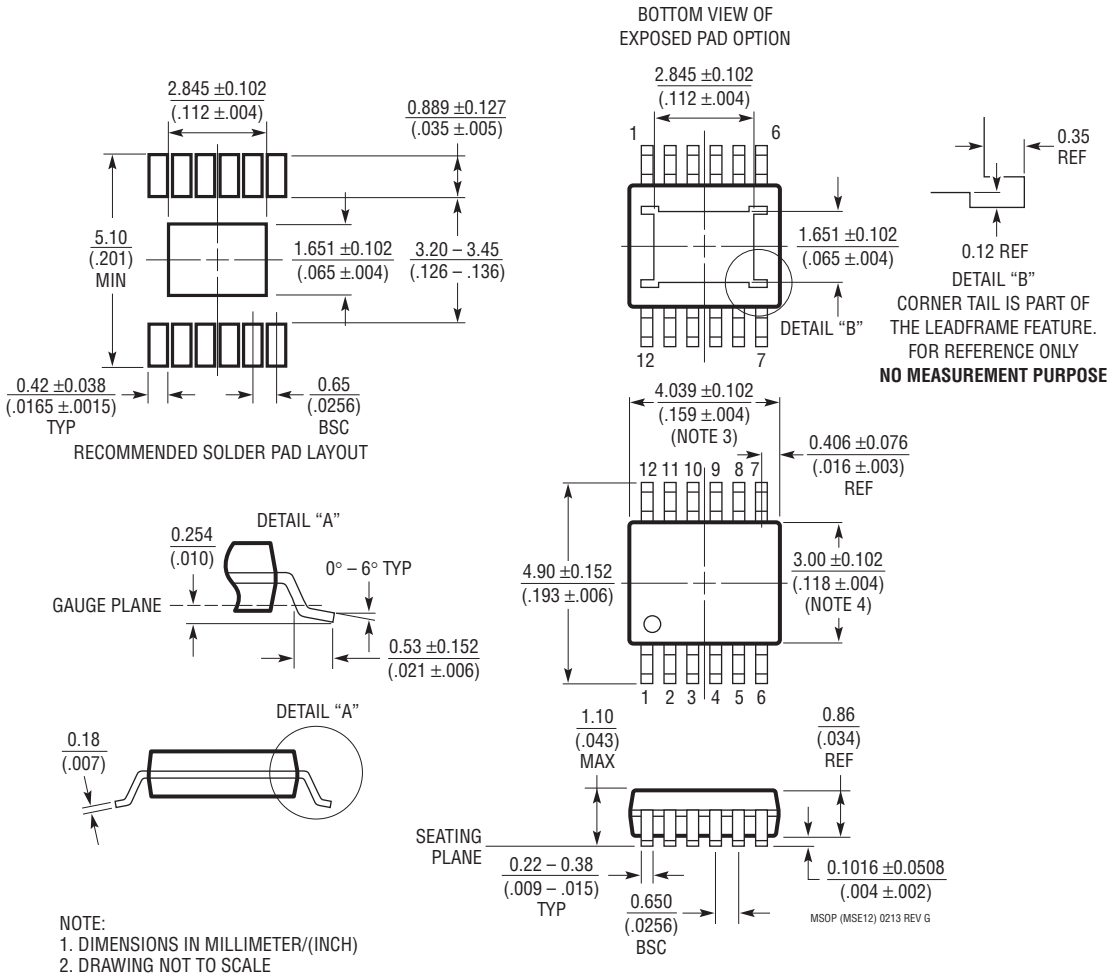



NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-1)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON TOP AND BOTTOM OF PACKAGE

# PACKAGE DESCRIPTION

**Please refer to http://www.linear.com/product/LTC3624#packaging for the most recent package drawings.**

**MSE Package**
**12-Lead Plastic MSOP, Exposed Die Pad**
(Reference LTC DWG # 05-08-1666 Rev G)




NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX
6. EXPOSED PAD DIMENSION DOES INCLUDE MOLD FLASH. MOLD FLASH ON E-PAD SHALL
   NOT EXCEED 0.254mm (.010") PER SIDE.

## REVISION HISTORY

| REV | DATE | DESCRIPTION | PAGE NUMBER |
|---|---|---|---|
| A | 04/14 | Added fixed output options. | 1 |
| | | Clarified Ordering Information. | 2 |
| | | Clarified Electrical Specifications. | 3, 4 |
| | | Clarified Pin Functions. | 7 |
| B | 08/14 | Clarified Typical Application | 1 |
| | | Clarified Pin Functions | 2 |
| | | Clarified $V_{FB}$ and $V_{OUT}$ in Electrical Specifications | 3 |
| | | Clarified Note 4 | 4 |
| | | Clarified Applications Information and Figure 1 | 10 |
| | | Figure 2 is now Figure 3 | 14, 15 |
| | | Bottom Typical Application clarified | 18 |
| C | 06/15 | Added MSOP package options and H-grade options | 2, 3 |
| | | Added H-grade electrical parameters and 150°C to Note 2 | 4 |
| | | Updated $I_Q$ vs Temperature graph to 150°C | 5 |
| | | Updated Oscillator Frequency and $V_{REF}$ graphs vs temperature to 150˚C | 6 |
| | | Updated Pin Functions for MSOP package versions | 7 |
| | | Added MSOP Package Description and drawing | 18 |
| D | 04/16 | Corrected a typographical error | 1 |



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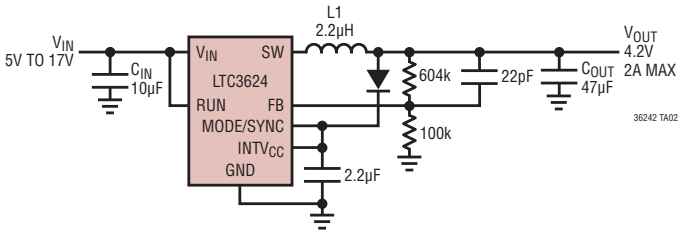
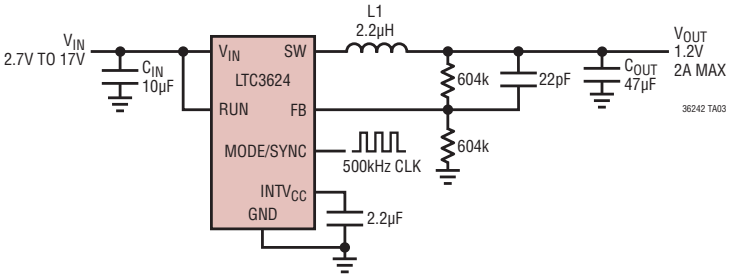
## TYPICAL APPLICATION

**4.2$V_{OUT}$, 1MHz, Burst Mode Operation**



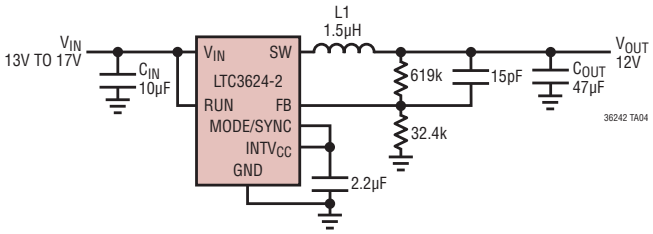

L1: COILCRAFT XAL4020 -222ME

**1.2$V_{OUT}$, Synced to 500kHz, Forced Continuous Mode**




L1: COILCRAFT XAL4020 -222ME

**12V Step-Down with 2A Output Current Limit, 2.25MHz**




L1: COILCRAFT XAL4020-152ME

## RELATED PARTS

| PART NUMBER | DESCRIPTION | COMMENTS |
|---|---|---|
| LTC3621 | 17V, 1A, 2.25MHz/1MHz Synchronous Step-Down DC/DC Converter | 95% Efficiency, $V_{IN}$: 2.7V to 17V, $V_{OUT(MIN)}$ = 0.6V, $I_Q$ = 3.5µA, $I_{SD}$ < 1µA, 2mm × 3mm DFN-6, MSOP-8E Packages |
| LTC3600 | 15V, 1.5A, 4MHz Synchronous Rail-to-Rail Single Resistor Step-Down Regulator | 95% Efficiency, $V_{IN}$: 4V to 15V, $V_{OUT(MIN)}$ = 0V, $I_Q$ = 700µA, $I_{SD}$ < 1µA, 3mm × 3mm DFN-12, MSOP-12E Packages |
| LTC3601 | 15V, 1.5A ($I_{OUT}$) 4MHz Synchronous Step-Down DC/DC Converter | 95% Efficiency, $V_{IN}$: 3.6V to 15V, $V_{OUT(MIN)}$ = 0.6V, $I_Q$ = 300µA, $I_{SD}$ < 14µA, 3mm × 3mm QFN-16, MSOP-16E Packages |
| LTC3603 | 15V, 2.5A ($I_{OUT}$) 3MHz Synchronous Step-Down DC/DC Converter | 95% Efficiency, $V_{IN}$: 4.5V to 15V, $V_{OUT(MIN)}$ = 0.6V, $I_Q$ = 75µA, $I_{SD}$ < 1µA, 4mm × 4mm QFN-20, MSOP-16E Packages |
| LTC3633/LTC3633A | 15V/20V, Dual 3A ($I_{OUT}$) 4MHz Synchronous Step-Down DC/DC Converter | 95% Efficiency, $V_{IN}$: 3.6V to 15V/20V, $V_{OUT(MIN)}$ = 0.6V, $I_Q$ = 500µA, $I_{SD}$ < 15µA, 4mm × 5mm QFN-28, TSSOP-28E Packages |
| LTC3605/LTC3605A | 15V/20V, 5A ($I_{OUT}$) 4MHz Synchronous Step-Down DC/DC Converter | 95% Efficiency, $V_{IN}$: 4V to 15V/20V, $V_{OUT(MIN)}$ = 0.6V, $I_Q$ = 2mA, $I_{SD}$ < 15µA, 4mm × 4mm QFN-24 Package |
| LTC3604 | 15V, 2.5A ($I_{OUT}$) 4MHz Synchronous Step-Down DC/DC Converter | 95% Efficiency, $V_{IN}$: 3.6V to 15V, $V_{OUT(MIN)}$ = 0.6V, $I_Q$ = 300µA, $I_{SD}$ < 14µA, 3mm × 3mm QFN-16, MSOP-16E Packages |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