



**THE DATASHEET OF  
LTC3720EGN#TRPBF**





**ABSOLUTE MAXIMUM RATINGS**

(Note 1)

Input Supply Voltage  
 $V_{IN}, I_{ON}$  ..... 36V to -0.3V

Boosted Topside Driver Supply Voltage  
 BOOST ..... 42V to -0.3V

SW, SENSE<sup>+</sup> Voltages ..... 36V to -5V

EXTV<sub>CC</sub>, (BOOST - SW), RUN/SS, V<sub>CC</sub>  
 VID0-VID4, PGOOD Voltages ..... 7V to -0.3V

FCB, V<sub>ON</sub>, V<sub>RNG</sub> Voltages ..... INTV<sub>CC</sub> + 0.3V to -0.3V

I<sub>TH</sub>, V<sub>FB</sub>, V<sub>OSENSE</sub> Voltages ..... 2.7V to -0.3V

TG, BG, INTV<sub>CC</sub>, EXTV<sub>CC</sub> Peak Currents ..... 2A

TG, BG, INTV<sub>CC</sub>, EXTV<sub>CC</sub> RMS Currents ..... 50mA

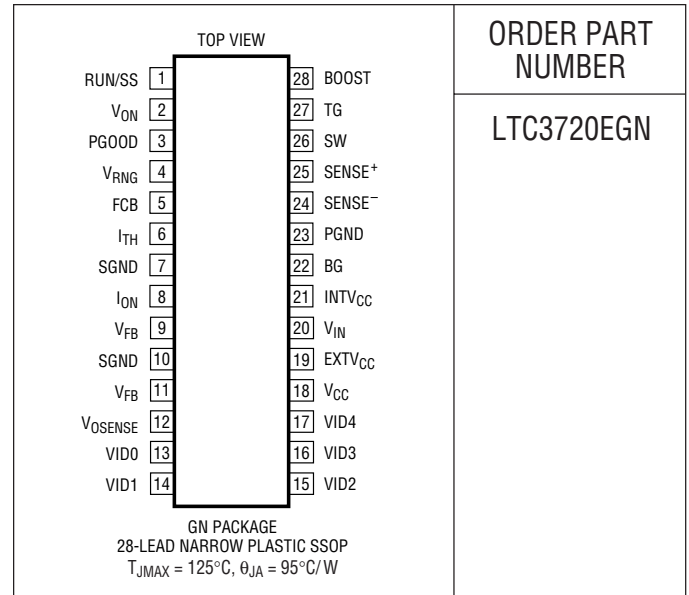
Operating Ambient Temperature Range  
 LTC3720EGN (Note 2) ..... -40°C to 85°C

Junction Temperature (Note 3) ..... 125°C

Storage Temperature Range ..... -65°C to 150°C

Lead Temperature (Soldering, 10 sec) ..... 300°C

**PACKAGE/ORDER INFORMATION**



ORDER PART NUMBER

LTC3720EGN

Consult LTC Marketing for parts specified with wider operating temperature ranges.

**ELECTRICAL CHARACTERISTICS**

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are T<sub>A</sub> = 25°C. V<sub>IN</sub> = 15V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	
<b>Main Control Loop</b>							
I <sub>Q</sub>	Input DC Supply Current			900	2000	μA	
	Normal Shutdown Supply Current			15	30	μA	
V <sub>FB</sub>	Feedback Reference Voltage	I <sub>TH</sub> = 1.2V (Note 4)	● 0.792	0.800	0.808	V	
ΔV <sub>FB(LINEREG)</sub>	Feedback Voltage Line Regulation	V <sub>IN</sub> = 4V to 30V, I <sub>TH</sub> = 1.2V (Note 4)		0.002		%/V	
ΔV <sub>FB(LOADREG)</sub>	Feedback Voltage Load Regulation	I <sub>TH</sub> = 0.5V to 1.9V (Note 4)	●	-0.05	-0.3	%	
I <sub>FB</sub>	Feedback Pin Input Current			-5	±50	nA	
g <sub>m(EA)</sub>	Error Amplifier Transconductance	I <sub>TH</sub> = 1.2V (Note 4)		1.4	1.7	2	mS
V <sub>FCB</sub>	Forced Continuous Threshold		● 0.76	0.8	0.84	V	
I <sub>FCB</sub>	Forced Continuous Pin Current	V <sub>FCB</sub> = 0.8V		-1	-2	μA	
t <sub>ON</sub>	On-Time	I <sub>ON</sub> = 60μA, V <sub>ON</sub> = 1.5V		200	250	300	ns
		I <sub>ON</sub> = 30μA, V <sub>ON</sub> = 1.5V		425	500	575	ns
t <sub>ON(MIN)</sub>	Minimum On-Time	I <sub>ON</sub> = 180μA, V <sub>ON</sub> = 0V		50	100	ns	
t <sub>OFF(MIN)</sub>	Minimum Off-Time	I <sub>ON</sub> = 60μA, V <sub>ON</sub> = 1.5V		250	400	ns	
V <sub>SENSE(MAX)</sub>	Maximum Current Sense Threshold V <sub>SENSE-</sub> - V <sub>SENSE+</sub>	V <sub>RNG</sub> = 1V, V <sub>FB</sub> = 0.76V	●	113	133	153	mV
		V <sub>RNG</sub> = 0V, V <sub>FB</sub> = 0.76V	●	79	93	107	mV
		V <sub>RNG</sub> = INTV <sub>CC</sub> , V <sub>FB</sub> = 0.76V	●	158	186	214	mV
V <sub>SENSE(MIN)</sub>	Minimum Current Sense Threshold V <sub>SENSE-</sub> - V <sub>SENSE+</sub>	V <sub>RNG</sub> = 1V, V <sub>FB</sub> = 0.84V		-67			mV
		V <sub>RNG</sub> = 0V, V <sub>FB</sub> = 0.84V		-47			mV
		V <sub>RNG</sub> = INTV <sub>CC</sub> , V <sub>FB</sub> = 0.84V		-93			mV
ΔV <sub>FB(OV)</sub>	Output Overvoltage Fault Threshold			5.5	7.5	9.5	%
V <sub>FB(UV)</sub>	Output Undervoltage Fault Threshold			520	600	680	mV
V <sub>RUN/SS(ON)</sub>	RUN Pin Start Threshold		● 0.8	1.5	2	V	

## ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are  $T_A = 25^\circ\text{C}$ .  $V_{IN} = 15\text{V}$  unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	
$V_{\text{RUN/SS(LE)}}$	RUN Pin Latchoff Enable Threshold	RUN/SS Pin Rising		4	4.5	V	
$V_{\text{RUN/SS(LT)}}$	RUN Pin Latchoff Threshold	RUN/SS Pin Falling		3.5		V	
$I_{\text{RUN/SS(C)}}$	Soft-Start Charge Current		-0.5	-1.2	-3	$\mu\text{A}$	
$I_{\text{RUN/SS(D)}}$	Soft-Start Discharge Current		0.8	1.8	3	$\mu\text{A}$	
$V_{\text{IN (UVLO)}}$	Undervoltage Lockout	$V_{\text{IN}}$ Falling $V_{\text{IN}}$ Rising	● ●	3.4 3.5	3.9 4.0	V V	
TG $R_{\text{UP}}$	TG Driver Pull-Up On Resistance	TG High		2	3	$\Omega$	
TG $R_{\text{DOWN}}$	TG Driver Pull-Down On Resistance	TG Low		2	3	$\Omega$	
BG $R_{\text{UP}}$	BG Driver Pull-Up On Resistance	BG High		3	4	$\Omega$	
BG $R_{\text{DOWN}}$	BG Driver Pull-Down On Resistance	BG Low		1	2	$\Omega$	
TG $t_r$	TG Rise Time	$C_{\text{LOAD}} = 3300\text{pF}$		20		ns	
TG $t_f$	TG Fall Time	$C_{\text{LOAD}} = 3300\text{pF}$		20		ns	
BG $t_r$	BG Rise Time	$C_{\text{LOAD}} = 3300\text{pF}$		20		ns	
BG $t_f$	BG Fall Time	$C_{\text{LOAD}} = 3300\text{pF}$		20		ns	
<b>Internal <math>V_{\text{CC}}</math> Regulator</b>							
$V_{\text{INTVCC}}$	Internal $V_{\text{CC}}$ Voltage	$6\text{V} < V_{\text{IN}} < 30\text{V}$ , $V_{\text{EXTVCC}} = 4\text{V}$	●	4.7	5	5.3	V
$\Delta V_{\text{LDO(LOADREG)}}$	Internal $V_{\text{CC}}$ Load Regulation	$I_{\text{CC}} = 0\text{mA}$ to $20\text{mA}$ , $V_{\text{EXTVCC}} = 4\text{V}$		-0.1	$\pm 2$		%
$V_{\text{EXTVCC}}$	EXTVCC Switchover Voltage	$I_{\text{CC}} = 20\text{mA}$ , $V_{\text{EXTVCC}}$ Rising	●	4.5	4.7		V
$\Delta V_{\text{EXTVCC}}$	EXTVCC Switch Drop Voltage	$I_{\text{CC}} = 20\text{mA}$ , $V_{\text{EXTVCC}} = 5\text{V}$		150	300		mV
$\Delta V_{\text{EXTVCC(HYS)}}$	EXTVCC Switchover Hysteresis			200			mV
<b>PGOOD Output</b>							
$\Delta V_{\text{FBH}}$	PGOOD Upper Threshold	$V_{\text{FB}}$ Rising		5.5	7.5	9.5	%
$\Delta V_{\text{FBL}}$	PGOOD Lower Threshold	$V_{\text{FB}}$ Falling		-5.5	-7.5	-9.5	%
$\Delta V_{\text{FB(HYS)}}$	PGOOD Hysteresis	$V_{\text{FB}}$ Returning		1	2		%
$V_{\text{PGL}}$	PGOOD Low Voltage	$I_{\text{PGOOD}} = 5\text{mA}$		0.15	0.4		V
<b>VID DAC</b>							
$V_{\text{CC}}$	Operating Supply Voltage Range			3.1	5.5		V
$V_{\text{VID(T)}}$	VID0-VID4 Logic Threshold Voltage	$V_{\text{CC}} = 3.3\text{V}$		0.4	1.2	2	V
$V_{\text{VID(LEAK)}}$	VID0-VID4 Leakage Current	$V_{\text{VID0}} - V_{\text{VID4}} = V_{\text{CC}}$		0.01	$\pm 1$		$\mu\text{A}$
$\Delta V_{\text{OSENSE}}$	DAC Output Accuracy	$V_{\text{OSENSE}}$ Programmed from 1.05V to 1.825V (Note 5), $V_{\text{CC}} = 5\text{V}$		-0.25	0	0.25	%
$R_{\text{PULLUP}}$	Pull-Up Resistance on VID	$V_{\text{DIODE}} = 0.6\text{V}$ (Note 6)		28	40	56	k $\Omega$
$R_{\text{VID}}$	Resistance from $V_{\text{OSENSE}}$ to $V_{\text{FB}}$			6	10	14	k $\Omega$
$I_{\text{VCC}}$	Supply Current	(Note 7)		1	10		$\mu\text{A}$

**Note 1:** Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

**Note 2:** The LTC3720E is guaranteed to meet performance specifications from  $0^\circ\text{C}$  to  $70^\circ\text{C}$ . Specifications over the  $-40^\circ\text{C}$  to  $85^\circ\text{C}$  operating temperature range are assured by design, characterization and correlation with statistical process controls.

**Note 3:**  $T_J$  is calculated from the ambient temperature  $T_A$  and power dissipation  $P_D$  as follows:

$$T_{\text{LTC3720EGN}} = T_A + (P_D \cdot 95^\circ\text{C/W})$$

**Note 4:** The LTC3720 is tested in a feedback loop that adjusts  $V_{\text{FB}}$  to achieve a specified error amplifier output voltage ( $I_{\text{TH}}$ ).

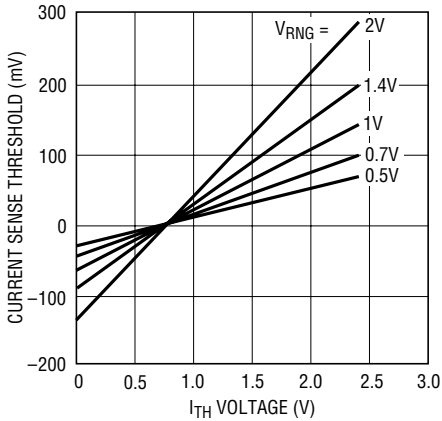
**Note 5:** The LTC3720 VID DAC is tested in a feedback loop that adjusts  $V_{\text{OSENSE}}$  to achieve a specified feedback voltage ( $V_{\text{FB}} = 0.8\text{V}$ ) for each DAC VID code.

**Note 6:** Each built-in pull-up resistor attached to VID inputs also has a series diode connected to  $V_{\text{CC}}$  to allow input voltages higher than the  $V_{\text{CC}}$  supply without damage or clamping. (See Operation section for further details.)

**Note 7:** Supply current is specified with all VID inputs floating. Due to the internal pull-ups on the VID pins, the supply current will increase depending on the number of grounded VID lines. Each grounded VID line will draw approximately  $(V_{\text{CC}} - 0.6\text{V})/40\text{k}$  mA. (See Operation section for further details.)

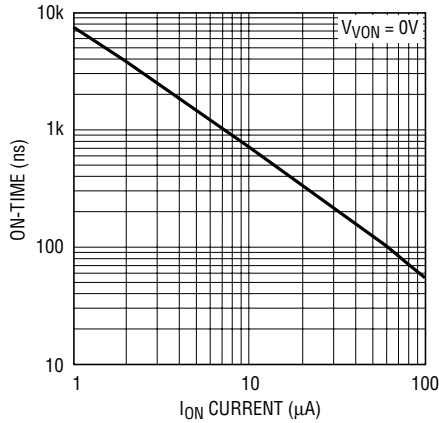
# TYPICAL PERFORMANCE CHARACTERISTICS

**Current Sense Threshold vs  $I_{TH}$  Voltage**



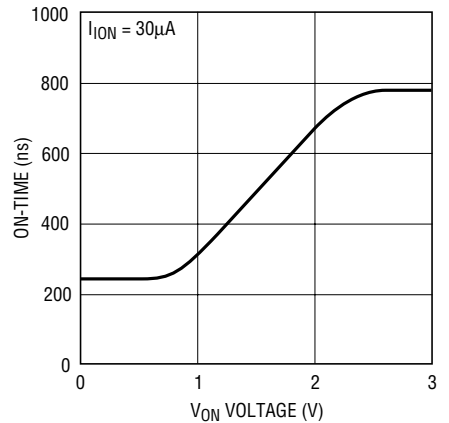
3720 G01

**On-Time vs  $I_{ON}$  Current**



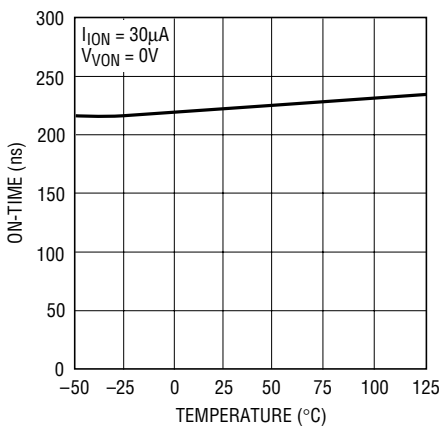
3720 G02

**On-Time vs  $V_{ON}$  Voltage**



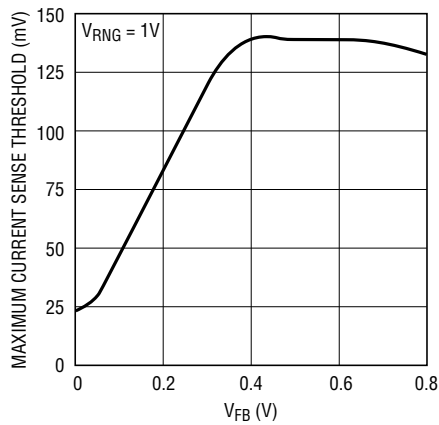
3720 G03

**On-Time vs Temperature**



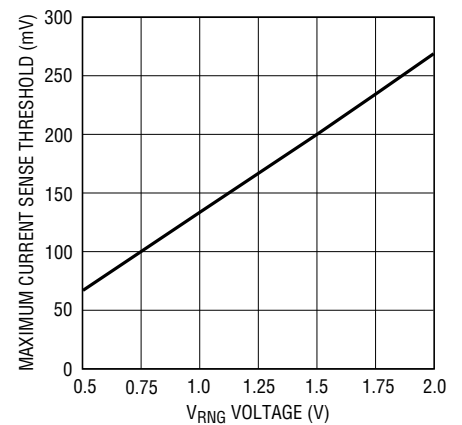
3720 G04

**Current Limit Foldback**



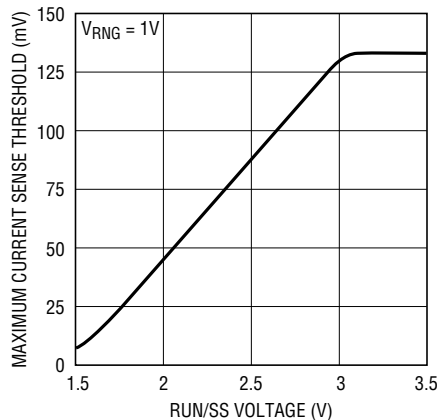
3720 G05

**Maximum Current Sense Threshold vs  $V_{RNG}$  Voltage**



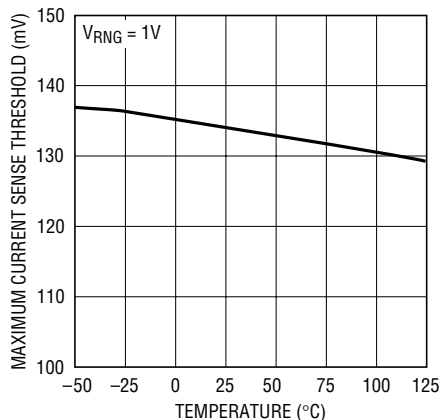
3720 G06

**Maximum Current Sense Threshold vs RUN/SS Voltage**



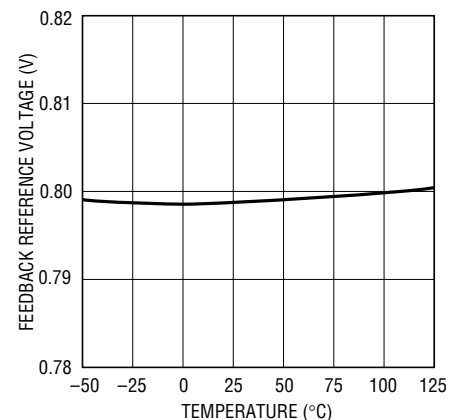
3729 G07

**Maximum Current Sense Threshold vs Temperature**



3720 G08

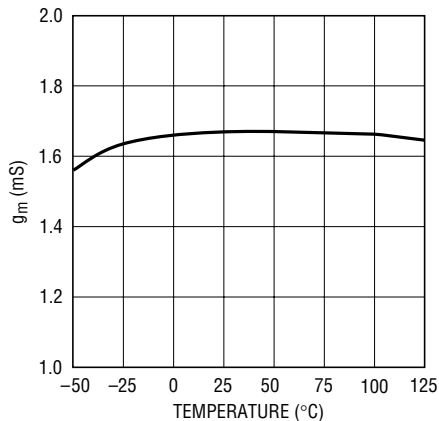
**Feedback Reference Voltage vs Temperature**



3720 G09

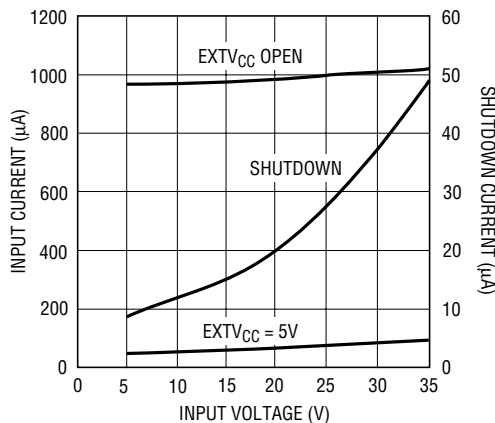
# TYPICAL PERFORMANCE CHARACTERISTICS

**Error Amplifier  $g_m$  vs Temperature**



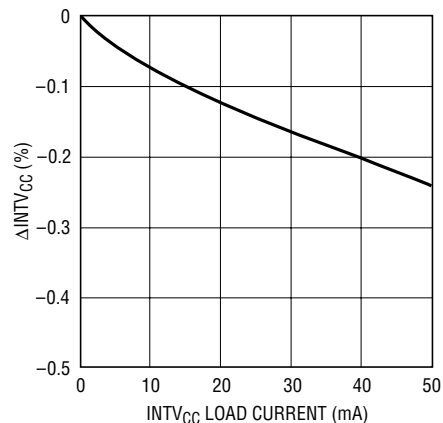
3720 G10

**Input and Shutdown Currents vs Input Voltage**



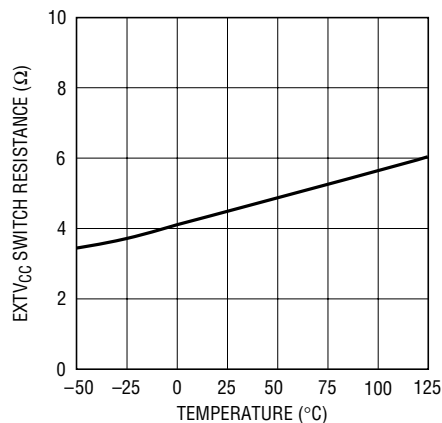
3720 G11

**INTV<sub>CC</sub> Load Regulation**



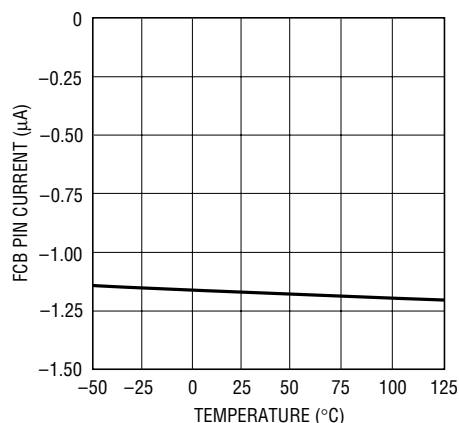
3720 G12

**EXTV<sub>CC</sub> Switch Resistance vs Temperature**



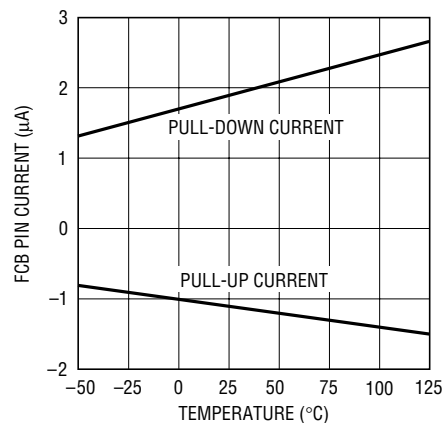
3720 G13

**FCB Pin Current vs Temperature**



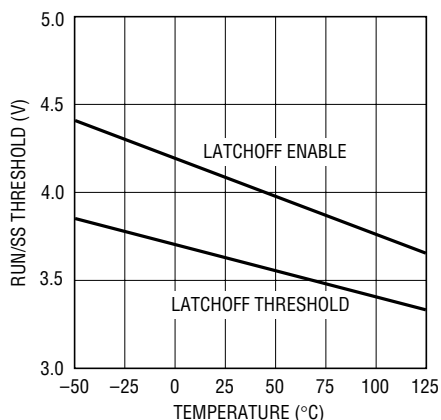
3720 G14

**RUN/SS Pin Current vs Temperature**



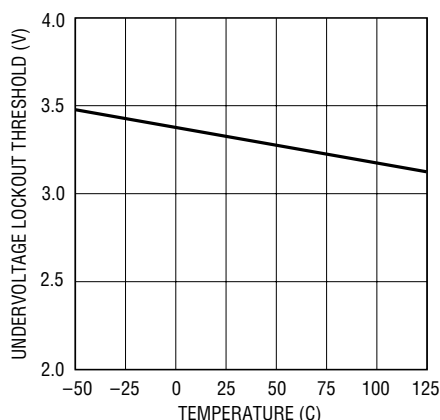
3720 G15

**RUN/SS Latchoff Thresholds vs Temperature**



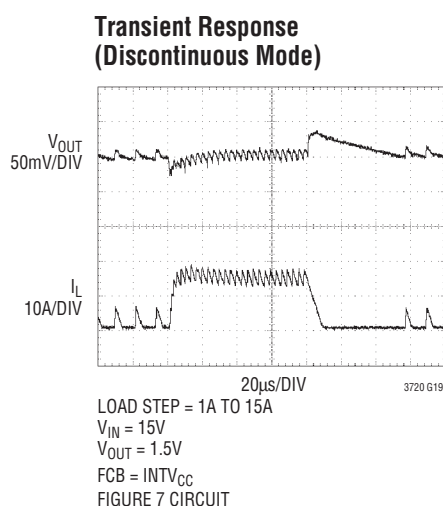
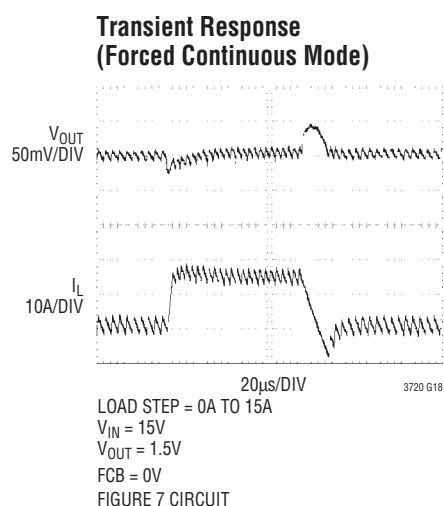
3720 G16

**Undervoltage Lockout Threshold vs Temperature**



3720 G17

## TYPICAL PERFORMANCE CHARACTERISTICS



## PIN FUNCTIONS

**RUN/SS (Pin 1):** Run Control and Soft-Start Input. A capacitor to ground at this pin sets the ramp time to full output current (approximately  $3s/\mu F$ ) and the time delay for overcurrent latching (see Applications Information). Forcing this pin below 0.8V shuts down the device.

**$V_{ON}$  (Pin 2):** On-Time Voltage Input. Voltage trip point for the on-time comparator. Tying this pin to the output voltage makes the on-time proportional to  $V_{OUT}$ . The comparator input defaults to 0.7V when the pin is grounded, 2.4V when the pin is tied to  $INTV_{CC}$ .

**PGOOD (Pin 3):** Power Good Output. Open drain logic output that is pulled to ground when the output voltage is not within  $\pm 7.5\%$  of the regulation point.

**$V_{RNG}$  (Pin 4):** Sense Voltage Range Input. The voltage at this pin is ten times the nominal sense voltage at maximum output current and can be set from 0.5V to 2V by a resistive divider from  $INTV_{CC}$ . The nominal sense voltage defaults to 70mV when this pin is tied to ground, 140mV when tied to  $INTV_{CC}$ .

**FCB (Pin 5):** Forced Continuous Input. Tie this pin to ground to force continuous synchronous operation at low load or to  $INTV_{CC}$  to enable discontinuous mode operation at low load.

**$I_{TH}$  (Pin 6):** Current Control Threshold and Error Amplifier Compensation Point. The current comparator threshold increases with this control voltage. The voltage ranges from 0V to 2.4V with 0.8V corresponding to zero sense voltage (zero current).

**SGND (Pin 7, 10):** Signal Ground. All small-signal components and compensation components should connect to this ground, which in turn connects to PGND at one point.

**$I_{ON}$  (Pin 8):** On-Time Current Input. Tie a resistor from  $V_{IN}$  to this pin to set the one-shot timer current and thereby set the switching frequency.

**$V_{FB}$  (Pin 9, 11):** Error Amplifier Feedback Input. This pin connects to both the error amplifier input and to the output of the internal resistive divider. It can be used to attach additional compensation components if desired.

**$V_{SENSE}$  (Pin 12):** Output Voltage Sense. The output voltage connects here to the input of the internal resistive feedback divider.

**VID0-VID4 (Pins 13, 14, 15, 16, 17):** VID Digital Inputs. The voltage identification (VID) code sets the internal feedback resistor divider ratio for different output voltages as shown in Table 1. If unconnected, the pins are pulled high by internal 40k pull-up resistors.

## PIN FUNCTIONS

**V<sub>CC</sub> (Pin 18):** Power Supply Voltage for VID. Range is from 3.1V to 5.5V.

**EXTV<sub>CC</sub> (Pin 19):** External V<sub>CC</sub> Input. When EXTV<sub>CC</sub> exceeds 4.7V, an internal switch connects this pin to INTV<sub>CC</sub> and shuts down the internal regulator so that controller and gate drive power is drawn from EXTV<sub>CC</sub>. Do not exceed 7V at this pin and ensure that EXTV<sub>CC</sub> < V<sub>IN</sub>.

**V<sub>IN</sub> (Pin 20):** Main Input Supply. Decouple this pin to PGND with an RC filter (1Ω, 0.1μF).

**INTV<sub>CC</sub> (Pin 21):** Internal 5V Regulator Output. The driver and control circuits are powered from this voltage. Decouple this pin to power ground with a minimum of 4.7μF low ESR tantalum capacitor.

**BG (Pin 22):** Bottom Gate Drive. Drives the gate of the bottom N-channel MOSFET between ground and INTV<sub>CC</sub>.

**PGND (Pin 23):** Power Ground. Connect this pin closely to the source of the bottom N-channel MOSFET, the (–) terminal of C<sub>VCC</sub> and the (–) terminal of C<sub>IN</sub>.

**SENSE<sup>–</sup> (Pin 24):** Current Sense Comparator Input. The (–) input is normally connected to PGND.

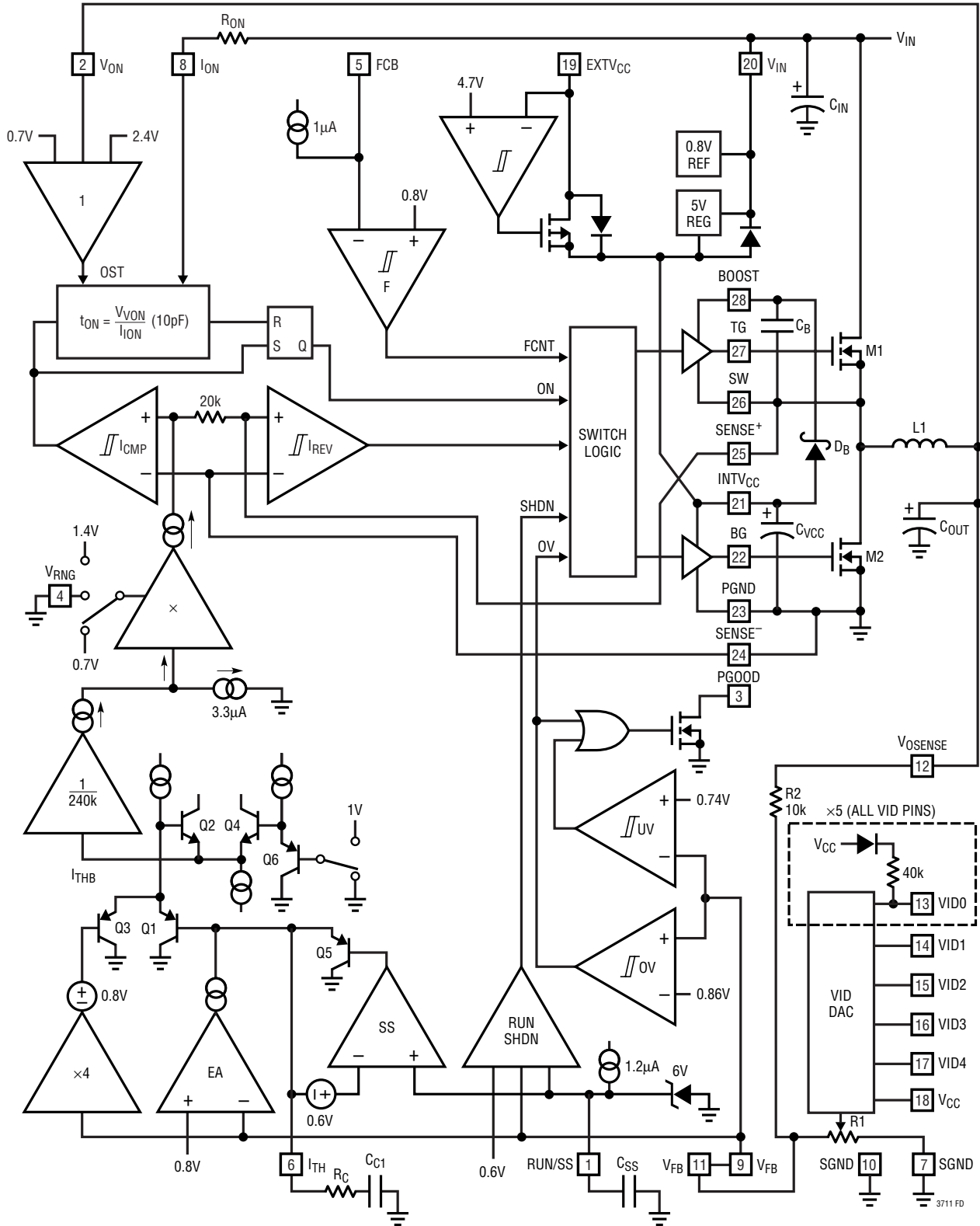
**SENSE<sup>+</sup> (Pin 25):** Current Sense Comparator Input. The (+) input to the current comparator is normally connected to the SW node unless using a sense resistor (see Applications Information).

**SW (Pin 26):** Switch Node. The (–) terminal of the bootstrap capacitor C<sub>B</sub> connects here. This pin swings from a diode voltage drop below ground up to V<sub>IN</sub>.

**TG (Pin 27):** Top Gate Drive. Drives the top N-channel MOSFET with a voltage swing equal to INTV<sub>CC</sub> superimposed on the switch node voltage SW.

**BOOST (Pin 28):** Boosted Floating Driver Supply. The (+) terminal of the bootstrap capacitor C<sub>B</sub> connects here. This pin swings from a diode voltage drop below INTV<sub>CC</sub> up to V<sub>IN</sub> + INTV<sub>CC</sub>.

FUNCTIONAL DIAGRAM



## OPERATION (Refer to Functional Diagram)

### Main Control Loop

The LTC3720 is a current mode controller for DC/DC step-down converters. In normal operation, the top MOSFET is turned on for a fixed interval determined by a one-shot timer OST. When the top MOSFET is turned off, the bottom MOSFET is turned on until the current comparator  $I_{CMP}$  trips, restarting the one-shot timer and initiating the next cycle. Inductor current is determined by sensing the voltage between the  $SENSE^-$  and  $SENSE^+$  pins using either the bottom MOSFET on-resistance or a separate sense resistor. The voltage on the  $I_{TH}$  pin sets the comparator threshold corresponding to inductor valley current. The error amplifier EA adjusts this voltage by comparing the feedback signal  $V_{FB}$  from the output voltage with an internal 0.8V reference. The feedback voltage is derived from the output voltage by a resistive divider DAC that is set by the VID code pins VID0-VID4. If the load current increases, it causes a drop in the feedback voltage relative to the reference. The  $I_{TH}$  voltage then rises until the average inductor current again matches the load current.

At low load currents, the inductor current can drop to zero and become negative. This is detected by current reversal comparator  $I_{REV}$  which then shuts off M2, resulting in discontinuous operation. Both switches will remain off with the output capacitor supplying the load current until the  $I_{TH}$  voltage rises above the zero current level (0.8V) to initiate another cycle. Discontinuous mode operation is disabled by comparator F when the FCB pin is brought below 0.8V, forcing continuous synchronous operation.

The operating frequency is determined implicitly by the top MOSFET on-time and the duty cycle required to maintain regulation. The one-shot timer generates an on-time that is proportional to the ideal duty cycle, thus holding frequency approximately constant with changes in  $V_{IN}$  and  $V_{OUT}$ . The nominal frequency can be adjusted with an external resistor  $R_{ON}$ .

Overvoltage and undervoltage comparators OV and UV pull the PGOOD output low if the output feedback voltage exits a  $\pm 7.5\%$  window around the regulation point. Furthermore, in an overvoltage condition, M1 is turned off and M2 is turned on and held on until the overvoltage condition clears.

Foldback current limiting is provided if the output is shorted to ground. As  $V_{FB}$  drops, the buffered current threshold voltage  $I_{THB}$  is pulled down by clamp Q3 to a 1V level set by Q4 and Q6. This reduces the inductor valley current level to one sixth of its maximum value as  $V_{FB}$  approaches 0V.

Pulling the RUN/SS pin low forces the controller into its shutdown state, turning off both M1 and M2. Releasing the pin allows an internal 1.2 $\mu$ A current source to charge up an external soft-start capacitor  $C_{SS}$ . When this voltage reaches 1.5V, the controller turns on and begins switching, but with the  $I_{TH}$  voltage clamped at approximately 0.6V below the RUN/SS voltage. As  $C_{SS}$  continues to charge, the soft-start current limit is removed.

### INTV<sub>CC</sub>/EXTV<sub>CC</sub> Power

Power for the top and bottom MOSFET drivers and most of the internal controller circuitry is derived from the INTV<sub>CC</sub> pin. The top MOSFET driver is powered from a floating bootstrap capacitor  $C_B$ . This capacitor is recharged from INTV<sub>CC</sub> through an external Schottky diode  $D_B$  when the top MOSFET is turned off. When the EXTV<sub>CC</sub> pin is grounded, an internal 5V low dropout regulator supplies the INTV<sub>CC</sub> power from  $V_{IN}$ . If EXTV<sub>CC</sub> rises above 4.7V, the internal regulator is turned off, and an internal switch connects EXTV<sub>CC</sub> to INTV<sub>CC</sub>. This allows a high efficiency source connected to EXTV<sub>CC</sub>, such as an external 5V supply or a secondary output from the converter, to provide the INTV<sub>CC</sub> power. Voltages up to 7V can be applied to EXTV<sub>CC</sub> for additional gate drive. If the input voltage is low and INTV<sub>CC</sub> drops below 3.5V, undervoltage lockout circuitry prevents the power switches from turning on.

## APPLICATIONS INFORMATION

The basic LTC3720 application circuit is shown in Figure 1. External component selection is primarily determined by the maximum load current and begins with the selection of the sense resistance and power MOSFET switches. The LTC3720 can use either a sense resistor or the on-resistance of the synchronous power MOSFET for determining the inductor current. The desired amount of ripple current and operating frequency largely determines the inductor value. Finally,  $C_{IN}$  is selected for its ability to handle the large RMS current into the converter and  $C_{OUT}$  is chosen with low enough ESR to meet the output voltage ripple and transient specification.

### Maximum Sense Voltage and $V_{RNG}$ Pin

Inductor current is determined by measuring the voltage across a sense resistance that appears between the  $SENSE^-$  and  $SENSE^+$  pins. The maximum sense voltage is set by the voltage applied to the  $V_{RNG}$  pin and is equal to approximately  $(0.133)V_{RNG}$ . The current mode control loop will not allow the inductor current valleys to exceed  $(0.133)V_{RNG}/R_{SENSE}$ . In practice, one should allow some margin for variations in the LTC3720 and external component values and a good guide for selecting the sense resistance is:

$$R_{SENSE} = \frac{V_{RNG}}{10 \cdot I_{OUT(MAX)}}$$

An external resistive divider from  $INTV_{CC}$  can be used to set the voltage of the  $V_{RNG}$  pin between 0.5V and 2V resulting in nominal sense voltages of 50mV to 200mV. Additionally, the  $V_{RNG}$  pin can be tied to  $SGND$  or  $INTV_{CC}$  in which case the nominal sense voltage defaults to 70mV or 140mV, respectively. The maximum allowed sense voltage is about 1.33 times this nominal value.

### Connecting the $SENSE^+$ and $SENSE^-$ Pins

The LTC3720 can be used with or without a sense resistor. When using a sense resistor, it is placed between the source of the bottom MOSFET M2 and ground. Connect the  $SENSE^+$  pin to the source of the bottom MOSFET and the  $SENSE^-$  pin to  $PGND$  so that the resistor appears

between the  $SENSE^+$  and  $SENSE^-$  pins. Kelvin connections at the sense resistor ensure accurate current sensing. Using a sense resistor provides a well defined current limit, but adds cost and reduces efficiency. Alternatively, one can eliminate the sense resistor and use the bottom MOSFET as the current sense element by simply connecting the  $SENSE^+$  pin to the switch node SW at the drain of the bottom MOSFET and keep  $SENSE^-$  connected to  $PGND$ . This improves efficiency, but one must carefully choose the MOSFET on-resistance as discussed below.

### Power MOSFET Selection

The LTC3720 requires two external N-channel power MOSFETs, one for the top (main) switch and one for the bottom (synchronous) switch. Important parameters for the power MOSFETs are the breakdown voltage  $V_{(BR)DSS}$ , threshold voltage  $V_{(GS)TH}$ , on-resistance  $R_{DS(ON)}$ , reverse transfer capacitance  $C_{RSS}$  and maximum current  $I_{DS(MAX)}$ .

The gate drive voltage is set by the 5V  $INTV_{CC}$  supply. Consequently, logic-level threshold MOSFETs must be used in LTC3720 applications. If the input voltage is expected to drop below 5V, then sub-logic level threshold MOSFETs should be considered.

When the bottom MOSFET is used as the current sense element, particular attention must be paid to its on-resistance. MOSFET on-resistance is typically specified with a maximum value  $R_{DS(ON)(MAX)}$  at 25°C. In this case, additional margin is required to accommodate the rise in MOSFET on-resistance with temperature:

$$R_{DS(ON)(MAX)} = \frac{R_{SENSE}}{\rho_T}$$

The  $\rho_T$  term is a normalization factor (unity at 25°C) accounting for the significant variation in on-resistance with temperature, typically about 0.4%/°C as shown in Figure 2. For a maximum temperature of 100°C, using a value  $\rho_T = 1.3$  is reasonable.

The power dissipated by the top and bottom MOSFETs strongly depends upon their respective duty cycles and

## APPLICATIONS INFORMATION

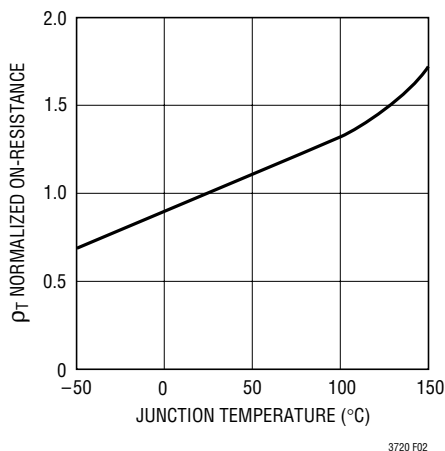


Figure 2.  $R_{DS(ON)}$  vs. Temperature

the load current. When the LTC3720 is operating in continuous mode, the duty cycles for the MOSFETs are:

$$D_{TOP} = \frac{V_{OUT}}{V_{IN}}$$

$$D_{BOT} = \frac{V_{IN} - V_{OUT}}{V_{IN}}$$

The resulting power dissipation in the MOSFETs at maximum output current are:

$$P_{TOP} = D_{TOP} I_{OUT(MAX)}^2 \rho_{T(TOP)} R_{DS(ON)(MAX)} + k V_{IN}^2 I_{OUT(MAX)} C_{RSS} f$$

$$P_{BOT} = D_{BOT} I_{OUT(MAX)}^2 \rho_{T(BOT)} R_{DS(ON)(MAX)}$$

Both MOSFETs have  $I^2R$  losses and the top MOSFET includes an additional term for transition losses, which are largest at high input voltages. The constant  $k = 1.7A^{-1}$  can be used to estimate the amount of transition loss. The bottom MOSFET losses are greatest when the bottom duty cycle is near 100%, during a short-circuit or at high input voltage.

### Operating Frequency

The choice of operating frequency is a tradeoff between efficiency and component size. Low frequency operation improves efficiency by reducing MOSFET switching losses but requires larger inductance and/or capacitance in order to maintain low output ripple voltage.

The operating frequency of LTC3720 applications is determined implicitly by the one-shot timer that controls the on-time  $t_{ON}$  of the top MOSFET switch. The on-time is set by the current into the  $I_{ON}$  pin and the voltage at the  $V_{ON}$  pin according to:

$$t_{ON} = \frac{V_{VON}}{I_{ION}} (10pF)$$

Tying a resistor  $R_{ON}$  from  $V_{IN}$  to the  $I_{ON}$  pin yields an on-time inversely proportional to  $V_{IN}$ . For a step-down converter, this results in approximately constant frequency operation as the input supply varies:

$$f = \frac{V_{OUT}}{V_{VON} R_{ON} (10pF)} \quad [Hz]$$

To hold frequency constant during output voltage changes, tie the  $V_{ON}$  pin to  $V_{OUT}$ . The  $V_{ON}$  pin has internal clamps that limit its input to the one-shot timer. If the pin is tied below 0.7V, the input to the one-shot is clamped at 0.7V. Similarly, if the pin is tied above 2.4V, the input is clamped at 2.4V.

Because the voltage at the  $I_{ON}$  pin is about 0.7V, the current into this pin is not exactly inversely proportional to  $V_{IN}$ , especially in applications with lower input voltages. To correct for this error, an additional resistor  $R_{ON2}$  connected from the  $I_{ON}$  pin to the 5V  $INTV_{CC}$  supply will further stabilize the frequency.

$$R_{ON2} = \frac{5V}{0.7V} R_{ON}$$

Changes in the load current magnitude will also cause frequency shift. Parasitic resistance in the MOSFET switches and inductor reduce the effective voltage across the inductance, resulting in increased duty cycle as the load current increases. By lengthening the on-time slightly as current increases, constant frequency operation can be maintained. This is accomplished with a resistive divider from the  $I_{TH}$  pin to the  $V_{ON}$  pin and  $V_{OUT}$ . The values required will depend on the parasitic resistances in the specific application. A good starting point is to feed about 25% of the voltage change at the  $I_{TH}$  pin to the  $V_{ON}$  pin as

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Figure 3. Correcting Frequency Shift with Load Current Changes

shown in Figure 3a. Place capacitance on the  $V_{ON}$  pin to filter out the  $I_{TH}$  variations at the switching frequency. The resistor load on  $I_{TH}$  reduces the DC gain of the error amp and degrades load regulation, which can be avoided by using the PNP emitter follower of Figure 3b.

### Inductor Selection

Given the desired input and output voltages, the inductor value and operating frequency determine the ripple current:

$$\Delta I_L = \left( \frac{V_{OUT}}{fL} \right) \left( 1 - \frac{V_{OUT}}{V_{IN}} \right)$$

Lower ripple current reduces core losses in the inductor, ESR losses in the output capacitors and output voltage ripple. Highest efficiency operation is obtained at low frequency with small ripple current. However, achieving this requires a large inductor. There is a tradeoff between component size, efficiency and operating frequency.

A reasonable starting point is to choose a ripple current that is about 40% of  $I_{OUT(MAX)}$ . The largest ripple current occurs at the highest  $V_{IN}$ . To guarantee that ripple current does not exceed a specified maximum, the inductance should be chosen according to:

$$L = \left( \frac{V_{OUT}}{f \Delta I_L (MAX)} \right) \left( 1 - \frac{V_{OUT}}{V_{IN} (MAX)} \right)$$

Once the value for  $L$  is known, the type of inductor must be selected. High efficiency converters generally cannot afford the core loss found in low cost powdered iron cores, forcing the use of more expensive ferrite, molypermalloy or Kool M $\mu$ <sup>®</sup> cores. A variety of inductors designed for high current, low voltage applications are available from manufacturers such as Sumida, Panasonic, Coiltronics, Coilcraft and Toko.

### Schottky Diode D1 Selection

The Schottky diode D1 shown in Figure 1 conducts during the dead time between the conduction of the power MOSFET switches. It is intended to prevent the body diode of the bottom MOSFET from turning on and storing charge during the dead time, which can cause a modest (about 1%) efficiency loss. The diode can be rated for about one half to one fifth of the full load current since it is on for only a fraction of the duty cycle. In order for the diode to be effective, the inductance between it and the bottom MOSFET must be as small as possible, mandating that these components be placed adjacently. The diode can be omitted if the efficiency loss is tolerable.

### $C_{IN}$ and $C_{OUT}$ Selection

The input capacitance  $C_{IN}$  is required to filter the square wave current at the drain of the top MOSFET. Use a low ESR capacitor sized to handle the maximum RMS current.

$$I_{RMS} \cong I_{OUT(MAX)} \frac{V_{OUT}}{V_{IN}} \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

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This formula has a maximum at  $V_{IN} = 2V_{OUT}$ , where  $I_{RMS} = I_{OUT(MAX)}/2$ . This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that ripple current ratings from capacitor manufacturers are often based on only 2000 hours of life which makes it advisable to derate the capacitor.

The selection of  $C_{OUT}$  is primarily determined by the ESR required to minimize voltage ripple and load step transients. The output ripple  $\Delta V_{OUT}$  is approximately bounded by:

$$\Delta V_{OUT} \leq \Delta I_L \left( ESR + \frac{1}{8fC_{OUT}} \right)$$

Since  $\Delta I_L$  increases with input voltage, the output ripple is highest at maximum input voltage. Typically, once the ESR requirement is satisfied, the capacitance is adequate for filtering and has the necessary RMS current rating.

Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements. Dry tantalum, special polymer, aluminum electrolytic and ceramic capacitors are all available in surface mount packages. Special polymer capacitors offer very low ESR but have lower capacitance density than other types. Tantalum capacitors have the highest capacitance density but it is important to only use types that have been surge tested for use in switching power supplies. Aluminum electrolytic capacitors have significantly higher ESR, but can be used in cost-sensitive applications providing that consideration is given to ripple current ratings and long term reliability. Ceramic capacitors have excellent low ESR characteristics but can have a high voltage coefficient and audible piezoelectric effects. The high Q of ceramic capacitors with trace inductance can also lead to significant ringing. When used as input capacitors, care must be taken to ensure that ringing from inrush currents and switching does not pose an overvoltage hazard to the power switches and controller. To dampen input voltage transients, add a small 5 $\mu$ F to 50 $\mu$ F aluminum electrolytic capacitor with an ESR in the range of 0.5 $\Omega$  to 2 $\Omega$ . High

performance through-hole capacitors may also be used, but an additional ceramic capacitor in parallel is recommended to reduce the effect of their lead inductance.

### Top MOSFET Driver Supply ( $C_B$ , $D_B$ )

An external bootstrap capacitor  $C_B$  connected to the BOOST pin supplies the gate drive voltage for the topside MOSFET. This capacitor is charged through diode  $D_B$  from  $INTV_{CC}$  when the switch node is low. When the top MOSFET turns on, the switch node rises to  $V_{IN}$  and the BOOST pin rises to approximately  $V_{IN} + INTV_{CC}$ . The boost capacitor needs to store about 100 times the gate charge required by the top MOSFET. In most applications a 0.1 $\mu$ F to 0.47 $\mu$ F X5R or X7R dielectric capacitor is adequate.

### Discontinuous Mode Operation and FCB Pin

The FCB pin determines whether the bottom MOSFET remains on when current reverses in the inductor. Tying this pin above its 0.8V threshold enables discontinuous operation where the bottom MOSFET turns off when inductor current reverses. The load current at which current reverses and discontinuous operation begins depends on the amplitude of the inductor ripple current and will vary with changes in  $V_{IN}$ . Tying the FCB pin below the 0.8V threshold forces continuous synchronous operation, allowing current to reverse at light loads and maintaining high frequency operation.

In addition to providing a logic input to force continuous operation, the FCB pin provides a means to maintain a flyback winding output when the primary is operating in discontinuous mode. The secondary output  $V_{SEC}$  is normally set as shown in Figure 4 by the turns ratio N of the transformer. However, if the controller goes into discontinuous mode and halts switching due to a light primary load current, then  $V_{SEC}$  will droop. An external resistor divider from  $V_{SEC}$  to the FCB pin sets a minimum voltage  $V_{SEC(MIN)}$  below which continuous operation is forced until  $V_{SEC}$  has risen above its minimum.

$$V_{SEC(MIN)} = 0.8V \left( 1 + \frac{R4}{R3} \right)$$

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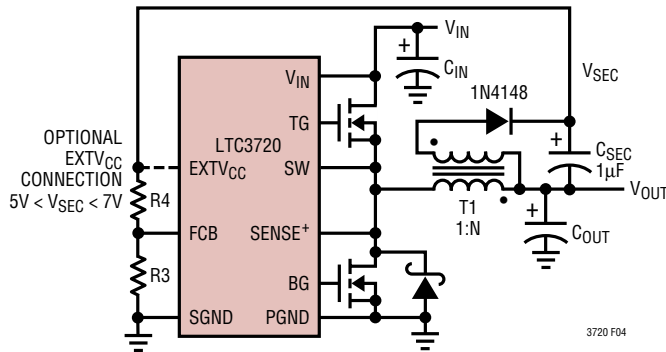


Figure 4. Secondary Output Loop and EXTV<sub>CC</sub> Connection

### Fault Conditions: Current Limit and Foldback

The maximum inductor current is inherently limited in a current mode controller by the maximum sense voltage. In the LTC3720, the maximum sense voltage is controlled by the voltage on the V<sub>RNG</sub> pin. With valley current control, the maximum sense voltage and the sense resistance determine the maximum allowed inductor valley current. The corresponding output current limit is:

$$I_{LIMIT} = \frac{V_{SNS(MAX)}}{R_{DS(ON)} \rho T^*} + \frac{1}{2} \Delta I_L$$

The current limit value should be checked to ensure that  $I_{LIMIT(MIN)} > I_{OUT(MAX)}$ . The minimum value of current limit generally occurs with the largest  $V_{IN}$  at the highest ambient temperature, conditions that cause the largest power loss in the converter. Note that it is important to check for self-consistency between the assumed MOSFET junction temperature and the resulting value of  $I_{LIMIT}$  which heats the MOSFET switches.

Caution should be used when setting the current limit based upon the  $R_{DS(ON)}$  of the MOSFETs. The maximum current limit is determined by the minimum MOSFET on-resistance. Data sheets typically specify nominal and maximum values for  $R_{DS(ON)}$ , but not a minimum. A reasonable assumption is that the minimum  $R_{DS(ON)}$  lies the same amount below the typical value as the maximum lies above it. Consult the MOSFET manufacturer for further guidelines.

To further limit current in the event of a short circuit to ground, the LTC3720 includes foldback current limiting. If the output falls by more than 25%, then the maximum sense voltage is progressively lowered to about one sixth of its full value.

### Minimum Off-time and Dropout Operation

The minimum off-time  $t_{OFF(MIN)}$  is the smallest amount of time that the LTC3720 is capable of turning on the bottom MOSFET, tripping the current comparator and turning the MOSFET back off. This time is generally about 350ns. The minimum off-time limit imposes a maximum duty cycle of  $t_{ON}/(t_{ON} + t_{OFF(MIN)})$ . If the maximum duty cycle is reached, due to a dropping input voltage for example, then the output will drop out of regulation. The minimum input voltage to avoid dropout is:

$$V_{IN(MIN)} = V_{OUT} \frac{t_{ON} + t_{OFF(MIN)}}{t_{ON}}$$

### Output Voltage Programming

The output voltage is digitally set to levels between 1.05V and 1.825V using the voltage identification (VID) inputs VID0-VID4. An internal 5-bit DAC configured as a precision resistive voltage divider sets the output voltage in increments according to Table 1. The VID codes are compatible with Intel VRM8.5 processor specifications. Each VID input is pulled up by an internal 40k pull-up resistor from the INTV<sub>CC</sub> supply and includes a series diode to prevent damage from VID inputs that exceed the supply.

### INTV<sub>CC</sub> Regulator

An internal P-channel low dropout regulator produces the 5V supply that powers the drivers and internal circuitry within the LTC3720. The INTV<sub>CC</sub> pin can supply up to 50mA RMS and must be bypassed to ground with a minimum of 4.7μF low ESR capacitor. Good bypassing is necessary to supply the high transient currents required by the MOSFET gate drivers. Applications using large MOSFETs with a high input voltage and high frequency of

\*Use  $R_{SENSE}$  value if a sense resistor is connected between SENSE+ and SENSE-.

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Table 1. VID Output Voltage Programming

VID4	VID3	VID2	VID1	VID0	V <sub>OUT</sub> (V)
0	0	0	0	0	1.250V
0	0	0	0	1	1.275V
0	0	0	1	0	1.200V
0	0	0	1	1	1.225V
0	0	1	0	0	1.150V
0	0	1	0	1	1.175V
0	0	1	1	0	1.100V
0	0	1	1	1	1.125V
0	1	0	0	0	1.050V
0	1	0	0	1	1.075V
0	1	0	1	0	1.800V
0	1	0	1	1	1.825V
0	1	1	0	0	1.750V
0	1	1	0	1	1.775V
0	1	1	1	0	1.700V
0	1	1	1	1	1.725V
1	0	0	0	0	1.650V
1	0	0	0	1	1.675V
1	0	0	1	0	1.600V
1	0	0	1	1	1.625V
1	0	1	0	0	1.550V
1	0	1	0	1	1.575V
1	0	1	1	0	1.500V
1	0	1	1	1	1.525V
1	1	0	0	0	1.450V
1	1	0	0	1	1.475V
1	1	0	1	0	1.400V
1	1	0	1	1	1.425V
1	1	1	0	0	1.350V
1	1	1	0	1	1.375V
1	1	1	1	0	1.300V
1	1	1	1	1	1.325V

operation may cause the LTC3720 to exceed its maximum junction temperature rating or RMS current rating. Most of the supply current drives the MOSFET gates unless an external EXT<sub>V<sub>CC</sub></sub> source is used. In continuous mode operation, this current is  $I_{GATECHG} = f(Q_{g(TOP)} + Q_{g(BOT)})$ . The junction temperature can be estimated from the equations given in Note 3 of the Electrical Characteristics. For example, the LTC3720EGN is limited to less than 19mA from a 30V supply:

$$T_J = 70^{\circ}\text{C} + (19\text{mA})(30\text{V})(95^{\circ}\text{C}/\text{W}) = 125^{\circ}\text{C}$$

For larger currents, consider using an external supply with the EXT<sub>V<sub>CC</sub></sub> pin.

### EXT<sub>V<sub>CC</sub></sub> Connection

The EXT<sub>V<sub>CC</sub></sub> pin can be used to provide MOSFET gate drive and control power from an external source during normal operation. Whenever the EXT<sub>V<sub>CC</sub></sub> pin is above 4.7V the internal 5V regulator is shut off and an internal 50mA P-channel switch connects the EXT<sub>V<sub>CC</sub></sub> pin to INT<sub>V<sub>CC</sub></sub>. INT<sub>V<sub>CC</sub></sub> power is supplied from EXT<sub>V<sub>CC</sub></sub> until this pin drops below 4.5V. Do not apply more than 7V to the EXT<sub>V<sub>CC</sub></sub> pin and ensure that  $\text{EXT}_{V_{CC}} \leq V_{IN}$ . The following list summarizes the possible connections for EXT<sub>V<sub>CC</sub></sub>:

1. EXT<sub>V<sub>CC</sub></sub> grounded. INT<sub>V<sub>CC</sub></sub> is always powered from the internal 5V regulator.
2. EXT<sub>V<sub>CC</sub></sub> connected to an external supply. A high efficiency supply compatible with the MOSFET gate drive requirements (typically 5V) can improve overall efficiency.
3. EXT<sub>V<sub>CC</sub></sub> connected to an output derived boost network. The low voltage output can be boosted using a charge pump or flyback winding to greater than 4.7V. The system will start-up using the internal linear regulator until the boosted output supply is available.

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### External Gate Drive Buffers

The LTC3720 drivers are adequate for driving up to about 60nC into MOSFET switches with RMS currents of 50mA. Applications with larger MOSFET switches or operating at higher frequencies requiring greater RMS currents will benefit from using external gate drive buffers such as the LTC1693. Alternately, the external buffer circuit shown in Figure 5 can be used. Note that the bipolar devices reduce the signal swing at the MOSFET gate and benefit from an increased  $EXTV_{CC}$  voltage of about 6V.

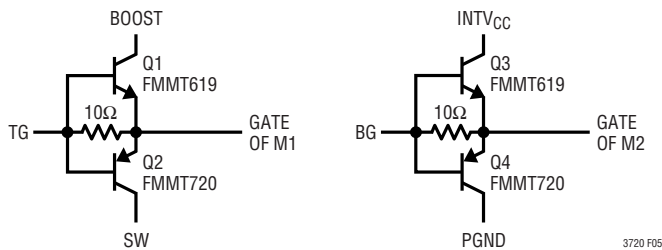


Figure 5. Optional External Gate Driver

### Soft-Start and Latchoff with the RUN/SS Pin

The RUN/SS pin provides a means to shut down the LTC3720 as well as a timer for soft-start and overcurrent latchoff. Pulling the RUN/SS pin below 0.8V puts the LTC3720 into a low quiescent current shutdown ( $I_Q < 30\mu A$ ). Releasing the pin allows an internal  $1.2\mu A$  current source to charge up the external timing capacitor  $C_{SS}$ . If RUN/SS has been pulled all the way to ground, there is a delay before starting of about:

$$t_{DELAY} = \frac{1.5V}{1.2\mu A} C_{SS} = (1.3s/\mu F) C_{SS}$$

When the voltage on RUN/SS reaches 1.5V, the LTC3720 begins operating with a clamp on  $I_{TH}$  of approximately 0.9V. As the RUN/SS voltage rises to 3V, the clamp on  $I_{TH}$  is raised until its full 2.4V range is available. This takes an additional  $1.3s/\mu F$ , during which the load current is folded

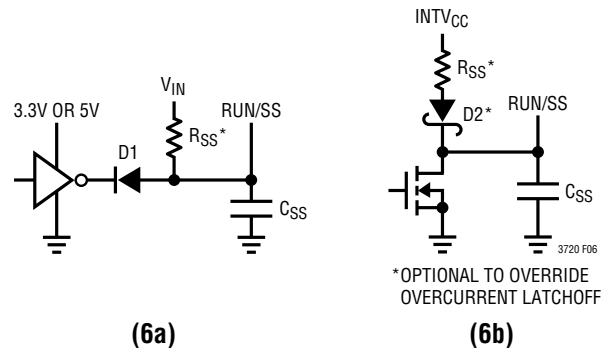


Figure 6. RUN/SS Pin Interfacing with Latchoff Defeated

back until the output reaches 75% of its final value. The pin can be driven from logic as shown in Figure 6. Diode D1 reduces the start delay while allowing  $C_{SS}$  to charge up slowly for the soft-start function.

After the controller has been started and given adequate time to charge up the output capacitor,  $C_{SS}$  is used as a short-circuit timer. After the RUN/SS pin charges above 4V, if the output voltage falls below 75% of its regulated value, then a short-circuit fault is assumed. A  $1.8\mu A$  current then begins discharging  $C_{SS}$ . If the fault condition persists until the RUN/SS pin drops to 3.5V, then the controller turns off both power MOSFETs, shutting down the converter permanently. The RUN/SS pin must be actively pulled down to ground in order to restart operation.

The overcurrent protection timer requires that the soft-start timing capacitor  $C_{SS}$  be made large enough to guarantee that the output is in regulation by the time  $C_{SS}$  has reached the 4V threshold. In general, this will depend upon the size of the output capacitance, output voltage and load current characteristic. A minimum soft-start capacitor can be estimated from:

$$C_{SS} > C_{OUT} V_{OUT} R_{SENSE} (10^{-4} [F/V s])$$

Generally  $0.1\mu F$  is more than sufficient.

Overcurrent latchoff operation is not always needed or desired. Load current is already limited during a short-circuit by the current foldback circuitry and latchoff

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operation can prove annoying during troubleshooting. The feature can be overridden by adding a pull-up current greater than  $5\mu\text{A}$  to the RUN/SS pin. The additional current prevents the discharge of  $C_{SS}$  during a fault and also shortens the soft-start period. Using a resistor to  $V_{IN}$  as shown in Figure 6a is simple, but slightly increases shutdown current. Connecting a resistor to  $\text{INTV}_{CC}$  as shown in Figure 6b eliminates the additional shutdown current, but requires a diode to isolate  $C_{SS}$ . Any pull-up network must be able to pull RUN/SS above the 4.5V maximum threshold that arms the latching circuit and overcome the  $4\mu\text{A}$  maximum discharge current.

### Efficiency Considerations

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Although all dissipative elements in the circuit produce losses, four main sources account for most of the losses in LTC3720 circuits:

1. DC  $I^2R$  losses. These arise from the resistances of the MOSFETs, inductor and PC board traces and cause the efficiency to drop at high output currents. In continuous mode the average output current flows through L, but is chopped between the top and bottom MOSFETs. If the two MOSFETs have approximately the same  $R_{DS(ON)}$ , then the resistance of one MOSFET can simply be summed with the resistances of L and the board traces to obtain the DC  $I^2R$  loss. For example, if  $R_{DS(ON)} = 0.01\Omega$  and  $R_L = 0.005\Omega$ , the loss will range from 1% up to 10% as the output current varies from 1A to 10A for a 1.5V output.

2. Transition loss. This loss arises from the brief amount of time the top MOSFET spends in the saturated region during switch node transitions. It depends upon the input voltage, load current, driver strength and MOSFET capacitance, among other factors. The loss is significant at input voltages above 20V and can be estimated from:

$$\text{Transition Loss} \cong (1.7A^{-1}) V_{IN}^2 I_{OUT} C_{RSS} f$$

3.  $\text{INTV}_{CC}$  current. This is the sum of the MOSFET driver and control currents. This loss can be reduced by supplying  $\text{INTV}_{CC}$  current through the  $\text{EXTV}_{CC}$  pin from a high efficiency source, such as an output derived boost network or alternate supply if available.

4.  $C_{IN}$  loss. The input capacitor has the difficult job of filtering the large RMS input current to the regulator. It must have a very low ESR to minimize the AC  $I^2R$  loss and sufficient capacitance to prevent the RMS current from causing additional upstream losses in fuses or batteries.

Other losses, including  $C_{OUT}$  ESR loss, Schottky diode D1 conduction loss during dead time and inductor core loss generally account for less than 2% additional loss.

When making adjustments to improve efficiency, the input current is the best indicator of changes in efficiency. If you make a change and the input current decreases, then the efficiency has increased. If there is no change in input current, then there is no change in efficiency.

### Checking Transient Response

The regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in load current. When a load step occurs,  $V_{OUT}$  immediately shifts by an amount equal to  $\Delta I_{LOAD}$  (ESR), where ESR is the effective series resistance of  $C_{OUT}$ .  $\Delta I_{LOAD}$  also begins to charge or discharge  $C_{OUT}$  generating a feedback error signal used by the regulator to return  $V_{OUT}$  to its steady-state value. During this recovery time,  $V_{OUT}$  can be monitored for overshoot or ringing that would indicate a stability problem. The  $I_{TH}$  pin external components shown in Figure 7 will provide adequate compensation for most applications. For a detailed explanation of switching control loop theory see Application Note 76.

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### Design Example

As a design example, take a supply with the following specifications:  $V_{IN} = 7V$  to  $24V$  (15V nominal),  $V_{OUT} = 1.05V$  to  $1.825V$  with typical at  $1.5V$ ,  $I_{OUT(MAX)} = 15A$ ,  $f = 300kHz$ . First, calculate the timing resistor with  $V_{ON} = V_{OUT}$ :

$$R_{ON} = \frac{1}{(300kHz)(10pF)} = 330k$$

and choose the inductor for about 40% ripple current at the maximum  $V_{IN}$ :

$$L = \frac{1.5V}{(300kHz)(0.4)(15A)} \left( 1 - \frac{1.5V}{24V} \right) = 0.8\mu H$$

Selecting a standard value of  $1\mu H$  results in a maximum ripple current of:

$$\Delta I_L = \frac{1.5V}{(300kHz)(1\mu H)} \left( 1 - \frac{1.5V}{24V} \right) = 4.7A$$

Next, choose the synchronous MOSFET switch. Because of the narrow duty cycle and large current, a single SO-8 MOSFET will have difficulty dissipating the power lost in the switch. Choosing two IRF7811A ( $R_{DS(ON)} = 0.013\Omega$ ,  $C_{RSS} = 60pF$ ,  $\theta_{JA} = 50^\circ C/W$ ) yields a nominal sense voltage of:

$$V_{SNS(NOM)} = (15A)(0.5)(1.3)(0.012\Omega) = 117mV$$

Tying  $V_{RNG}$  to  $INTV_{CC}$  will set the current sense voltage range for a nominal value of  $140mV$  with current limit occurring at  $186mV$ . To check if the current limit is acceptable, assume a junction temperature of about  $100^\circ C$  above a  $50^\circ C$  ambient with  $\rho_{150^\circ C} = 1.6$ :

$$I_{LIMIT} \geq \frac{186mV}{(0.5)(1.6)(0.012\Omega)} + \frac{1}{2}(4.7A) = 18A$$

and double check the assumed  $T_J$  in the MOSFET:

$$P_{BOT} = \frac{24V - 1.5V}{24V} \left( \frac{21.7A}{2} \right)^2 (1.6)(0.012\Omega) = 2.12W$$

$$T_J = 50^\circ C + (2.12W)(50^\circ C/W) = 156^\circ C$$

Because the top MOSFET is on for such a short time, a single IRF7811A will be sufficient. Checking its power dissipation at current limit with  $\rho_{90^\circ C} = 1.3$ :

$$\begin{aligned} P_{BOT} &= \frac{1.5V}{24V} (21.7A)^2 (1.3)(0.012\Omega) + \\ &\quad (1.7)(24V)^2 (21.7A)(60pF)(300kHz) \\ &= 0.46W + 0.38W = 0.84W \end{aligned}$$

$$T_J = 50^\circ C + (0.84W)(50^\circ C/W) = 92^\circ C$$

The junction temperatures will be significantly less at nominal current, but this analysis shows that careful attention to heat sinking will be necessary in this circuit.

$C_{IN}$  is chosen for an RMS current rating of about  $6A$  at temperature. The output capacitors are chosen for a low ESR of  $0.005\Omega$  to minimize output voltage changes due to inductor ripple current and load steps. The ripple voltage will be only:

$$\begin{aligned} \Delta V_{OUT(RIPPLE)} &= \Delta I_L(MAX) (ESR) \\ &= (4.7A) (0.005\Omega) = 24mV \end{aligned}$$

## APPLICATIONS INFORMATION

However, a 0A to 15A load step will cause an output change of up to:

$$\Delta V_{OUT(STEP)} = \Delta I_{LOAD} (ESR) = (15A) (0.005\Omega) = 75mV$$

The complete circuit is shown in Figure 7.

### Active Voltage Positioning

Active voltage positioning (also termed load “deregulation” or droop) describes a technique where the output voltage varies with load in a controlled manner. It is useful in applications where rapid load steps are the main cause of error in the output voltage. By positioning the output voltage above the regulation point at zero load, and below the regulation point at full load, one can use more of the

error budget for the load step. This allows one to reduce the number of output capacitors by relaxing the ESR requirement.

In the design example, Figure 7, five 0.025Ω capacitors are required in parallel to keep the output voltage within tolerance. Using active voltage positioning, the same specification can be met with only three capacitors. In this case, the load step will cause an output voltage change of:

$$\Delta V_{OUT(STEP)} = (15A) \left( \frac{1}{3} \right) (0.025\Omega) = 125mV$$

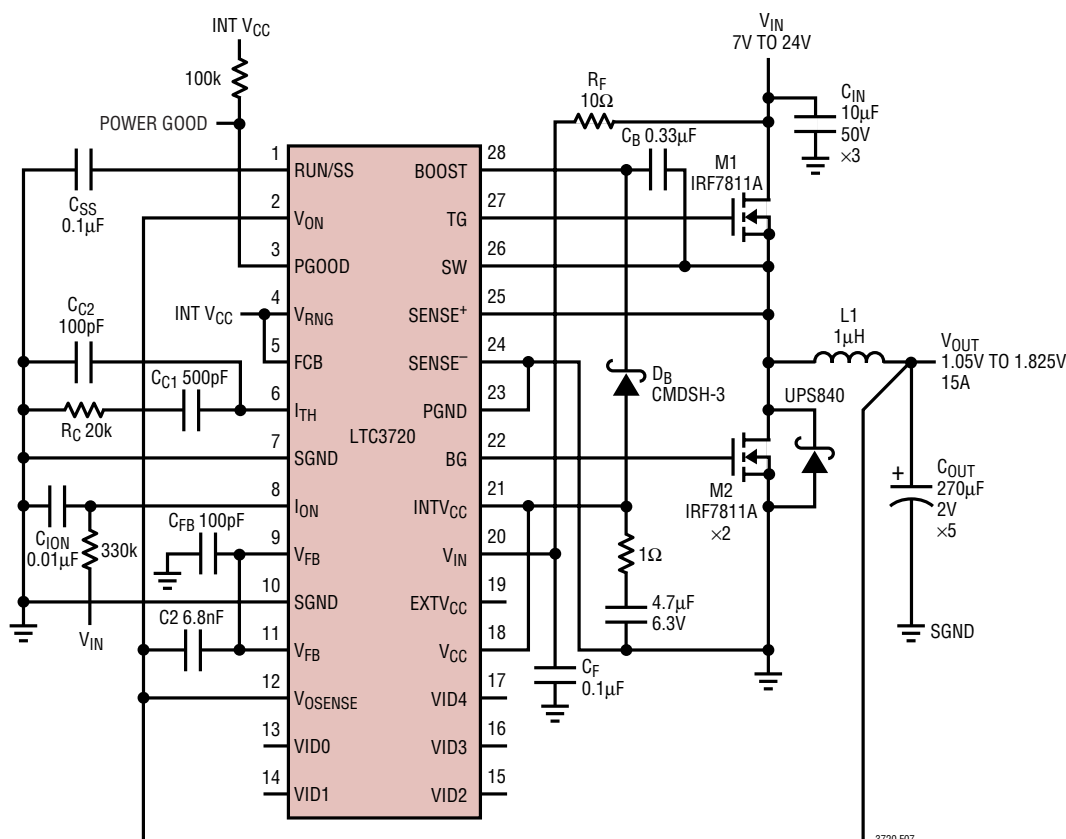


Figure 7. 15A CPU Core Voltage Regulator at 300kHz

## APPLICATIONS INFORMATION

By positioning the output voltage 60mV above the regulation point at no load, it will only drop 65mV below the regulation point after the load step, well within the  $\pm 100\text{mV}$  tolerance.

Implementing active voltage positioning requires setting a precise gain between the sensed current and the output voltage. Because of the variability of MOSFET on-resistance, it is prudent to use a sense resistor with active voltage positioning. In order to minimize power lost in this resistor, a low value is chosen of  $0.003\Omega$ . The nominal sense voltage will now be:

$$V_{\text{SNS(NOM)}} = (0.003\Omega)(15\text{A}) = 45\text{mV}$$

To maintain a reasonable current limit, the voltage on the  $V_{\text{RNG}}$  pin is reduced to its minimum value of 0.5V, corresponding to a 50mV nominal sense voltage.

Next, the gain of the LTC3720 error amplifier must be determined. The change in  $I_{\text{TH}}$  voltage for a corresponding change in the output current is:

$$\begin{aligned}\Delta I_{\text{TH}} &= \left( \frac{12\text{V}}{V_{\text{RNG}}} \right) R_{\text{SENSE}} \Delta I_{\text{OUT}} \\ &= (24)(0.003\Omega)(15\text{A}) = 1.08\text{V}\end{aligned}$$

The corresponding change in the output voltage is determined by the gain of the error amplifier and feedback divider. The LTC3720 error amplifier has a transconductance  $g_m$  that is constant over both temperature and a wide  $\pm 40\text{mV}$  input range. Thus, by connecting a load resistance  $R_{\text{VP}}$  to the  $I_{\text{TH}}$  pin, the error amplifier gain can be precisely set for accurate active voltage positioning.

$$\Delta I_{\text{TH}} = g_m R_{\text{VP}} \left( \frac{0.8\text{V}}{V_{\text{OUT}}} \right) \Delta V_{\text{OUT}}$$

Solving for this resistance value:

$$\begin{aligned}R_{\text{VP}} &= \frac{V_{\text{OUT}} \Delta I_{\text{TH}}}{(0.8\text{V})g_m \Delta V_{\text{OUT}}} \\ &= \frac{(1.5\text{V})(1.08\text{V})}{(0.8\text{V})(1.7\text{mS})(125\text{mV})} = 9.53\text{k}\end{aligned}$$

The gain setting resistance  $R_{\text{VP}}$  is implemented with two resistors,  $R_{\text{VP1}}$  connected from  $I_{\text{TH}}$  to ground and  $R_{\text{VP2}}$  connected from  $I_{\text{TH}}$  to  $\text{INTV}_{\text{CC}}$ . The parallel combination of these resistors must equal  $R_{\text{VP}}$  and their ratio determines nominal value of the  $I_{\text{TH}}$  pin voltage when the error amplifier input is zero. To center the load line around the regulation point, the  $I_{\text{TH}}$  pin voltage must be set to correspond to half the output current. The relation between  $I_{\text{TH}}$  voltage and the output current is:

$$\begin{aligned}I_{\text{TH(NOM)}} &= \left( \frac{12\text{V}}{V_{\text{RNG}}} \right) R_{\text{SENSE}} \left( I_{\text{OUT}} - \frac{1}{2} \Delta I_{\text{L}} \right) + 0.8\text{V} \\ &= \left( \frac{12\text{V}}{0.5\text{V}} \right) (0.003\Omega) \left( 7.5\text{A} - \frac{1}{2} 4.7\text{A} \right) + 0.8\text{V} \\ &= 1.17\text{V}\end{aligned}$$

Solving for the required values of the resistors:

$$\begin{aligned}R_{\text{VP1}} &= \frac{5\text{V}}{5\text{V} - I_{\text{TH(NOM)}}} R_{\text{VP}} = \frac{5\text{V}}{5\text{V} - 1.17\text{V}} 9.53\text{k} \\ &= 12.44\text{k} \\ R_{\text{VP2}} &= \frac{5\text{V}}{I_{\text{TH(NOM)}}} R_{\text{VP}} = \frac{5\text{V}}{1.17\text{V}} 9.53\text{k} = 40.73\text{k}\end{aligned}$$

## APPLICATIONS INFORMATION

The modified circuit is shown in Figure 8. Figures 9 and 10 show the transient response without and with active voltage positioning. Both circuits easily stay within  $\pm 100\text{mV}$  of the 1.5V output. However, the circuit with active voltage

positioning accomplishes this with only three output capacitors rather than five. Refer to Linear Technology Design Solutions 10 for additional information about active voltage positioning.

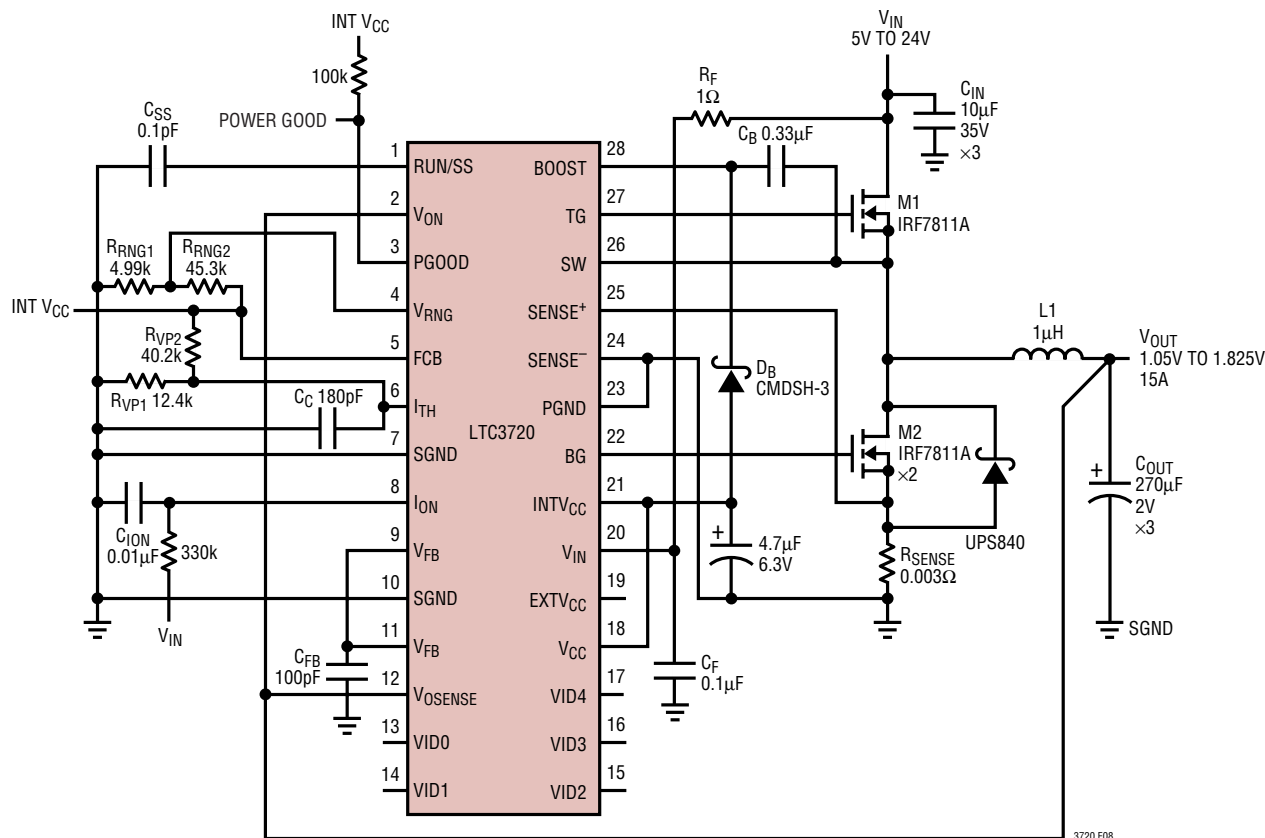


Figure 8. 15A CPU Core Voltage Regulator with Active Voltage Positioning at 300kHz

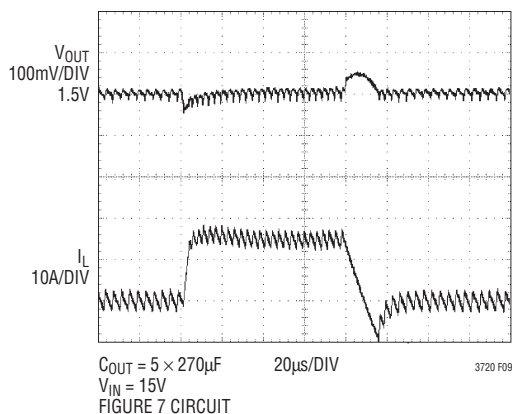


Figure 9. Normal Transient Response ( $C_{OUT} = 5 \times 270\mu\text{F}$ )

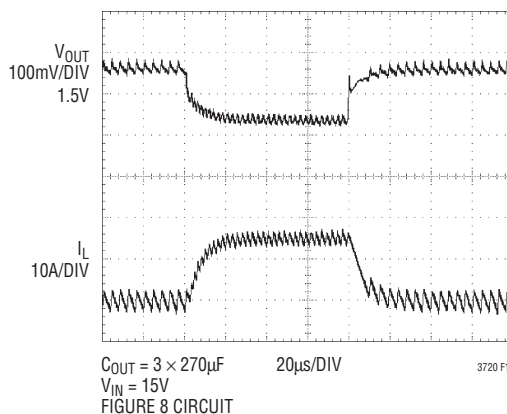


Figure 10. Transient Response with Active Voltage Positioning ( $C_{OUT} = 3 \times 270\mu\text{F}$ )

## APPLICATIONS INFORMATION

### PC Board Layout Checklist

When laying out the printed circuit board, use the following checklist to ensure proper operation of the controller. These items are also illustrated in Figure 11.

- Segregate the signal and power grounds. All small signal components should return to the SGND pin at one point which is then tied to the PGND pin close to the source of M2.
- Place M2 as close to the controller as possible, keeping the SENSE<sup>-</sup>, BG and SENSE<sup>+</sup> traces short.
- Connect the input capacitor(s) C<sub>IN</sub> close to the power MOSFETs. This capacitor carries the MOSFET AC current. Minimize the loop area formed by C<sub>IN</sub>, M1 and M2.
- Keep the high dV/dT SW, BOOST and TG nodes away from sensitive small-signal nodes.
- Connect the INTV<sub>CC</sub> decoupling capacitor C<sub>VCC</sub> closely to the INTV<sub>CC</sub> and PGND pins.
- Connect the top driver boost capacitor C<sub>B</sub> closely to the BOOST and SW pins.
- Connect the V<sub>IN</sub> pin decoupling capacitor C<sub>F</sub> closely to the V<sub>IN</sub> and PGND pins.
- VID0-VID4 interface circuitry must return to SGND.

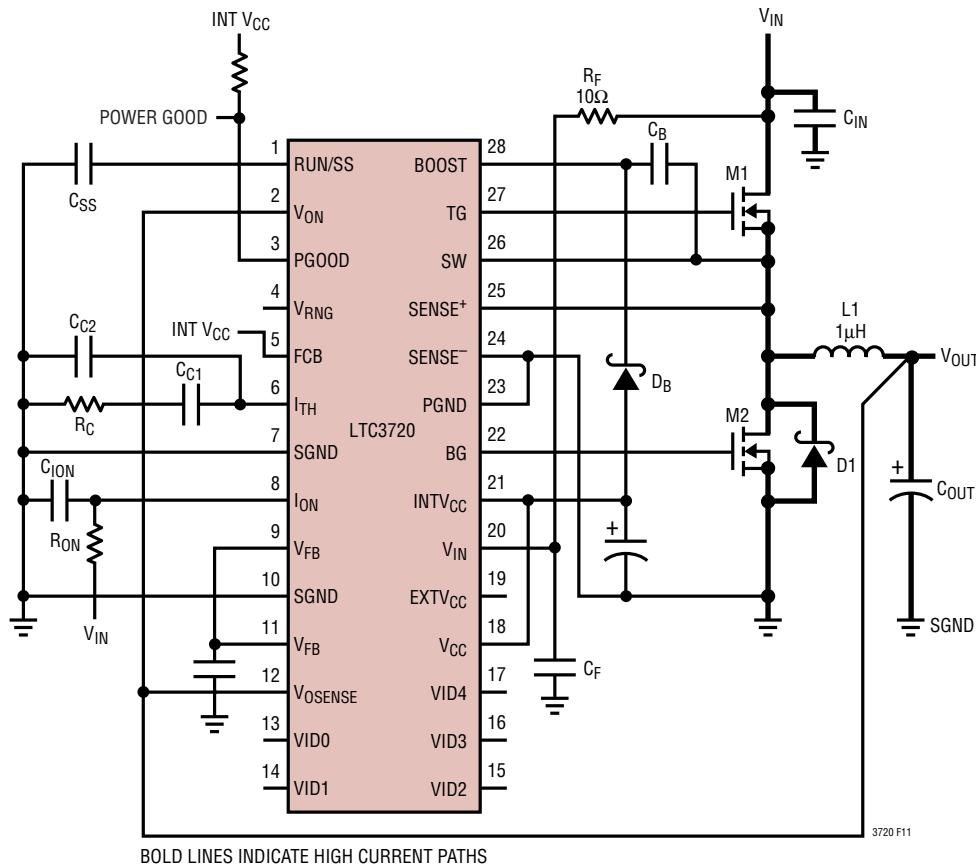
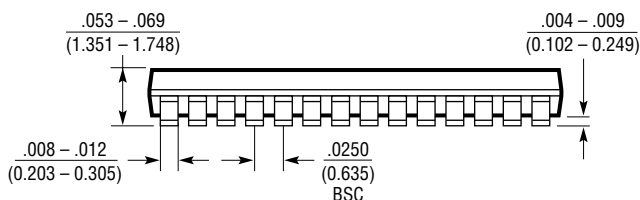
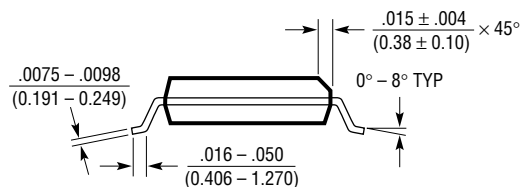
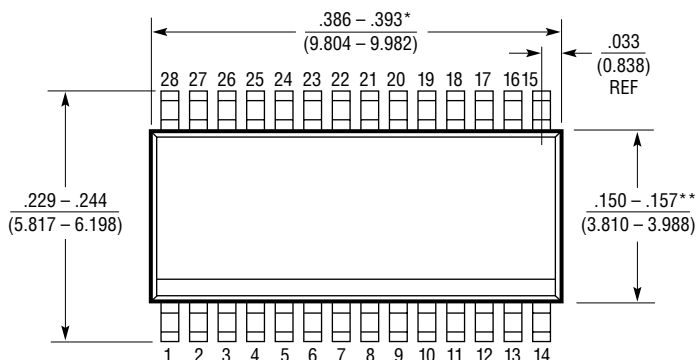
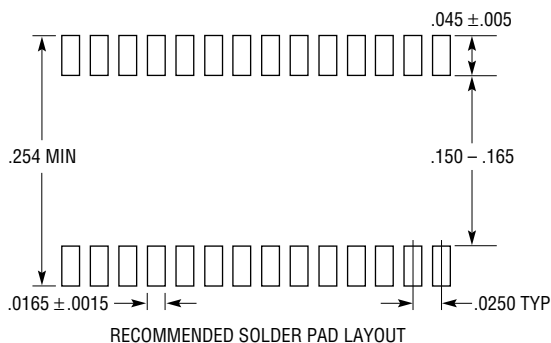


Figure 11. LTC3720 Layout Diagram

# PACKAGE DESCRIPTION

## GN Package 28-Lead Plastic SSOP (Narrow .150 Inch) (Reference LTC DWG # 05-08-1641)



- NOTE:
1. CONTROLLING DIMENSION: INCHES
  2. DIMENSIONS ARE IN  $\frac{\text{INCHES}}{\text{MILLIMETERS}}$
  3. DRAWING NOT TO SCALE

\*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE  
 \*\*DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

GN28 (SSOP) 0502

## RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1628-PG	Dual, 2-Phase Synchronous Step-Down Controller	Power Good Output, Minimum Input/Output Capacitors, $3.5V \leq V_{IN} \leq 36V$
LTC1628-SYNC	Dual, 2-Phase Synchronous Step-Down Controller	Synchronizable 150kHz to 300kHz
LTC1709-7/-8/-8.5/-9	2-Phase Synchronous Step-Down Controllers with 5-Bit VID	Up to 42A Outputs, Various VID Tables, Mobile, Desktop, Server, $3.5V \leq V_{IN} \leq 36V$
LTC1735	Synchronous Step-Down Controller	Burst Mode™ Operation, 16-Pin Narrow SSOP, $3.5V \leq V_{IN} \leq 36V$
LTC1736	Synchronous Step-Down Controller with 5-Bit VID	Mobile VID, $0.925V \leq V_{OUT} \leq 2V$ , $3.5V \leq V_{IN} \leq 36V$
LTC1772	SOT-23 Step-Down Controller	Current Mode, 550kHz, Very Small Solution Size
LTC1773	Synchronous Step-Down Controller	Up to 95% Efficiency, 550kHz, $2.65V \leq V_{IN} \leq 8.5V$ , $0.8V \leq V_{OUT} \leq V_{IN}$ , Synchronizable to 750kHz
LTC1778/LTC1778-1 LTC3778	No R <sub>SENSE</sub> Synchronous Step-Down Controllers	No Sense Resistor Required, $4V \leq V_{IN} \leq 36V$ , $0.8V \leq V_{OUT} \leq (0.9) V_{IN}$
LTC1876	2-Phase, Dual Synchronous Step-Down Controller with Step-Up Regulator	$2.6V \leq V_{IN} \leq 36V$ , Power Good Output, 300kHz Operation
LTC3701	Dual, 2-Phase Step-Down Controller	Current Mode, 550kHz, Small 16-Pin SSOP, $2.5V \leq V_{IN} < 9.8V$
LTC3711	5-Bit Adjustable, Low Duty Cycle Step-Down Controller	$0.925V \leq V_{OUT} \leq 2V$ , $V_{IN}$ up to 36V, 24-Pin GN
LTC3728LX LTC3728/LTC3728L	Dual, 550kHz, 2-Phase Synchronous Step-Down Controllers	Phase Lockable Fixed Frequency from 250kHz to 550kHz, 5mm × 5mm QFN and SSOP Packages, Small Inductors and Capacitors, Integrated MOSFET Drivers
LTC3730/LTC3732	3-Phase Synchronous DC/DC Step-Down Controllers	IMVP III and VRM 9.0/9.1 Compliant, 600kHz per Phase, $I_{OUT} \leq 60A$ , Integrated MOSFET Drivers
LTC3831	DDR Memory Termination Power Supply	$V_{OUT} = 1/2 V_{IN}$ , $I_{OUT}$ up to 15A, $3V \leq V_{IN} \leq 8V$ , 700μA Supply Current, 16-Pin SSOP Package

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