THE DATASHEET OF

LTC3892EUH#PBF

www.win-source.net 0086-755-83957316

60V Low I_Q, Dual, 2-Phase Synchronous Step-Down DC/DC Controller

FEATURES

- **Wide V_{IN} Range: 4.5V to 60V (65V Abs Max)**
- **Wide Output Voltage Range: 0.8V ≤ V_{OUT} ≤ 99% • V_{IN}**
- **Adjustable Gate Drive Level 5V to 10V (OPTI-DRIVE)**
- **No External Bootstrap Diodes Required**
- **Low Operating I_Q: 29µA (One Channel On)**
- Selectable Gate Drive UVLO Thresholds
- Out-of-Phase Operation Reduces Required Input Capacitance and Power Supply Induced Noise
- Phase-Lockable Frequency: 75kHz to 850kHz
- Selectable Continuous, Pulse Skipping or Low Ripple Burst Mode® Operation at Light Loads
- Selectable Current Limit (LTC3892/LTC3892-2)
- Very Low Dropout Operation: 99% Duty Cycle
- Power Good Output Voltage Monitors (LTC3892/LTC3892-2)
- Low Shutdown I_Q: 3.6µA
- Small 32-Lead 5mm × 5mm QFN Package (LTC3892/LTC3892-2) or TSSOP Package (LTC3892-1)

APPLICATIONS

- Automotive and Industrial Power Systems
- Distributed DC Power Systems
- High Voltage Battery Operated Systems

DESCRIPTION

The LTC®3892/LTC3892-1/LTC3892-2 is a high performance dual step-down DC/DC switching regulator controller that drives all N-channel synchronous power MOSFET stages. Power loss and noise are minimized by operating the two controller output stages out-of-phase.

The gate drive voltage can be programmed from 5V to 10V to allow the use of logic or standard-level FETs and to maximize efficiency. Internal switches in the top gate drivers eliminate the need for external bootstrap diodes.

A wide 4.5V to 60V input supply range encompasses a wide range of intermediate bus voltages and battery chemistries. Output voltages up to 99% of V_{IN} can be regulated. OPTI-LOOP® compensation allows the transient response and loop stability to be optimized over a wide range of output capacitance and ESR values.

The 29µA no-load quiescent current extends operating run time in battery powered systems. For a comparison of the LTC3892 to the LTC3892-1 and LTC3892-2, see Table 1 in the Pin Functions section of this data sheet.

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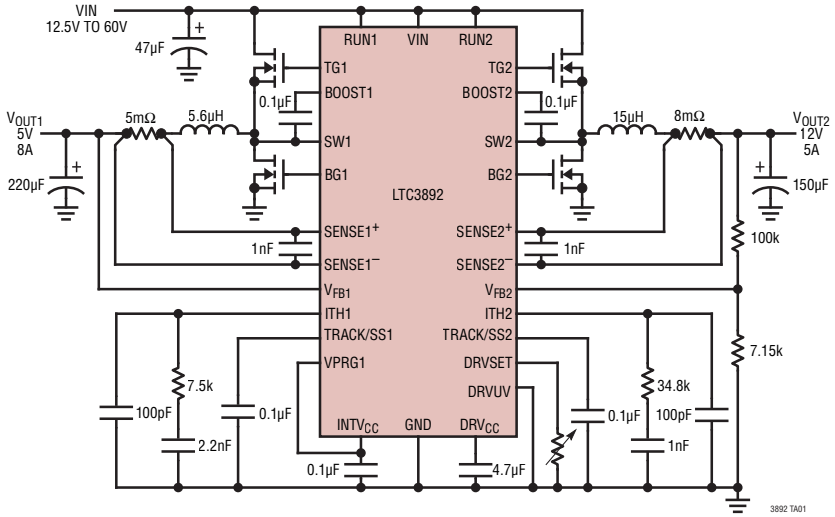
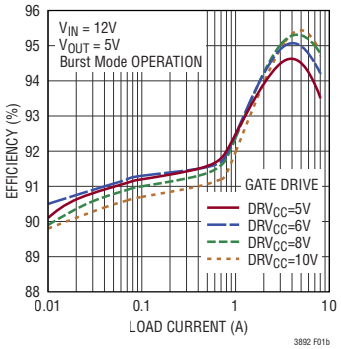
TYPICAL APPLICATION

High Efficiency Dual 5V/12V Output Step-Down Converter



Efficiency vs Output Current

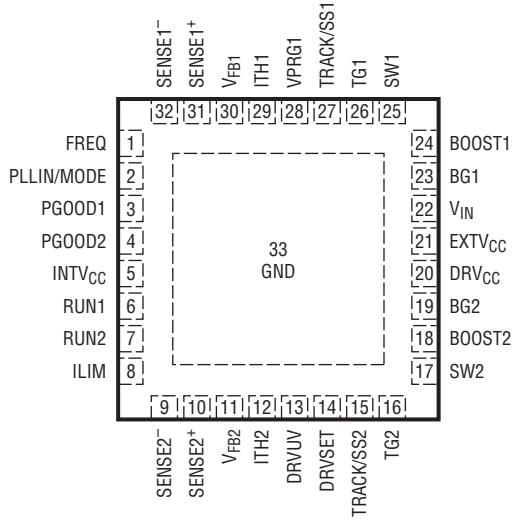


ABSOLUTE MAXIMUM RATINGS (Notes 1, 3)

Input Supply Voltage (V_{IN}) ..... –0.3V to 65V
Top Side Driver Voltages
(BOOST1, BOOST2) ..... –0.3V to 76V
Switch Voltage (SW1, SW2) ..... –5V to 70V
DRV_{CC}, (BOOST1-SW1),
(BOOST2-SW2) ..... –0.3V to 11V
BG1, BG2, TG1, TG2 ..... (Note 8)
RUN1, RUN2 Voltages ..... –0.3V to 65V
$SENSE1^+$, $SENSE2^+$, $SENSE1^-$
$SENSE2^-$ Voltages ..... –0.3V to 65V
PLLIN/MODE, FREQ Voltages ..... –0.3V to 6V
$EXTV_{CC}$ Voltage ..... –0.3V to 14V
I_{TH1}, I_{TH2}, V_{FB1}, V_{FB2} Voltages ..... –0.3V to 6V
DRVSET, DRVUV Voltages ..... –0.3V to 6V
TRACK/SS1, TRACK/SS2 Voltages ..... –0.3V to 6V
PGOOD1, PGOOD2 Voltages
(LTC3892/LTC3892-2) ..... –0.3V to 6V
VPRG1, ILIM Voltages
(LTC3892/LTC3892-2) ..... –0.3V to 6V
Operating Junction Temperature Range (Note 2)
LTC3892E, LTC3892I,
LTC3892E-1, LTC3892I-1,
LTC3892E-2, LTC3892I-2 ..... –40°C to 125°C
LTC3892H,
LTC3892H-1, LTC3892H-2 ..... –40°C to 150°C
LTC3892MP, LTC3892MP-1,
LTC3892MP-2 ..... –55°C to 150°C
Storage Temperature Range ..... –65°C to 150°C

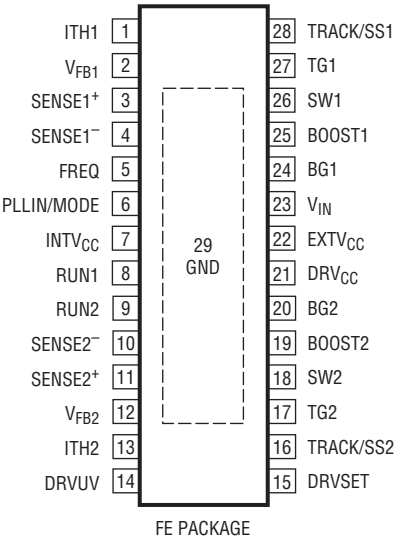
PIN CONFIGURATION

LTC3892/LTC3892-2



UH PACKAGE
32-LEAD (5mm × 5mm) PLASTIC QFN
T_{JMAX} = 150°C, θ_{JA} = 44°C/W
EXPOSED PAD (PIN 33) IS GND, MUST BE CONNECTED TO GND

LTC3892-1



FE PACKAGE
28-LEAD PLASTIC TSSOP
T_{JMAX} = 150°C, θ_{JA} = 30°C/W
EXPOSED PAD (PIN 29) IS GND, MUST BE CONNECTED TO GND

ORDER INFORMATION http://www.linear.com/product/LTC3892#orderinfo

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3892EUH#PBF	LTC3892EUH#TRPBF	3892	32-Lead (5mm × 5mm) Plastic QFN	–40°C to 125°C
LTC3892IUH#PBF	LTC3892IUH#TRPBF	3892	32-Lead (5mm × 5mm) Plastic QFN	–40°C to 125°C
LTC3892HUH#PBF	LTC3892HUH#TRPBF	3892	32-Lead (5mm × 5mm) Plastic QFN	–40°C to 150°C
LTC3892MPUH#PBF	LTC3892MPUH#TRPBF	3892	32-Lead (5mm × 5mm) Plastic QFN	–55°C to 150°C
LTC3892EFE-1#PBF	LTC3892EFE-1#TRPBF	LTC3892FE-1	28-Lead Plastic TSSOP	–40°C to 125°C
LTC3892IFE-1#PBF	LTC3892IFE-1#TRPBF	LTC3892FE-1	28-Lead Plastic TSSOP	–40°C to 125°C
LTC3892HFE-1#PBF	LTC3892HFE-1#TRPBF	LTC3892FE-1	28-Lead Plastic TSSOP	–40°C to 150°C
LTC3892MPFE-1#PBF	LTC3892MPFE-1#TRPBF	LTC3892FE-1	28-Lead Plastic TSSOP	–55°C to 150°C
LTC3892EUH-2#PBF	LTC3892EUH-2#TRPBF	38922	32-Lead (5mm × 5mm) Plastic QFN	–40°C to 125°C
LTC3892IUH-2#PBF	LTC3892IUH-2#TRPBF	38922	32-Lead (5mm × 5mm) Plastic QFN	–40°C to 125°C
LTC3892HUH-2#PBF	LTC3892HUH-2#TRPBF	38922	32-Lead (5mm × 5mm) Plastic QFN	–40°C to 150°C
LTC3892MPUH-2#PBF	LTC3892MPUH-2#TRPBF	38922	32-Lead (5mm × 5mm) Plastic QFN	–55°C to 150°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/

For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/ . Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{IN} = 12V, $V_{RUN1,2}$ = 5V, V_{EXTVCC} = 0V, V_{DRVSET} = 0V, VPRG1 = FLOAT unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Input Supply Operating Voltage Range			4.5		60	V
V_{FB1}	Channel 1 Regulated Feedback Voltage	(Note 4) ITH1 Voltage = 1.2V					
		0°C to 85°C, VPRG1 = FLOAT (LTC3892/LTC3892-2) or LTC3892-1		0.792	0.800	0.808	V
		VPRG1 = FLOAT (LTC3892/LTC3892-2) or LTC3892-1	●	0.788	0.800	0.812	V
		VPRG1 = 0V (LTC3892/LTC3892-2)	●	3.234	3.3	3.366	V
		VPRG1 = $INTV_{CC}$ (LTC3892/LTC3892-2)	●	4.890	5.0	5.110	V
V_{FB2}	Channel 2 Regulated Feedback Voltage	(Note 4) ITH2 Voltage = 1.2V					V
		0°C to 85°C		0.792	0.800	0.808	V
			●	0.788	0.800	0.812	
I_{FB2}	Channel 2 Feedback Current	(Note 4)			–2	±50	nA
I_{FB1}	Channel 1 Feedback Current	(Note 4)					
		VPRG1 = FLOAT (LTC3892/LTC3892-2) or LTC3892-1			–0.002	±0.05	µA
		VPRG1 = 0V (LTC3892/LTC3892-2)			4	6	µA
		VPRG1 = $INTV_{CC}$ (LTC3892/LTC3892-2)			4	6	µA
$V_{REFLNREG}$	Reference Voltage Line Regulation	(Note 4) V_{IN} = 4.5V to 60V			0.002	0.02	%/V
$V_{LOADREG}$	Output Voltage Load Regulation	(Note 4) Measured in Servo Loop, ΔITH Voltage = 1.2V to 0.7V	●		0.01	0.1	%
		(Note 4) Measured in Servo Loop, ΔITH Voltage = 1.2V to 2V	●		–0.01	–0.1	%
$g_{m1,2}$	Transconductance Amplifier g_m	(Note 4) ITH1,2 = 1.2V, Sink/Source 5µA			2		mmho
I_Q	Input DC Supply Current	(Note 5) V_{DRVSET} = 0V					
	Pulse-Skipping or Forced Continuous Mode (One Channel On)	RUN1 = 5V and RUN2 = 0V or RUN2 = 5V and RUN1 = 0V, $V_{FB1,2}$ = 0.83V (No Load)			1.6		mA
	Pulse-Skipping or Forced Continuous Mode (Both Channels On)	RUN1,2 = 5V, $V_{FB1,2}$ = 0.83V (No Load)			2.8		mA
	Sleep Mode (One Channel On)	RUN1 = 5V and RUN2 = 0V or RUN2 = 5V and RUN1 = 0V, $V_{FB1,2}$ = 0.83V (No Load)	●		29	55	µA
	Sleep Mode (Both Channels On)	RUN1,2 = 5V, $V_{FB1,2}$ = 0.83V (No Load)			34	55	µA
	Shutdown	RUN1,2 = 0V			3.6	10	µA
UVLO	Undervoltage Lockout	DRV_{CC} Ramping Up					
		DRVUV = 0V	●		4.0	4.2	V
		DRVUV = $INTV_{CC}$	●		7.5	7.8	V
		DRV_{CC} Ramping Down					
		DRVUV = 0V	●	3.6	3.8	4.0	V
		DRVUV = $INTV_{CC}$	●	6.4	6.7	7.0	V
$V_{OVL1,2}$	Feedback Overvoltage Protection	Measured at $V_{FB1,2}$ Relative to Regulated $V_{FB1,2}$ (LTC3892/LTC3892-1)		7	10	13	%
$I_{SENSE1,2}+$	$SENSE^+$ Pin Current					±1	µA
$I_{SENSE1,2}–$	$SENSE^–$ Pins Current	$V_{OUT1,2} < V_{INTVCC} – 0.5V$				±1	µA
		$V_{OUT1,2} > V_{INTVCC} + 0.5V$			700		µA
$DF_{MAX(TG)}$	Maximum Duty Factor for TG	In Dropout, FREQ = 0V		97.5	99		%
$I_{TRACK/SS1,2}$	Soft-Start Charge Current	$V_{TRACK/SS1,2}$ = 0V		8	10	12	µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{IN} = 12V, $V_{RUN1,2}$ = 5V, V_{EXTVCC} = 0V, V_{DRVSET} = 0V, VPRG1 = FLOAT unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V_{RUN1,2}$ ON	RUN Pin On Threshold	V_{RUN1}, V_{RUN2} Rising	●	1.22	1.275	1.33	V
$V_{RUN1,2}$ Hyst	RUN Pin Hysteresis				75		mV
$V_{SENSE(MAX)}$	Maximum Current Sense Threshold	$V_{FB1,2}$ = 0.7V, $V_{SENSE1,2}$– = 3.3V					
		I_{LIM} = FLOAT (LTC3892/LTC3892-2) or LTC3892-1	●	66	75	84	mV
		I_{LIM} = 0V (LTC3892/LTC3892-2)	●	43	50	58	mV
		I_{LIM} = $INTV_{CC}$ (LTC3892/LTC3892-2)	●	90	100	109	mV
$V_{SENSE(MATCH)}$	Matching Between $V_{SENSE1(MAX)}$ and $V_{SENSE2(MAX)}$	$V_{FB1,2}$ = 0.7V, $V_{SENSE1,2}$– = 3.3V					
		I_{LIM} = FLOAT (LTC3892/LTC3892-2) or LTC3892-1	●	–8	0	8	mV
		I_{LIM} = 0V (LTC3892/LTC3892-2)	●	–8	0	8	mV
		I_{LIM} = $INTV_{CC}$ (LTC3892/LTC3892-2)	●	–8	0	8	mV
Gate Driver							
TG1,2	Pull-Up On-Resistance Pull-Down On-Resistance	V_{DRVSET} = $INTV_{CC}$			2.2 1.0		Ω Ω
BG1,2	Pull-Up On-Resistance Pull-Down On-Resistance	V_{DRVSET} = $INTV_{CC}$			2.2 1.0		Ω Ω
BDSW1,2	BOOST to DRV_{CC} Switch On-Resistance	V_{SW} = 0V, V_{DRVSET} = $INTV_{CC}$			3.7		Ω
	TG Transition Time:	(Note 6) V_{DRVSET} = $INTV_{CC}$					
TG1,2 t_r	Rise Time	C_{LOAD} = 3300pF			25		ns
TG1,2 t_f	Fall Time	C_{LOAD} = 3300pF			15		ns
	BG Transition Time:	(Note 6) V_{DRVSET} = $INTV_{CC}$					
BG1,2 t_r	Rise Time	C_{LOAD} = 3300pF			25		ns
BG1,2 t_f	Fall Time	C_{LOAD} = 3300pF			15		ns
TG/BG t_{1D}	Top Gate Off to Bottom Gate On Delay Synchronous Switch-On Delay Time	C_{LOAD} = 3300pF Each Driver, V_{DRVSET} = $INTV_{CC}$			55		ns
BG/TG t_{1D}	Bottom Gate Off to Top Gate On Delay Top Switch-On Delay Time	C_{LOAD} = 3300pF Each Driver, V_{DRVSET} = $INTV_{CC}$			50		ns
$t_{ON(MIN)1,2}$	TG Minimum On-Time	(Note 7) V_{DRVSET} = $INTV_{CC}$			80		ns
DRV_{CC} Linear Regulator							
$V_{DRVCC(INT)}$	DRV_{CC} Voltage from Internal V_{IN} LDO	V_{EXTVCC} = 0V					
		7V < V_{IN} < 60V, DRVSET = 0V		5.8	6.0	6.2	V
		11V < V_{IN} < 60V, DRVSET = $INTV_{CC}$		9.6	10.0	10.4	V
$V_{LDOREG(INT)}$	DRV_{CC} Load Regulation from V_{IN} LDO	I_{CC} = 0mA to 50mA, V_{EXTVCC} = 0V			0.9	2.0	%
$V_{DRVCC(EXT)}$	DRV_{CC} Voltage from Internal $EXTV_{CC}$ LDO	7V < V_{EXTVCC} < 13V, DRVSET = 0V		5.8	6.0	6.2	V
		11V < V_{EXTVCC} < 13V, DRVSET = $INTV_{CC}$		9.6	10.0	10.4	V
$V_{LDOREG(EXT)}$	DRV_{CC} Load Regulation from Internal $EXTV_{CC}$ LDO	I_{CC} = 0mA to 50mA, V_{EXTVCC} = 8.5V, V_{DRVSET} = 0V			0.7	2.0	%
V_{EXTVCC}	$EXTV_{CC}$ LDO Switchover Voltage	$EXTV_{CC}$ Ramping Positive					
		DRVUV = 0V		4.5	4.7	4.9	V
		DRVUV = $INTV_{CC}$		7.4	7.7	8.0	V
V_{LDOHYS}	$EXTV_{CC}$ Hysteresis				250		mV
$V_{DRVCC(50k\Omega)}$	Programmable DRV_{CC}	R_{DRVSET} = 50kΩ, V_{EXTVCC} = 0V			5.0		V
$V_{DRVCC(70k\Omega)}$	Programmable DRV_{CC}	R_{DRVSET} = 70kΩ, V_{EXTVCC} = 0V		6.4	7.0	7.6	V
$V_{DRVCC(90k\Omega)}$	Programmable DRV_{CC}	R_{DRVSET} = 90kΩ, V_{EXTVCC} = 0V			9.0		V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{IN} = 12V, $V_{RUN1,2,3}$ = 5V, V_{EXTVCC} = 0V, V_{DRVSET} = 0V, VPRG1 = FLOAT unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Oscillator and Phase-Locked Loop							
$f_{25k\Omega}$	Programmable Frequency	R_{FREQ} =25kΩ, PLLIN/MODE = DC Voltage			105		kHz
$f_{65k\Omega}$	Programmable Frequency	R_{FREQ} = 65kΩ, PLLIN/MODE = DC Voltage		375	440	505	kHz
$f_{105k\Omega}$	Programmable Frequency	R_{FREQ} = 105kΩ, PLLIN/MODE = DC Voltage			835		kHz
f_{LOW}	Low Fixed Frequency	V_{FREQ} = 0V, PLLIN/MODE = DC Voltage		320	350	380	kHz
f_{HIGH}	High Fixed Frequency	V_{FREQ} = $INTV_{CC}$, PLLIN/MODE = DC Voltage		485	535	585	kHz
f_{SYNC}	Synchronizable Frequency	PLLIN/MODE = External Clock	●	75		850	kHz
PLLIN V_{IH} PLLIN V_{IL}	PLLIN/MODE Input High Level PLLIN/MODE Input Low Level	PLLIN/MODE = External Clock PLLIN/MODE = External Clock	● ●	2.5		 0.5	V V
PGOOD1 and PGOOD2 Outputs (LTC3892/LTC3892-2)							
V_{PGL}	PGOOD Voltage Low	I_{PGOOD} = 2mA			0.2	0.4	V
I_{PGOOD}	PGOOD Leakage Current	V_{PGOOD} = 5V				±1	µA
V_{PG}	PGOOD Trip Level	V_{FB} with Respect to Set Regulated Voltage V_{FB} Ramping Negative Hysteresis		 –13	 –10 2.5	 –7	 % %
		V_{FB} with Respect to Set Regulated Voltage V_{FB} Ramping Positive Hysteresis		 7	 10 2.5	 13	 % %
t_{PG}	Delay for Reporting a Fault				35		µs

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Ratings for extended periods may affect device reliability and lifetime.

Note 2: The LTC3892/LTC3892-1/LTC3892-2 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC3892E/LTC3892E-1/LTC3892E-2 is guaranteed to meet performance specifications from 0°C to 85°C. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3892I/LTC3892I-1/LTC3892I-2 is guaranteed over the –40°C to 125°C operating junction temperature range, the LTC3892H/LTC3892H-1/LTC3892H-2 is guaranteed over the –40°C to 150°C operating junction temperature range, and the LTC3892MP/LTC3892MP-1/LTC3892MP-2 is tested and guaranteed over the –55°C to 150°C operating junction temperature range. High junction temperatures degrade operating lifetimes; operating lifetime is derated for junction temperatures greater than 125°C. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors. The junction temperature (T_J, in °C) is calculated from the ambient temperature (T_A, in °C) and power dissipation (P_D, in Watts) according to the formula:

$$T_J = T_A + (P_D \bullet \theta_{JA})$$

where θ_{JA} = 44°C/W for the QFN package and where θ_{JA} = 30°C/W for the TSSOP package.

Note 3: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. The maximum rated junction temperature will be exceeded when this protection is active. Continuous operation above the specified absolute maximum operating junction temperature may impair device reliability or permanently damage the device.

Note 4: The LTC3892/LTC3892-1/LTC3892-2 is tested in a feedback loop that servos $V_{ITH1,2}$ to a specified voltage and measures the resultant $V_{FB1,2}$. The specification at 85°C is not tested in production and is assured by design, characterization and correlation to production testing at other temperatures (125°C for the LTC3892E/LTC3892E-1/LTC3892E-2 and LTC3892I/LTC3892I-1/LTC3892I-2, 150°C for the LTC3892H/LTC3892H-1/LTC3892H-2 and LTC3892MP/LTC3892MP-1/LTC3892MP-2). For the LTC3892I/LTC3892I-1/LTC3892I-2 and LTC3892H/LTC3892H-1/LTC3892H-2, the specification at 0°C is not tested in production and is assured by design, characterization and correlation to production testing at –40°C. For the LTC3892MP/LTC3892MP-1/LTC3892MP-2, the specification at 0°C is not tested in production and is assured by design, characterization and correlation to production testing at –55°C.

Note 5: Dynamic supply current is higher due to the gate charge being delivered at the switching frequency. See Applications information.

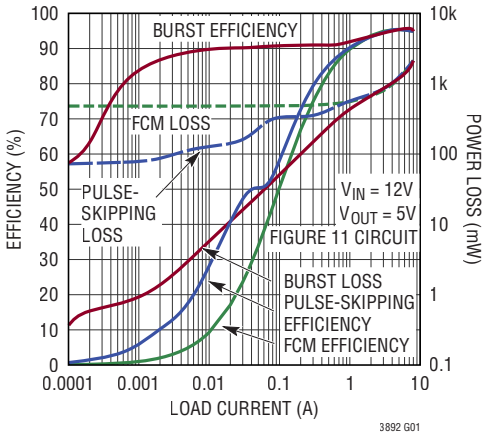
Note 6: Rise and fall times are measured using 10% and 90% levels. Delay times are measured using 50% levels

Note 7: The minimum on-time condition is specified for an inductor peak-to-peak ripple current >40% of I_{MAX} (See Minimum On-Time Considerations in the Applications Information section)

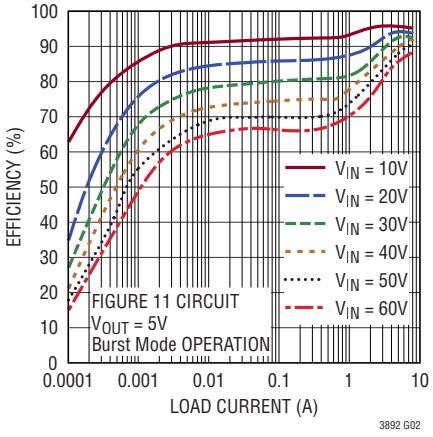
Note 8: Do not apply a voltage or current source to these pins. They must be connected to capacitive loads only, otherwise permanent damage may occur.

TYPICAL PERFORMANCE CHARACTERISTICS

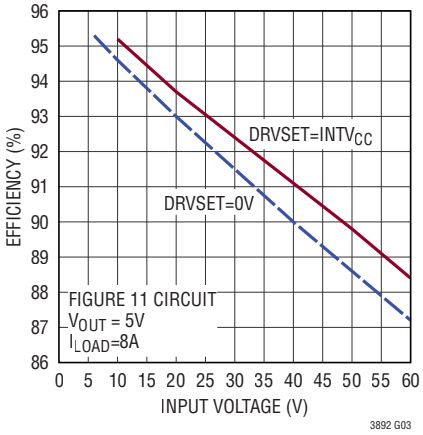
Efficiency and Power Loss vs Load Current



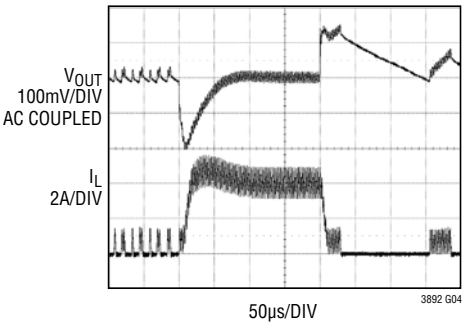
Efficiency vs Output Current



Efficiency vs Input Voltage



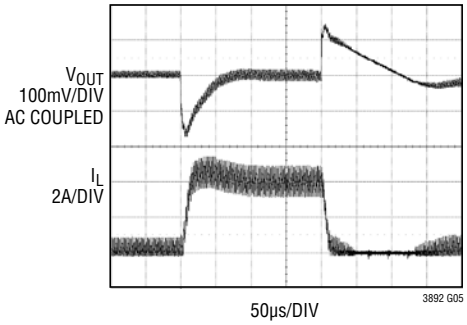
Load Step Burst Mode Operation



50µs/DIV

V_{IN} = 12V
V_{OUT} = 5V
FIGURE 13 CIRCUIT

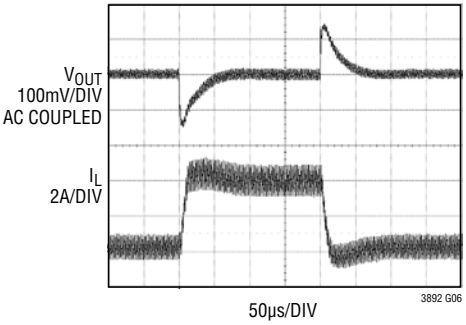
Load Step Pulse-Skipping Mode



50µs/DIV

V_{IN} = 12V
V_{OUT} = 5V
FIGURE 13 CIRCUIT

Load Step Forced Continuous Mode

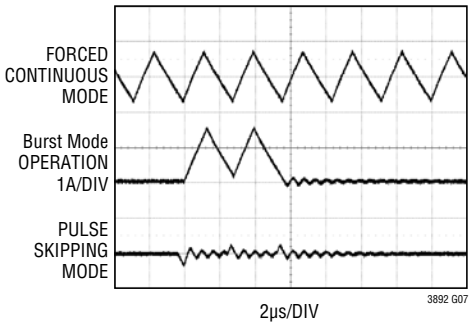


50µs/DIV

V_{IN} = 12V
V_{OUT} = 5V
FIGURE 13 CIRCUIT

TYPICAL PERFORMANCE CHARACTERISTICS

Inductor Current at Light Load



V_{IN} = 12V
V_{OUT} = 5V
I_{LOAD} = 1mA
FIGURE 13 CIRCUIT

Soft Start-Up

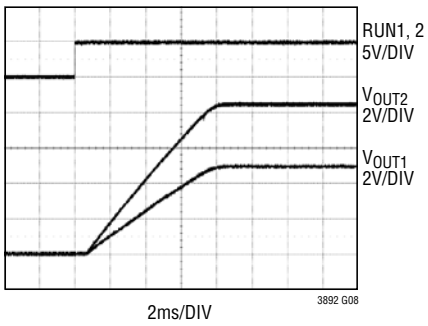
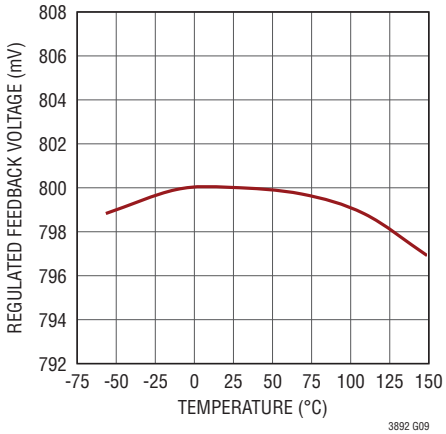
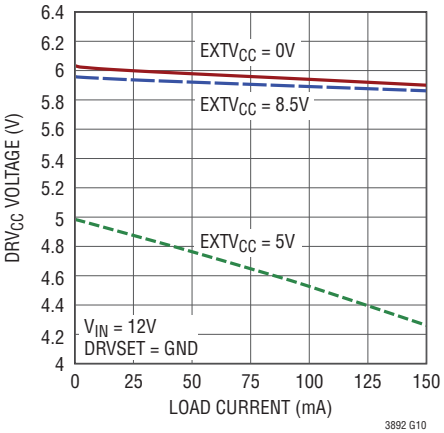


FIGURE 13 CIRCUIT

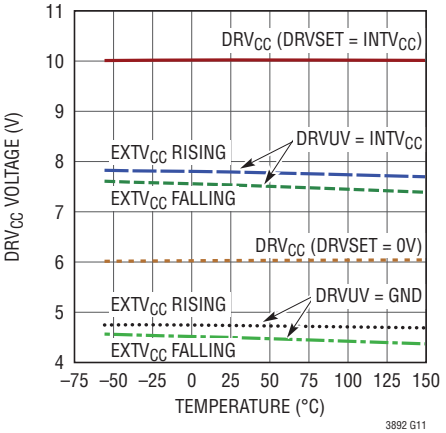
Regulated Feedback Voltage vs Temperature



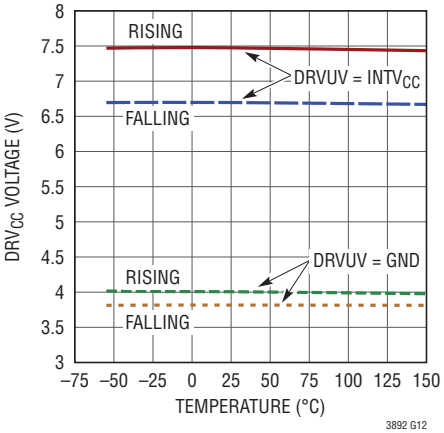
DRV_{CC} and $EXTV_{CC}$ vs Load Current



$EXTV_{CC}$ Switchover and DRV_{CC} Voltages vs Temperature

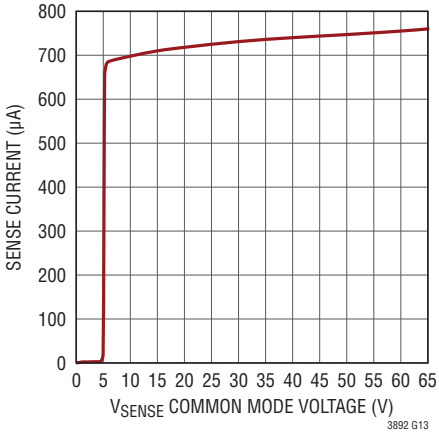


Undervoltage Lockout Threshold vs Temperature

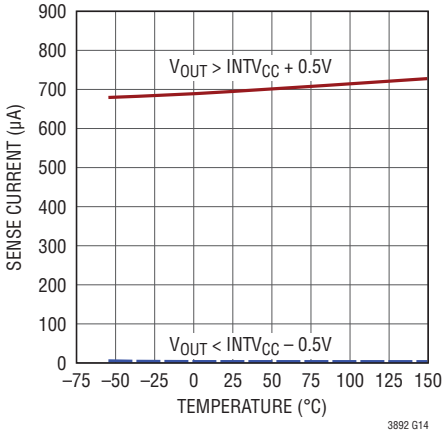


TYPICAL PERFORMANCE CHARACTERISTICS

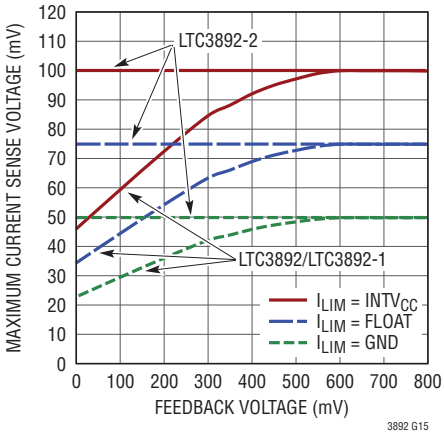
SENSE Pins Total Input Current vs V_{SENSE} Voltage



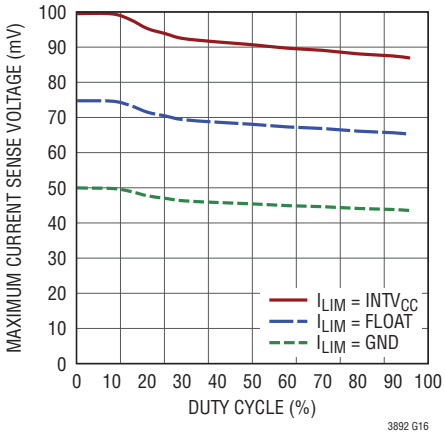
SENSE⁻ Pin Input Bias Current vs Temperature



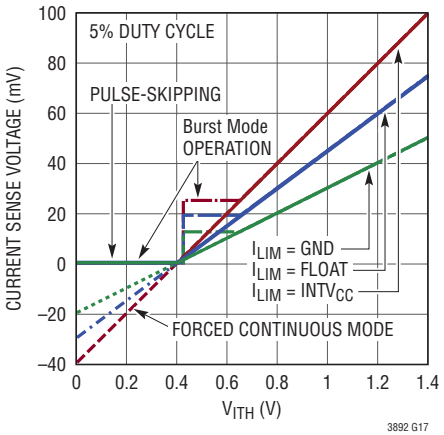
Foldback Current Limit



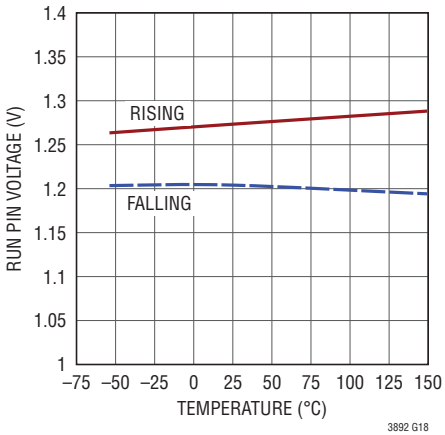
Maximum Current Sense Threshold vs Duty Cycle



Maximum Current Sense Threshold vs I_{TH} Voltage

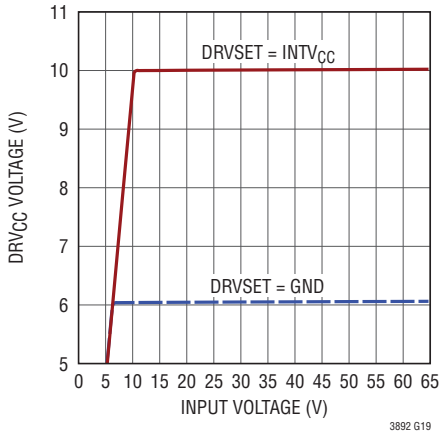


Shutdown (RUN) Threshold vs Temperature

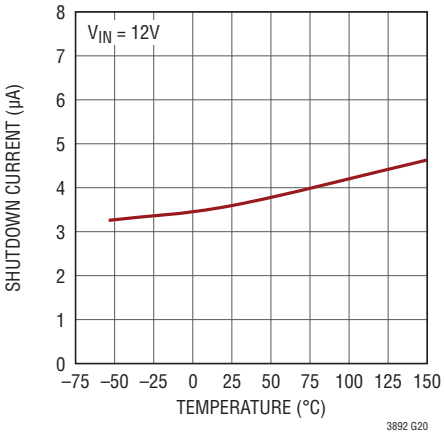


TYPICAL PERFORMANCE CHARACTERISTICS

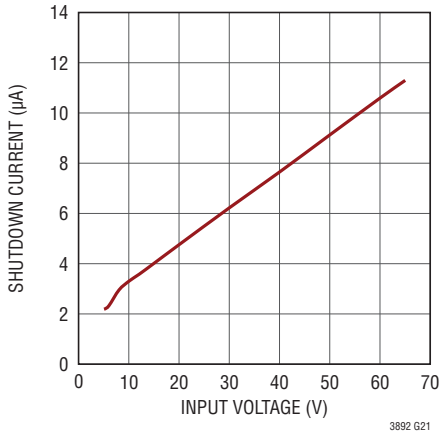
DRV_{CC} Line Regulation



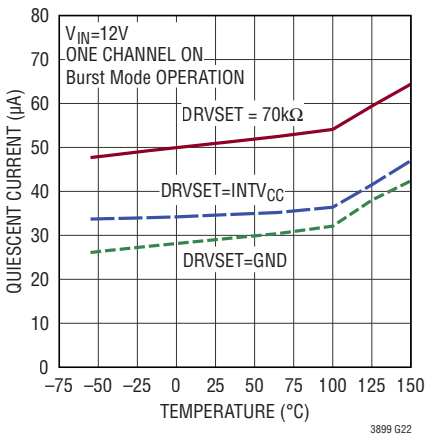
Shutdown Current vs Temperature



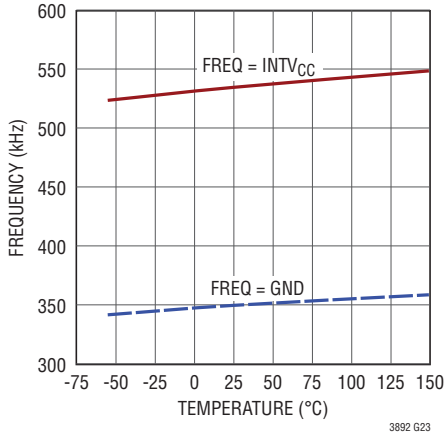
Shutdown Current vs Input Voltage



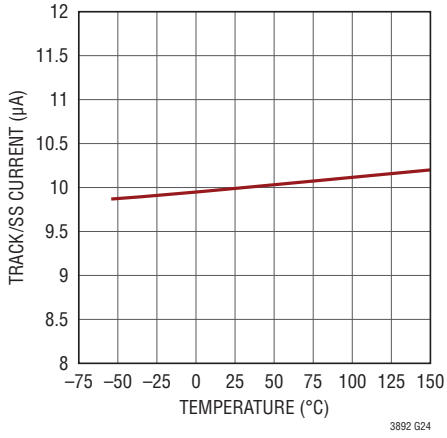
Quiescent Current vs Temperature



Oscillator Frequency vs Temperature



TRACK/SS Pull-Up Current vs Temperature



PIN FUNCTIONS (QFN (LTC3892 and LTC3892-2)/TSSOP (LTC3892-1))

FREQ (Pin 1/ Pin 5): The frequency control pin for the internal VCO. Connecting this pin to GND forces the VCO to a fixed low frequency of 350kHz. Connecting this pin to $INTV_{CC}$ forces the VCO to a fixed high frequency of 535kHz. Other frequencies between 50kHz and 900kHz can be programmed using a resistor between FREQ and GND. The resistor and an internal 20µA source current create a voltage used by the internal oscillator to set the frequency.

PLLIN/MODE (Pin 2/Pin 6): External Synchronization Input to Phase Detector and Forced Continuous Mode Input. When an external clock is applied to this pin, the phase-locked loop will force the rising TG1 signal to be synchronized with the rising edge of the external clock, and the regulators will operate in forced continuous mode on the LTC3892/LTC3892-1 and in pulse-skipping mode on the LTC3892-2. When not synchronizing to an external clock, this input, which acts on both controllers, determines how the LTC3892/LTC3892-1/LTC3892-2 operates at light loads. Pulling this pin to ground selects Burst Mode operation. An internal 100k resistor to ground also invokes Burst Mode operation when the pin is floated. Tying this pin to $INTV_{CC}$ forces continuous inductor current operation. Tying this pin to a voltage greater than 1.1V and less than $INTV_{CC}$ – 1.3V selects pulse-skipping operation. This can be done by connecting a 100k resistor from this pin to $INTV_{CC}$.

PGOOD1, PGOOD2 (Pins 3, 4/NA): Open-Drain Logic Output. PGOOD1,2 is pulled to ground when the voltage on the respective $V_{FB1,2}$ pin is not within ±10% of its set point. These pins are available on the LTC3892 and LTC3892-2, but not on the LTC3892-1.

$INTV_{CC}$ (Pin 5/Pin 7): Output of the Internal 5V Low Dropout Regulator. The low voltage analog and digital circuits are powered from this voltage source. A low ESR 0.1µF ceramic bypass capacitor should be connected between $INTV_{CC}$ and GND, as close as possible to the IC. $INTV_{CC}$ should not be used to power or bias any external circuitry other than to configure the FREQ, PLLIN/MODE, DRVSET, DRVUV and VPRG1 pins.

RUN1, RUN2 (Pins 6, 7/Pins 8, 9): Run Control Inputs for Each Controller. Forcing any of these pins below 1.2V shuts down that controller. Forcing both of these pins below 0.7V shuts down the entire LTC3892/LTC3892-1/LTC3892-2, reducing quiescent current to approximately 3.6µA.

ILIM (Pin 8/NA): Current Comparator Sense Voltage Range Input. Tying this pin to GND or $INTV_{CC}$ or floating it sets the maximum current sense threshold (for both channels) to one of three different levels (50mV, 100mV, or 75mV respectively). This pin is available on the LTC3892 and LTC3892-2, but not on the LTC3892-1. For the LTC3892-1, the maximum current sense threshold is 75mV.

V_{FB2} (Pin 11/Pin 12): This pin receives the remotely sensed feedback voltage for channel 2 from an external resistor divider across the output.

DRVUV (Pin13/Pin 14): Determines the higher or lower DRV_{CC} UVLO and $EXTV_{CC}$ switchover thresholds, as listed on the Electrical Characteristics table. Connecting DRVUV to GND chooses the lower thresholds whereas tying DRVUV to $INTV_{CC}$ chooses the higher thresholds.

DRVSET (Pin 14/Pin 15): Sets the regulated output voltage of the DRV_{CC} LDO regulator. Connecting this pin to GND sets DRV_{CC} to 6V whereas connecting it to $INTV_{CC}$ sets DRV_{CC} to 10V. Voltages between 5V and 10V can be programmed by placing a resistor (50k to 100k) between the DRVSET pin and GND.

DRV_{CC} (Pin 20/Pin 21): Output of the Internal or External Low Dropout (LDO) Regulator. The gate drivers are powered from this voltage source. The DRV_{CC} voltage is set by the DRVSET pin. Must be decoupled to ground with a minimum of 4.7µF ceramic or other low ESR capacitor. Do not use the DRV_{CC} pin for any other purpose.

$EXTV_{CC}$ (Pin 21/Pin 22): External Power Input to an Internal LDO Connected to DRV_{CC}. This LDO supplies DRV_{CC} power, bypassing the internal LDO powered from V_{IN} whenever $EXTV_{CC}$ is higher than its switchover threshold (4.7V or 7.7V depending on the DRVUV pin). See $EXTV_{CC}$ Connection in the Applications Information section. Do not float or exceed 14V on this pin. Do not connect $EXTV_{CC}$ to a voltage greater than V_{IN}. Connect to GND if not used.

V_{IN} (Pin 22/Pin 23): Main Supply Pin. A bypass capacitor should be tied between this pin and the GND pin.

BG1, BG2 (Pins 23, 19/Pins 24, 20): High Current Gate Drives for Bottom N-Channel MOSFETs. Voltage swing at these pins is from ground to DRV_{CC}.

PIN FUNCTIONS (QFN (LTC3892 and LTC3892-2)/TSSOP (LTC3892-1))

BOOST1, BOOST2 (Pins 24, 18/Pins 25, 19): Bootstrapped Supplies to the Topside Floating Drivers. Capacitors are connected between the BOOST and SW pins. Voltage swing at BOOST1 and BOOST2 pins is from approximately DRV_{CC} to ($V_{IN1,2}$ + DRV_{CC}).

SW1, SW2 (Pins 25, 17/Pins 26, 18): Switch Node Connections to Inductors.

TG1, TG2 (Pins 26, 16/Pins 27, 17): High Current Gate Drives for Top N-Channel MOSFETs. These are the outputs of floating drivers with a voltage swing equal to DRV_{CC} superimposed on the switch node voltage SW.

TRACK/SS1, TRACK/SS2 (Pins 27, 15/Pins 28, 16): External Tracking and Soft-Start Input. The LTC3892/LTC3892-1/LTC3892-2 regulates the negative input (EA^-) of the error amplifier to the smaller of 0.8V or the voltage on the TRACK/SS pin. An internal 10µA pull-up current source is connected to this pin. A capacitor to ground at this pin sets the ramp time at start-up to the final regulated output voltage. Alternatively, a resistor divider on another supply connected to the TRACK/SS pin allows the LTC3892/LTC3892-1/LTC3892-2 output voltage to track the other supply during start-up. The TRACK/SS pin is pulled low in shutdown or in undervoltage lockout.

VPRG1 (Pin 28/NA): Channel 1 Output Voltage Control Pin. This pin sets channel 1 to adjustable output mode using external feedback resistors or fixed 3.3V/5V output mode. Floating this pin allows the output to be programmed from 0.8V to 60V with an external resistor divider, regulating V_{FB1} to 0.8V. This pin is available on the LTC3892 and LTC3892-2, but not on the LTC3892-1.

ITH1, ITH2 (Pins 29, 12/Pins 1, 13): Error Amplifier Outputs and Switching Regulator Compensation Points. Each associated channel's current comparator trip point increases with this control voltage.

V_{FB1} (Pin 30/Pin 2): For the LTC3892-1, this pin receives the remotely sensed feedback voltage for channel 1 from an external resistor divider across the output.

For the LTC3892 and LTC3892-2, if the VPRG1 pin is floating, the V_{FB1} pin receives the remotely sensed feedback voltage for channel 1 from an external resistor divider across the output. If VPRG1 is tied to GND or $INTV_{CC}$, the V_{FB1} pin receives the remotely sensed output voltage directly.

$SENSE1^+$, $SENSE2^+$ (Pins 31, 10/Pins 3, 11): The (+) Input to the Differential Current Comparators. The ITH pin voltage and controlled offsets between the $SENSE^-$ and $SENSE^+$ pins in conjunction with R_{SENSE} set the current trip threshold.

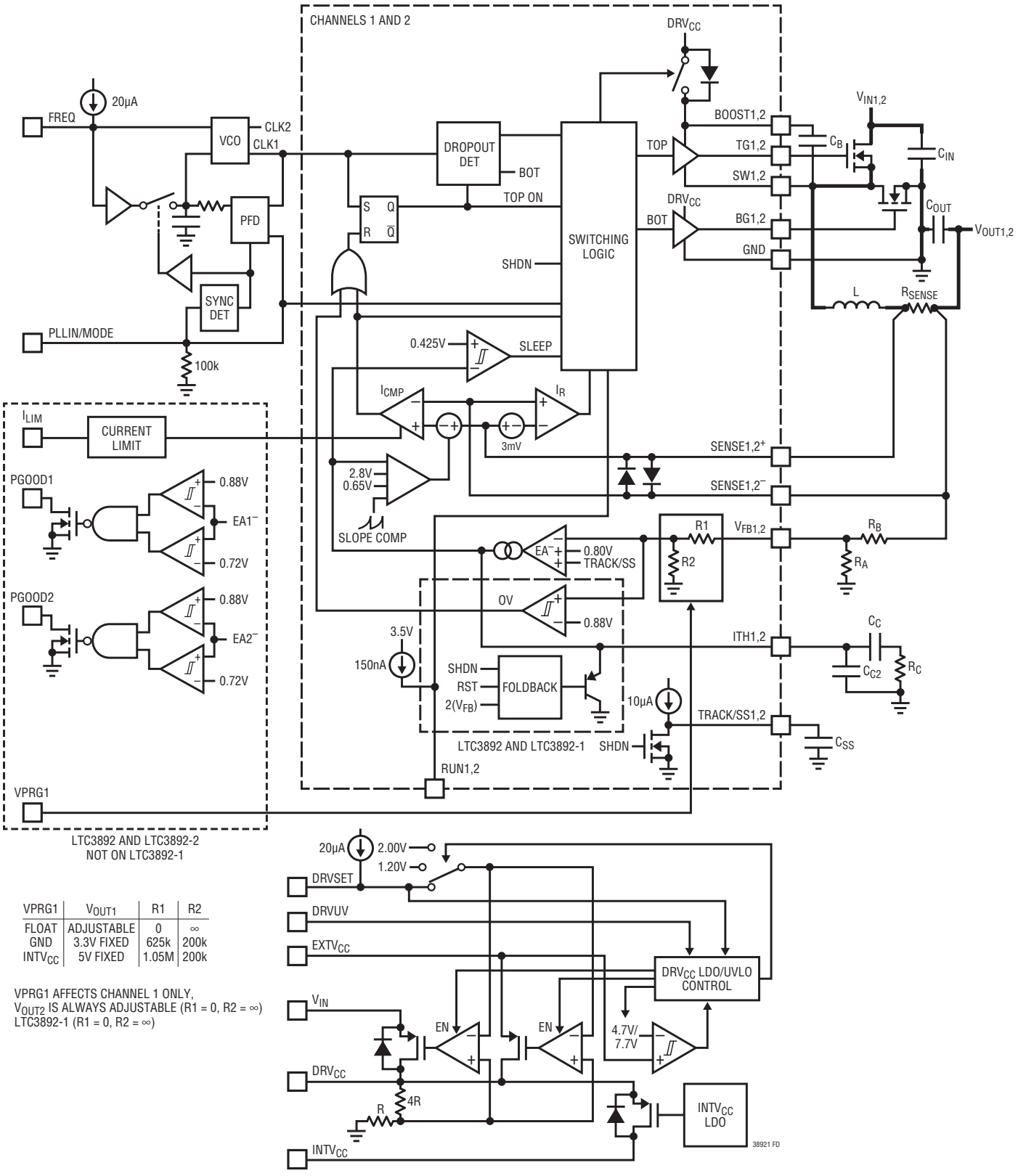
$SENSE1^-$, $SENSE2^-$ (Pins 32, 9/Pins 4, 10): The (–) Input to the Differential Current Comparators. When SENSE1,2$^-$ is greater than $INTV_{CC}$, then SENSE1,2$^-$ pin supplies current to the current comparator.

GND (Exposed Pad Pin 33/Exposed Pad Pin 29): Ground. The exposed pad must be soldered to the PCB for rated electrical and thermal performance.

Table 1. Summary of the Differences Between the LTC3892, LTC3892-1 and LTC3892-2

	LTC3892	LTC3892-1	LTC3892-2
ILIM pin for selectable current sense voltage?	Yes; 50mV, 75mV, or 100mV	**No; fixed 75mV**	Yes; 50mV, 75mV, or 100mV
VPRG1 pin for fixed or adjustable V_{OUT1}?	Yes; fixed 3.3V or 5V (with internal resistor divider) or adjustable with external resistor divider	**No; only adjustable with external resistor divider**	Yes; fixed 3.3V or 5V (with internal resistor divider) or adjustable with external resistor divider
Independent PGOOD output for each channel?	Yes; PGOOD1 and PGOOD2	**No PGOOD function**	Yes; PGOOD1 and PGOOD2
Output overvoltage protection bottom gate "crowbar?"	Yes; BG forced on	Yes; BG forced on	**No; BG not forced on**
Current foldback during overcurrent events?	Yes	Yes	No
Light load operation when synchronized to external clock using PLLIN/MODE	Forced Continuous	Forced Continuous	**Pulse-skipping (Discontinuous)**
Package	32-Pin 5mm x 5mm QFN (UH32)	**28-Lead TSSOP (FE28)**	32-Pin 5mm x 5mm QFN (UH32)

FUNCTIONAL DIAGRAMS



VPRG1	V_{OUT1}	R1	R2
FLOAT	ADJUSTABLE	0	∞
GND	3.3V FIXED	625k	200k
$INTV_{CC}$	5V FIXED	1.05M	200k

VPRG1 AFFECTS CHANNEL 1 ONLY,
V_{OUT2} IS ALWAYS ADJUSTABLE (R1 = 0, R2 = ∞)
LTC3892-1 (R1 = 0, R2 = ∞)

OPERATION (Refer to the Functional Diagrams)

Main Control Loop

The LTC3892/LTC3892-1/LTC3892-2 uses a constant frequency, current mode step-down architecture. The two controller channels operate 180° out of phase with each other. During normal operation, the external top MOSFET is turned on when the clock for that channel sets the RS latch, and is turned off when the main current comparator, I_{CMP}, resets the RS latch. The peak inductor current at which I_{CMP} trips and resets the latch is controlled by the voltage on the ITH pin, which is the output of the error amplifier, EA. The error amplifier compares the output voltage feedback signal at the V_{FB} pin (which is generated with an external resistor divider connected across the output voltage, V_{OUT}, to ground) to the internal 0.800V reference voltage. When the load current increases, it causes a slight decrease in V_{FB} relative to the reference, which causes the EA to increase the ITH voltage until the average inductor current matches the new load current.

After the top MOSFET is turned off each cycle, the bottom MOSFET is turned on until either the inductor current starts to reverse, as indicated by the current comparator I_R, or the beginning of the next clock cycle.

$DRV_{CC}/EXTV_{CC}/INTV_{CC}$ Power

Power for the top and bottom MOSFET drivers is derived from the DRV_{CC} pin. The DRV_{CC} supply voltage can be programmed from 5V to 10V through control of the DRVSET pin. When the $EXTV_{CC}$ pin is tied to a voltage below its switchover voltage (4.7V or 7.7V depending on the DRVSET voltage), the V_{IN} LDO (low dropout linear regulator) supplies power from V_{IN} to DRV_{CC}. If $EXTV_{CC}$ is taken above its switchover voltage, the V_{IN} LDO is turned off and an $EXTV_{CC}$ LDO is turned on. Once enabled, the $EXTV_{CC}$ LDO supplies power from $EXTV_{CC}$ to DRV_{CC}. Using the $EXTV_{CC}$ pin allows the DRV_{CC} power to be derived from a high efficiency external source such as one of the LTC3892/LTC3892-1/LTC3892-2 switching regulator outputs.

Each top MOSFET driver is biased from the floating bootstrap capacitor, C_B, which normally recharges during each cycle through an internal switch whenever SW goes low. If the input voltage decreases to a voltage close to its output, the loop may enter dropout and attempt to turn on the top MOSFET continuously. The dropout detector detects this and forces the top MOSFET off for about one-twelfth of the clock period every tenth cycle to allow C_B to recharge, resulting in about 99% duty cycle.

The $INTV_{CC}$ supply powers most of the other internal circuits in the LTC3892/LTC3892-1/LTC3892-2. The $INTV_{CC}$ LDO regulates to a fixed value of 5V and its power is derived from the DRV_{CC} supply.

Shutdown and Start-Up (RUN, TRACK/SS Pins)

The two channels of the LTC3892/LTC3892-1/LTC3892-2 can be independently shut down using the RUN1 and RUN2 pins. Pulling a RUN pin below 1.2V shuts down the main control loop for that channel. Pulling both pins below 0.7V disables both controllers and most internal circuits, including the DRV_{CC} and $INTV_{CC}$ LDOs. In this state, the LTC3892/LTC3892-1/LTC3892-2 draws only 3.6µA of quiescent current.

Releasing a RUN pin allows a small 150nA internal current to pull up the pin to enable that controller. Each RUN pin may be externally pulled up or driven directly by logic. Each RUN pin can tolerate up to 65V (absolute maximum), so it can be conveniently tied to V_{IN} in always-on applications where one or both controllers are enabled continuously and never shut down.

The start-up of each controller's output voltage V_{OUT} is controlled by the voltage on the TRACK/SS pin (TRACK/SS1 for channel 1, TRACK/SS2 for channel 2). When the voltage on the TRACK/SS pin is less than the 0.8V internal reference, the LTC3892/LTC3892-1/LTC3892-2 regulates the V_{FB} voltage to the TRACK/SS pin voltage instead of the 0.8V reference. This allows the TRACK/SS pin to be used to program a soft-start by connecting an external capacitor from the TRACK/SS pin to GND. An internal 10µA pull-up current charges this capacitor creating a voltage ramp on the TRACK/SS pin. As the TRACK/SS voltage rises linearly from 0V to 0.8V (and beyond up to about 4V), the output voltage V_{OUT} rises smoothly from zero to its final value.

OPERATION (Refer to the Functional Diagrams)

Alternatively the TRACK/SS pins can be used to make the start-up of V_{OUT} to track that of another supply. Typically, this requires connecting to the TRACK/SS pin an external resistor divider from the other supply to ground (see Applications Information section).

Light Load Current Operation (Burst Mode Operation, Pulse-Skipping or Forced Continuous Mode) (PLLIN/MODE Pin)

The LTC3892/LTC3892-1/LTC3892-2 can be enabled to enter high efficiency Burst Mode operation, pulse-skipping mode, or forced continuous conduction mode at low load currents. To select Burst Mode operation, tie the PLLIN/MODE pin to GND. To select forced continuous operation, tie the PLLIN/MODE pin to $INTV_{CC}$. To select pulse-skipping mode, tie the PLLIN/MODE pin to a DC voltage greater than 1.1V and less than $INTV_{CC}$ – 1.3V. This can be done by connecting a 100kΩ resistor between PLLIN/MODE and $INTV_{CC}$.

When a controller is enabled for Burst Mode operation, the minimum peak current in the inductor is set to approximately 25% of the maximum sense voltage even when the voltage on the ITH pin indicates a lower value. If the average inductor current is higher than the load current, the error amplifier, EA, will decrease the voltage on the ITH pin. When the ITH voltage drops below 0.425V, the internal sleep signal goes high (enabling sleep mode) and both external MOSFETs are turned off. The ITH pin is then disconnected from the output of the EA and parked at 0.450V.

In sleep mode, much of the internal circuitry is turned off, reducing the quiescent current that the LTC3892/LTC3892-1/LTC3892-2 draws. If one channel is in sleep mode and the other channel is shut down, the LTC3892/LTC3892-1/LTC3892-2 draws only 29µA of quiescent current (with DRVSET = 0V). If both channels are in sleep mode, it draws only 34µA of quiescent current. In sleep mode, the load current is supplied by the output capacitor. As the output voltage decreases, the EA's output begins to rise. When the output voltage drops enough, the ITH pin is reconnected to the output of the EA, the sleep signal goes low, and the controller resumes normal operation by turning on the top external MOSFET on the next cycle of the internal oscillator.

When a controller is enabled for Burst Mode operation, the inductor current is not allowed to reverse. The reverse current comparator (I_R) turns off the bottom external MOSFET just before the inductor current reaches zero, preventing it from reversing and going negative. Thus, the controller operates discontinuously.

In forced continuous operation, the inductor current is allowed to reverse at light loads or under large transient conditions. The peak inductor current is determined by the voltage on the ITH pin, just as in normal operation. In this mode, the efficiency at light loads is lower than in Burst Mode operation. However, continuous operation has the advantage of lower output voltage ripple and less interference to audio circuitry. In forced continuous mode, the output ripple is independent of load current.

When the PLLIN/MODE pin is connected for pulse-skipping mode, the LTC3892/LTC3892-1/LTC3892-2 operates in PWM pulse-skipping mode at light loads. In this mode, constant frequency operation is maintained down to approximately 1% of designed maximum output current. At very light loads, the current comparator, I_{CMP}, may remain tripped for several cycles and force the external top MOSFET to stay off for the same number of cycles (i.e., skipping pulses). The inductor current is not allowed to reverse (discontinuous operation). This mode, like forced continuous operation, exhibits low output ripple as well as low audio noise and reduced RF interference as compared to Burst Mode operation. It provides higher low current efficiency than forced continuous mode, but not nearly as high as Burst Mode operation.

When an external clock is connected to the PLLIN/MODE pin to synchronize the internal oscillator (see the Frequency Selection and Phase-Locked Loop section), the LTC3892/LTC3892-1 operate in forced continuous mode while the LTC3892-2 operates in discontinuous pulse skipping mode.

OPERATION (Refer to the Functional Diagrams)

Frequency Selection and Phase-Locked Loop (FREQ and PLLIN/MODE Pins)

The selection of switching frequency is a trade-off between efficiency and component size. Low frequency operation increases efficiency by reducing MOSFET switching losses, but requires larger inductance and/or capacitance to maintain low output ripple voltage.

The switching frequency of the LTC3892/LTC3892-1/LTC3892-2's controllers can be selected using the FREQ pin.

If the PLLIN/MODE pin is not being driven by an external clock source, the FREQ pin can be tied to GND, tied to $INTV_{CC}$ or programmed through an external resistor. Tying FREQ to GND selects 350kHz while tying FREQ to $INTV_{CC}$ selects 535kHz. Placing a resistor between FREQ and GND allows the frequency to be programmed between 50kHz and 900kHz, as shown in Figure 9.

A phase-locked loop (PLL) is available on the LTC3892/LTC3892-1/LTC3892-2 to synchronize the internal oscillator to an external clock source that is connected to the PLLIN/MODE pin. The LTC3892/LTC3892-1/LTC3892-2's phase detector adjusts the voltage (through an internal lowpass filter) of the VCO input to align the turn-on of controller 1's external top MOSFET to the rising edge of the synchronizing signal. Thus, the turn-on of controller 2's external top MOSFET is 180° out of phase to the rising edge of the external clock source.

The VCO input voltage is prebiased to the operating frequency set by the FREQ pin before the external clock is applied. If prebiased near the external clock frequency, the PLL loop only needs to make slight changes to the VCO input in order to synchronize the rising edge of the external clock's to the rising edge of TG1. The ability to prebias the loop filter allows the PLL to lock-in rapidly without deviating far from the desired frequency.

The typical capture range of the LTC3892/LTC3892-1/LTC3892-2's phase-locked loop is from approximately 55kHz to 1MHz, with a guarantee to be between 75kHz and 850kHz. In other words, the LTC3892/LTC3892-1/LTC3892-2's PLL is guaranteed to lock to an external clock source whose frequency is between 75kHz and 850kHz.

The typical input clock thresholds on the PLLIN/MODE pin are 1.6V (rising) and 1.1V (falling). It is recommended that the external clock source swing from ground (0V) to at least 2.5V.

When an external clock is connected to the PLLIN/MODE pin to synchronize the internal oscillator, the LTC3892/LTC3892-1 operate in forced continuous mode while the LTC3892-2 operates in discontinuous pulse skipping mode.

Output Overvoltage Protection (LTC3892/LTC3892-1, Not On LTC3892-2)

Each channel has an overvoltage comparator that guards against transient overshoots as well as other more serious conditions that may overvoltage the output. When the $V_{FB1,2}$ pin rises by more than 10% above its regulation point of 0.800V, the top MOSFET is turned off and the bottom MOSFET is turned on until the overvoltage condition is cleared.

Foldback Current (LTC3892/LTC3892-1, Not On LTC3892-2)

When the output voltage falls to less than 70% of its nominal level, foldback current limiting is activated, progressively lowering the peak current limit in proportion to the severity of the overcurrent or short-circuit condition. Foldback current limiting is disabled during the soft-start interval (as long as the $V_{FB1,2}$ voltage is keeping up with the TRACK/SS1,2 voltage).

Current foldback limiting is intended to limit power dissipation during overcurrent and short-circuit fault conditions. Note that while the current foldback function does not exist on the LTC3892-2 version, it is still inherently protected during these fault conditions. The LTC3892/LTC3892-1/LTC3892-2's peak current mode control architecture constantly monitors the inductor current and prevents current runaway under all conditions.

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The Typical Application on the first page is a basic LTC3892/LTC3892-1/LTC3892-2 application circuit. LTC3892/LTC3892-1/LTC3892-2 can be configured to use either DCR (inductor resistance) sensing or low value resistor sensing. The choice between the two current sensing schemes is largely a design trade-off between cost, power consumption and accuracy. DCR sensing is becoming popular because it saves expensive current sensing resistors and is more power efficient, especially in high current applications. However, current sensing resistors provide the most accurate current limits for the controller. Other external component selection is driven by the load requirement, and begins with the selection of R_{SENSE} (if R_{SENSE} is used) and inductor value. Next, the power MOSFETs and Schottky diodes are selected. Finally, input and output capacitors are selected.

SENSE+ and SENSE– Pins

The SENSE+ and SENSE– pins are the inputs to the current comparators. The common mode voltage range on these pins is 0V to 65V (absolute maximum), enabling the LTC3892/LTC3892-1/LTC3892-2 to regulate output voltages up to a nominal 60V (allowing margin for tolerances and transients). The SENSE+ pin is high impedance over the full common mode range, drawing at most ±1µA. This high impedance allows the current comparators to be used in inductor DCR sensing. The impedance of the SENSE– pin changes depending on the common mode voltage. When SENSE– is less than $INTV_{CC}$ – 0.5V, a small current of less than 1µA flows out of the pin. When SENSE– is above $INTV_{CC}$ + 0.5V, a higher current (≈700µA) flows into the pin. Between $INTV_{CC}$ – 0.5V and $INTV_{CC}$ + 0.5V, the current transitions from the smaller current to the higher current.

Filter components mutual to the sense lines should be placed close to the LTC3892/LTC3892-1/LTC3892-2, and the sense lines should run close together to a Kelvin connection underneath the current sense element (shown in Figure 1). Sensing current elsewhere can effectively add parasitic inductance and capacitance to the current sense element, degrading the information at the sense terminals and making the programmed current limit unpredictable. If DCR sensing is used (Figure 2b), resistor R1 should be placed close to the switching node, to prevent noise from coupling into sensitive small-signal nodes.

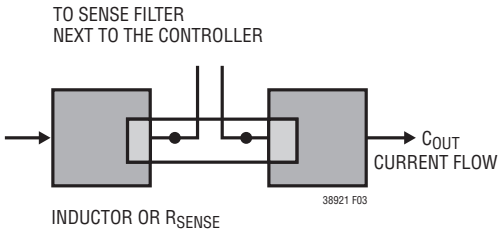

Figure 1. Sense Lines Placement with Inductor or Sense Resistor

Low Value Resistor Current Sensing

A typical sensing circuit using a discrete resistor is shown in Figure 2a. R_{SENSE} is chosen based on the required output current.

Each controller's current comparator has a maximum threshold $V_{SENSE(MAX)}$. For the LTC3892-1, $V_{SENSE(MAX)}$ is fixed at 75mV, while for the LTC3892 and LTC3892-2, $V_{SENSE(MAX)}$ is either 50mV, 75mV or 100mV, as determined by the state of the ILIM pin. The current comparator threshold voltage sets the peak of the inductor current, yielding a maximum average output current, I_{MAX}, equal to the peak value less half the peak-to-peak ripple current, ΔI_L. To calculate the sense resistor value, use the equation:

$$R_{SENSE} = \frac{V_{SENSE(MAX)}}{I_{MAX} + \frac{\Delta I_L}{2}}$$

When using a controller in very low dropout conditions, the maximum output current level will be reduced due to the internal compensation required to meet stability criteria for buck regulators operating at greater than 50% duty factor. A curve is provided in the Typical Performance Characteristics section to estimate this reduction in peak inductor current depending upon the operating duty factor.

Inductor DCR Sensing

For applications requiring the highest possible efficiency at high load currents, the LTC3892/LTC3892-1/LTC3892-2 is capable of sensing the voltage drop across the inductor DCR, as shown in Figure 2b. The DCR of the inductor represents the small amount of DC winding resistance of

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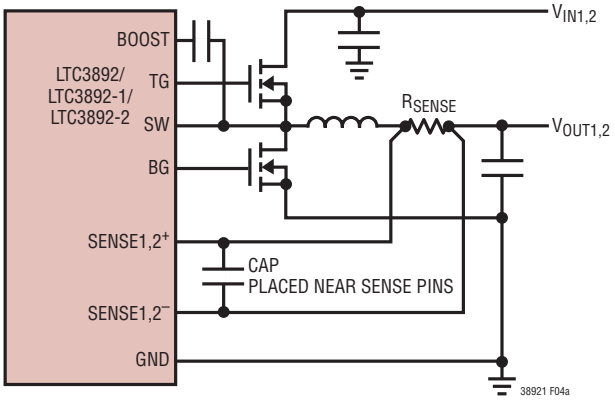
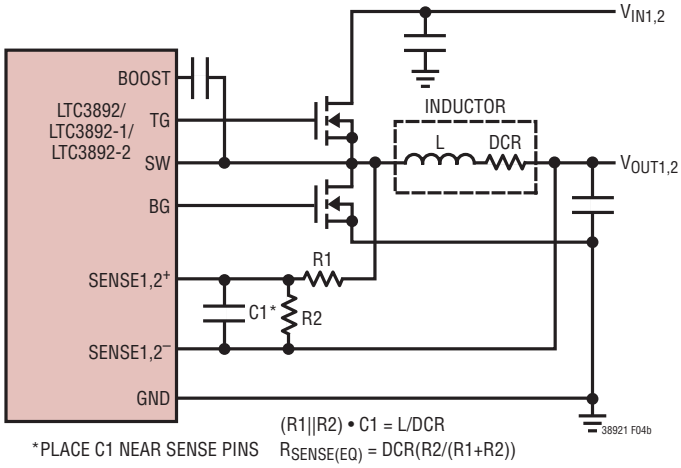


(2a) Using a Resistor to Sense Current



(2b) Using the Inductor DCR to Sense Current

Figure 2. Current Sensing Methods

the copper, which can be less than 1mΩ for today's low value, high current inductors. In a high current application requiring such an inductor, power loss through a sense resistor would cost several points of efficiency compared to inductor DCR sensing.

If the external (R1||R2) • C1 time constant is chosen to be exactly equal to the L/DCR time constant, the voltage drop across the external capacitor is equal to the drop across the inductor DCR multiplied by R2/(R1 + R2). R2 scales the voltage across the sense terminals for applications where the DCR is greater than the target sense resistor value. To properly dimension the external filter components, the DCR of the inductor must be known. It can be measured using a good RLC meter, but the DCR tolerance is not always the same and varies with temperature; consult the manufacturers' data sheets for detailed information.

Using the inductor ripple current value from the Inductor Value Calculation section, the target sense resistor value is:

$$R_{SENSE(EQUIV)} = \frac{V_{SENSE(MAX)}}{I_{MAX} + \frac{\Delta I_L}{2}}$$

To ensure that the application will deliver full load current over the full operating temperature range, choose the minimum value for $V_{SENSE(MAX)}$ in the Electrical Characteristics table.

Next, determine the DCR of the inductor. When provided, use the manufacturer's maximum value, usually given at 20°C. Increase this value to account for the temperature coefficient of copper resistance, which is approximately 0.4%/°C. A conservative value for $T_{L(MAX)}$ is 100°C.

To scale the maximum inductor DCR to the desired sense resistor value (R_D), use the divider ratio:

$$R_D = \frac{R_{SENSE(EQUIV)}}{DCR_{MAX}\ at\ T_{L(MAX)}}$$

C1 is usually selected to be in the range of 0.1µF to 0.47µF. This forces R1|| R2 to around 2k, reducing error that might have been caused by the SENSE+ pin's ±1µA current.

The equivalent resistance R1||R2 is scaled to the room temperature inductance and maximum DCR:

$$R1||R2 = \frac{L}{(DCR\ at\ 20°C) \bullet C1}$$

The sense resistor values are:

$$R1 = \frac{R1||R2}{R_D};\quad R2 = \frac{R1 \bullet R_D}{1 - R_D}$$

The maximum power loss in R1 is related to duty cycle, and will occur in continuous mode at the maximum input voltage:

$$P_{LOSS}\ R1 = \frac{\left(V_{IN(MAX)} - V_{OUT}\right) \bullet V_{OUT}}{R1}$$

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Ensure that R1 has a power rating higher than this value. If high efficiency is necessary at light loads, consider this power loss when deciding whether to use DCR sensing or sense resistors. Light load power loss can be modestly higher with a DCR network than with a sense resistor, due to the extra switching losses incurred through R1. However, DCR sensing eliminates a sense resistor, reduces conduction losses and provides higher efficiency at heavy loads. Peak efficiency is about the same with either method.

Inductor Value Calculation

The operating frequency and inductor selection are interrelated in that higher operating frequencies allow the use of smaller inductor and capacitor values. So why would anyone ever choose to operate at lower frequencies with larger components? The answer is efficiency. A higher frequency generally results in lower efficiency because of MOSFET switching and gate charge losses. In addition to this basic trade-off, the effect of inductor value on ripple current and low current operation must also be considered.

The inductor value has a direct effect on ripple current. The inductor ripple current, ΔI_L, decreases with higher inductance or higher frequency and increases with higher V_{IN}:

$$\Delta I_L = \frac{1}{(f)(L)} V_{OUT}\left(1-\frac{V_{OUT}}{V_{IN}}\right)$$

Accepting larger values of ΔI_L allows the use of low inductances, but results in higher output voltage ripple and greater core losses. A reasonable starting point for setting ripple current is $\Delta I_L = 0.3(I_{MAX})$. The maximum ΔI_L occurs at the maximum input voltage.

The inductor value also has secondary effects. The transition to Burst Mode operation begins when the average inductor current required results in a peak current below 25% of the current limit determined by R_{SENSE}. Lower inductor values (higher ΔI_L) will cause this to occur at lower load currents, which can cause a dip in efficiency in the upper range of low current operation. In Burst Mode operation, lower inductance values will cause the burst frequency to decrease.

Inductor Core Selection

Once the value for L is known, the type of inductor must be selected. Core loss is independent of core size for a fixed inductor value, but it is very dependent on inductance value selected. As inductance increases, core losses go down. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase.

Ferrite designs have very low core loss and are preferred for high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates hard, which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequent output voltage ripple. Do not allow the core to saturate!

Power MOSFET and Schottky Diode (Optional) Selection

Two external power MOSFETs must be selected for each controller in the LTC3892/LTC3892-1/LTC3892-2: one N-channel MOSFET for the top (main) switch and one N-channel MOSFET for the bottom (synchronous) switch.

The peak-to-peak drive levels are set by the DRV_{CC} voltage. This voltage can range from 5V to 10V depending on configuration of the DRVSET pin. Therefore, both logic-level and standard-level threshold MOSFETs can be used in most applications depending on the programmed DRV_{CC} voltage. Different UVLO thresholds appropriate for logic-level or standard-level threshold MOSFETs can be selected by the DRVUV pin. Pay close attention to the BV_{DSS} specification for the MOSFETs as well.

The LTC3892/LTC3892-1/LTC3892-2's unique ability to adjust the gate drive level between 5V to 10V (OPTI-DRIVE) allows an application circuit to be precisely optimized for efficiency. When adjusting the gate drive level, the final arbiter is the total input current for the regulator. If a change is made and the input current decreases, then the efficiency has improved. If there is no change in input current, then there is no change in efficiency.

Selection criteria for the power MOSFETs include the on-resistance $R_{DS(ON)}$, Miller capacitance C_{MILLER}, input

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voltage and maximum output current. Miller capacitance, C_{MILLER}, can be approximated from the gate charge curve usually provided on the MOSFET manufacturers' data sheet. C_{MILLER} is equal to the increase in gate charge along the horizontal axis while the curve is approximately flat divided by the specified change in V_{DS}. This result is then multiplied by the ratio of the application applied V_{DS} to the gate charge curve specified V_{DS}. When the IC is operating in continuous mode the duty cycles for the top and bottom MOSFETs are given by:

$$\text{Main Switch Duty Cycle} = \frac{V_{OUT}}{V_{IN}}$$

$$\text{Synchronous Switch Duty Cycle} = \frac{V_{IN} - V_{OUT}}{V_{IN}}$$

The MOSFET power dissipations at maximum output current are given by:

$$P_{MAIN} = \frac{V_{OUT}}{V_{IN}}\left(I_{OUT(MAX)}\right)^2(1+\delta)R_{DS(ON)} +$$

$$(V_{IN})^2\left(\frac{I_{OUT(MAX)}}{2}\right)(R_{DR})(C_{MILLER})\bullet$$

$$\left[\frac{1}{V_{DRVCC} - V_{THMIN}} + \frac{1}{V_{THMIN}}\right](f)$$

$$P_{SYNC} = \frac{V_{IN} - V_{OUT}}{V_{IN}}\left(I_{OUT(MAX)}\right)^2(1+\delta)R_{DS(ON)}$$

where δ is the temperature dependency of $R_{DS(ON)}$ and R_{DR} (approximately 2Ω) is the effective driver resistance at the MOSFET's Miller threshold voltage. V_{THMIN} is the typical MOSFET minimum threshold voltage.

Both MOSFETs have I^2R losses while the main N-channel equations include an additional term for transition losses, which are highest at high input voltages. For V_{IN} < 20V the high current efficiency generally improves with larger MOSFETs, while for V_{IN} > 20V the transition losses rapidly increase to the point that the use of a higher $R_{DS(ON)}$ device with lower C_{MILLER} actually provides higher efficiency. The synchronous MOSFET losses are greatest at high input voltage when the top switch duty factor is low or during a short-circuit when the synchronous switch is on close to 100% of the period.

The term (1 + δ) is generally given for a MOSFET in the form of a normalized $R_{DS(ON)}$ vs Temperature curve, but δ = 0.005/°C can be used as an approximation for low voltage MOSFETs.

Optional Schottky diodes placed across the synchronous MOSFET conduct during the dead-time between the conduction of the two power MOSFETs. This prevents the body diode of the synchronous MOSFET from turning on, storing charge during the dead-time and requiring a reverse recovery period that could cost as much as 3% in efficiency at high V_{IN}. A 1A to 3A Schottky is generally a good compromise for both regions of operation due to the relatively small average current. Larger diodes result in additional transition losses due to their larger junction capacitance.

C_{IN} and C_{OUT} Selection

The selection of C_{IN} is simplified by the 2-phase architecture and its impact on the worst-case RMS current drawn through the input network (battery/fuse/capacitor). It can be shown that the worst-case capacitor RMS current occurs when only one controller is operating. The controller with the highest $(V_{OUT})(I_{OUT})$ product needs to be used in the formula shown in Equation 1 to determine the maximum RMS capacitor current requirement. Increasing the output current drawn from the other controller will actually decrease the input RMS ripple current from its maximum value. The opt-of-phase technique typically reduces the input capacitor's RMS ripple current by a factor of 30% to 70% when compared to a single phase power supply solution.

In continuous mode, the source current of the top MOSFET is a square wave of duty cycle $(V_{OUT})/(V_{IN})$. To prevent large voltage transients, a low ESR capacitor sized for the maximum RMS current of one channel must be used. The maximum RMS capacitor current is given by:

$$C_{IN}\ \text{Required}\ I_{RMS} \approx \frac{I_{MAX}}{V_{IN}}\left[\left(V_{OUT}\right)\left(V_{IN} - V_{OUT}\right)\right]^{1/2} \quad (1)$$

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This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that capacitor manufacturers' ripple current ratings are often based on only 2000 hours of life. This makes it advisable to further derate the capacitor, or to choose a capacitor rated at a higher temperature than required. Several capacitors may be paralleled to meet size or height requirements in the design. Due to the high operating frequency of the LTC3892/LTC3892-1/LTC3892-2, ceramic capacitors can also be used for C_{IN}. Always consult the manufacturer if there is any question.

The benefit of the LTC3892/LTC3892-1/LTC3892-2 2-phase operation can be calculated by using Equation 1 for the higher power controller and then calculating the loss that would have resulted if both controller channels switched on at the same time. The total RMS power lost is lower when both controllers are operating due to the reduced overlap of current pulses required through the input capacitor's ESR. This is why the input capacitor's requirement calculated above for the worst-case controller is adequate for the dual controller design. Also, the input protection fuse resistance, battery resistance, and PC board trace resistance losses are also reduced due to the reduced peak currents in a 2-phase system. The overall benefit of a multiphase design will only be fully realized when the source impedance of the power supply/battery is included in the efficiency testing. The drains of the top MOSFETs should be placed within 1cm of each other and share a common C_{IN}(s). Separating the drains and C_{IN} may produce undesirable voltage and current resonances at V_{IN}.

A small (0.1µF to 1µF) bypass capacitor between the chip V_{IN} pin and ground, placed close to the LTC3892/LTC3892-1/LTC3892-2, is also suggested. A 2.2Ω to 10Ω resistor placed between C_{IN} (C1) and the V_{IN} pin provides further isolation, but is not required.

The selection of C_{OUT} is driven by the effective series resistance (ESR). Typically, once the ESR requirement is satisfied, the capacitance is adequate for filtering. The output ripple (ΔV_{OUT}) is approximated by:

$$\Delta V_{OUT} \approx \Delta I_L \left(ESR + \frac{1}{8 \bullet f \bullet C_{OUT}} \right)$$

where f is the operating frequency, C_{OUT} is the output capacitance and ΔI_L is the ripple current in the inductor. The output ripple is highest at maximum input voltage since ΔI_L increases with input voltage.

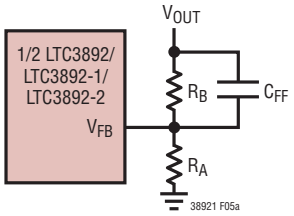
Setting Output Voltage

The LTC3892/LTC3892-1/LTC3892-2 output voltages are set by an external feedback resistor divider carefully placed across the output, as shown in Figure 3a. The regulated output voltage is determined by:

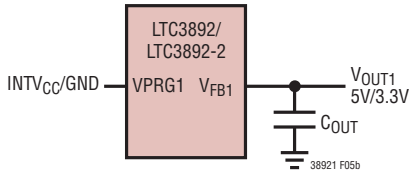
$$V_{OUT} = 0.8V \left(1 + \frac{R_B}{R_A} \right)$$

To improve the frequency response, a feedforward capacitor, C_{FF}, may be used. Great care should be taken to route the V_{FB} line away from noise sources, such as the inductor or the SW line.

For the LTC3892 and LTC3892-2, channel 1 has the option to be programmed to a fixed 5V or 3.3V output through control of the VPRG1 pin (not available on the LTC3892-1). Figure 3b shows how the V_{FB1} pin is used to sense the output voltage in fixed output mode. Tying VPRG1 to $INTV_{CC}$ or GND programs V_{OUT1} to 5V or 3.3V, respectively. Floating VPRG1 sets V_{OUT1} to adjustable output mode using external resistors.



(3a) Setting Adjustable Output Voltage



(3b) Setting CH1 (LTC3892) to Fixed 5V/3.3V Voltage

Figure 3. Setting Buck Output Voltage

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RUN Pins

The LTC3892/LTC3892-1/LTC3892-2 is enabled using the RUN1 and RUN2 pins. The RUN pins have a rising threshold of 1.275V with 75mV of hysteresis. Pulling a RUN pin below 1.2V shuts down the main control loop for that channel. Pulling both RUN pins below 0.7V disables the controllers and most internal circuits, including the DRV_{CC} and $INTV_{CC}$ LDOs. In this state, the LTC3892/LTC3892-1/LTC3892-2 draws only 3.6µA of quiescent current.

Releasing a RUN pin allows a small 150nA internal current to pull up the pin to enable that controller. Because of condensation or other small board leakage pulling the pin down, it is recommended the RUN pins be externally pulled up or driven directly by logic. Each RUN pin can tolerate up to 65V (absolute maximum), so it can be conveniently tied to V_{IN} in always-on applications where one or more controllers are enabled continuously and never shut down.

The RUN pins can be implemented as a UVLO by connecting them to the output of an external resistor divider network off V_{IN}, as shown in Figure 4.

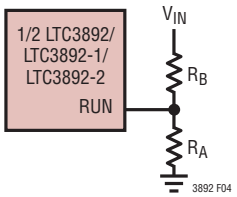

Figure 4. Using the RUN Pins as a UVLO

The rising and falling UVLO thresholds are calculated using the RUN pin thresholds and pull-up current:

$$V_{UVLO(RISING)} = 1.275V\left(1+\frac{R_B}{R_A}\right) - 150nA \bullet R_B$$

$$V_{UVLO(FALLING)} = 1.20V\left(1+\frac{R_B}{R_A}\right) - 150nA \bullet R_B$$

Tracking and Soft-Start (TRACK/SS1, TRACK/SS2 Pins)

The start-up of each V_{OUT} is controlled by the voltage on the TRACK/SS pin (TRACK/SS1 for channel 1, TRACK/SS2 for channel 2). When the voltage on the TRACK/SS pin is less than the internal 0.8V reference, the LTC3892/LTC3892-1/LTC3892-2 regulates the V_{FB} pin voltage to the voltage on the TRACK/SS pin instead of the internal reference. The TRACK/SS pin can be used to program an external soft-start function or to allow V_{OUT} to track another supply during start-up.

Soft-start is enabled by simply connecting a capacitor from the TRACK/SS pin to ground, as shown in Figure 5. An internal 10µA current source charges the capacitor, providing a linear ramping voltage at the TRACK/SS pin. The LTC3892/LTC3892-1/LTC3892-2 will regulate its feedback voltage (and hence V_{OUT}) according to the voltage on the TRACK/SS pin, allowing V_{OUT} to rise smoothly from 0V to its final regulated value. The total soft-start time will be approximately:

$$t_{SS} = C_{SS} \bullet \frac{0.8V}{10\mu A}$$

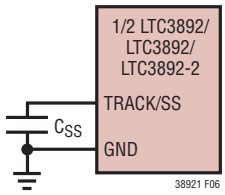

Figure 5. Using the TRACK/SS Pin to Program Soft-Start

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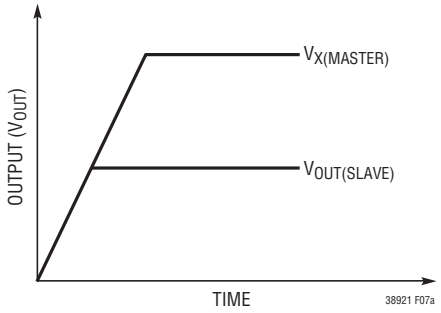
Alternatively, the TRACK/SS1 and TRACK/SS2 pins can be used to track two (or more) supplies during start-up, as shown qualitatively in Figures 6a and 6b. To do this, a resistor divider should be connected from the master supply (V_X) to the TRACK/SS pin of the slave supply (V_{OUT}), as shown in Figure 7. During start-up V_{OUT} will track V_X according to the ratio set by the resistor divider:

$$\frac{V_X}{V_{OUT}} = \frac{R_A}{R_{TRACKA}} \bullet \frac{R_{TRACKA} + R_{TRACKB}}{R_A + R_B}$$

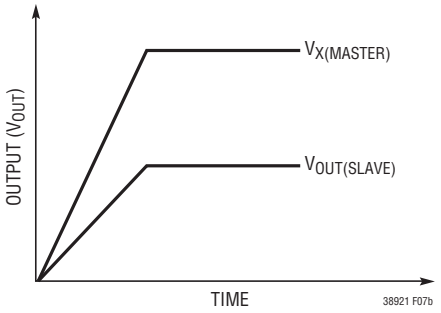
For coincident tracking ($V_{OUT} = V_X$ during start-up),

$R_A = R_{TRACKA}$

$R_B = R_{TRACKB}$



(6a) Coincident Tracking



(6b) Ratiometric Tracking

Figure 6. Two Different Modes of Output Voltage Tracking

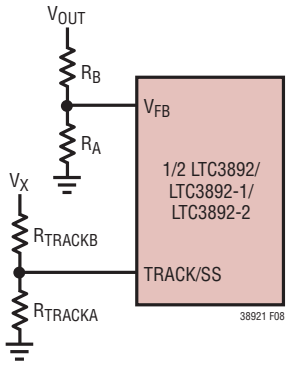


Figure 7. Using the TRACK/SS Pin for Tracking

DRV_{CC} and $INTV_{CC}$ Regulators and $EXTV_{CC}$ (OPTI-DRIVE)

The LTC3892/LTC3892-1/LTC3892-2 features two separate internal P-channel low dropout linear regulators (LDO) that supply power at the DRV_{CC} pin from either the V_{IN} supply pin or the $EXTV_{CC}$ pin depending on the connections of the $EXTV_{CC}$, DRVSET, and DRVUV pins. A third P-channel LDO supplies power at the $INTV_{CC}$ pin from the DRV_{CC} pin. DRV_{CC} powers the gate drivers whereas $INTV_{CC}$ powers much of the LTC3892/LTC3892-1/LTC3892-2's internal circuitry. The V_{IN} LDO and the $EXTV_{CC}$ LDO regulate DRV_{CC} between 5V to 10V, depending on how the DRVSET pin is set. Each of these LDOs can supply a peak current of at least 50mA and must be bypassed to ground with a minimum of 4.7µF ceramic capacitor. Good bypassing is needed to supply the high transient currents required by the MOSFET gate drivers and to prevent interaction between the channels. The $INTV_{CC}$ supply must be bypassed with a 0.1µF ceramic capacitor.

The DRVSET pin programs the DRV_{CC} supply voltage and the DRVUV pin selects different DRV_{CC} UVLO and $EXTV_{CC}$ switchover threshold voltages. Table 2a summarizes the different DRVSET pin configurations along with the voltage settings that go with each configuration. Table 2b summarizes the different DRVUV pin settings. Tying the

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DRVSET pin to $INTV_{CC}$ programs DRV_{CC} to 10V. Tying the DRVSET pin to GND programs DRV_{CC} to 6V. By placing a 50k to 100k resistor between DRVSET and GND the DRV_{CC} voltage can be programmed between 5V to 10V, as shown in Figure 8.

Table 2a

DRVSET PIN	DRV_{CC} VOLTAGE
GND	6V
$INTV_{CC}$	10V
Resistor to GND 50k to 100k	5V to 10V

Table 2b

DRVUV PIN	DRV_{CC} UVLO RISING / FALLING THRESHOLDS	$EXTV_{CC}$ SWITCHOVER RISING / FALLING THRESHOLD
GND	4.0V / 3.8V	4.7V / 4.45V
$INTV_{CC}$	7.5V / 6.7V	7.7V / 7.45V

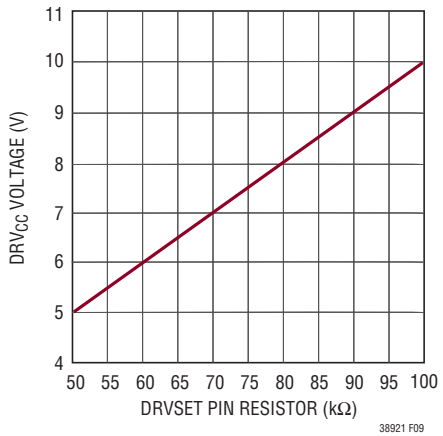

Figure 8. Relationship Between DRV_{CC} Voltage and Resistor Value at DRVSET Pin

High input voltage applications in which large MOSFETs are being driven at high frequencies may cause the maximum junction temperature rating for the LTC3892/LTC3892-1/LTC3892-2 to be exceeded. The DRV_{CC} current, which is dominated by the gate charge current, may be supplied by either the V_{IN} LDO or the $EXTV_{CC}$ LDO. When the voltage on the $EXTV_{CC}$ pin is less than its switchover threshold (4.7V or 7.7V as determined by the DRVUV pin described above), the V_{IN} LDO is enabled. Power dissipation for the IC in this case is highest and is equal to $V_{IN} \bullet I_{DRVCC}$. The gate charge current is dependent on operating frequency as discussed in the Efficiency Considerations section. The junction temperature can be estimated by using the equations given in Note 2 of the Electrical Characteristics. For example, using the LTC3892 in the QFN package, the DRV_{CC} current is limited to less than 31mA from a 40V supply when not using the $EXTV_{CC}$ supply at a 70°C ambient temperature:

$$T_J = 70°C + (31mA)(40V)(44°C/W) = 125°C$$

To prevent the maximum junction temperature from being exceeded, the V_{IN} supply current must be checked while operating in forced continuous mode (PLLIN/MODE = $INTV_{CC}$) at maximum V_{IN}.

When the voltage applied to $EXTV_{CC}$ rises above its switchover threshold, the V_{IN} LDO is turned off and the $EXTV_{CC}$ LDO is enabled. The $EXTV_{CC}$ LDO remains on as long as the voltage applied to $EXTV_{CC}$ remains above the switchover threshold minus the comparator hysteresis. The $EXTV_{CC}$ LDO attempts to regulate the DRV_{CC} voltage to the voltage as programmed by the DRVSET pin, so while $EXTV_{CC}$ is less than this voltage, the LDO is in dropout and the DRV_{CC} voltage is approximately equal to $EXTV_{CC}$. When $EXTV_{CC}$ is greater than the programmed voltage, up to an absolute maximum of 14V, DRV_{CC} is regulated to the programmed voltage.

Using the $EXTV_{CC}$ LDO allows the MOSFET driver and control power to be derived from one of the LTC3892/LTC3892-1/LTC3892-2's switching regulator outputs ($4.7V/7.7V \le V_{OUT} \le 14V$) during normal operation and from the V_{IN} LDO when the output is out of regulation (e.g., start-up, short circuit). If more current is required through the $EXTV_{CC}$ LDO than is specified, an external Schottky diode can be added between the $EXTV_{CC}$ and DRV_{CC} pins. In this case, do not apply more than 10V to the $EXTV_{CC}$ pin and make sure that $EXTV_{CC} \le V_{IN}$.

Significant efficiency and thermal gains can be realized by powering DRV_{CC} from the output, since the V_{IN} current resulting from the driver and control currents will be scaled by a factor of (Duty Cycle)/(Switcher Efficiency).

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For 5V to 14V regulator outputs, this means connecting the $EXTV_{CC}$ pin directly to V_{OUT}. Tying the $EXTV_{CC}$ pin to an 8.5V supply reduces the junction temperature in the previous example from 125°C to:

$$T_J = 70°C + (31mA)(8.5V)(44°C/W) = 82°C$$

However, for 3.3V and other low voltage outputs, additional circuitry is required to derive DRV_{CC} power from the output.

The following list summarizes the four possible connections for $EXTV_{CC}$:

1. $EXTV_{CC}$ grounded. This will cause DRV_{CC} to be powered from the internal V_{IN} regulator resulting in increased power dissipation in the LTC3892/LTC3892-1/LTC3892-2 at high input voltages.
2. $EXTV_{CC}$ connected directly to V_{OUT}. This is the normal connection for a 5V to 14V regulator and provides the highest efficiency.
3. $EXTV_{CC}$ connected to an external supply. If an external supply is available in the 5V to 14V range, it may be used to power $EXTV_{CC}$ providing it is compatible with the MOSFET gate drive requirements. Ensure that $EXTV_{CC} < V_{IN}$.
4. $EXTV_{CC}$ connected to an output-derived boost network. For 3.3V and other low voltage regulators, efficiency gains can still be realized by connecting $EXTV_{CC}$ to an output-derived voltage that has been boosted to greater than 4.7V/7.7V.

Topside MOSFET Driver Supply (C_B)

External bootstrap capacitors, C_B, connected to the BOOST pins supply the gate drive voltage for the topside MOSFET. The LTC3892/LTC3892-1/LTC3892-2 features an internal switch between DRV_{CC} and the BOOST pin for each controller. These internal switches eliminate the need for external bootstrap diodes between DRV_{CC} and BOOST. Capacitor C_B in the Functional Diagram is charged through this internal switch from DRV_{CC} when the SW pin is low. When the topside MOSFET is to be turned on, the driver places the C_B voltage across the gate-source of the MOSFET. This enhances the top MOSFET switch and turns it on. The switch node voltage, SW, rises to V_{IN} and the BOOST pin follows. With the topside MOSFET on, the boost voltage is above the input supply: $V_{BOOST} = V_{IN} + V_{DRVCC}$. The value of the boost capacitor, C_B, needs to be 100 times that of the total input capacitance of the topside MOSFET(s).

Fault Conditions: Current Limit and Current Foldback

The LTC3892/LTC3892-1 (not the LTC3892-2) includes current foldback to help limit load current when an output is shorted to ground. If the output voltage falls below 70% of its nominal output level, then the maximum sense voltage is progressively lowered from 100% to 40% of its maximum selected value.

Under short-circuit conditions with very low duty cycles, the channel will begin cycle skipping in order to limit the short-circuit current. In this situation the bottom MOSFET will be dissipating most of the power but less than in normal operation. The short-circuit ripple current is determined by the minimum on-time, $t_{ON(MIN)}$, of the LTC3892/LTC3892-1/LTC3892-2 (≈80ns), the input voltage and inductor value:

$$\Delta I_{L(SC)} = t_{ON(MIN)} \left(\frac{V_{IN}}{L} \right)$$

The resulting average short-circuit current is:

$$I_{SC} = 40\% \bullet I_{LIM(MAX)} - \frac{1}{2} \Delta I_{L(SC)} \quad \text{(LTC3892/LTC3892-1)}$$

$$I_{SC} = I_{LIM(MAX)} - \frac{1}{2} \Delta I_{L(SC)} \quad \text{(LTC3892-2)}$$

Fault Conditions: Overvoltage Protection (Crowbar) (LTC3892/LTC3892-1; not on LTC3892-2)

The overvoltage crowbar is designed to blow a system input fuse when the output voltage of the regulator rises much higher than nominal levels. The crowbar causes huge currents to flow, that blow the fuse to protect against a shorted top MOSFET if the short occurs while the controller is operating.

A comparator monitors the output for overvoltage conditions. The comparator detects faults greater than 10%

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above the nominal output voltage. When this condition is sensed, the top MOSFET is turned off and the bottom MOSFET is turned on until the overvoltage condition is cleared. The bottom MOSFET remains on continuously for as long as the overvoltage condition persists; if V_{OUT} returns to a safe level, normal operation automatically resumes.

A shorted top MOSFET will result in a high current condition which will open the system fuse. The switching regulator will regulate properly with a leaky top MOSFET by altering the duty cycle to accommodate the leakage.

Fault Conditions: Overtemperature Protection

At higher temperatures, or in cases where the internal power dissipation causes excessive self heating on chip (such as DRV_{CC} short to ground), the overtemperature shutdown circuitry will shut down the LTC3892/LTC3892-1/LTC3892-2. When the junction temperature exceeds approximately 175°C, the overtemperature circuitry disables the DRV_{CC} LDO, causing the DRV_{CC} supply to collapse and effectively shutting down the entire LTC3892/LTC3892-1/LTC3892-2 chip. Once the junction temperature drops back to the approximately 155°C, the DRV_{CC} LDO turns back on. Long-term overstress (T_J > 125°C) should be avoided as it can degrade the performance or shorten the life of the part.

Phase-Locked Loop and Frequency Synchronization

The LTC3892/LTC3892-1/LTC3892-2 has an internal phase-locked loop (PLL) comprised of a phase frequency detector, a lowpass filter, and a voltage-controlled oscillator (VCO). This allows the turn-on of the top MOSFET of controller 1 to be locked to the rising edge of an external clock signal applied to the PLLIN/MODE pin. The turn-on of controller 2's top MOSFET is thus 180° out of phase with the external clock. The phase detector is an edge sensitive digital type that provides zero degrees phase shift between the external and internal oscillators. This type of phase detector does not exhibit false lock to harmonics of the external clock.

If the external clock frequency is greater than the internal oscillator's frequency, f_{OSC}, then current is sourced continuously from the phase detector output, pulling up the VCO input. When the external clock frequency is less than f_{OSC}, current is sunk continuously, pulling down the VCO input.

If the external and internal frequencies are the same but exhibit a phase difference, the current sources turn on for an amount of time corresponding to the phase difference. The voltage at the VCO input is adjusted until the phase and frequency of the internal and external oscillators are identical. At the stable operating point, the phase detector output is high impedance and the internal filter capacitor, CLP, holds the voltage at the VCO input.

Note that the LTC3892/LTC3892-1/LTC3892-2 can only be synchronized to an external clock whose frequency is within range of the LTC3892/LTC3892-1/LTC3892-2's internal VCO, which is nominally 55kHz to 1MHz. This is guaranteed to be between 75kHz and 850kHz. Typically, the external clock (on the PLLIN/MODE pin) input high threshold is 1.6V, while the input low threshold is 1.1V. The LTC3892/LTC3892-1/LTC3892-2 is guaranteed to synchronize to an external clock that swings up to at least 2.5V and down to 0.5V or less.

Rapid phase locking can be achieved by using the FREQ pin to set a free-running frequency near the desired synchronization frequency. The VCO's input voltage is prebiased at a frequency corresponding to the frequency set by the FREQ pin. Once prebiased, the PLL only needs to adjust the frequency slightly to achieve phase lock and synchronization. Although it is not required that the free-running frequency be near the external clock frequency, doing so will prevent the operating frequency from passing through a large range of frequencies as the PLL locks.

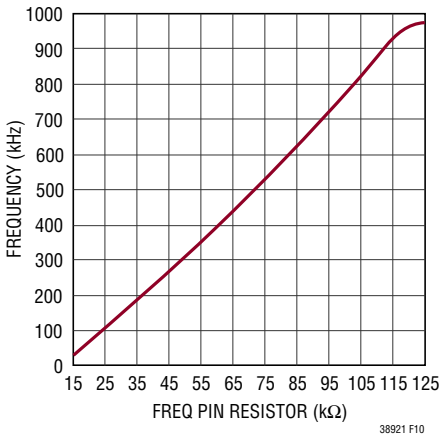

Figure 9. Relationship Between Oscillator Frequency and Resistor Value at the FREQ Pin

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Table 3 summarizes the different states in which the FREQ pin can be used. When synchronized to an external clock, the LTC3892/LTC3892-1/LTC3892-2 operates in forced continuous mode at light loads.

Table 3

FREQ PIN	PLLIN/MODE PIN	FREQUENCY
0V	DC Voltage	350kHz
$INTV_{CC}$	DC Voltage	535kHz
Resistor to GND	DC Voltage	50kHz to 900kHz
Any of the Above	External Clock 75kHz to 850kHz	Phase Locked to External Clock

Minimum On-Time Considerations

Minimum on-time, $t_{ON(MIN)}$, is the smallest time duration that the LTC3892/LTC3892-1/LTC3892-2 is capable of turning on the top MOSFET. It is determined by internal timing delays and the gate charge required to turn on the top MOSFET. Low duty cycle applications may approach this minimum on-time limit and care should be taken to ensure that:

$$t_{ON(MIN)} < \frac{V_{OUT}}{V_{IN}(f)}$$

If the duty cycle falls below what can be accommodated by the minimum on-time, the controller will begin to skip cycles. The output voltage will continue to be regulated, but the ripple voltage and current will increase.

The minimum on-time for the LTC3892/LTC3892-1/LTC3892-2 is approximately 80ns. However, as the peak sense voltage decreases, the minimum on-time gradually increases up to about 130ns. This is of particular concern in forced continuous applications with low ripple current at light loads. If the duty cycle drops below the minimum on-time limit in this situation, a significant amount of cycle skipping can occur with correspondingly larger current and voltage ripple.

Efficiency Considerations

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Percent efficiency can be expressed as:

%Efficiency = 100% – (L1 + L2 + L3 + ...)

where L1, L2, etc. are the individual losses as a percentage of input power.

Although all dissipative elements in the circuit produce losses, four main sources usually account for most of the losses in LTC3892/LTC3892-1/LTC3892-2 circuits: 1) IC V_{IN} current, 2) DRV_{CC} regulator current, 3) I^2R losses, 4) Topside MOSFET transition losses.

1. The V_{IN} current is the DC supply current given in the Electrical Characteristics table, which excludes MOSFET driver and control currents. V_{IN} current typically results in a small (<0.1%) loss.

2. DRV_{CC} current is the sum of the MOSFET driver and control currents. The MOSFET driver current results from switching the gate capacitance of the power MOSFETs. Each time a MOSFET gate is switched from low to high to low again, a packet of charge, dQ, moves from DRV_{CC} to ground. The resulting dQ/dt is a current out of DRV_{CC} that is typically much larger than the control circuit current. In continuous mode, $I_{GATECHG} = f(Q_T + Q_B)$, where Q_T and Q_B are the gate charges of the topside and bottom side MOSFETs.

   Supplying DRV_{CC} from an output-derived source power through $EXTV_{CC}$ will scale the V_{IN} current required for the driver and control circuits by a factor of (Duty Cycle)/(Efficiency). For example, in a 20V to 5V application, 10mA of DRV_{CC} current results in approximately 2.5mA of V_{IN} current. This reduces the midcurrent loss from 10% or more (if the driver was powered directly from V_{IN}) to only a few percent.

3. I^2R losses are predicted from the DC resistances of the fuse (if used), MOSFET, inductor, current sense resistor and input and output capacitor ESR. In continuous mode the average output current flows through L and R_{SENSE}, but is chopped between the topside MOSFET and the synchronous MOSFET. If the two MOSFETs have approximately the same $R_{DS(ON)}$, then the resistance of one MOSFET can simply be summed with the resistances of L, R_{SENSE} and ESR to obtain I^2R losses.

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For example, if each $R_{DS(ON)}$ = 30mΩ, R_L = 50mΩ, R_{SENSE} = 10mΩ and R_{ESR} = 40mΩ (sum of both input and output capacitance losses), then the total resistance is 130mΩ. This results in losses ranging from 3% to 13% as the output current increases from 1A to 5A for a 5V output, or a 4% to 20% loss for a 3.3V output. Efficiency varies as the inverse square of V_{OUT} for the same external components and output power level. The combined effects of increasingly lower output voltages and higher currents required by high performance digital systems is not doubling but quadrupling the importance of loss terms in the switching regulator system!

4. Transition losses apply only to the top MOSFET(s), and become significant only when operating at high input voltages (typically 20V or greater). Transition losses can be estimated from:

$$\text{Transition Loss} = (1.7) \bullet V_{IN}^2 \bullet I_{O(MAX)} \bullet C_{RSS} \bullet f$$

Other hidden losses such as copper trace and internal battery resistances can account for an additional 5% to 10% efficiency degradation in portable systems. It is very important to include these system level losses during the design phase. The internal battery and fuse resistance losses can be minimized by making sure that C_{IN} has adequate charge storage and very low ESR at the switching frequency. A 25W supply will typically require a minimum of 20µF to 40µF of capacitance having a maximum of 20mΩ to 50mΩ of ESR. Other losses including Schottky conduction losses during dead-time and inductor core losses generally account for less than 2% total additional loss.

Checking Transient Response

The regulator loop response can be checked by looking at the load current transient response. Switching regulators take several cycles to respond to a step in DC (resistive) load current. When a load step occurs, V_{OUT} shifts by an amount equal to $\Delta I_{LOAD(ESR)}$, where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT} generating the feedback error signal that forces the regulator to adapt to the current change and return V_{OUT} to its steady-state value. During this recovery time V_{OUT} can be monitored for excessive overshoot or ringing, which would indicate a stability problem. OPTI-LOOP compensation allows the transient response to be optimized over a wide range of output capacitance and ESR values. The availability of the ITH pin not only allows optimization of control loop behavior, but it also provides a DC-coupled and AC-filtered closed-loop response test point. The DC step, rise time and settling at this test point truly reflects the closed-loop response. Assuming a predominantly second order system, phase margin and/or damping factor can be estimated using the percentage of overshoot seen at this pin. The bandwidth can also be estimated by examining the rise time at the pin. The ITH external components shown in Figure 12 circuit will provide an adequate starting point for most applications.

The ITH series R_C-C_C filter sets the dominant pole-zero loop compensation. The values can be modified slightly to optimize transient response once the final PC layout is done and the particular output capacitor type and value have been determined. The output capacitors need to be selected because the various types and values determine the loop gain and phase. An output current pulse of 20% to 80% of full-load current having a rise time of 1µs to 10µs will produce output voltage and ITH pin waveforms that will give a sense of the overall loop stability without breaking the feedback loop.

Placing a power MOSFET directly across the output capacitor and driving the gate with an appropriate signal generator is a practical way to produce a realistic load step condition. The initial output voltage step resulting from the step change in output current may not be within the bandwidth of the feedback loop, so this signal cannot be used to determine phase margin. This is why it is better to look at the ITH pin signal which is in the feedback loop and is the filtered and compensated control loop response.

The gain of the loop will be increased by increasing R_C and the bandwidth of the loop will be increased by decreasing C_C. If R_C is increased by the same factor that C_C is decreased, the zero frequency will be kept the same, thereby keeping the phase shift the same in the most critical frequency range of the feedback loop. The output voltage settling behavior is related to the stability of the closed-loop system and will demonstrate the actual overall supply performance.

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A second, more severe transient is caused by switching in loads with large (>1µF) supply bypass capacitors. The discharged bypass capacitors are effectively put in parallel with C_{OUT}, causing a rapid drop in V_{OUT}. No regulator can alter its delivery of current quickly enough to prevent this sudden step change in output voltage if the load switch resistance is low and it is driven quickly. If the ratio of C_{LOAD} to C_{OUT} is greater than 1:50, the switch rise-time should be controlled so that the load rise-time is limited to approximately 25 • C_{LOAD}. Thus a 10µF capacitor would require a 250µs rise time, limiting the charging current to about 200mA.

Design Example

As a design example for one channel, assume V_{IN} = 12V (nominal), V_{IN} = 22V (maximum), V_{OUT} = 3.3V, I_{MAX} = 5A, $V_{SENSE(MAX)}$ = 75mV and f = 350kHz. The inductance value is chosen first based on a 30% ripple current assumption. The highest value of ripple current occurs at the maximum input voltage. Tie the FREQ pin to GND, generating 350kHz operation. The minimum inductance for 30% ripple current is:

$$\Delta I_L = \frac{V_{OUT}}{(f)(L)}\left(1-\frac{V_{OUT}}{V_{IN(NOM)}}\right)$$

A 4.7µH inductor will produce 29% ripple current. The peak inductor current will be the maximum DC value plus one half the ripple current, or 5.73A. Increasing the ripple current will also help ensure that the minimum on-time of 80ns is not violated. The minimum on-time occurs at maximum V_{IN}:

$$t_{ON(MIN)} = \frac{V_{OUT}}{V_{IN(MAX)}(f)} = \frac{3.3V}{22V(350kHz)} = 429ns$$

The equivalent R_{SENSE} resistor value can be calculated by using the minimum value for the maximum current sense threshold (66mV):

$$R_{SENSE} \le \frac{66mV}{5.73A} \approx 0.01\Omega$$

Choosing 1% resistors: R_A = 25k and R_B = 78.7k yields an output voltage of 3.32V.

The power dissipation on the topside MOSFET can be easily estimated. Choosing a Fairchild FDS6982S dual MOSFET results in: $R_{DS(ON)}$ = 0.035Ω/0.022Ω, C_{MILLER} = 215pF. At maximum input voltage with T(estimated) = 50°C:

$$P_{MAIN} = \frac{3.3V}{22V}(5A)^2\left[1+(0.005)(50°C-25°C)\right](0.035\Omega)+(22V)^2\frac{5A}{2}(2.5\Omega)(215pF)\bullet\left[\frac{1}{6V-2.3V}+\frac{1}{2.3V}\right](350kHz) = 308mW$$

A short-circuit to ground will result in a folded back current of:

$$I_{SC} = \frac{34mV}{0.01\Omega}-\frac{1}{2}\left(\frac{80ns(22V)}{4.7\mu H}\right) = 3.21A$$

with a typical value of $R_{DS(ON)}$ and δ = (0.005/°C)(25°C) = 0.125. The resulting power dissipated in the bottom MOSFET is:

P_{SYNC} = $(3.21A)^2$ (1.125) (0.022Ω) = 255mW

which is less than under full-load conditions.

C_{IN} is chosen for an RMS current rating of at least 3A at temperature assuming only this channel is on. C_{OUT} is chosen with an ESR of 0.02Ω for low output ripple. The output ripple in continuous mode will be highest at the maximum input voltage. The output voltage ripple due to ESR is approximately:

$V_{O(RIPPLE)}$ = R_{ESR} (ΔI_L) = 0.02Ω (1.45A) = 29mV_{P-P}

PC Board Layout Checklist

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the IC. Figure 10 illustrates the current waveforms present in the various branches of the 2-phase synchronous buck regulators operating in the continuous mode. Check the following in your layout:

1. Are the top N-channel MOSFETs MTOP1 and MTOP2 located within 1cm of each other with a common drain connection at C_{IN}? Do not attempt to split the input decoupling for the two channels as it can cause a large resonant loop.

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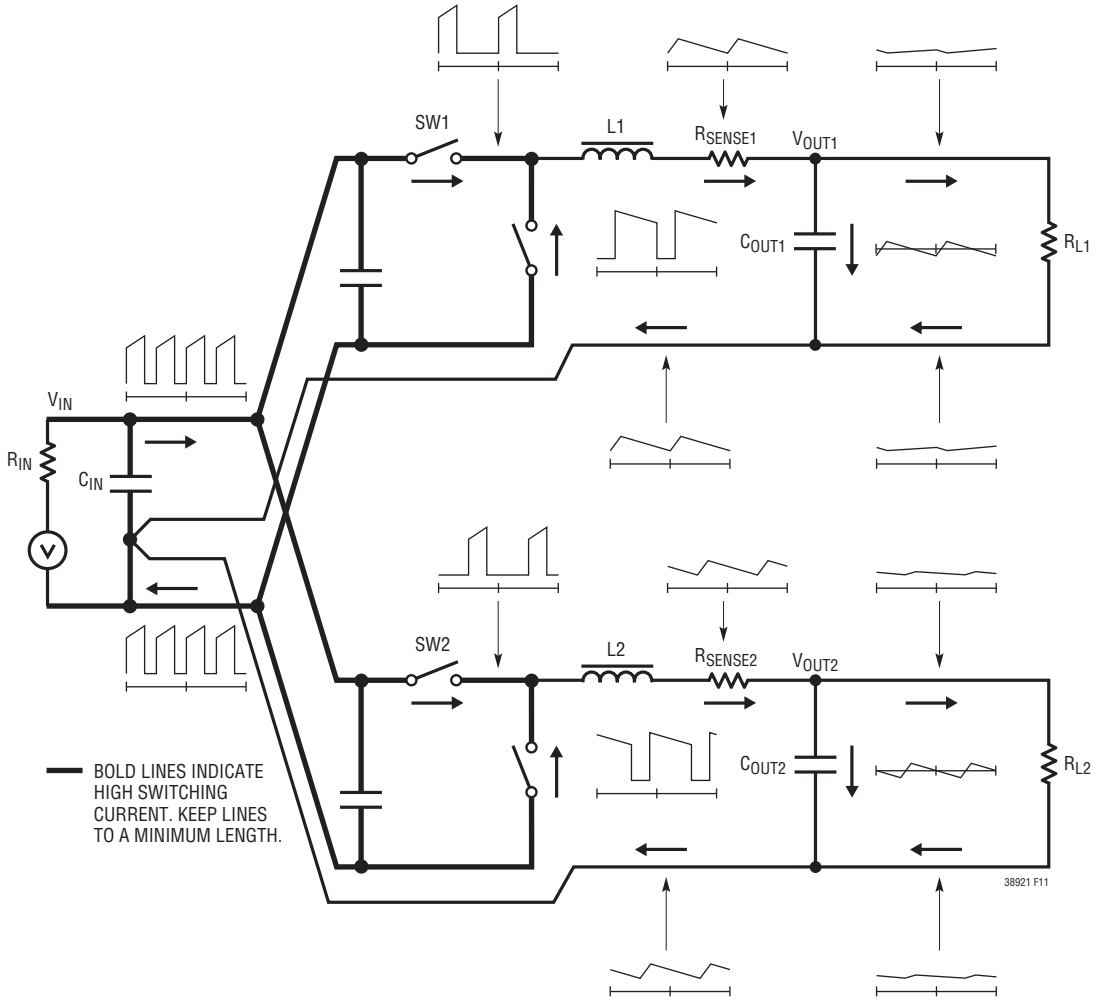

Figure 10. Branch Current Waveforms

2. Are the signal and power grounds kept separate? The combined IC signal ground pin and the ground return of C_{DRVCC} must return to the combined C_{OUT} (–) terminals. The path formed by the top N-channel MOSFET, Schottky diode and the C_{IN} capacitor should have short leads and PC trace lengths. The output capacitor (–) terminals should be connected as close as possible to the (–) terminals of the input capacitor by placing the capacitors next to each other and away from the Schottky loop described above.

3. Does the LTC3892/LTC3892-1/LTC3892-2 V_{FB} pin's resistive divider connect to the (+) terminal of C_{OUT}? The resistive divider must be connected between the (+) terminal of C_{OUT} and signal ground. The feedback resistor connections should not be along the high current input feeds from the input capacitor(s).

4. Are the SENSE$^-$ and SENSE$^+$ leads routed together with minimum PC trace spacing? The filter capacitor between SENSE$^+$ and SENSE$^-$ should be as close as possible to the IC. Ensure accurate current sensing with Kelvin connections at the SENSE resistor.

5. Is the DRV_{CC} and decoupling capacitor connected close to the IC, between the DRV_{CC} and the ground pin? This capacitor carries the MOSFET drivers' current peaks.

6. Keep the switching nodes (SW1, SW2), top gate (TG1, TG2), and boost nodes (BOOST1, BOOST2) away from sensitive small-signal nodes, especially from the op-

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posites channel's voltage and current sensing feedback pins. All of these nodes have very large and fast moving signals and therefore should be kept on the output side of the LTC3892/LTC3892-1/LTC3892-2 and occupy minimum PC trace area.

7. Use a modified star ground technique: a low impedance, large copper area central grounding point on the same side of the PC board as the input and output capacitors with tie-ins for the bottom of the DRV_{CC} decoupling capacitor, the bottom of the voltage feedback resistive divider and the GND pin of the IC.

PC Board Layout Debugging

Start with one controller at a time. It is helpful to use a DC-50MHz current probe to monitor the current in the inductor while testing the circuit. Monitor the output switching node (SW pin) to synchronize the oscilloscope to the internal oscillator and probe the actual output voltage as well. Check for proper performance over the operating voltage and current range expected in the application. The frequency of operation should be maintained over the input voltage range down to dropout and until the output load drops below the low current operation threshold—typically 25% of the maximum designed current level in Burst Mode operation.

The duty cycle percentage should be maintained from cycle to cycle in a well-designed, low noise PCB implementation. Variation in the duty cycle at a subharmonic rate can suggest noise pickup at the current or voltage sensing inputs or inadequate loop compensation. Overcompensation of the loop can be used to tame a poor PC layout if regulator bandwidth optimization is not required. Only after each controller is checked for its individual performance should both should multiple controllers be turned on at the same time. A particularly difficult region of operation is when one channel is nearing its current comparator trip point when the other channel is turning on its top MOSFET. This occurs around 50% duty cycle on either channel due to the phasing of the internal clocks and may cause minor duty cycle jitter.

Reduce V_{IN} from its nominal level to verify operation of the regulator in dropout. Check the operation of the undervoltage lockout circuit by further lowering V_{IN} while monitoring the outputs to verify operation.

Investigate whether any problems exist only at higher output currents or only at higher input voltages. If problems coincide with high input voltages and low output currents, look for capacitive coupling between the BOOST, SW, TG, and possibly BG connections and the sensitive voltage and current pins. The capacitor placed across the current sensing pins needs to be placed immediately adjacent to the pins of the IC. This capacitor helps to minimize the effects of differential noise injection due to high frequency capacitive coupling. If problems are encountered with high current output loading at lower input voltages, look for inductive coupling between C_{IN}, Schottky and the top MOSFET components to the sensitive current and voltage sensing traces. In addition, investigate common ground path voltage pickup between these components and the GND pin of the IC.

An embarrassing problem, which can be missed in an otherwise properly working switching regulator, results when the current sensing leads are hooked up backwards. The output voltage under this improper hookup will still be maintained but the advantages of current mode control will not be realized. Compensation of the voltage loop will be much more sensitive to component selection. This behavior can be investigated by temporarily shorting out the current sensing resistor—don't worry, the regulator will still maintain control of the output voltage.

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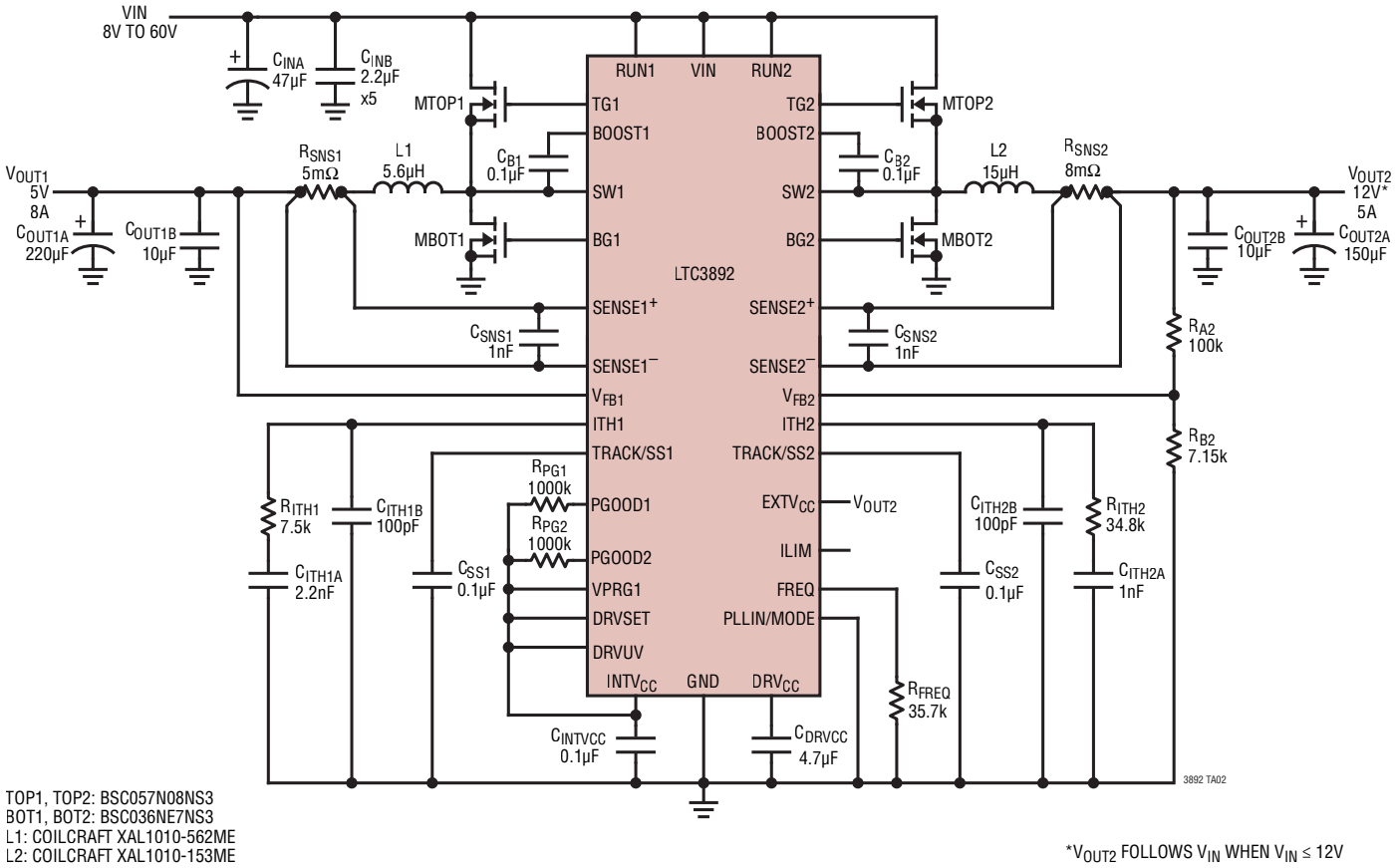
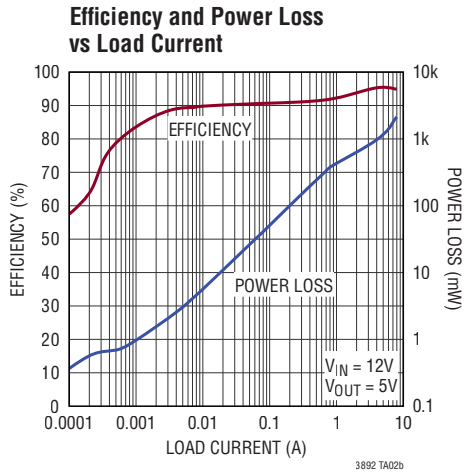


TOP1, TOP2: BSC057N08NS3
BOT1, BOT2: BSC036NE7NS3
L1: COILCRAFT XAL1010-562ME
L2: COILCRAFT XAL1010-153ME

*V_{OUT2} FOLLOWS V_{IN} WHEN $V_{IN} \leq 12V$

Figure 11. High Efficiency Dual 5V/12V Step-Down Converter with 10V Gate Drive



TYPICAL APPLICATIONS

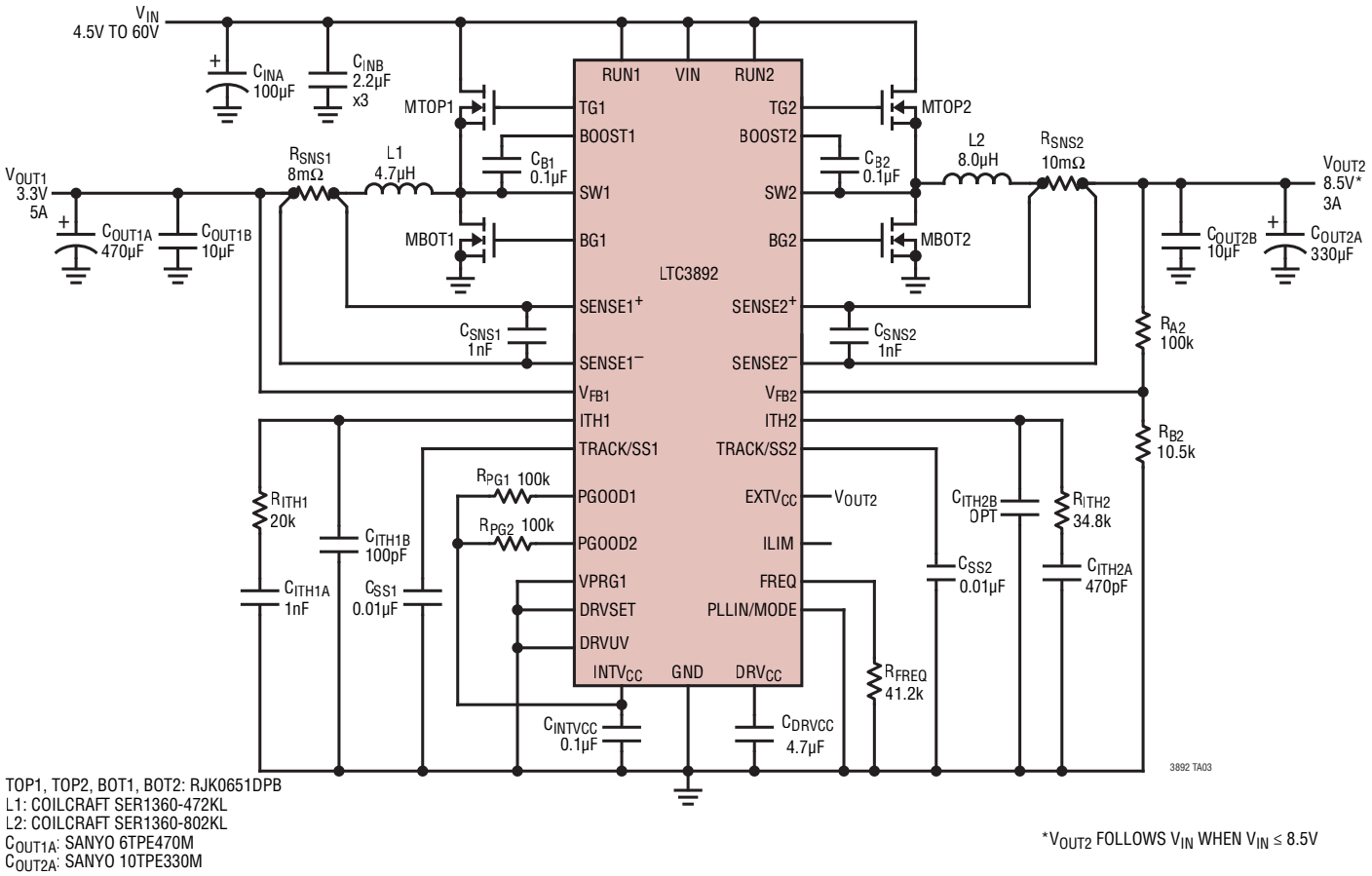
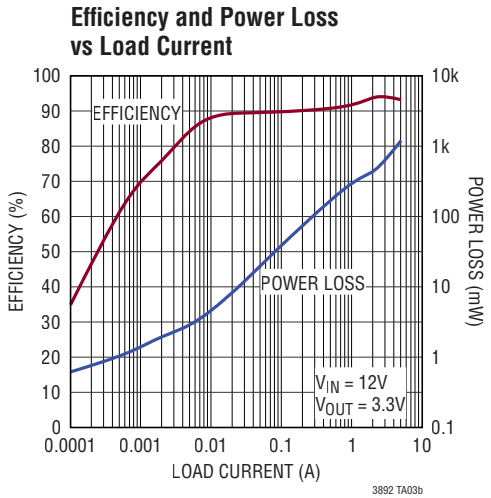
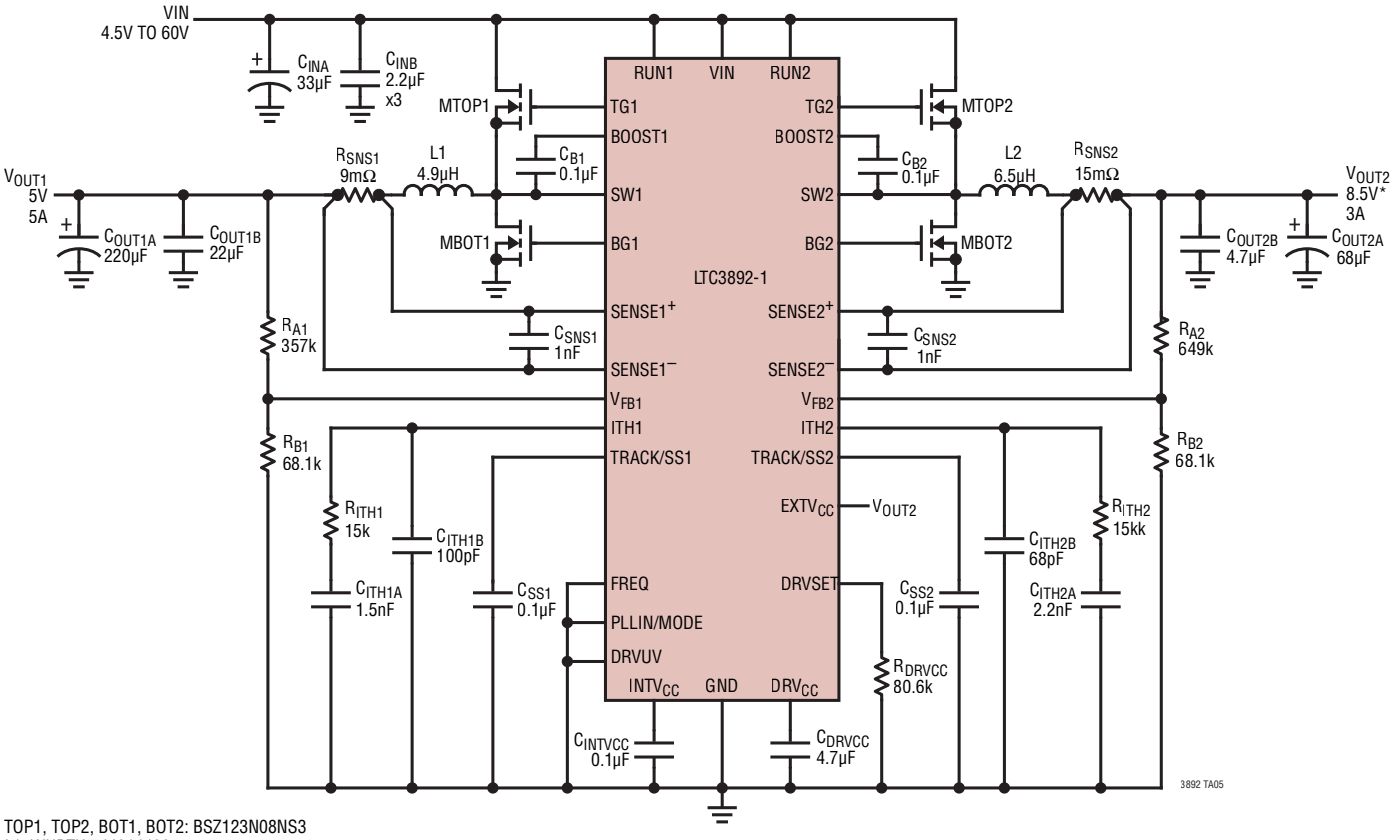


Figure 12. High Efficiency Dual 3.3V/8.5V Step-Down Converter with 6V Gate Drive



TYPICAL APPLICATIONS



TOP1, TOP2, BOT1, BOT2: BSZ123N08NS3
L1: WURTH 744314490
L2: WURTH 744314490
C_{OUT1A}: SANYO 6TPB220ML
C_{OUT2A}: SANYO 10TPC68M

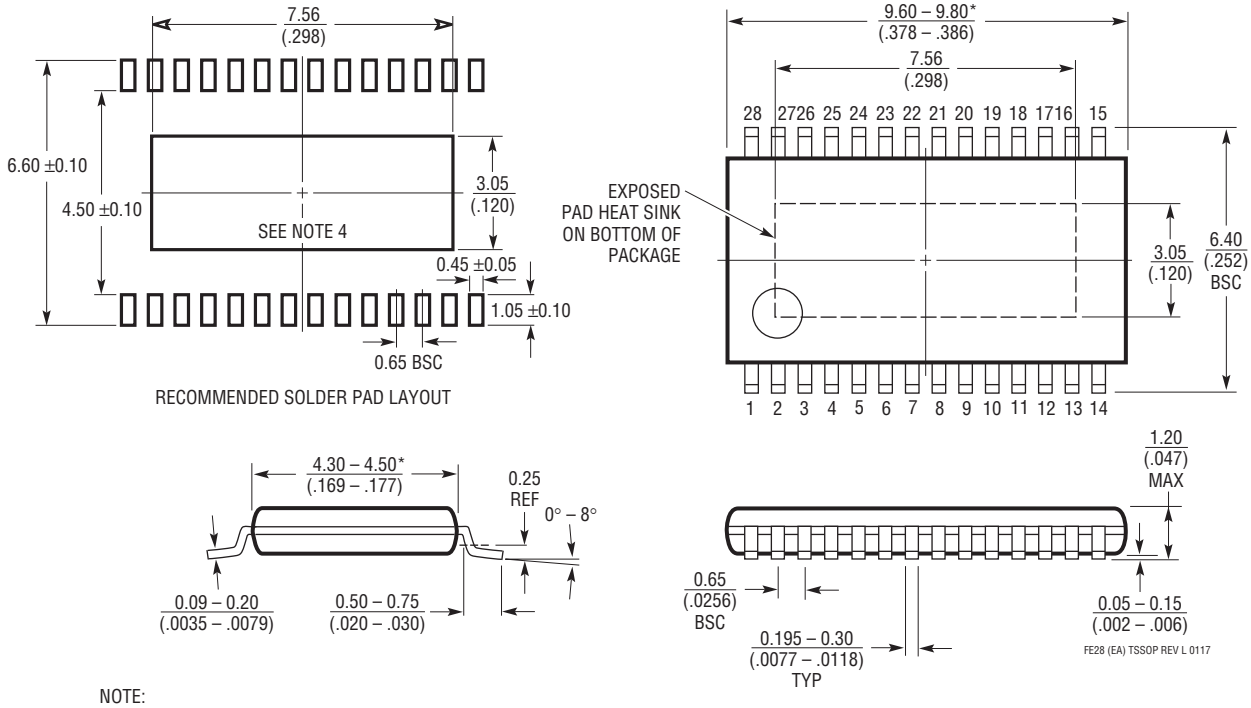
*V_{OUT2} FOLLOWS V_{IN} WHEN $V_{IN} \leq 8.5V$

Figure 13. High Efficiency Dual-Phase Step-Down 5V/8.5V Converter with 8V Gate Drive

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTC3892#packaging for the most recent package drawings.

FE Package
28-Lead Plastic TSSOP (4.4mm)
(Reference LTC DWG # 05-08-1663 Rev L)
Exposed Pad Variation EA



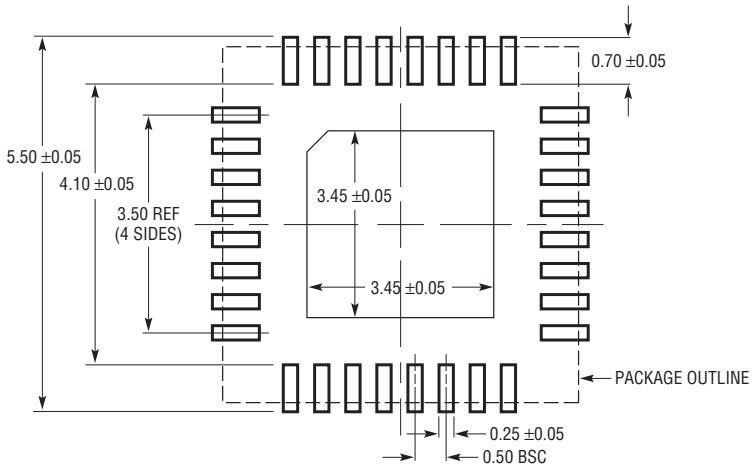
NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN MILLIMETERS (INCHES)
3. DRAWING NOT TO SCALE
4. RECOMMENDED MINIMUM PCB METAL SIZE FOR EXPOSED PAD ATTACHMENT

*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.150mm (.006") PER SIDE

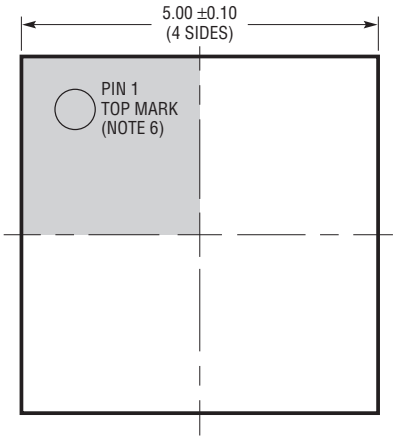
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTC3892#packaging for the most recent package drawings.

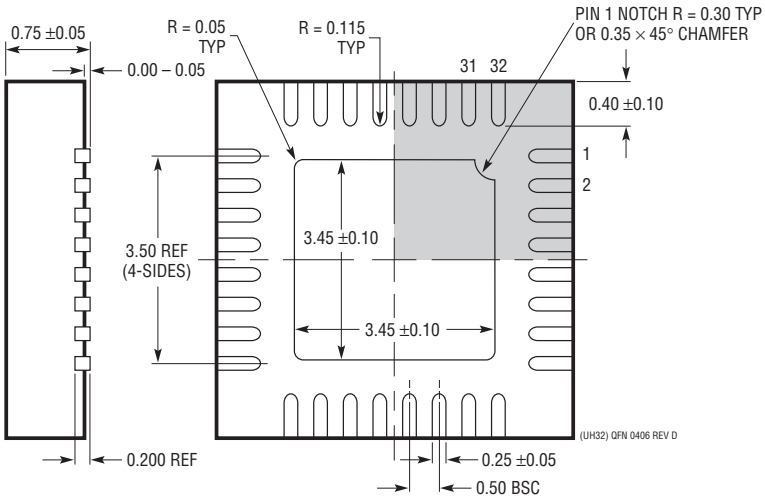
UH Package
32-Lead Plastic QFN (5mm × 5mm)
(Reference LTC DWG # 05-08-1693 Rev D)



RECOMMENDED SOLDER PAD LAYOUT
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



BOTTOM VIEW—EXPOSED PAD



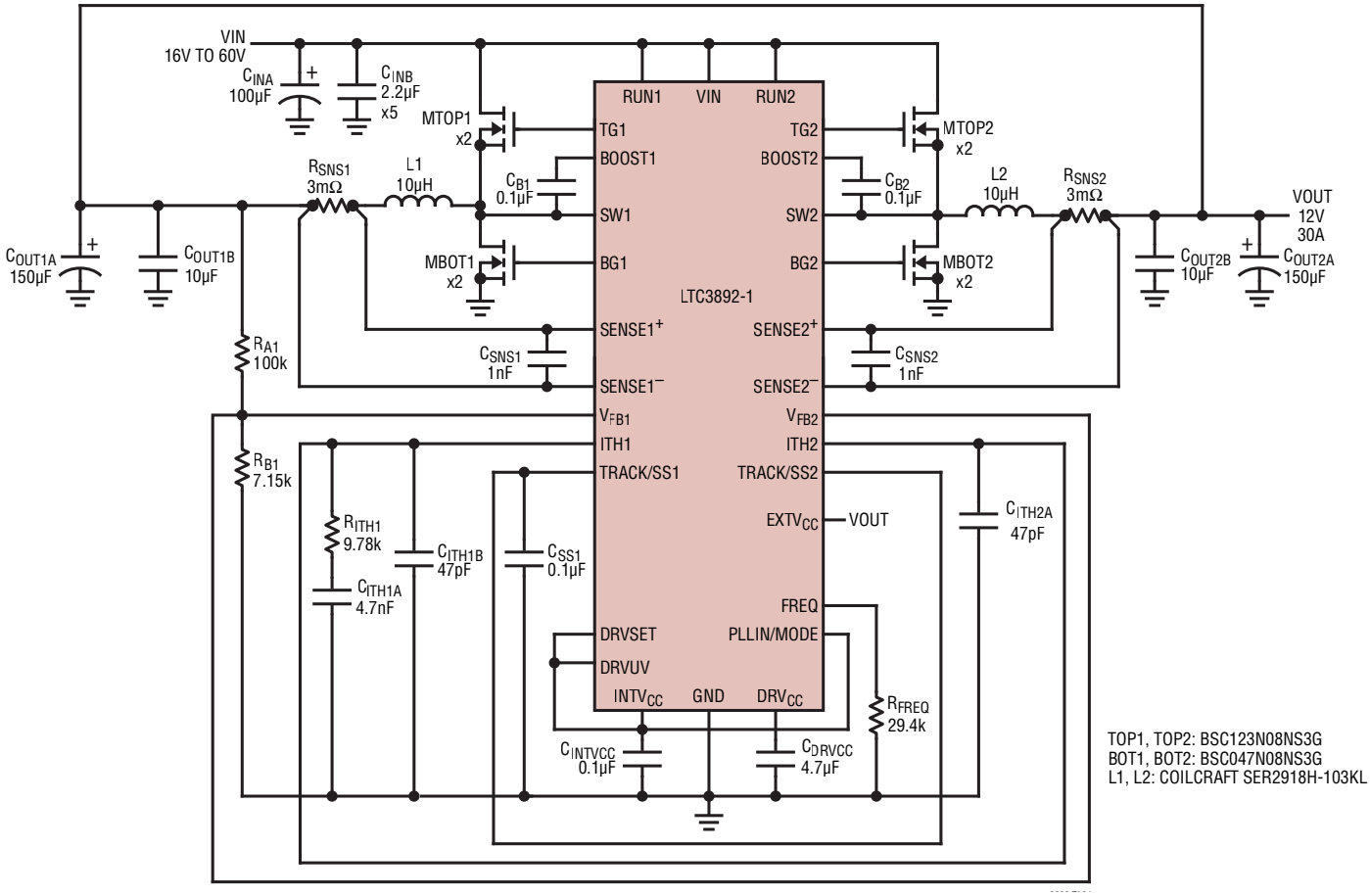
NOTE:
1. DRAWING PROPOSED TO BE A JEDEC PACKAGE OUTLINE
   M0-220 VARIATION WHHD-(X) (TO BE APPROVED)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE
   MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION
   ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	12/15	Add LTC3892-2 Version	1 to 38
B	05/16	Modified graph, Oscillator Frequency vs Temperature	10
C	07/17	Corrected LTC3892-2 Part Marking Corrected $EXTV_{CC}$ Pin Description	5 11

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

TYPICAL APPLICATION



TOP1, TOP2: BSC123N08NS3G
BOT1, BOT2: BSC047N08NS3G
L1, L2: COILCRAFT SER2918H-103KL

Figure 14. High Current Dual-Phase Single Output Step-Down 12V Converter

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3890/LTC3890-1 LTC3890-2/LTC3890-3	60V, Low I_Q, Dual 2-Phase Synchronous Step-Down DC/DC Controller with 99% Duty Cycle	PLL Fixed Frequency 50kHz to 900kHz, 4V ≤ V_{IN} ≤ 60V, 0.8V ≤ V_{OUT} ≤ 24V, I_Q = 50µA
LTC3891	60V, Low I_Q, Synchronous Step-Down DC/DC Controller with 99% Duty Cycle	PLL Fixed Frequency 50kHz to 900kHz, 4V ≤ V_{IN} ≤ 60V, 0.8V ≤ V_{OUT} ≤ 24V, I_Q = 50µA
LTC3864	60V, Low I_Q, High Voltage DC/DC Controller with 100% Duty Cycle	Fixed Frequency 50kHz to 850kHz, 3.5V ≤ V_{IN} ≤ 60V, 0.8V ≤ V_{OUT} ≤ V_{IN}, I_Q = 40µA, MSOP-12E, 3mm × 4mm DFN-12
LTC3899	60V, Triple Output, Buck/Buck/Boost Synchronous Controller with 29µA Burst Mode I_Q	4.5V (Down to 2.2V after Start-Up) ≤ V_{IN} ≤ 60V, V_{OUT} Up to 60V, Buck V_{OUT} Range: 0.8V to 60V, Boost V_{OUT} Up to 60V
LTC3859AL	38V, Low I_Q, Triple Output, Buck/Buck/Boost Synchronous Controller with 28µA Burst Mode I_Q	4.5V (Down to 2.5V after Start-Up) ≤ V_{IN} ≤ 38V, V_{OUT} Up to 60V, Buck V_{OUT} Range: 0.8V to 24V, Boost V_{OUT} Up to 60V,
LTC3857/LTC3857-1 LTC3858/LTC3858-1	38V, Low I_Q, Dual Output 2-Phase Synchronous Step-Down DC/DC Controller with 99% Duty Cycle	PLL Fixed Operating Frequency 50kHz to 900kHz, 4V ≤ V_{IN} ≤ 38V, 0.8V ≤ V_{OUT} ≤ 24V, I_Q = 50µA/170µA
LTC3807	38V, Low I_Q, Synchronous Step-Down Controller with 24V Output Voltage Capability	PLL Fixed Frequency 50kHz to 900kHz, 4V ≤ V_{IN} ≤ 38V, 0.8V ≤ V_{OUT} ≤ 24V, I_Q = 50µA

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