THE DATASHEET OF

LTC4000IGN-1#PBF

High Voltage High Current Controller for Battery Charging with Maximum Power Point Control

FEATURES

- **Maximum Power Control: Solar Panel Input Compatible**
- **Complete High Performance Battery Charger When Paired with a DC/DC Converter**
- **Wide Input and Output Voltage Range: 3V to 60V**
- **Input Ideal Diode for Low Loss Reverse Blocking and Load Sharing**
- **Output Ideal Diode for Low Loss PowerPath™ and Load Sharing with the Battery**
- **Programmable Charge Current: ±1% Accuracy**
- **±0.25% Accurate Programmable Float Voltage**
- Programmable C/X or Timer Based Charge Termination
- NTC Input for Temperature Qualified Charging
- 28-Lead 4mm × 5mm QFN or SSOP Packages

APPLICATIONS

- Solar Powered Battery Charger Systems
- Battery Charger with High Impedance Input Source, e.g., Fuel Cell or Wind Turbine
- Battery Equipped Industrial or Portable Military Equipments

DESCRIPTION

The LTC®4000-1 is a high voltage, high performance controller that converts many externally compensated DC/DC power supplies into full-featured battery chargers with maximum power point control. In contrast to the LTC4000, the LTC4000-1 has an input voltage regulation loop instead of the input current regulation loop.

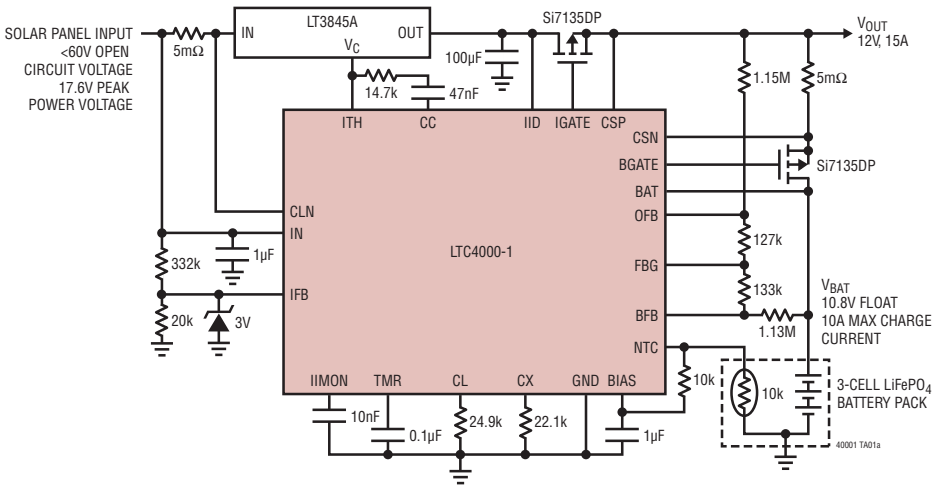
Features of the LTC4000-1's battery charger include: accurate (±0.25%) programmable float voltage, selectable timer or current termination, temperature qualified charging using an NTC thermistor, automatic recharge, C/10 trickle charge for deeply discharged cells, bad battery detection and status indicator outputs. The battery charger also includes precision current sensing that allows lower sense voltages for high current applications.

The LTC4000-1 supports intelligent PowerPath control. An external PFET provides low loss reverse current protection. Another external PFET provides low loss charging or discharging of the battery. This second PFET also facilitates an instant-on feature that provides immediate downstream system power even when connected to a heavily discharged or shorted battery.

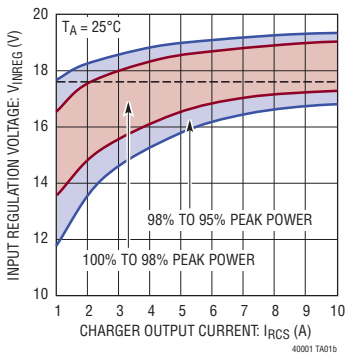
The LTC4000-1 is available in a low profile 28-lead 4mm × 5mm QFN and SSOP packages.

TYPICAL APPLICATION

10.8V at 10A Charger for Three $LiFePO_4$ Cells with a Solar Panel Input



Solar Panel Input Regulation, Achieves Max Power Point to Greater than 98%

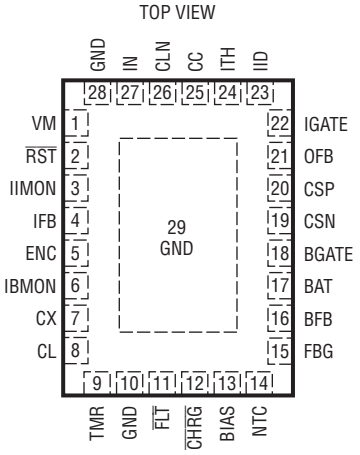


ABSOLUTE MAXIMUM RATINGS

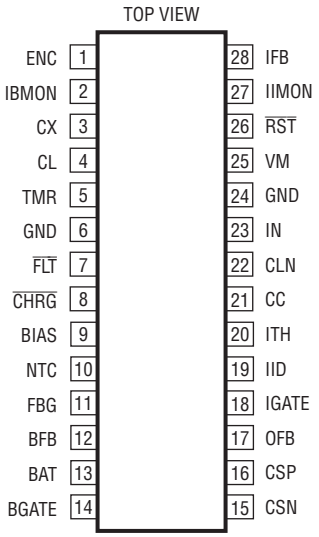
(Note 1)

IN, CLN, IID, CSP, CSN, BAT ..... –0.3V to 62V
IN-CLN, CSP-CSN ..... –1V to 1V
OFB, BFB, FBG ..... –0.3V to 62V
FBG ..... –1mA to 2mA
IGATE ..... Max (V_{IID}, V_{CSP}) – 10V to Max (V_{IID}, V_{CSP})
BGATE ..... Max (V_{BAT}, V_{CSN}) – 10V to Max (V_{BAT}, V_{CSN})
ENC, CX, NTC, VM ..... –0.3V to V_{BIAS}
IFB, CL, TMR, IIMON, CC ..... –0.3V to V_{BIAS}
BIAS ..... –0.3V to Min (6V, V_{IN})
IBMON ..... –0.3V to Min (V_{BIAS}, V_{CSP})
ITH ..... –0.3V to 6V
$\overline{CHRG}$, $\overline{FLT}$, $\overline{RST}$ ..... –0.3V to 62V
$\overline{CHRG}$, $\overline{FLT}$, $\overline{RST}$ ..... –1mA to 2mA
Operating Junction Temperature Range
(Note 2) ..... 125°C
Lead Temperature (Soldering, 10 sec)
SSOP Package ..... 300°C
Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



UFD PACKAGE
28-LEAD (4mm × 5mm) PLASTIC QFN
T_{JMAX} = 125°C, θ_{JA} = 43°C/W, θ_{JC} = 4°C/W
EXPOSED PAD (PIN 29) IS GND, MUST BE SOLDERED TO PCB



GN PACKAGE
28-LEAD PLASTIC SSOP
T_{JMAX} = 125°C, θ_{JA} = 80°C/W, θ_{JC} = 25°C/W

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC4000EUFD-1#PBF	LTC4000EUFD-1#TRPBF	40001	28-Lead (4mm × 5mm) Plastic QFN	–40°C to 125°C
LTC4000IUFD-1#PBF	LTC4000IUFD-1#TRPBF	40001	28-Lead (4mm × 5mm) Plastic QFN	–40°C to 125°C
LTC4000EGN-1#PBF	LTC4000EGN-1#TRPBF	LTC4000GN-1	28-Lead Plastic SSOP	–40°C to 125°C
LTC4000IGN-1#PBF	LTC4000IGN-1#TRPBF	LTC4000GN-1	28-Lead Plastic SSOP	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = V_{CLN} = 3V to 60V unless otherwise noted (Notes 2, 3).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Input Supply Operating Range		●	3		60	V
I_{IN}	Input Quiescent Operating Current				0.4		mA
I_{BAT}	Battery Pin Operating Current	$V_{IN} \geq 3V$, $V_{CSN} = V_{CSP} \geq V_{BAT}$	●		50	100	µA
	Battery Only Quiescent Current	$V_{IN} = 0V$, $V_{CSN} = V_{CSP} \leq V_{BAT}$	●		10	20	µA
Shutdown							
	ENC Input Voltage Low		●			0.4	V
	ENC Input Voltage High		●	1.5			V
	ENC Pull-Up Current	$V_{ENC} = 0V$		–4	–2	–0.5	µA
	ENC Open Circuit Voltage	V_{ENC} = Open	●	1.5	2.5		V
Voltage Regulation							
V_{IFB_REG}	Input Feedback Voltage		●	0.985	1.000	1.010	V
	IFB Input Current	$V_{IFB} = 1.0V$			± 0.1		µA
V_{BFB_REG}	Battery Feedback Voltage		 ●	1.133 1.120	1.136 1.136	1.139 1.147	V V
	BFB Input Current	$V_{BFB} = 1.2V$			± 0.1		µA
V_{OFB_REG}	Output Feedback Voltage		●	1.176	1.193	1.204	V
	OFB Input Current	$V_{OFB} = 1.2V$			± 0.1		µA
R_{FBG}	Ground Return Feedback Resistance		●		100	400	Ω
$V_{RECHRG(RISE)}$	Rising Recharge Battery Threshold Voltage	% of V_{BFB_REG}	●	96.9	97.6	98.3	%
$V_{RECHRG(HYS)}$	Recharge Battery Threshold Voltage Hysteresis	% of V_{BFB_REG}			0.5		%
$V_{OUT(INST\_ON)}$	Instant-On Battery Voltage Threshold	% of V_{BFB_REG}	●	82	86	90	%
V_{LOBAT}	Falling Low Battery Threshold Voltage	% of V_{BFB_REG}	●	65	68	71	%
$V_{LOBAT(HYS)}$	Low Battery Threshold Voltage Hysteresis	% of V_{BFB_REG}			3		%
Current Monitoring and Regulation							
	Ratio of Monitored-Current Voltage to Sense Voltage	$V_{IN,CLN} \leq 50mV$, $V_{IIMON}/V_{IN,CLN}$ $V_{CSP,CSN} \leq 50mV$, $V_{IBMON}/V_{CSP,CSN}$	●	18.5	20	21	V/V
V_{OS}	Sense Voltage Offset	$V_{CSP,CSN} \leq 50mV$, $V_{CSP} = 60V$ or $V_{IN,CLN} \leq 50mV$, $V_{IN} = 60V$ (Note 4)		–300		300	µV
	CLN, CSP, CSN Common Mode Range	(Note 4)	●	3		60	V
	CLN Pin Current				±1		µA
	CSP Pin Current	V_{IGATE} = Open, $V_{IID} = 0V$			90		µA
	CSN Pin Current	V_{BGATE} = Open, $V_{BAT} = 0V$			45		µA
I_{CL}	Pull-Up Current for the Charge Current Limit Programming Pin		●	–55	–50	–45	µA
I_{CL_TRKL}	Pull-Up Current for the Charge Current Limit Programming Pin in Trickle Charge Mode	$V_{BFB} < V_{LOBAT}$	●	–5.5	–5.0	–4.5	µA
	Input Current Monitor Resistance to GND			40	90	140	kΩ
	Charge Current Monitor Resistance to GND			40	90	140	kΩ
	A5 Error Amp Offset for the Charge Current Loop (See Figure 1)	$V_{CL} = 0.8V$	●	–10	0	10	mV
	Maximum Programmable Current Limit Voltage Range		●	0.985	1.0	1.015	V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = V_{CLN} = 3V to 60V unless otherwise noted (Notes 2, 3).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Charge Termination							
	CX Pin Pull-Up Current	V_{CX} = 0.1V	●	–5.5	–5.0	–4.5	µA
$V_{CX,IBMON(OS)}$	CX Comparator Offset Voltage, IBMON Falling	V_{CX} = 0.1V	●	0.5	10	25	mV
$V_{CX,IBMON(HYS)}$	CX Comparator Hysteresis Voltage				5		mV
	TMR Pull-Up Current	V_{TMR} = 0V			–5.0		µA
	TMR Pull-Down Current	V_{TMR} = 2V			5.0		µA
	TMR Pin Frequency	C_{TMR} = 0.01µF		400	500	600	Hz
	TMR Threshold for CX Termination		●		2.1	2.5	V
t_T	Charge Termination Time	C_{TMR} = 0.1µF	●	2.3	2.9	3.5	h
t_T/t_{BB}	Ratio of Charge Terminate Time to Bad Battery Indicator Time	C_{TMR} = 0.1µF	●	3.95	4	4.05	h/h
$V_{NTC(COLD)}$	NTC Cold Threshold	V_{NTC} Rising, % of V_{BIAS}	●	73	75	77	%
$V_{NTC(HOT)}$	NTC Hot Threshold	V_{NTC} Falling, % of V_{BIAS}	●	33	35	37	%
$V_{NTC(HYS)}$	NTC Thresholds Hysteresis	% of V_{BIAS}			5		%
$V_{NTC(OPEN)}$	NTC Open Circuit Voltage	% of V_{BIAS}	●	45	50	55	%
$R_{NTC(OPEN)}$	NTC Open Circuit Input Resistance				300		kΩ
Voltage Monitoring and Open Drain Status Pins							
$V_{VM(TH)}$	VM Input Falling Threshold		●	1.176	1.193	1.204	V
$V_{VM(HYS)}$	VM Input Hysteresis				40		mV
	VM Input Current	V_{VM} = 1.2V			±0.1		µA
$I_{\overline{RST},\overline{CHRG},\overline{FLT}(LKG)}$	Open Drain Status Pins Leakage Current	V_{PIN} = 60V			±1		µA
$V_{\overline{RST},\overline{CHRG},\overline{FLT}(VOL)}$	Open Drain Status Pins Voltage Output Low	I_{PIN} = 1mA	●			0.4	V
Input PowerPath Control							
	Input PowerPath Forward Regulation Voltage	$V_{IID,CSP}$, 3V ≤ V_{CSP} ≤ 60V	●	0.1	8	20	mV
	Input PowerPath Fast Reverse Turn-Off Threshold Voltage	$V_{IID,CSP}$, 3V ≤ V_{CSP} ≤ 60V, V_{IGATE} = V_{CSP} – 2.5V, $\Delta I_{IGATE}/\Delta V_{IID,CSP}$ ≥ 100µA/mV	●	–90	–50	–20	mV
	Input PowerPath Fast Forward Turn-On Threshold Voltage	$V_{IID,CSP}$, 3V ≤ V_{CSP} ≤ 60V, V_{IGATE} = V_{IID} – 1.5V, $\Delta I_{IGATE}/\Delta V_{IID,CSP}$ ≥ 100µA/mV	●	40	80	130	mV
	Input Gate Turn-Off Current	V_{IID} = V_{CSP}, V_{IGATE} = V_{CSP} – 1.5V			–0.3		µA
	Input Gate Turn-On Current	V_{CSP} = V_{IID} – 20mV, V_{IGATE} = V_{IID} – 1.5V			0.3		µA
$I_{IGATE(FASTOFF)}$	Input Gate Fast Turn-Off Current	V_{CSP} = V_{IID} + 0.1V, V_{IGATE} = V_{CSP} – 5V			–0.5		mA
$I_{IGATE(FASTON)}$	Input Gate Fast Turn-On Current	V_{CSP} = V_{IID} – 0.2V, V_{IGATE} = V_{IID} – 1.5V			0.7		mA
$V_{IGATE(ON)}$	Input Gate Clamp Voltage	I_{IGATE} = 2µA, V_{IID} = 12V to 60V, V_{CSP} = V_{IID} – 0.5V, Measure V_{IID} – V_{IGATE}	●		13	15	V
	Input Gate Off Voltage	I_{IGATE} = – 2µA, V_{IID} = 3V to 59.5V, V_{CSP} = V_{IID} + 0.5V, Measure V_{CSP} – V_{IGATE}	●		0.45	0.7	V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = V_{CLN} = 3V to 60V unless otherwise noted (Notes 2, 3).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Battery PowerPath Control							
	Battery Discharge PowerPath Forward Regulation Voltage	$V_{BAT,CSN}$, 2.8V ≤ V_{BAT} ≤ 60V	●	0.1	8	20	mV
	Battery PowerPath Fast Reverse Turn-Off Threshold Voltage	$V_{BAT,CSN}$, 2.8V ≤ V_{BAT} ≤ 60V, Not Charging, V_{BGATE} = V_{CSN} – 2.5V, $\Delta I_{BGATE}/\Delta V_{BAT,CSN}$ ≥ 100µA/mV	●	–90	–50	–20	mV
	Battery PowerPath Fast Forward Turn-On Threshold Voltage	$V_{BAT,CSN}$, 2.8V ≤ V_{CSN} ≤ 60V, V_{BGATE} = V_{BAT} – 1.5V, $\Delta I_{BGATE}/\Delta V_{BAT,CSN}$ ≥ 100µA/mV	●	40	80	130	mV
	Battery Gate Turn-Off Current	V_{BGATE} = V_{CSN} – 1.5V, V_{CSN} ≥ V_{BAT}, V_{OFB} < $V_{OUT(INST\_ON)}$ and Charging in Progress, or V_{CSN} = V_{BAT} and Not Charging			–0.3		µA
	Battery Gate Turn-On Current	V_{BGATE} = V_{BAT} – 1.5V, V_{CSN} ≥ V_{BAT}, V_{OFB} > $V_{OUT(INST\_ON)}$ and Charging in Progress, or V_{CSN} = V_{BAT} – 20mV			0.3		µA
$I_{BGATE(FASTOFF)}$	Battery Gate Fast Turn-Off Current	V_{CSN} = V_{BAT} + 0.1V and Not Charging, V_{BGATE} = V_{CSN} – 5V			–0.5		mA
$I_{BGATE(FASTON)}$	Battery Gate Fast Turn-On Current	V_{CSN} = V_{BAT} – 0.2V, V_{BGATE} = V_{BAT} – 1.5V			0.7		mA
$V_{BGATE(ON)}$	Battery Gate Clamp Voltage	I_{BGATE} = 2µA, V_{BAT} = 12V to 60V, V_{CSN} = V_{BAT} – 0.5V, Measure V_{BAT} – V_{BGATE}	●		13	15	V
	Battery Gate Off Voltage	I_{BGATE} = – 2µA, V_{BAT} = 2.8V to 59.5V, V_{CSN} = V_{BAT} + 0.5V and not Charging, Measure V_{CSN} – V_{BGATE}	●		0.45	0.7	V
BIAS Regulator Output and Control Pins							
V_{BIAS}	BIAS Output Voltage	No Load	●	2.4	2.9	3.5	V
ΔV_{BIAS}	BIAS Output Voltage Load Regulation	I_{BIAS} = – 0.5mA			–0.5	–10	%
	BIAS Output Short-Circuit Current	V_{BIAS} = 0V			–20		mA
	Transconductance of Error Amp	CC = 1V			0.5		mA/V
	Open Loop DC Voltage Gain of Error Amp	CC = Open			80		dB
$I_{ITH(PULL\_UP)}$	Pull-Up Current on the ITH Pin	V_{ITH} = 0V, CC = 0V		–6	–5	–4	µA
$I_{ITH(PULL\_DOWN)}$	Pull-Down Current on the ITH Pin	V_{ITH} = 0.4V, CC = Open	●	0.5	1		mA
	Open Loop DC Voltage Gain of ITH Driver	ITH = Open			60		dB

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC4000-1 is tested under conditions such that $T_J \approx T_A$. The LTC4000E-1 is guaranteed to meet specifications from 0°C to 85°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC4000I-1 is guaranteed over the full –40°C to 125°C operating junction temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors. The junction temperature (T_J, in °C) is calculated from the ambient temperature (T_A, in °C) and power dissipation (P_D, in Watts) according to the following formula:

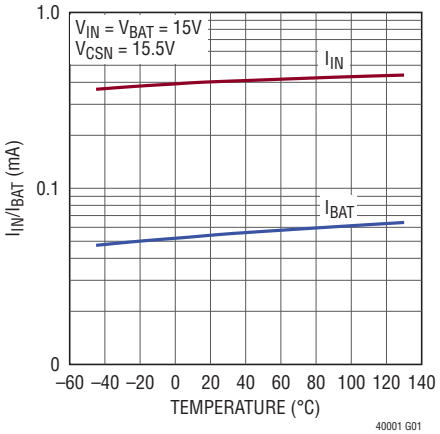
$T_J = T_A + (P_D \bullet \theta_{JA})$, where θ_{JA} (in °C/W) is the package thermal impedance.

Note 3: All currents into pins are positive; all voltages are referenced to GND unless otherwise noted.

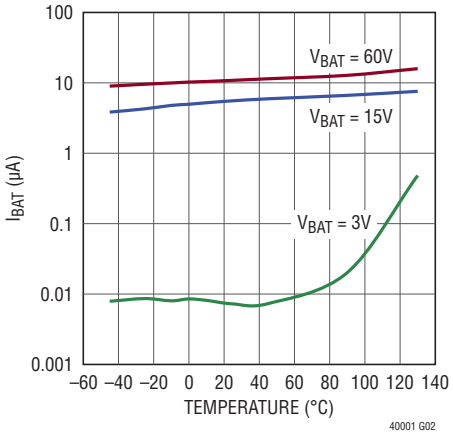
Note 4: These parameters are guaranteed by design and are not 100% tested.

TYPICAL PERFORMANCE CHARACTERISTICS

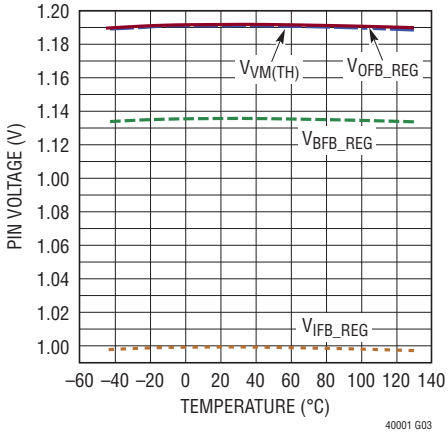
Input Quiescent Current and Battery Quiescent Current Over Temperature



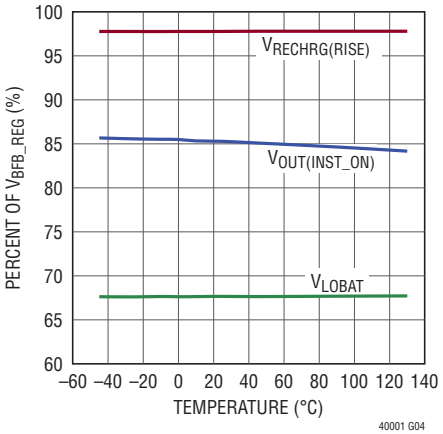
Battery Only Quiescent Current Over Temperature



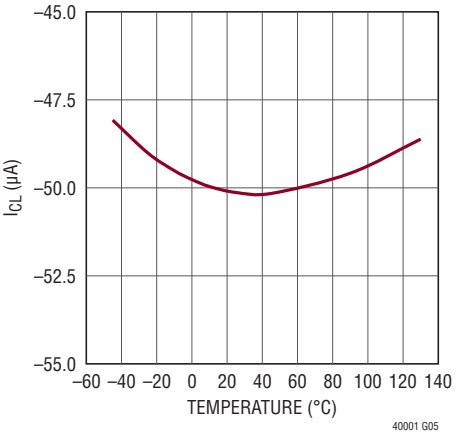
Input Voltage Regulation Feedback, Battery Float Voltage Feedback, Output Voltage Regulation Feedback and VM Falling Threshold Over Temperature



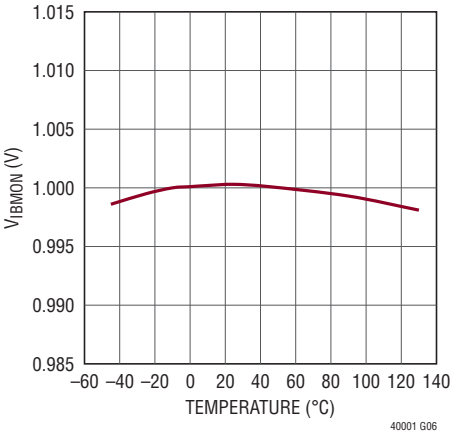
Battery Thresholds: Rising Recharge, Instant-On Regulation and Falling Low Battery As a Percentage of Battery Float Feedback Over Temperature



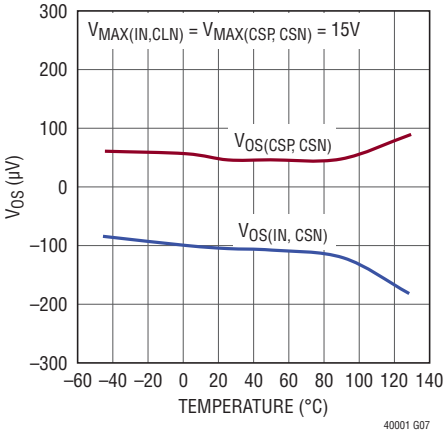
CL Pull-Up Current Over Temperature



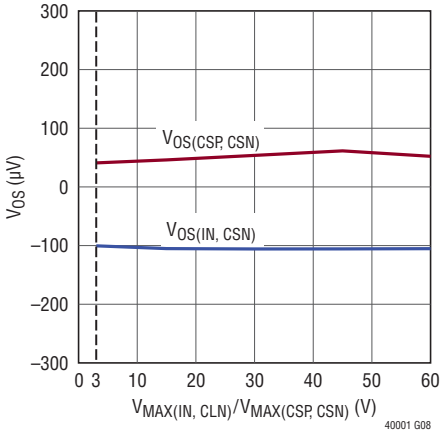
Maximum Programmable Current Limit Voltage Over Temperature



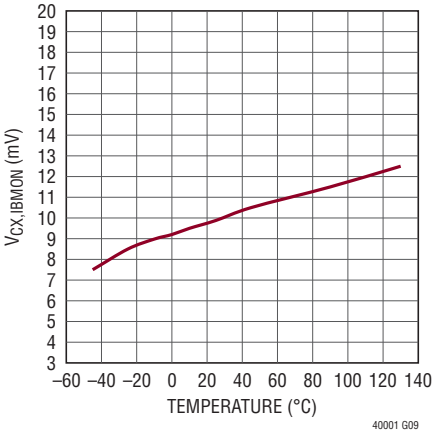
Current Sense Offset Voltage Over Temperature



Current Sense Offset Voltage Over Common Mode Voltage Range

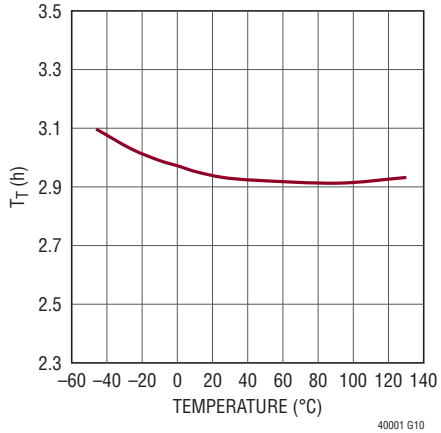


CX Comparator Offset Voltage with V_{IBMON} Falling Over Temperature

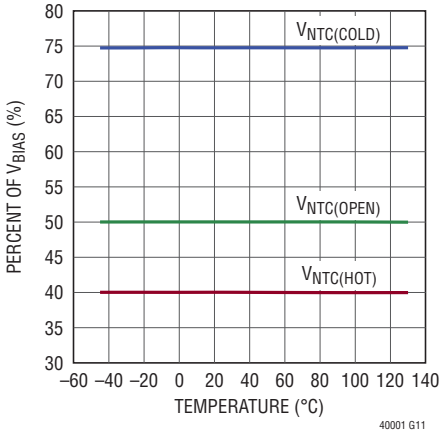


TYPICAL PERFORMANCE CHARACTERISTICS

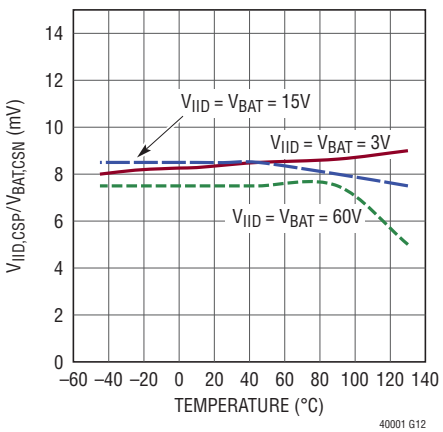
Charge Termination Time with 0.1µF Timer Capacitor Over Temperature



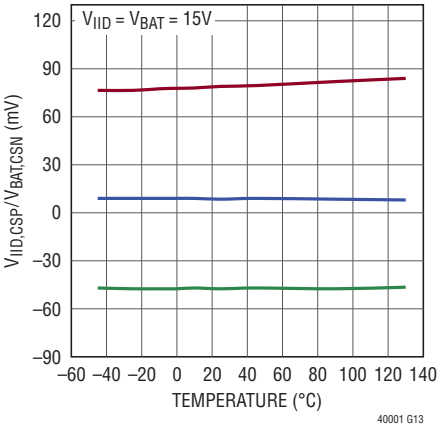
NTC Thresholds Over Temperature



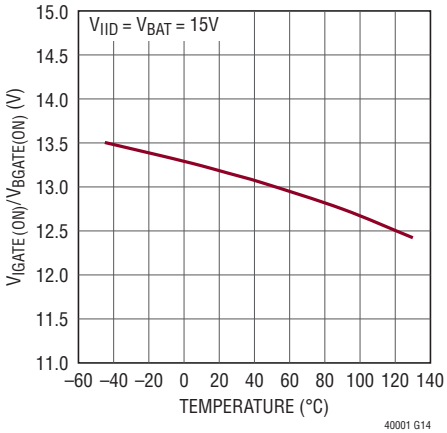
PowerPath Forward Voltage Regulation Over Temperature



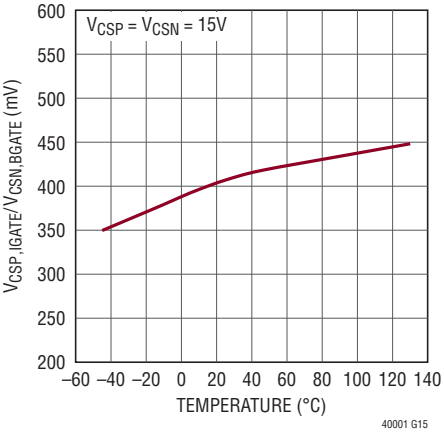
PowerPath Fast Off, Fast On and Forward Regulation Over Temperature



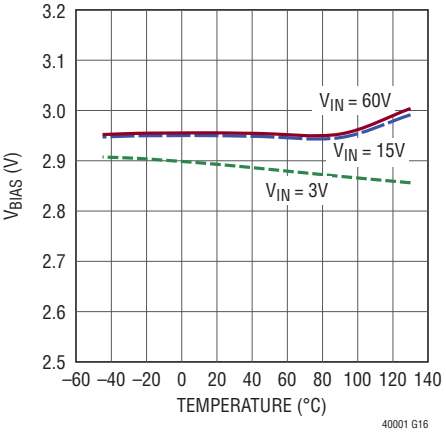
PowerPath Turn-On Gate Clamp Voltage Over Temperature



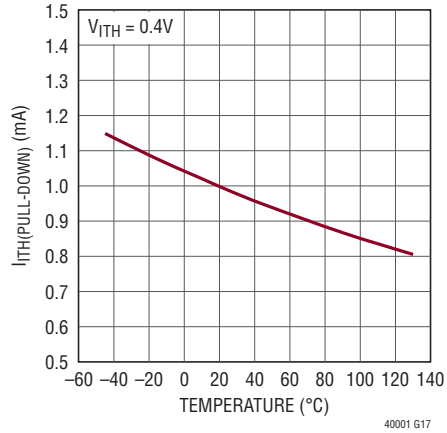
PowerPath Turn-Off Gate Voltage Over Temperature



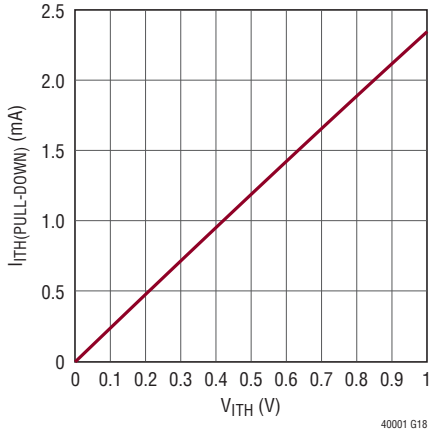
BIAS Voltage at 0.5mA Load Over Temperature



I_{TH} Pull-Down Current Over Temperature



I_{TH} Pull-Down Current vs V_{ITH}



PIN FUNCTIONS (QFN/SSOP)

VM (Pin 1/Pin 25): Voltage Monitor Input. High impedance input to an accurate comparator with a 1.193V threshold (typical). This pin controls the state of the $\overline{RST}$ output pin. Connect a resistor divider (R_{VM1}, R_{VM2}) between the monitored voltage and GND, with the center tap point connected to this pin. The falling threshold of the monitored voltage is calculated as follows:

$$V_{VM\_RST} = \frac{R_{VM1} + R_{VM2}}{R_{VM2}} \bullet 1.193V$$

where R_{VM2} is the bottom resistor between the VM pin and GND. Tie to the BIAS pin if voltage monitoring function is not used.

$\overline{RST}$ (Pin 2/Pin 26): High Voltage Open Drain Reset Output. When the voltage at the VM pin is below 1.193V, this status pin is pulled low. When driven low, this pin can disable a DC/DC converter when connected to the converter's enable pin. This pin can also drive an LED to provide a visual status indicator of a monitored voltage. Short this pin to GND when not used.

IIMON (Pin 3/Pin 27): Input Current Monitor. The voltage on this pin is 20 times (typical) the sense voltage ($V_{IN,CLN}$) across the input current sense resistor(R_{IS}), therefore providing a voltage proportional to the input current. Connect an appropriate capacitor to this pin to obtain a voltage representation of the time-average input current. Leave this pin open when input current monitoring function is not needed.

IFB (Pin 4/Pin 28): Input Voltage Feedback Pin. This pin is a high impedance input pin used to sense the input voltage level. In regulation, the input voltage loop sets the voltage on this feedback pin to 1.000V. When the input feedback voltage drops below 1.000V, the ITH pin is pulled down to reduce the load on the input source. Connect this pin to the center node of a resistor divider between the IN pin and GND to set the input voltage regulation level. This regulation level can then be obtained as follows:

$$V_{IN\_REG} = \left(\frac{R_{OFB1}}{R_{OFB2}} + 1\right) \bullet 1.000V$$

If the input voltage regulation feature is not used, connect the IFB pin to the BIAS pin.

ENC (Pin 5/Pin 1): Enable Charging Pin. High impedance digital input pin. Pull this pin above 1.5V to enable charging and below 0.5V to disable charging. Leaving this pin open causes the internal 2µA pull-up current to pull the pin to 2.5V (typical).

IBMON (Pin 6/Pin 2): Battery Charge Current Monitor. The voltage on this pin is 20 times (typical) the sense voltage ($V_{CSP,CSN}$) across the battery current sense resistor (R_{CS}), therefore providing a voltage proportional to the battery charge current. Connect an appropriate capacitor to this pin to obtain a voltage representation of the time-average battery charge current. Short this pin to GND to disable charge current limit feature.

CX (Pin 7/Pin 3): Charge Current Termination Programming. Connect the charge current termination programming resistor (R_{CX}) to this pin. This pin is a high impedance input to a comparator and sources 5µA of current. When the voltage on this pin is greater than the charge current monitor voltage (V_{IBMON}), the $\overline{CHRG}$ pin turns high impedance indicating that the CX threshold is reached. When this occurs, the charge current is immediately terminated if the TMR pin is shorted to the BIAS pin, otherwise charging continues until the charge termination timer expires. The charge current termination value is determined using the following formula:

$$I_{C/X} = \frac{\left(0.25\mu A \bullet R_{CX}\right) - 0.5mV}{R_{CS}}$$

Where R_{CS} is the sense resistor connected to the CSP and the CSN pins. Note that if $R_{CX} = R_{CL} \leq 19.1k\Omega$, where R_{CL} is the charge current programming resistor, then the charge current termination value is one tenth the full charge current, more familiarly known as C/10. Short this pin to GND to disable CX termination.

CL (Pin 8/Pin 4): Charge Current Limit Programming. Connect the charge current programming resistor (R_{CL}) to this pin. This pin sources 50µA of current. The regulation loop compares the voltage on this pin with the charge current monitor voltage (V_{IBMON}), and drives the ITH pin accordingly to ensure that the programmed charge current limit

PIN FUNCTIONS (QFN/SSOP)

is not exceeded. The charge current limit is determined using the following formula:

$$I_{CLIM} = 2.5\mu A \bullet \left(\frac{R_{CL}}{R_{CS}}\right)$$

Where R_{CS} is the sense resistor connected to the CSP and the CSN pins. Leave the pin open for the maximum charge current limit of $50mV/R_{CS}$.

TMR (Pin 9/Pin 5): Charge Timer. Attach 1nF of external capacitance (C_{TMR}) to GND for each 104 seconds of charge termination time and 26 seconds of bad battery indicator time. Short to GND to prevent bad battery indicator time and charge termination time from expiring – allowing a continuous trickle charge and top off float voltage regulation charge. Short to BIAS to disable bad battery detect and enable C/X charging termination.

GND (Pins 10, 28, 29/Pins 6, 24): Device Ground Pins. Connect the ground pins to a suitable PCB copper ground plane for proper electrical operation. The QFN package exposed pad must be soldered to PCB ground for rated thermal performance.

$\overline{FLT}$, $\overline{CHRG}$ (Pin 11, Pin 12/Pin 7, Pin 8): Charge Status Indicator Pins. These pins are high voltage open drain pull down pins. The $\overline{FLT}$ pin pulls down when there is an under or over temperature condition during charging or when the voltage on the BFB pin stays below the low battery threshold during charging for a period longer than the bad battery indicator time. The $\overline{CHRG}$ pin pulls down during a charging cycle. Please refer to the application information section for details on specific modes indicated by the combination of the states of these two pins. Pull up each of these pins with an LED in series with a resistor to a voltage source to provide a visual status indicator. Short these pins to GND when not used.

BIAS (Pin 13/Pin 9): 2.9V Regulator Output. Connect a capacitor of at least 470nF to bypass this 2.9V regulated voltage output. Use this pin to bias the resistor divider to set up the voltage at the NTC pin.

NTC (Pin 14/Pin 10): Thermistor Input. Connect a thermistor from NTC to GND, and a corresponding resistor from BIAS to NTC. The voltage level on this pin determines if the battery temperature is safe for charging. The charge current and charge timer are suspended if the thermistor indicates a temperature that is unsafe for charging. Once the temperature returns to the safe region, charging resumes. Leave the pin open or connected to a capacitor to disable the temperature qualified charging function.

FBG (Pin 15/Pin 11): Feedback Ground Pin. This is the ground return pin for the resistor dividers connected to the BFB and OFB pins. As soon as the voltage at IN is valid (>3V typical), this pin has a 100Ω resistance to GND. When the voltage at IN is not valid, this pin is disconnected from GND to ensure that the resistor dividers connected to the BFB and OFB pins do not continue to drain the battery when the battery is the only available power source.

BFB (Pin 16/Pin 12): Battery Feedback Voltage Pin. This pin is a high impedance input pin used to sense the battery voltage level. In regulation, the battery float voltage loop sets the voltage on this pin to 1.136V (typical). Connect this pin to the center node of a resistor divider between the BAT pin and the FBG pin to set the battery float voltage. The battery float voltage can then be obtained as follows:

$$V_{FLOAT} = \frac{R_{BFB2} + R_{BFB1}}{R_{BFB2}} \bullet 1.136V$$

BAT (Pin 17/Pin 13): Battery Pack Connection. Connect the battery to this pin. This pin is the anode of the battery ideal diode driver (the cathode is the CSN pin).

BGATE (Pin 18/Pin 14): External Battery PMOS Gate Drive Output. When not charging, the BGATE pin drives the external PMOS to behave as an ideal diode from the BAT pin (anode) to the CSN pin (cathode). This allows efficient delivery of any required additional power from the battery to the downstream system connected to the CSN pin.

When charging a heavily discharged battery, the BGATE pin is regulated to set the output feedback voltage (OFB pin) to 86% of the battery float voltage (0.974V typical). This allows the instant-on feature, providing an immediate valid voltage level at the output when the LTC4000-1 is charging a heavily discharged battery. Once the voltage on the OFB pin is above the 0.974V typical value, then the BGATE pin is driven low to ensure an efficient charging path from the CSN pin to the BAT pin.

PIN FUNCTIONS (QFN/SSOP)

CSN (Pin 19/Pin 15): Charge Current Sense Negative Input and Battery Ideal Diode Cathode. Connect a sense resistor between this pin and the CSP pin. The LTC4000-1 senses the voltage across this sense resistor and regulates it to a voltage equal to 1/20th (typical) of the voltage set at the CL pin. The maximum regulated sense voltage is 50mV. The CSN pin is also the cathode input of the battery ideal diode driver (the anode input is the BAT pin). Tie this pin to the CSP pin if no charge current limit is desired. Refer to the Applications Information section for complete details.

CSP (Pin 20/Pin 16): Charge Current Sense Positive Input and Input Ideal Diode Cathode. Connect a sense resistor between this pin and the CSN pin for charge current sensing and regulation. This input should be tied to CSN to disable the charge current regulation function. This pin is also the cathode of the input ideal diode driver (the anode is the IID pin).

OFB (Pin 21/Pin 17): Output Feedback Voltage Pin. This pin is a high impedance input pin used to sense the output voltage level. In regulation, the output voltage loop sets the voltage on this feedback pin to 1.193V. Connect this pin to the center node of a resistor divider between the CSP pin and the FBG pin to set the output voltage when battery charging is terminated and all the output load current is provided from the input. The output voltage can then be obtained as follows:

$$V_{OUT} = \frac{R_{OFB2} + R_{OFB1}}{R_{OFB2}} \bullet 1.193V$$

When charging a heavily discharged battery (such that $V_{OFB} < V_{OUT(INST\_ON)}$), the battery PowerPath PMOS connected to BGATE is regulated to set the voltage on this feedback pin to 0.974V (approximately 86% of the battery float voltage). The instant-on output voltage is then as follows:

$$V_{OUT(INST\_ON)} = \frac{R_{OFB2} + R_{OFB1}}{R_{OFB2}} \bullet 0.974V$$

IGATE (Pin 22/Pin 18): Input PMOS Gate Drive Output. The IGATE pin drives the external PMOS to behave as an ideal diode from the IID pin (anode) to the CSP pin (cathode) when the voltage at the IN pin is within its operating range (3V to 60V). To ensure that the input PMOS is turned off when the IN pin voltage is not within its operating range, connect a 10M resistor from this pin to the CSP pin.

IID (Pin 23/Pin 19): Input Ideal Diode Anode. This pin is the anode of the input ideal diode driver (the cathode is the CSP pin).

ITH (Pin 24/Pin 20): High Impedance Control Voltage Pin. When any of the regulation loops (input voltage, charge current, battery float voltage or the output voltage) indicate that its limit is reached, the ITH pin will sink current (up to 1mA) to regulate that particular loop at the limit. In many applications, this ITH pin is connected to the control/compensation node of a DC/DC converter. Without any external pull-up, the operating voltage range on this pin is GND to 2.5V. With an external pull-up, the voltage on this pin can be pulled up to 6V. Note that the impedance connected to this pin affects the overall loop gain. For details, refer to the Applications Information section.

CC (Pin 25/Pin 21): Converter Compensation Pin. Connect an R-C network from this pin to the ITH pin to provide a suitable loop compensation for the converter used. Refer to the Applications Information section for discussion and procedure on choosing an appropriate R-C network for a particular DC/DC converter.

CLN (Pin 26/Pin 22): Input Current Sense Negative Input. Connect a sense resistor between this pin and the IN pin. The LTC4000-1 senses the voltage across this sense resistor and sets the voltage on the IIMON pin equal to 20 times this voltage. Tie this pin to the IN pin if the input current monitoring feature is not used. Refer to the Applications Information section for complete details.

IN (Pin 27/Pin 23): Input Supply Voltage: 3V to 60V. Supplies power to the internal circuitry and the BIAS pin. Connect the power source to the downstream system and the battery charger to this pin. This pin is also the positive sense pin for the input current monitor. Connect a sense resistor between this pin and the CLN pin. Tie this pin to CLN if the input current monitoring feature is not used. A local 0.1µF bypass capacitor to ground is recommended on this pin.

BLOCK DIAGRAM

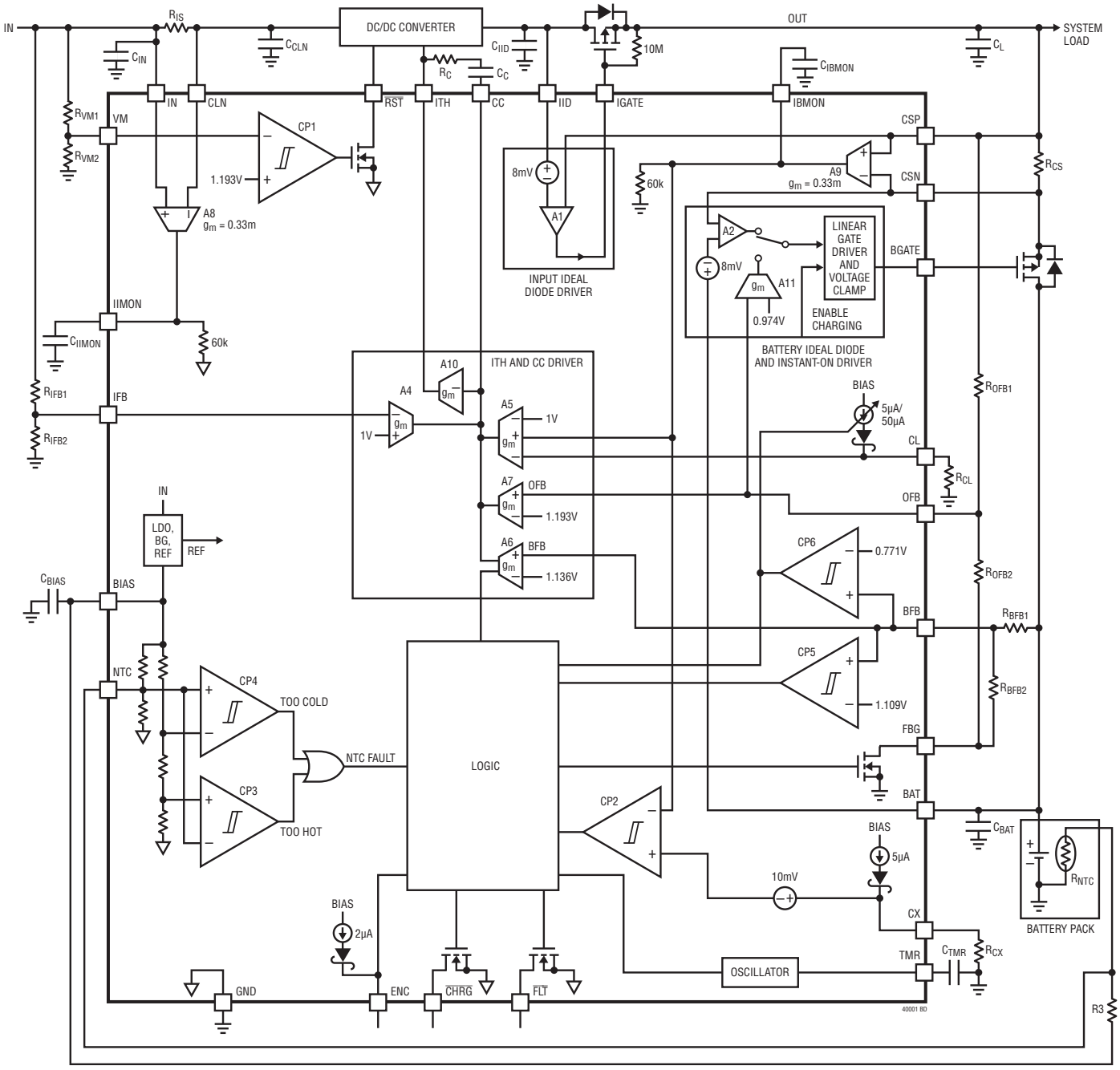


Figure 1. LTC4000-1 Functional Block Diagram

OPERATION

Overview

The LTC4000-1 is designed to simplify the conversion of any externally compensated DC/DC converter into a high performance battery charger with PowerPath control. It only requires the DC/DC converter to have a control or external-compensation pin (usually named VC or ITH) whose voltage level varies in a positive monotonic way with its output. The output variable can be either output voltage or output current. For the following discussion, refer to the Block Diagram in Figure 1.

The LTC4000-1 includes four different regulation loops: input voltage, charge current, battery float voltage and output voltage (A4-A7). Whichever loop requires the lowest voltage on the ITH pin for its regulation controls the external DC/DC converter.

The input voltage regulation loop ensures that the input voltage level does not drop below the programmed level. The charge current regulation loop ensures that the programmed battery charge current limit (using a resistor at CL) is not exceeded. The float voltage regulation loop ensures that the programmed battery stack voltage (using a resistor divider from BAT to FBG via BFB) is not exceeded. The output voltage regulation loop ensures that the programmed system output voltage (using a resistor divider from CSP to FBG via OFB) is not exceeded. The LTC4000-1 also provides monitoring pins for the input current and charge current at the IIMON and IBMON pins respectively.

The LTC4000-1 features an ideal diode controller at the input from the IID pin to the CSP pin and a PowerPath controller at the output from the BAT pin to the CSN pin. The output PowerPath controller behaves as an ideal diode controller when not charging. When charging, the output PowerPath controller has two modes of operation. If V_{OFB} is greater than $V_{OUT(INST\_ON)}$, BGATE is driven low. When V_{OFB} is less than $V_{OUT(INST\_ON)}$, a linear regulator implements the instant-on feature. This feature provides regulation of the BGATE pin so that a valid voltage level is immediately available at the output when the LTC4000-1 is charging an over-discharged, dead or short faulted battery.

The state of the ENC pin determines whether charging is enabled. When ENC is grounded, charging is disabled and the battery float voltage loop is disabled. Charging is enabled when the ENC pin is left floating or pulled high (≥1.5V)

The LTC4000-1 offers several user configurable battery charge termination schemes. The TMR pin can be configured for either C/X termination, charge timer termination or no termination. After a particular charge cycle terminates, the LTC4000-1 features an automatic recharge cycle if the battery voltage drops below 97.6% of the programmed float voltage.

Trickle charge mode drops the charge current to one tenth of the normal charge current (programmed using a resistor from the CL pin to GND) when charging into an over discharged or dead battery. When trickle charging, a capacitor on the TMR pin can be used to program a time out period. When this bad battery timer expires and the battery voltage fails to charge above the low battery threshold (V_{LOBAT}), the LTC4000-1 will terminate charging and indicate a bad battery condition through the status pins ($\overline{FLT}$ and $\overline{CHRG}$).

The LTC4000-1 also includes an NTC pin, which provides temperature qualified charging when connected to an NTC thermistor thermally coupled to the battery pack. To enable this feature, connect the thermistor between the NTC and the GND pins, and a corresponding resistor from the BIAS pin to the NTC pin. The LTC4000-1 also provides a charging status indicator through the $\overline{FLT}$ and the $\overline{CHRG}$ pins.

Aside from biasing the thermistor-resistor network, the BIAS pin can also be used for a convenient pull up voltage. This pin is the output of a low dropout voltage regulator that is capable of providing up to 0.5mA of current. The regulated voltage on the BIAS pin is available as soon as the IN pin is within its operating range (≥3V).

Input Ideal Diode

The input ideal diode feature provides low loss conduction and reverse blocking from the IID pin to the CSP pin. This reverse blocking prevents reverse current from the output (CSP pin) to the input (IID pin) which causes unnecessary drain on the battery and in some cases may result in unexpected DC/DC converter behavior.

The ideal diode behavior is achieved by controlling an external PMOS connected to the IID pin (drain) and the

OPERATION

CSP pin (source). The controller (A1) regulates the external PMOS by driving the gate of the PMOS device such that the voltage drop across IID and CSP is 8mV (typical). When the external PMOS ability to deliver a particular current with an 8mV drop across its source and drain is exceeded, the voltage at the gate clamps at $V_{IGATE(ON)}$ and the PMOS behaves like a fixed value resistor ($R_{DS(ON)}$).

Note that this input ideal diode function is only enabled when the voltage at the IN pin is within its operating range (3V to 60V). To ensure that the external PMOS is turned off when the voltage at the IN pin is not within is operating range, a 10M pull-up resistor between the IGATE and the CSP pin is recommended.

Input Voltage Regulation

One of the loops driving the ITH and CC pins is the input voltage regulation loop (Figure 2). This loop prevents the input voltage from dropping below the programmed level.

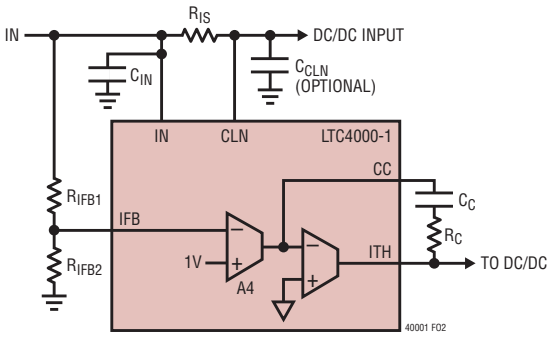


Figure 2. Input Voltage Regulation Loop

When the input source is high impedance, the input voltage drops as the load current increases. In that case there exists a voltage level at which the available power from the input is maximum. For example, solar panels often specify V_{MP}, corresponding to the panel voltage at which maximum power is achieved. With the LTC4000-1 input voltage regulation, this maximum power voltage level can be programmed at the IFB pin. The input voltage regulation loop regulates ITH to ensure that the input voltage level does not drop below this programmed level.

Battery Charger Overview

In addition to the input voltage regulation loop, the LTC4000-1 regulates charge current, battery voltage and output voltage.

When a battery charge cycle begins, the battery charger first determines if the battery is over-discharged. If the battery feedback voltage is below V_{LOBAT}, an automatic trickle charge feature uses the charge current regulation loop to set the battery charge current to 10% of the programmed full-scale value. If the TMR pin is connected to a capacitor or open, the bad battery detection timer is enabled. When this bad battery detection timer expires and the battery voltage is still below V_{LOBAT}, the battery charger automatically terminates and indicates, via the $\overline{FLT}$ and $\overline{CHRG}$ pins, that the battery was unresponsive to charge current.

Once the battery voltage is above V_{LOBAT}, the charge current regulation loop begins charging in full power constant-current mode. In this case, the programmed full charge current is set with a resistor on the CL pin.

Depending on available input power and external load conditions, the battery charger may not be able to charge at the full programmed rate. The external load is always prioritized over the battery charge current. The input voltage programming is always observed, and only additional power is available to charge the battery. When system loads are light, battery charge current is maximized.

Once the float voltage is achieved, the battery float voltage regulation loop takes over from the charge current regulation loop and initiates constant voltage charging. In constant voltage charging, charge current slowly declines.

Charge termination can be configured with the TMR pin in several ways. If the TMR pin is tied to the BIAS pin, C/X termination is selected. In this case, charging is terminated when constant voltage charging reduces the charge current to the C/X level programmed at the CX pin. Connecting a capacitor to the TMR pin selects the charge timer termination and a charge termination timer is started at the beginning of constant voltage charging. Charging terminates when the termination timer expires. When continuous charging at the float voltage is desired, tie the TMR pin to GND to disable termination.

Upon charge termination, the PMOS connected to BGATE behaves as an ideal diode from BAT to CSN. The diode function prevents charge current but provides current to the system load as needed. If the system load can be completely supplied from the input, the battery PMOS turns

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off. While terminated, if the input voltage loop is not in regulation, the output voltage regulation loop takes over to ensure that the output voltage at CSP remains in control. The output voltage regulation loop regulates the voltage at the CSP pin such that the output feedback voltage at the OFB pin is 1.193V.

If the system load requires more power than is available from the input, the battery ideal diode controller provides supplemental power from the battery. When the battery voltage discharges below 97.1% of the float voltage ($V_{BFB} < V_{RECHRG(FALL)}$), the automatic recharge feature initiates a new charge cycle.

Charge Current Regulation

The first loop involved in a normal charging cycle is the charge current regulation loop (Figure 3). This loop drives the ITH and CC pins. This loop ensures that the charge current sensed through the charge current sense resistor (R_{CS}) does not exceed the programmed full charge current.

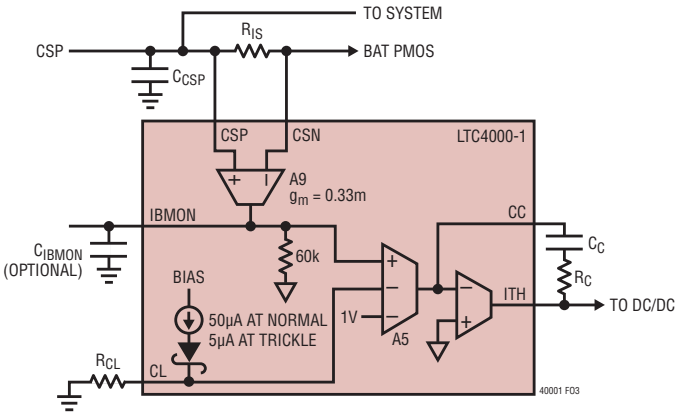

Figure 3. Charge Current Regulation Loop

Battery Voltage Regulation

Once the float voltage is reached, the battery voltage regulation loop takes over from the charge current regulation loop (Figure 4).

The float voltage level is programmed using the feedback resistor divider between the BAT pin and the FBG pin with the center node connected to the BFB pin. Note that the ground return of the resistor divider is connected to the FBG pin. The FBG pin disconnects the resistor divider load when $V_{IN} < 3V$ to ensure that the float voltage resistor divider does not consume battery current when the battery is the only available power source. For $V_{IN} \geq 3V$, the typical resistance from the FBG pin to GND is 100Ω.

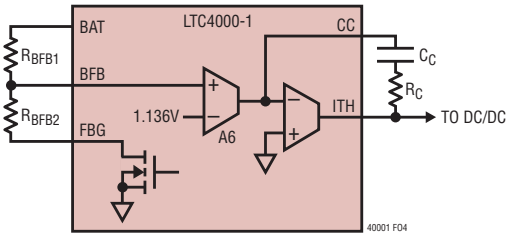

Figure 4. Battery Float Voltage Regulation Loop with FBG

Output Voltage Regulation

When charging terminates and the system load is completely supplied from the input, the PMOS connected to BGATE is turned off. In this scenario, the output voltage regulation loop takes over from the battery float voltage regulation loop (Figure 5). The output voltage regulation loop regulates the voltage at the CSP pin such that the output feedback voltage at the OFB pin is 1.193V.

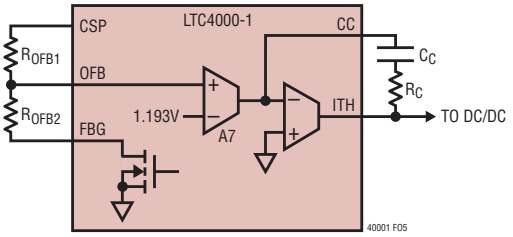

Figure 5. Output Voltage Regulation Loop with FBG

Battery Instant-On and Ideal Diode

The LTC4000-1 controls the external PMOS connected to the BGATE pin with a controller similar to the input ideal diode controller driving the IGATE pin. When not charging, the PMOS behaves as an ideal diode between the BAT (anode) and the CSN (cathode) pins. The controller (A2) regulates the external PMOS to achieve low loss conduction by driving the gate of the PMOS device such that the voltage drop from the BAT pin to the CSN pin is 8mV. When the ability to deliver a particular current with an 8mV drop across the PMOS source and drain is exceeded, the voltage at the gate clamps at $V_{BGATE(ON)}$ and the PMOS behaves like a fixed value resistor ($R_{DS(ON)}$).

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The ideal diode behavior allows the battery to provide current to the load when the input supply is in current limit or the DC/DC converter is slow to react to an immediate load increase at the output. In addition to the ideal diode behavior, BGATE also allows current to flow from the CSN pin to the BAT pin during charging.

There are two regions of operation when current is flowing from the CSN pin to the BAT pin. The first is when charging into a battery whose voltage is below the instant-on threshold ($V_{OFB} < V_{OUT(INST\_ON)}$). In this region of operation, the controller regulates the voltage at the CSP pin to be approximately 86% of the final float voltage level ($V_{OUT(INST\_ON)}$). This feature provides a CSP voltage significantly higher than the battery voltage when charging into a heavily discharged battery. This instant-on feature allows the LTC4000-1 to provide sufficient voltage at the output (CSP pin), independent of the battery voltage.

The second region of operation is when the battery feedback voltage is greater than or equal to the instant-on threshold ($V_{OUT(INST\_ON)}$). In this region, the BGATE pin is driven low and clamped at $V_{BGATE(ON)}$ to allow the PMOS to turn completely on, reducing any power dissipation due to the charge current.

Battery Temperature Qualified Charging

The battery temperature is measured by placing a negative temperature coefficient (NTC) thermistor close to the battery pack. The comparators CP3 and CP4 implement the temperature detection as shown in the Block Diagram in Figure 1. The rising threshold of CP4 is set at 75% of V_{BIAS} (cold threshold) and the falling threshold of CP3 is set at 35% of V_{BIAS} (hot threshold). When the voltage at the NTC pin is above 75% of V_{BIAS} or below 35% of V_{BIAS} then the LTC4000-1 pauses any charge cycle in progress. When the voltage at the NTC pin returns to the range of 40% to 70% of V_{BIAS}, charging resumes.

When charging is paused, the external charging PMOS turns off and charge current drops to zero. If the LTC4000-1 is charging in the constant voltage mode and the charge termination timer is enabled, the timer pauses until the thermistor indicates a return to a valid temperature. If the battery charger is in the trickle charge mode and the bad battery detection timer is enabled, the bad battery timer pauses until the thermistor indicates a return to a valid temperature.

Input UVLO and Voltage Monitoring

The regulated voltage on the BIAS pin is available as soon as $V_{IN} \geq 3V$. When $V_{IN} \geq 3V$, the FBG pin is pulled low to GND with a typical resistance of 100Ω and the rest of the chip functionality is enabled.

When the IN pin is high impedance and a battery is connected to the BAT pin, the BGATE pin is pulled down with a 2µA (typical) current source to hold the battery PMOS gate voltage at $V_{BGATE(ON)}$ below V_{BAT}. This allows the battery to power the output. The total quiescent current consumed by LTC4000-1 from the battery when IN is not valid is typically ≤ 10µA.

When the IN pin is high impedance, the input ideal diode function for the external FET connected to the IGATE pin is disabled. To ensure that this FET is completely turned off when the voltage at the IN pin is not within its operating range, connect a 10M pull-up resistor between the IGATE pin and the CSP pin.

Besides the internal input UVLO, the LTC4000-1 also provides voltage monitoring through the VM pin. The $\overline{RST}$ pin is pulled low when the voltage on the VM pin falls below 1.193V (typical). On the other hand, when the voltage on the VM pin rises above 1.233V (typical), the $\overline{RST}$ pin is high impedance.

One common use of this voltage monitoring feature is to ensure that the converter is turned off when the voltage at the input is below a certain level. In this case, connect the $\overline{RST}$ pin to the DC/DC converter chip select or enable pin (see Figure 6).

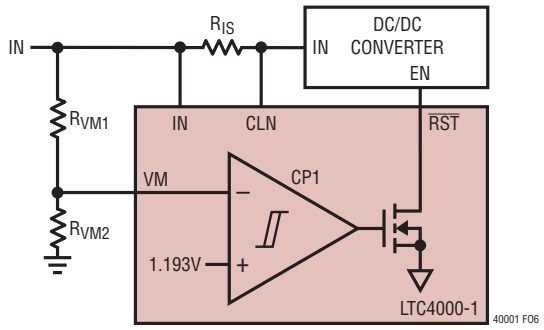

Figure 6. Input Voltage Monitoring with $\overline{RST}$ Connected to the EN Pin of the DC/DC Converter

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Input Ideal Diode PMOS Selection

The input external PMOS is selected based on the expected maximum current, power dissipation and reverse voltage drop. The PMOS must be able to withstand a gate to source voltage greater than $V_{IGATE(ON)}$ (15V maximum) or the maximum regulated voltage at the IID pin, whichever is less. A few appropriate external PMOS for a number of different requirements are shown at Table 1.

Table 1. PMOS

PART NUMBER	$R_{DS(ON)}$ AT V_{GS} = 10V (Ω)	MAX ID (A)	MAX VDS (V)	MANUFACTURER
SiA923EDJ	0.054	4.5	–20	Vishay
Si9407BDY	0.120	4.7	–60	Vishay
Si4401BDY	0.014	10.5	–40	Vishay
Si4435DDY	0.024	11.4	–30	Vishay
SUD19P06-60	0.060	18.3	–60	Vishay
Si7135DP	0.004	60	–30	Vishay

Note that in general the larger the capacitance seen on the IGATE pin, the slower the response of the ideal diode driver. The fast turn off and turn on current is limited to –0.5mA and 0.7mA typical respectively ($I_{IGATE(FASTOFF)}$ and $I_{IGATE(FASTON)}$). If the driver can not react fast enough to a sudden increase in load current, most of the extra current is delivered through the body diode of the external PMOS. This increases the power dissipation momentarily. It is important to ensure that the PMOS is able to withstand this momentary increase in power dissipation.

The operation section also mentioned that an external 10M pull-up resistor is recommended between the IGATE pin and the CSP pin when the IN pin voltage is expected to be out of its operating range, at the same time that the external input ideal diode PMOS is expected to be completely turned off. Note that this additional pull-up resistor increases the forward voltage regulation of the ideal diode function ($V_{IID,CSP}$) from the typical value of 8mV.

The increase in this forward voltage is calculated according to the following formula:

$$\Delta V_{IID,CSP}\ REG = V_{GSON} \bullet 20k/R_{IGATE}$$

where V_{GSON} is the source to gate voltage required to achieve the desired ON resistance of the external PMOS and R_{IGATE} is the external pull-up resistor from the IGATE pin to the CSP pin. Therefore, for a 10M R_{IGATE} resistor and assuming a 10V V_{GSON}, the additional forward voltage regulation is $\Delta V_{IID,CSP}$ REG = 20mV, and the total forward voltage regulation is 28mV (typ). It is recommended to set the R_{IGATE} such that this additional forward voltage regulation value does not exceed 40mV.

Input Current Monitoring

The input current through the sense resistor is available for monitoring through the IIMON pin. The voltage on the IIMON pin varies with the current through the sense resistor as follows:

$$V_{IIMON} = 20 \bullet I_{RIS} \bullet R_{IS} = 20 \bullet (V_{IN} - V_{CLN})$$

If the input current is noisy, add a filter capacitor to the CLN pin to reduce the AC content. For example, when using a buck DC/DC converter, the use of a C_{CLN} capacitor is strongly recommended. Where the highest accuracy is important, pick the value of C_{CLN} such that the AC content is less than or equal to 50% of the average voltage across the sense resistor.

The voltage on the IIMON pin can be filtered further by putting a capacitor on the pin (C_{IIMON}).

Charge Current Limit Setting and Monitoring

The regulated full charge current is set according to the following formula:

$$R_{CS} = \frac{V_{CL}}{20 \bullet I_{CLIM}}$$

where V_{CL} is the voltage on the CL pin. The CL pin is internally pulled up with an accurate current source of 50µA. Therefore, an equivalent formula to obtain the charge current limit is:

$$R_{CL} = \frac{I_{CLIM} \bullet R_{CS}}{2.5\mu A} \Rightarrow I_{CLIM} = \frac{R_{CL}}{R_{CS}} \bullet 2.5\mu A$$

The charge current through the sense resistor is available for monitoring through the IBMON pin. The voltage on the IBMON pin varies with the current through the sense resistor as follows:

$$V_{IBMON} = 20 \bullet I_{RCS} \bullet R_{CS} = 20 \bullet (V_{CSP} - V_{CSN})$$

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The regulation voltage level at the IBMON pin is clamped at 1V with an accurate internal reference. At 1V on the IBMON pin, the charge current limit is regulated to the following value:

$$I_{CLIM(MAX)}(A) = \frac{0.050V}{R_{CS}(\Omega)}$$

When this maximum charge current limit is desired, leave the CL pin open or set it to a voltage >1.05V such that amplifier A5 can regulate the IBMON pin voltage accurately to the internal reference of 1V.

When the output current waveform of the DC/DC converter or the system load current is noisy, it is recommended that a capacitor is connected to the CSP pin (C_{CSP}). This is to reduce the AC content of the current through the sense resistor (R_{CS}). Where the highest accuracy is important, pick the value of C_{CSP} such that the AC content is less than or equal to 50% of the average voltage across the sense resistor. Similar to the IIMON pin, the voltage on the IBMON pin is filtered further by putting a capacitor on the pin (C_{IBMON}). This filter capacitor should *not* be arbitrarily large as it will slow down the overall compensated charge current regulation loop. For details on the loop compensation, refer to the Compensation section.

Battery Float Voltage Programming

When the value of R_{BFB1} is much larger than 100Ω, the final float voltage is determined using the following formula:

$$R_{BFB1} = \left(\frac{V_{FLOAT}}{1.136V} - 1\right) R_{BFB2}$$

When higher accuracy is important, a slightly more accurate final float voltage can be determined using the following formula:

$$V_{FLOAT} = \left(\frac{R_{BFB1} + R_{BFB2}}{R_{BFB2}} \bullet 1.136V\right) - \left(\frac{R_{BFB1}}{R_{BFB2}} \bullet V_{FBG}\right)$$

where V_{FBG} is the voltage at the FBG pin during float voltage regulation, which accounts for all the current from all resistor dividers that are connected to this pin (R_{FBG} = 100Ω typical).

Low Battery Trickle Charge Programming and Bad Battery Detection

When charging into an over-discharged or dead battery ($V_{BFB} < V_{LOBAT}$), the pull-up current at the CL pin is reduced to 10% of the normal pull-up current. Therefore, the trickle charge current is set using the following formula:

$$R_{CL} = \frac{I_{CLIM(TRKL)} \bullet R_{CS}}{0.25\mu A} \Rightarrow I_{CLIM(TRKL)} = 0.25\mu A \bullet \frac{R_{CL}}{R_{CS}}$$

Therefore, when 50µA•R_{CL} is less than 1V, the following relation is true:

$$I_{CLIM(TRKL)} = \frac{I_{CLIM}}{10}$$

Once the battery voltage rises above the low battery voltage threshold, the charge current level rises from the trickle charge current level to the full charge current level.

The LTC4000-1 also features bad battery detection. This detection is disabled if the TMR pin is grounded or tied to BIAS. However, when a capacitor is connected to the TMR pin, a bad battery detection timer is started as soon as trickle charging starts. If at the end of the bad battery detection time the battery voltage is still lower than the low battery threshold, charging is terminated and the part indicates a bad battery condition by pulling the $\overline{FLT}$ pin low and leaving the $\overline{CHRG}$ pin high impedance.

The bad battery detection time can be programmed according to the following formula:

$$C_{TMR}(nF) = t_{BADBAT}(h) \bullet 138.5$$

Note that once a bad battery condition is detected, the condition is latched. In order to re-enable charging, remove the battery and connect a new battery whose voltage causes BFB to rise above the recharge battery threshold ($V_{RECHRG(RISE)}$). Alternatively toggle the ENC pin or remove and reapply power to IN.

C/X Detection, Charge Termination and Automatic Recharge

Once the constant voltage charging is reached, there are two ways in which charging can terminate. If the TMR pin is tied to BIAS, the battery charger terminates as soon as

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the charge current drops to the level programmed by the CX pin. The C/X current termination level is programmed according to the following formula:

$$R_{CX} = \frac{(I_{C/X} \bullet R_{CS}) + 0.5mV}{0.25\mu A} \Rightarrow I_{C/X} = \frac{(0.25\mu A \bullet R_{CX}) - 0.5mV}{R_{CS}}$$

where R_{CS} is the charge current sense resistor connected between the CSP and the CSN pins.

When the voltage at BFB is higher than the recharge threshold (97.6% of float), the C/X comparator is enabled. In order to ensure proper C/X termination coming out of a paused charging condition, connect a capacitor on the CX pin according to the following formula:

$$C_{CX} = 100C_{BGATE}$$

where C_{BGATE} is the total capacitance connected to the BGATE pin.

For example, a typical capacitance of 1nF requires a capacitor greater than 100nF connected to the CX pin to ensure proper C/X termination behavior.

If a capacitor is connected to the TMR pin, as soon as the constant voltage charging is achieved, a charge termination timer is started. When the charge termination timer expires, the charge cycle terminates. The total charge termination time can be programmed according to the following formula:

$$C_{TMR}(nF) = t_{TERMINATE}(h) \bullet 34.6$$

If the TMR pin is grounded, charging never terminates and the battery voltage is held at the float voltage. Note that regardless of which termination behavior is selected, the $\overline{CHRG}$ and $\overline{FLT}$ pins will both assume a high impedance state as soon as the charge current falls below the programmed C/X level.

After the charger terminates, the LTC4000-1 automatically restarts another charge cycle if the battery feedback voltage drops below 97.1% of the programmed final float voltage ($V_{RECHRG(FALL)}$). When charging restarts, the $\overline{CHRG}$ pin pulls low and the $\overline{FLT}$ pin remains high impedance.

Output Voltage Regulation Programming

The output voltage regulation level is determined using the following formula:

$$R_{OFB1} = \left(\frac{V_{OUT}}{1.193} - 1\right) \bullet R_{OFB2}$$

As in the battery float voltage calculation, when higher accuracy is important, a slightly more accurate output is determined using the following formula:

$$V_{OUT} = \left(\frac{R_{OFB1} + R_{OFB2}}{R_{OFB2}} \bullet 1.193V\right) - \left(\frac{R_{OFB1}}{R_{OFB2}} \bullet V_{FBG}\right)$$

where V_{FBG} is the voltage at the FBG pin during output voltage regulation, which accounts for all the current from all resistor dividers that are connected to this pin.

Battery Instant-On and Ideal Diode External PMOS Consideration

The instant-on voltage level is determined using the following formula:

$$V_{OUT(INST\_ON)} = \frac{R_{OFB1} + R_{OFB2}}{R_{OFB2}} \bullet 0.974V$$

Note that R_{OFB1} and R_{OFB2} are the same resistors that program the output voltage regulation level. Therefore, the output voltage regulation level is always 122.5% of the instant-on voltage level.

During instant-on operation, it is critical to consider the charging PMOS power dissipation. When the battery voltage is below the low battery threshold (V_{LOBAT}), the power dissipation in the PMOS can be calculated as follows:

$$P_{TRKL} = [0.86 \bullet V_{FLOAT} - V_{BAT}] \bullet I_{CLIM(TRKL)}$$

where $I_{CLIM(TRKL)}$ is the trickle charge current limit.

On the other hand, when the battery voltage is above the low battery threshold but still below the instant-on threshold, the power dissipation can be calculated as follows:

$$P_{INST\_ON} = [0.86 \bullet V_{FLOAT} - V_{BAT}] \bullet I_{CLIM}$$

where I_{CLIM} is the full scale charge current limit.

For example, when charging a 3-cell Lithium Ion battery with a programmed full charged current of 1A, the float voltage is 12.6V, the bad battery voltage level is 8.55V and the instant-on voltage level is 10.8V. During instant-on operation and in the trickle charge mode, the worst case

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maximum power dissipation in the PMOS is 1.08W. When the battery voltage is above the bad battery voltage level, then the worst case maximum power dissipation is 2.25W.

When overheating of the charging PMOS is a concern, it is recommended that the user add a temperature detection circuit that pulls down on the NTC pin. This pauses charging whenever the external PMOS temperature is too high. A sample circuit that performs this temperature detection function is shown in Figure 7.

Similar to the input external PMOS, the charging external PMOS must be able to withstand a gate to source voltage greater than $V_{BGATE(ON)}$ (15V maximum) or the maximum regulated voltage at the CSP pin, whichever is less. Consider the expected maximum current, power dissipation and instant-on voltage drop when selecting this PMOS. The PMOS suggestions in Table 1 are an appropriate starting point depending on the application.

Float Voltage, Output Voltage and Instant-On Voltage Dependencies

The formulas for setting the float voltage, output voltage and instant-on voltage are repeated here:

$$V_{FLOAT} = \frac{R_{BFB1} + R_{BFB2}}{R_{BFB2}} \bullet 1.136V$$

$$V_{OUT} = \frac{R_{OFB1} + R_{OFB2}}{R_{OFB2}} \bullet 1.193V$$

$$V_{OUT(INST\_ON)} = \frac{R_{OFB1} + R_{OFB2}}{R_{OFB2}} \bullet 0.974V$$

In the typical application, V_{OUT} is set higher than V_{FLOAT} to ensure that the battery is charged fully to its intended float voltage. On the other hand, V_{OUT} should not be programmed too high since $V_{OUT(INST\_ON)}$, the minimum voltage on CSP, depends on the same resistors R_{OFB1} and R_{OFB2} that set V_{OUT}. As noted before, this means that the output voltage regulation level is always 122.5% of the instant-on voltage. The higher the programmed value of $V_{OUT(INST\_ON)}$, the larger the operating region when the charger PMOS is driven in the linear region where it is less efficient.

If R_{OFB1} and R_{OFB2} are set to be equal to R_{BFB1} and R_{BFB2} respectively, then the output voltage is set at 105% of the float voltage and the instant-on voltage is set at 86% of the float voltage. Figure 8 shows the range of possible

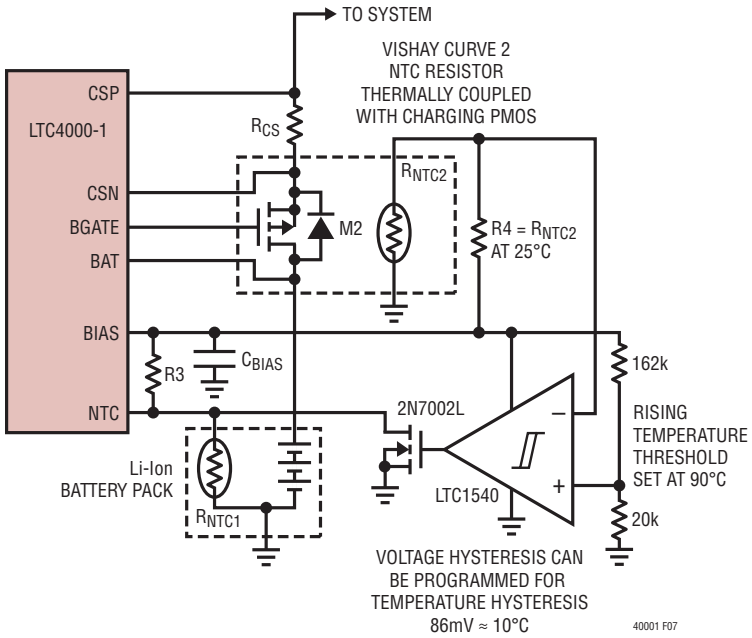

Figure 7. Charging PMOS Overtemperature Detection Circuit Protecting PMOS from Overheating

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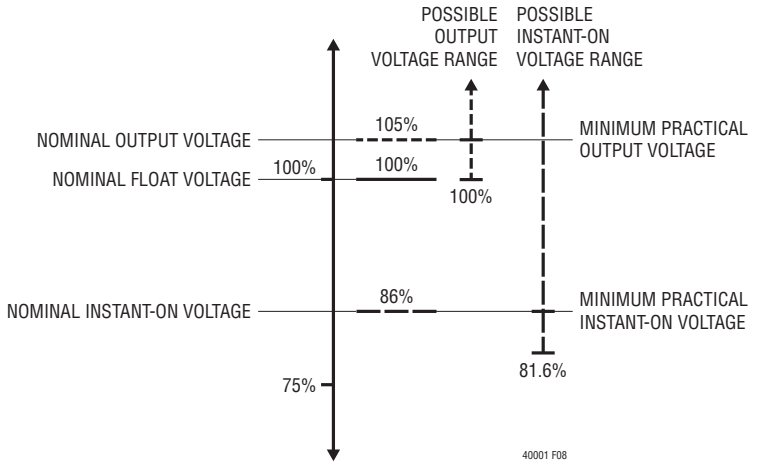

Figure 8. Possible Voltage Ranges for V_{OUT} and $V_{OUT(INST\_ON)}$ in Ideal Scenario

output voltages that can be set for $V_{OUT(INST\_ON)}$ and V_{OUT} with respect to V_{FLOAT} to ensure the battery can be fully charged in an ideal scenario.

Taking into account possible mismatches between the resistor dividers as well as mismatches in the various regulation loops, V_{OUT} should not be programmed to be less than 105% of V_{FLOAT} to ensure that the battery can be fully charged. This automatically means that the instant-on voltage level should not be programmed to be less than 86% of V_{FLOAT}.

Battery Temperature Qualified Charging

To use the battery temperature qualified charging feature, connect an NTC thermistor, R_{NTC}, between the NTC pin and the GND pin, and a bias resistor, R3, from the BIAS pin to the NTC pin (Figure 9). Thermistor manufacturer datasheets usually include either a temperature lookup table or a formula relating temperature to the resistor value at that corresponding temperature.

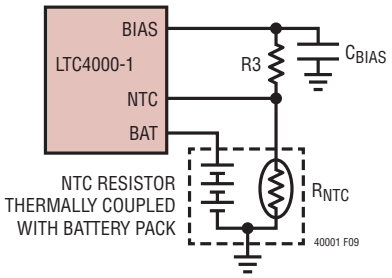

Figure 9. NTC Thermistor Connection

In a simple application, R3 is a 1% resistor with a value equal to the value of the chosen NTC thermistor at 25°C (R25). In this simple setup, the LTC4000-1 will pause charging when the resistance of the NTC thermistor drops to 0.54 times the value of R25. For a Vishay Curve 2 thermistor, this corresponds to approximately 41.5°C. As the temperature drops, the resistance of the NTC thermistor rises. The LTC4000-1 is also designed to pause charging when the value of the NTC thermistor increases to three times the value of R25. For a Vishay Curve 2 thermistor, this corresponds to approximately –1.5°C. With Vishay Curve 2 thermistor, the hot and cold comparators each have approximately 5°C of hysteresis to prevent oscillation about the trip point.

The hot and cold threshold can be adjusted by changing the value of R3. Instead of simply setting R3 to be equal to R25, R3 is set according to one of the following formulas:

$$R3 = \frac{R_{NTC}\ \text{at cold\_threshold}}{3}$$

or

$$R3 = 1.857 \bullet R_{NTC}\ \text{at hot\_threshold}$$

Notice that with only one degree of freedom (i.e. adjusting the value of R3), the user can only use one of the formulas above to set either the cold or hot threshold but not both. If the value of R3 is set to adjust the cold threshold, the value of the NTC resistor at the hot threshold is then

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equal to 0.179 • R_{NTC} at cold_threshold. Similarly, if the value of R3 is set to adjust the hot threshold, the value of the NTC resistor at the cold threshold is then equal to 5.571 • R_{NTC} at cold_threshold.

Note that changing the value of R3 to be larger than R25 will move both the hot and cold threshold lower and vice versa. For example, using a Vishay Curve 2 thermistor whose nominal value at 25°C is 100k, the user can set the cold temperature to be at 5°C by setting the value of R3 = 75k, which automatically then sets the hot threshold at approximately 50°C.

It is possible to adjust the hot and cold threshold independently by introducing another resistor as a second degree of freedom (Figure 10). The resistor R_D in effect reduces the sensitivity of the resistance between the NTC pin and ground. Therefore, intuitively this resistor will move the hot threshold to a hotter temperature and the cold threshold to a colder temperature.

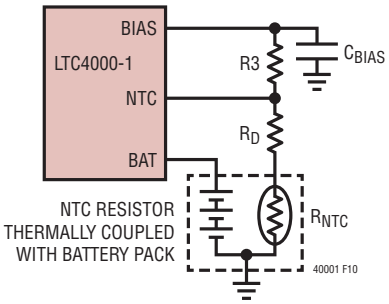

Figure 10. NTC Thermistor Connection with Desensitizing Resistor R_D

The value of R3 and R_D can now be set according to the following formula:

$$R3 = \frac{R_{NTC}\ \text{at cold\_threshold} - R_{NTC}\ \text{at hot\_threshold}}{2.461}$$

$$R_D = 0.219 \bullet R_{NTC}\ \text{at cold\_threshold} - 1.219 \bullet R_{NTC}\ \text{at hot\_threshold}$$

Note the important caveat that this method can only be used to desensitize the thermal effect on the thermistor and hence push the hot and cold temperature thresholds apart from each other. When using the formulas above, if the user finds that a negative value is needed for R_D, the two temperature thresholds selected are too close to each other and a higher sensitivity thermistor is needed.

For example, this method can be used to set the hot and cold thresholds independently to 60°C and –5°C. Using a Vishay Curve 2 thermistor whose nominal value at 25°C is 100k, the formula results in R3 = 130k and R_D = 41.2k for the closest 1% resistors values.

To increase thermal sensitivity such that the valid charging temperature band is much smaller than 40°C, it is possible to put a PTC (positive thermal coefficient) resistor in series with R3 between the BIAS pin and the NTC pin. This PTC resistor also needs to be thermally coupled with the battery. Note that this method increases the number of thermal sensing connections to the battery pack from one wire to three wires. The exact value of the nominal PTC resistor required can be calculated using a similar method as described above, keeping in mind that the threshold at the NTC pin is always 75% and 35% of V_{BIAS}.

Leaving the NTC pin floating or connecting it to a capacitor disables all NTC functionality.

Battery Voltage Temperature Compensation

Some battery chemistries have charge voltage requirements that vary with temperature. Lead-acid batteries in particular experience a significant change in charge voltage requirements as temperature changes. For example, manufacturers of large lead-acid batteries recommend a float charge of 2.25V/cell at 25°C. This battery float voltage, however, has a temperature coefficient which is typically specified at –3.3mV/°C per cell.

The LTC4000-1 employs a resistor feedback network to program the battery float voltage. manipulation of this network makes for an efficient implementation of various temperature compensation schemes of battery float voltage.

A simple solution for tracking such a linear voltage dependence on temperature is to use the LM234 3-terminal temperature sensor. This creates an easily programmable linear temperature dependent characteristic.

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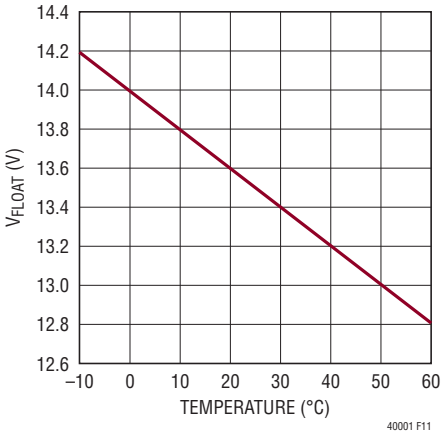

Figure 11. Lead-Acid 6-Cell Float Charge Voltage vs Temperature Using LM234 with the Feedback Network

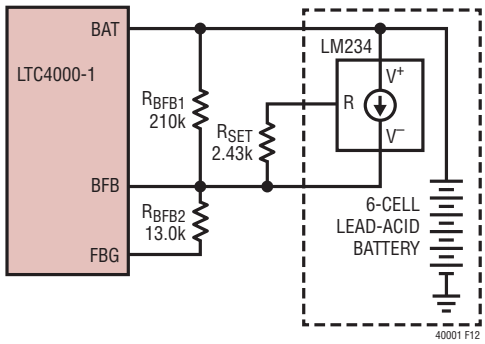

Figure 12. Battery Voltage Temperature Compensation Circuit

In the circuit shown in Figure 12,

$$R_{BFB1} = -R_{SET} \bullet (TC \bullet 4405)$$

and

$$R_{BFB2} = \frac{R_{BFB1} \bullet 1.136V}{\left(V_{FLOAT(25°C)} + R_{BFB1} \bullet \left(\frac{0.0677}{R_{SET}}\right)\right) - 1.136V}$$

Where: TC = temperature coefficient in V/°C and $V_{FLOAT(25°C)}$ is the desired battery float voltage at 25°C in V.

For example, a 6-cell lead-acid battery has a float charge voltage that is commonly specified at 2.25V/cell at 25°C or 13.5V, and a –3.3mV/°C per cell temperature coefficient or –19.8mV/°C. Substituting these two parameters (TC = –19.8mV/°C and $V_{FLOAT(25°C)}$ = 13.5V) and R_{SET} = 2.43k into the equation, we obtained the following values: R_{BFB1} = 210k and R_{BFB2} = 13.0k.

3-Step Charging for Lead-Acid Battery

The LTC4000-1 naturally lends itself to charging applications requiring a constant current step followed by constant voltage. Furthermore, the LTC4000-1 additional features such as trickle charging, bad battery detection and C/X or timer termination makes it an excellent fit for Lithium based battery charging applications. Figure 13 and Table 2 show the normal steps involved in Lithium battery charging.

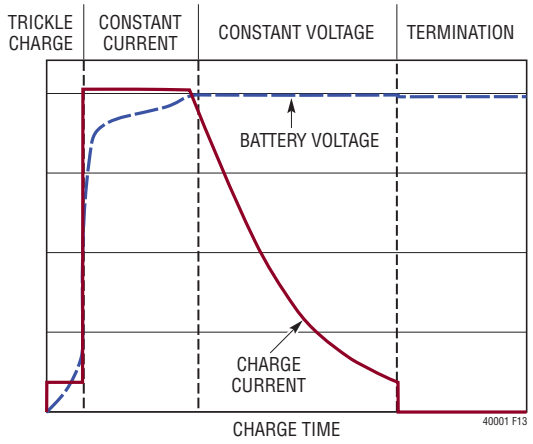

Figure 13. Li-Ion Typical Charging Cycle

Table 2. Lithium Based Battery Charging Steps

STEP	CHARGE METHOD	DURATION
Trickle Charge	Constant Current at a Lower Current Value, Usually 1/10th of Full Charge Current	Until Battery Voltage Rises Above Low Battery Threshold
		Time Limit Set at TMR Pin
Constant Current	Constant Current at Full Charge Current	Until Battery Voltage Reaches Float Voltage
		No Time Limit
Constant Voltage	Constant Voltage	Terminate Either When Charge Current Falls to the Programmed Level at the CX Pin or after the Termination Timer at TMR Pin Expires
Recharge	Initiate Constant Current Again When Battery Voltage Drops Below Recharge Threshold	

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On the other hand, the LTC4000-1 is also easily configurable to handle lead-acid based battery charging. One of the common methods used in lead-acid battery charging is called 3-step charging (Bulk, Absorption and Float). Figure 14 and Table 3 summarize the normal steps involved in a typical 3-step charging of a lead-acid battery.

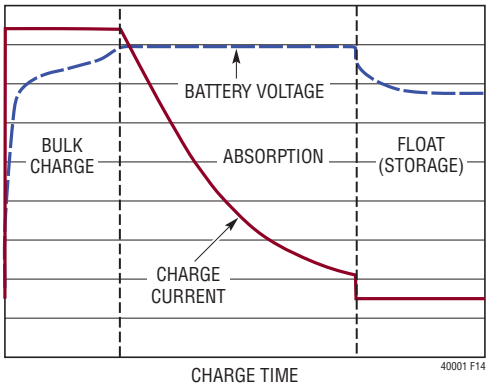

Figure 14. Lead-Acid 3-Step Charging Cycle

Table 3. Lead-Acid Battery Charging Steps

STEP	CHARGE METHOD	DURATION
Bulk Charge	Constant Current	Until Battery Voltage Reaches Absorption Voltage
		No Time Limit
Absorption	Constant Voltage at the Absorption Voltage Level	Terminate When Charge Current Falls to the Programmed Level at the CX Pin
Float (Storage)	Constant Voltage at the Lower Float Voltage Level (Float Voltage Is Lower than the Absorption Voltage)	Indefinite
Recharge	Initiate Bulk Charge Again When Battery Voltage Drops Below Recharge Threshold	

Figure 15 shows the configuration needed to implement this 3-step lead-acid battery charging with the LTC4000-1.

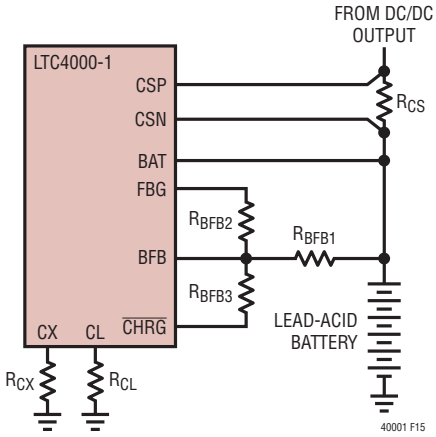

Figure 15. 3-Step Lead-Acid Circuit Configuration

When a charging cycle is initiated, the $\overline{CHRG}$ pin is pulled low. The charger first enters the bulk charge step, charging the battery with a constant current programmed at the CL pin:

$$I_{CLIM} = \frac{MIN(50mV, 2.5\mu A \bullet R_{CL})}{R_{CS}}$$

When the battery voltage rises to the Absorption voltage level:

$$V_{ABSRP} = \left(\frac{R_{BFB1}(R_{BFB2} + R_{BFB3})}{R_{BFB2}R_{BFB3}} + 1\right) \bullet 1.136V$$

the charger enters the Absorption step, charging the battery at a constant voltage at this absorption voltage level.

As the charge current drops to the C/X level:

$$I_{CLIM} = \frac{(0.25\mu A \bullet R_{CX}) - 0.5mV}{R_{CS}}$$

the $\overline{CHRG}$ pin turns high impedance and now the charger enters the Float (Storage) step, charging the battery voltage at the constant float voltage level:

$$V_{FLOAT} = \left(\frac{R_{BFB1}}{R_{BFB2}} + 1\right) \bullet 1.136V$$

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Note that in this configuration, the recharge threshold is 97.6% of the float voltage level. When the battery voltage drops below this level, the whole 3-step charging cycle is reinitiated starting with the bulk charge.

Some systems require trickle charging of an over discharged lead-acid battery. This feature can be included using the CL pin of the LTC4000-1. In the configuration shown in Figure 15, when the battery voltage is lower than 68% of the Absorption level, the pull-up current on the CL pin is reduced to 10% of the normal pull-up current. Therefore, the trickle charge current can be set at the following level:

$$I_{CLIM} = \frac{MIN(50mV, 0.25\mu A \bullet R_{CL})}{R_{CS}}$$

If this feature is not desired, leave the CL pin open to set the regulation voltage across the charge current sense resistor (RCS) always at 50mV.

The $\overline{FLT}$ and $\overline{CHRG}$ Indicator Pins

The $\overline{FLT}$ and $\overline{CHRG}$ pins in the LTC4000-1 provide status indicators. Table 4 summarizes the mapping of the pin states to the part status.

Table 4. $\overline{FLT}$ and $\overline{CHRG}$ Status Indicator

$\overline{FLT}$	$\overline{CHRG}$	STATUS
0	0	NTC Over Ranged – Charging Paused
1	0	Charging Normally
0	1	Charging Terminated and Bad Battery Detected
1	1	$V_{IBMON} < (V_{C/X} – 10mV)$

where 1 indicates a high impedance state and 0 indicates a low impedance pull-down state.

Note that $V_{IBMON} < (V_{CX} – 10mV)$ corresponds to charge termination only if the C/X termination is selected. If the charger timer termination is selected, constant voltage charging may continue for the remaining charger timer period even after the indicator pins indicate that $V_{IBMON} < (V_{CX} – 10mV)$. This is also true when no termination is selected, constant voltage charging will continue even after the indicator pins indicate that $V_{IBMON} < (V_{CX} – 10mV)$.

The BIAS Pin

For ease of use the LTC4000-1 provides a low dropout voltage regulator output on the BIAS pin. Designed to provide up to 0.5mA of current at 2.9V, this pin requires at least 470nF of low ESR bypass capacitance for stability.

Use the BIAS pin as the pull-up source for the NTC resistor networks, since the internal reference for the NTC circuitry is based on a ratio of the voltage on the BIAS pin. Furthermore, various 100k pull-up resistors can be conveniently connected to the BIAS pin.

Setting the Input Voltage Monitoring Resistor Divider

The falling threshold voltage level for this monitoring function can be calculated as follows:

$$R_{VM1} = \left(\frac{V_{VM\_RST}}{1.193V} – 1\right) \bullet R_{VM2}$$

where R_{VM1} and R_{VM2} form a resistor divider connected between the monitored voltage and GND, with the center tap point connected to the VM pin as shown in Figure 6. The rising threshold voltage level can be calculated similarly.

Input Voltage Programming

Connecting a resistor divider from V_{IN} to the IFB pin enables programming of a minimum input supply voltage. This feature is typically used to program the peak power voltage for a high impedance input source. Referring to Figure 2, the input voltage regulation level is determined using the following formula:

$$R_{IFB1} = \left(\frac{V_{IN\_REG}}{1V} – 1\right) R_{IFB2}$$

Where V_{IN_REG} is the minimum regulation input voltage level, below which the current draw from the input source is reduced.

Combining the Input Voltage Programming and the Input Voltage Monitoring Resistor Divider

When connected to the same input voltage node, the input voltage monitoring and the input voltage regulation resistor divider can be combined (see Figure 16).

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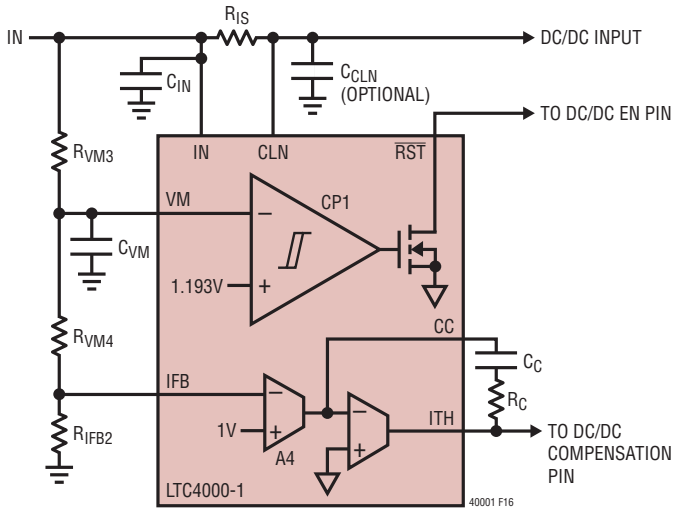

Figure 16. Input Voltage Monitoring and Input Voltage Regulation Resistor Divider Combined

In this configuration use the following formula to determine the values of the three resistors:

$$R_{VM3} = \left(1 - \frac{1.193V}{V_{VM\_RST}}\right)\left(\frac{V_{IN\_REG}}{1V}\right)R_{IFB2}$$

$$R_{VM4} = \left(1.193\left(\frac{V_{IN\_REG}}{V_{VM\_RST}}\right) - 1\right)R_{IFB2}$$

Note that for the R_{VM4} value to be positive, the ratio of V_{IN_REG} to V_{VM_RST} has to be greater than 0.838.

When the RST pin of the LTC4000-1 is connected to the $\overline{SHDN}$ or RUN pin of the converter, it is recommended that the value of V_{IN_REG} is set higher than the V_{VM_RST} pin by a significant margin. This is to ensure that any voltage noise or ripple on the input supply pin does not cause the RST pin to shut down the converter prematurely, preventing the input regulation loop from functioning as expected.

As discussed in the input current monitoring section, noise issues on the input node can be reduced by placing a large filter capacitor on the CLN node (C_{CLN}). To further reduce the effect of any noise on the monitoring function, another filter capacitor placed on the VM pin (C_{VM}) is recommended.

MPPT Temperature Compensation – Solar Panel Example

The input regulation loop of the LTC4000-1 allows a user to program a minimum input supply voltage regulation level allowing for high impedance source to provide maximum available power. With typical high impedance source such as a solar panel, this maximum power point varies with temperature.

A typical solar panel is comprised of a number of series-connected cells, each cell being a forward-biased p-n junction. As such, the open-circuit voltage (V_{OC}) of a solar cell has a temperature coefficient that is similar to a common p-n junction diode, about –2mV/°C. The peak power point voltage (V_{MP}) for a crystalline solar panel can be approximated as a fixed percentage of V_{OC}, so the temperature coefficient for the peak power point is similar to that of V_{OC}.

Panel manufacturers typically specify the 25°C values for V_{OC}, V_{MP} and the temperature coefficient for V_{OC}, making determination of the temperature coefficient for V_{MP} of a typical panel straight forward.

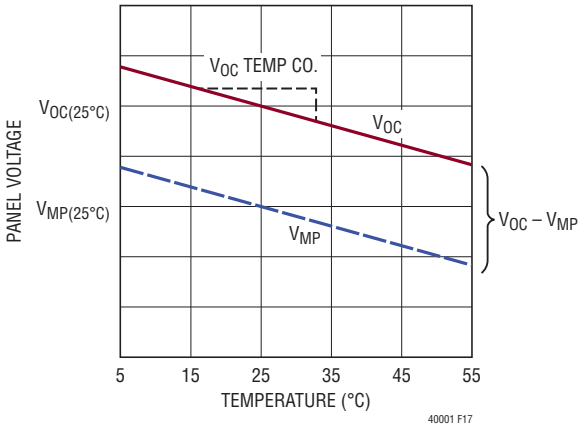

Figure 17. Temperature Characteristic of a Solar Panel Open Circuit and Peak Power Point Voltages

In a manner similar to the battery float voltage temperature compensation, implementation of the MPPT temperature compensation can be accomplished by incorporating an LM234 into the input voltage feedback network. Using the

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feedback network in Figure 18, a similar set of equations can be used to determine the resistor values:

$$R_{IFB1} = -R_{SET} \bullet (TC \bullet 4405)$$

and

$$R_{IFB2} = \frac{R_{IFB1} \bullet 1V}{\left(V_{MP(25°C)} + R_{IFB1} \bullet \left(\frac{0.0677}{R_{SET}}\right)\right) - 1V}$$

Where: TC = temperature coefficient in V/°C, and $V_{MP(25°C)}$ = maximum power point voltage at 25°C in V.

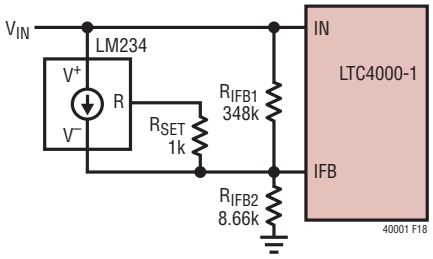

Figure 18. Maximum Power Point Voltage Temperature Compensation Feedback Network

For example, given a common 36-cell solar panel that has the following specified characteristics:

Open circuit voltage (V_{OC}) = 21.7V

Maximum power voltage (V_{MP}) = 17.6V

Open-circuit voltage temperature coefficient (V_{OC}) = –78mV/°C

As the temperature coefficient for V_{MP} is similar to that of V_{OC}, the specified temperature coefficient for V_{OC} (TC) of –78mV/°C and the specified peak power voltage ($V_{MP(25°C)}$) of 17.6V can be inserted into the equations to calculate the appropriate resistor values for the temperature compensation network in Figure 18. With R_{SET} equal to 1kΩ, then:

R_{SET} = 1kΩ, R_{IFB1} = 348kΩ, R_{IFB2} = 8.66kΩ.

Compensation

In order for the LTC4000-1 to control the external DC/DC converter, it has to be able to overcome the sourcing bias current of the ITH or VC pin of the DC/DC converter. The typical sinking capability of the LTC4000-1 at the ITH pin is 1mA at 0.4V with a maximum voltage range of 0V to 6V.

It is imperative that the local feedback of the DC/DC converter be set up such that during regulation of any of the LTC4000-1 loops this local loop is out of regulation and sources as much current as possible from its ITH/VC pin. For example for a DC/DC converter regulating its output voltage, it is recommended that the converter feedback divider is programmed to be greater than 110% of the output voltage regulation level programmed at the OFB pin.

There are four feedback loops to consider when setting up the compensation for the LTC4000-1. As mentioned before these loops are: the input voltage loop, the charge current loop, the float voltage loop and the output voltage loop. All of these loops have an error amp (A4-A7) followed by another amplifier (A10) with the intermediate node driving the CC pin and the output of A10 driving the ITH pin as shown in Figure 19. The most common compensation network of a series capacitor (C_C) and resistor (R_C) between the CC pin and the ITH pin is shown here.

Each of the loops has slightly different dynamics due to differences in the feedback signal path. The analytic description of the input voltage regulation loop is included in the Appendix section. Please refer to the LTC4000 data sheet for the analytic description of the other three loops. In most situations, an alternative empirical approach to compensation, as described here, is more practical.

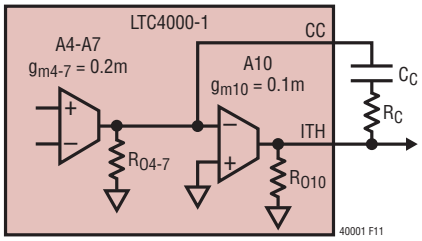

Figure 19. Error Amplifier Followed by Output Amplifier Driving CC and ITH Pins

Empirical Loop Compensation

Based on the analytical expressions and the transfer function from the ITH pin to the input and output current of the external DC/DC converter, the user can analytically

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determine the complete loop transfer function of each of the loops. Once these are obtained, it is a matter of analyzing the gain and phase bode plots to ensure that there is enough phase and gain margin at unity crossover with the selected values of R_C and C_C for all operating conditions.

Even though it is clear that an analytical compensation method is possible, sometimes certain complications render this method difficult to tackle. These complications include the lack of easy availability of the switching converter transfer function from the ITH or VC control node to its input or output current, and the variability of parameter values of the components such as the ESR of the output capacitor or the $R_{DS(ON)}$ of the external PFETs.

Therefore a simpler and more practical way to compensate the LTC4000-1 is provided here. This empirical method involves injecting an AC signal into the loop, observing the loop transient response and adjusting the C_C and R_C values to quickly iterate towards the final values. Much of the detail of this method is derived from Application Note 19 which can be found at www.linear.com using AN19 in the search box.

Figure 20 shows the recommended setup to inject an AC-coupled output load variation into the loop. A function generator with 50Ω output impedance is coupled through a 50Ω/1000µF series RC network to the regulator output. Generator frequency is set at 50Hz. Lower frequencies may cause a blinking scope display and higher frequencies may not allow sufficient settling time for the output transient. Amplitude of the generator output is typically set at $5V_{P-P}$ to generate a $100mA_{P-P}$ load variation. For lightly loaded outputs (I_{OUT} < 100mA), this level may be too high for small signal response. If the positive and negative transition settling waveforms are significantly different, amplitude should be reduced. Actual amplitude is not particularly important because it is the shape of the resulting regulator output waveform which indicates loop stability.

A 2-pole oscilloscope filter with f = 10kHz is used to block switching frequencies. Regulators without added LC output filters have switching frequency signals at their outputs which may be much higher amplitude than the low frequency settling waveform to be studied. The filter frequency is high enough for most applications to pass the settling waveform with no distortion.

Oscilloscope and generator connections should be made exactly as shown in Figure 20 to prevent ground loop errors. The oscilloscope is synced by connecting the channel B probe to the generator output, with the ground clip of the second probe connected to exactly the same place as channel A ground. The standard 50Ω BNC sync output of the generator should not be used because of ground loop errors. It may also be necessary to isolate either the generator or oscilloscope from its third wire (earth

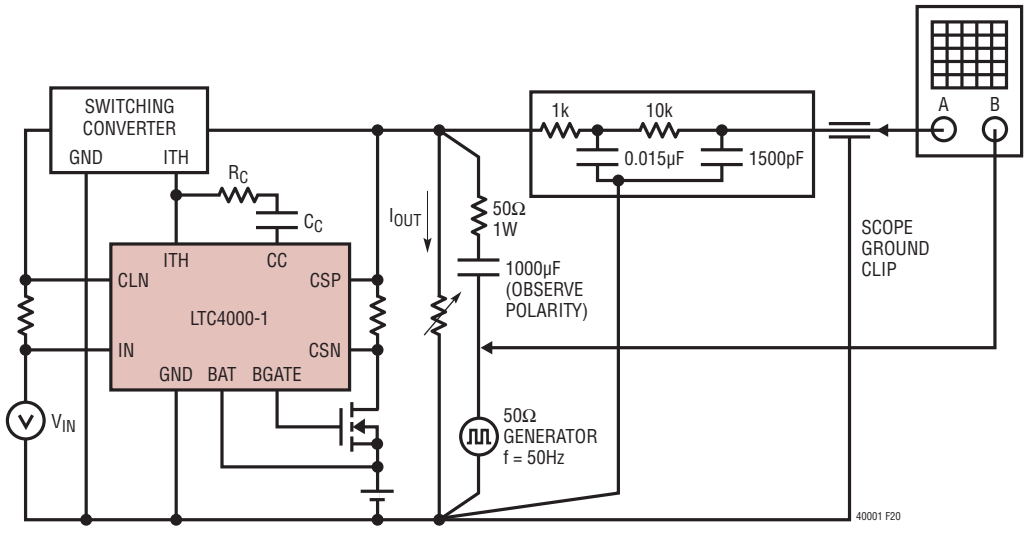

Figure 20. Empirical Loop Compensation Setup

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ground) connection in the power plug to prevent ground loop errors in the scope display. These ground loop errors are checked by connecting channel A probe tip to exactly the same point as the probe ground clip. Any reading on channel A indicates a ground loop problem.

Once the proper setup is made, finding the optimum values for the frequency compensation network is fairly straightforward. Initially, C_C is made large (≥1µF) and R_C is made small (≈10k). This nearly always ensures that the regulator will be stable enough to start iteration. Now, if the regulator output waveform is single-pole over damped (see the waveforms in Figure 21), the value of C_C is reduced in steps of about 2:1 until the response becomes slightly under damped. Next, R_C is increased in steps of 2:1 to introduce a loop zero. This will normally improve damping and allow the value of C_C to be further reduced. Shifting back and forth between R_C and C_C variations will allow one to quickly find optimum values.

If the regulator response is under damped with the initial large value of C_C, R_C should be increased immediately before larger values of C_C are tried. This will normally bring about the over damped starting condition for further iteration.

The optimum values for R_C and C_C normally means the smallest value for C_C and the largest value for R_C which still guarantee well damped response, and which result in the largest loop bandwidth and hence loop settling that is as rapid as possible. The reason for this approach is that it minimizes the variations in output voltage caused by input ripple voltage and output load transients.

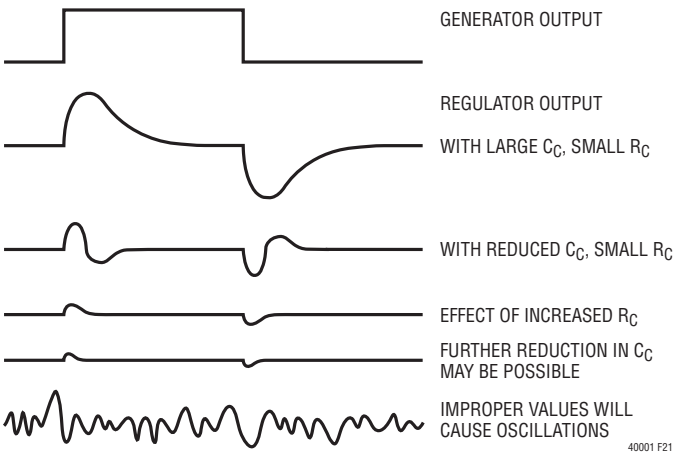

Figure 21. Typical Output Transient Response at Various Stability Level

A switching regulator which is grossly over damped will never oscillate, but it may have unacceptably large output transients following sudden changes in input voltage or output loading. It may also suffer from excessive overshoot problems on startup or short circuit recovery. To guarantee acceptable loop stability under all conditions, the initial values chosen for R_C and C_C should be checked under all conditions of input voltage and load current. The simplest way of accomplishing this is to apply load currents of minimum, maximum and several points in between. At each load current, input voltage is varied from minimum to maximum while observing the settling waveform.

If large temperature variations are expected for the system, stability checks should also be done at the temperature extremes. There can be significant temperature variations in several key component parameters which affect stability; in particular, input and output capacitor value and their ESR, and inductor permeability. The external converter parametric variations also need some consideration especially the transfer function from the ITH/VC pin voltage to the output variable (voltage or current). The LTC4000-1 parameters that vary with temperature include the transconductance and the output resistance of the error amplifiers (A4-A7). For modest temperature variations, conservative over damping under worst-case room temperature conditions is usually sufficient to guarantee adequate stability at all temperatures.

One measure of stability margin is to vary the selected values of both R_C and C_C by 2:1 in all four possible combinations. If the regulator response remains reasonably well damped under all conditions, the regulator can be considered fairly tolerant of parametric variations. Any tendency towards an under damped (ringing) response indicates that a more conservative compensation may be needed.

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DESIGN EXAMPLE

In this design example, the LTC4000-1 is paired with the LT3845A buck converter to create a 10A, 3-cell $LiFePO_4$ battery charger. The circuit is shown on the front page and is repeated here in Figure 22.

- With R_{IFB2} set at 20k, the input voltage monitoring falling threshold is set at 15V and the input voltage regulation level is set at 17.6V according to the following formulas:

$$R_{VM3} = \left(1 - \frac{1.193V}{15V}\right)\left(\frac{17.6V}{1V}\right)20k\Omega = 324k\Omega$$

$$R_{VM4} = \left(1.193V\left(\frac{17.6V}{15V}\right) - 1\right)20k\Omega = 8.06k\Omega$$

- The input current sense resistor is set at 5mΩ. Therefore, the voltage at the IIMON pin is related to the input current according to the following formula:

$$V_{IIMON} = (0.1\Omega) \bullet I_{RIS}$$

- R_{CL} is set at 24.9kΩ such that the voltage at the CL pin is 1.25V. Similar to the IIMON pin, the regulation voltage on the IBMON pin is clamped at 1V with an accurate internal reference. Therefore, the charge current limit is set at 10A according to the following formula:

$$I_{CLIM(MAX)} = \frac{0.050V}{R_{CS}} = \frac{0.050V}{5m\Omega} = 10A$$

- The trickle charge current level is consequently set at 1.25A, according to the following formula:

$$I_{CLIM(TRKL)} = 0.25\mu A \bullet \frac{24.9k\Omega}{5m\Omega} = 1.25A$$

- The battery float voltage is set at 10.8V according to the following formula:

$$R_{BFB1} = \left(\frac{10.8}{1.136} - 1\right) \bullet 133k\Omega \approx 1.13M\Omega$$

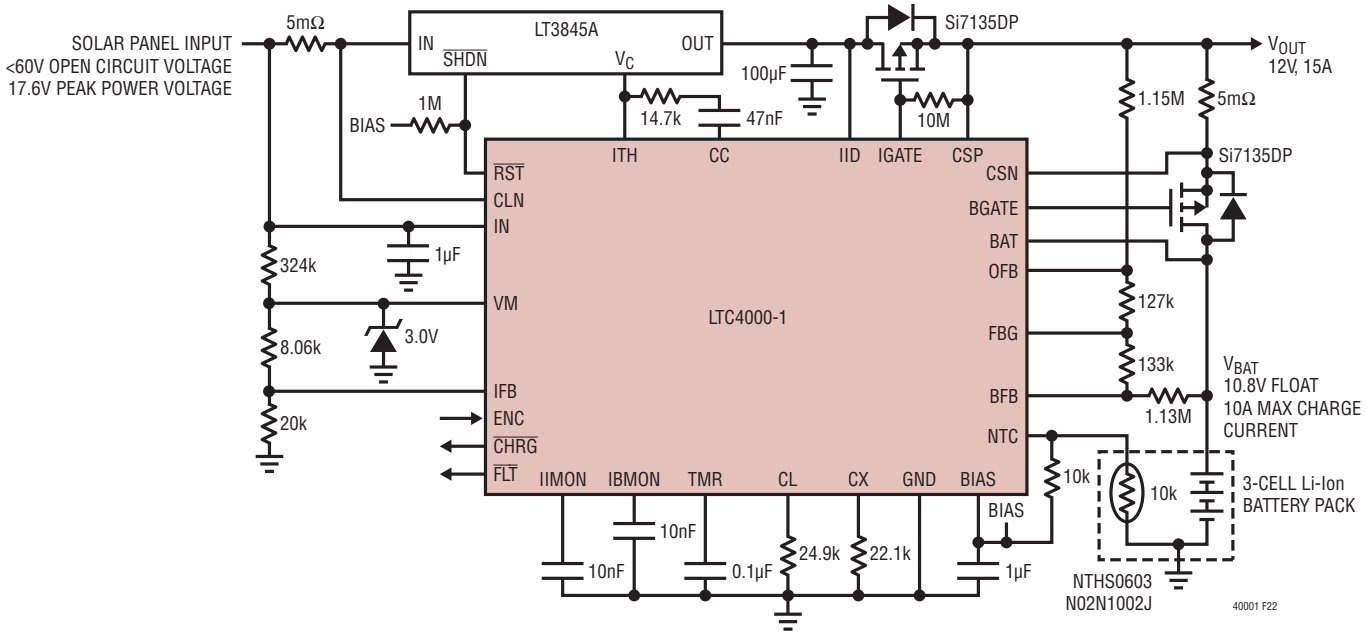

Figure 22. 10.8V at 10A Charger for Three $LiFePO_4$ Cells with Solar Panel Input

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- The bad battery detection time is set at 43 minutes according to the following formula:

$$C_{TMR}(nF) = t_{BADBAT}(h) \bullet 138.5 = \frac{43}{60} \bullet 138.5 = 100nF$$

- The charge termination time is set at 2.9 hours according to the following formula:

$$C_{TMR}(nF) = t_{TERMINATE}(h) \bullet 34.6 = 2.9 \bullet 34.6 = 100nF$$

- The C/X current termination level is programmed at 1A according to the following formula:

$$R_{CX} = \frac{(1A \bullet 5m\Omega) + 0.5mV}{0.25\mu A} \approx 22.1k\Omega$$

Note that in this particular solution, the timer termination is selected since a capacitor connects to the TMR pin. Therefore, this C/X current termination level only applies to the $\overline{CHRG}$ indicator pin.

- The output voltage regulation level is set at 12V according to the following formula:

$$R_{OFB1} = \left(\frac{12}{1.193} - 1\right) \bullet 127k\Omega \approx 1.15M\Omega$$

- The instant-on voltage level is consequently set at 9.79V according to the following formula:

$$V_{INST\_ON} = \frac{1150k\Omega + 127k\Omega}{127k\Omega} \bullet 0.974V = 9.79V$$

The worst-case power dissipation during instant-on operation can be calculated as follows:

- During trickle charging:

$$P_{TRKL} = [0.86 \bullet V_{FLOAT} - V_{BAT}] \bullet I_{CLIM\_TRKL}$$
$$= [0.86 \bullet 10.8] \bullet 1A$$
$$= 9.3W$$

- And beyond trickle charging:

$$P_{INST\_ON} = [0.86 \bullet V_{FLOAT} - V_{BAT}] \bullet I_{CLIM}$$
$$= [0.86 \bullet 10.8 - 7.33] \bullet 10A$$
$$= 19.3W$$

Therefore, depending on the layout and heat sink available to the charging PMOS, the suggested PMOS over temperature detection circuit included in Figure 7 may need to be included.

- The range of valid temperature for charging is set at –1.5°C to 41.5°C by picking a 10k Vishay Curve 2 NTC thermistor that is thermally coupled to the battery, and connecting this in series with a regular 10k resistor to the BIAS pin.

- For compensation, the procedure described in the empirical loop compensation section is followed. As recommended, first a 1µF C_C and 10k R_C is used, which sets all the loops to be stable. For an example of typical transient responses, the charge current regulation loop when V_{OFB} is regulated to $V_{OUT(INST\_ON)}$ is used here. Figure 23 shows the recommended setup to inject a DC-coupled charge current variation into this particular loop. The input to the CL pin is a square wave at 70Hz with the low level set at 120mV and the high level set at 130mV, corresponding to a 1.2A and 1.3A charge current (100mA charge current step). Therefore, in this particular example the trickle charge current regulation stability is examined. Note that the nominal trickle charge current in this example is programmed at 1.25A (R_{CL} = 24.9kΩ).

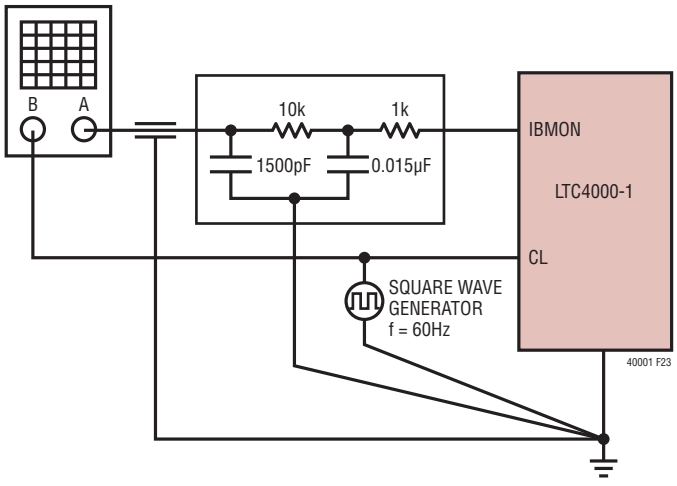

Figure 23. Charge Current Regulation Loop Compensation Setup

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With C_C = 1µF, R_C = 10k at V_{IN} = 20V, V_{BAT} = 7V, V_{CSP} regulated at 9.8V and a 0.2A output load condition at CSP, the transient response for a 100mA charge current step observed at IBMON is shown in Figure 24.

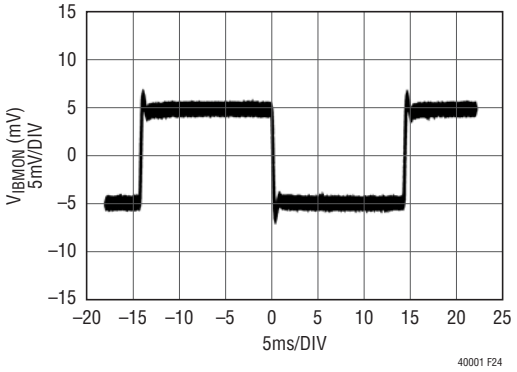

Figure 24. Transient Response of Charge Current Regulation Loop Observed at IBMON When V_{OFB} is Regulated to $V_{OUT(INST\_ON)}$ with C_C = 1µF, R_C = 10k for a 100mA Charge Current Step

The transient response shows a small overshoot with slow settling indicating a fast minor loop within a well damped overall loop. Therefore, the value of C_C is reduced iteratively until C_C = 22nF. The transient response of the same loop with C_C = 22nF and R_C = 10k is shown in Figure 25.

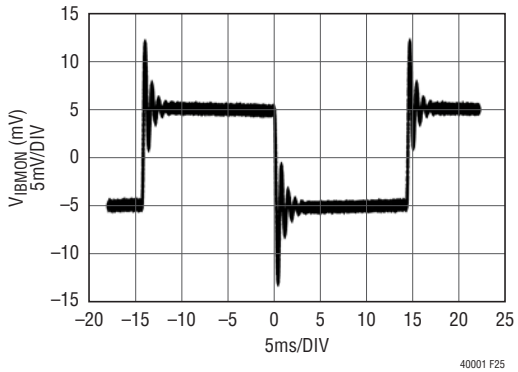

Figure 25. Transient Response of Charge Current Regulation Loop Observed at IBMON When V_{OFB} is Regulated to $V_{OUT(INST\_ON)}$ with C_C = 22nF, R_C = 10k for a 100mA Charge Current Step

The transient response now indicates an overall under damped system. As noted in the empirical loop compensation section, the value of R_C is now increased iteratively until R_C = 20k. The transient response of the same loop with C_C = 22nF and R_C = 20k is shown in Figure 26.

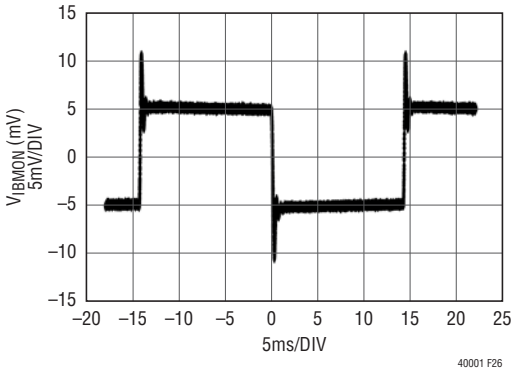

Figure 26. Transient Response of Charge Current Regulation Loop Observed at IBMON When V_{OFB} is Regulated to $V_{OUT(INST\_ON)}$ with C_C = 22nF, R_C = 20k for a 100mA Charge Current Step

Note that the transient response is close to optimum with some overshoot and fast settling. If after iteratively increasing the value of R_C, the transient response again indicates an over damped system, the step of reducing C_C can be repeated. These steps of reducing C_C followed by increasing R_C can be repeated continuously until one arrives at a stable loop with the smallest value of C_C and the largest value of R_C. In this particular example, these values are found to be C_C = 22nF and R_C = 20kΩ.

After arriving at these final values of R_C and C_C, the stability margin is checked by varying the values of both R_C and C_C by 2:1 in all four possible combinations. After which the setup condition is varied, including varying the input voltage level and the output load level and the transient response is checked at these different setup conditions. Once the desired responses on all different conditions are obtained, the values of R_C and C_C are noted.

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This same procedure is then repeated for the other four loops: the input voltage regulation, the output voltage regulation, the battery float voltage regulation and finally the charge current regulation when $V_{OFB} > V_{OUT(INST\_ON)}$. Note that the resulting optimum values for each of the loops may differ slightly. The final values of C_C and R_C are then selected by combining the results and ensuring the most conservative response for all the loops. This usually entails picking the largest value of C_C and the smallest value of R_C based on the results obtained for all the loops. In this particular example, the value of C_C is finally set to 47nF and R_C = 14.7kΩ.

BOARD LAYOUT CONSIDERATIONS

In the majority of applications, the most important parameter of the system is the battery float voltage. Therefore, the user needs to be extra careful when placing and routing the feedback resistor R_{BFB1} and R_{BFB2}. In particular, the battery sense line connected to R_{BFB1} and the ground return line for the LTC4000-1 must be Kelvined back to where the battery output and the battery ground are located respectively. Figure 27 shows this Kelvin sense configuration.

For accurate current sensing, the sense lines from R_{IS} and R_{CS} (Figure 27) must be Kelvined back all the way to the sense resistors terminals. The two sense lines of each resistor must also be routed close together and away from noise sources to minimize error. Furthermore, current filtering capacitors should be placed strategically to ensure that very little AC current is flowing through these sense resistors as mentioned in the applications section.

The decoupling capacitors C_{IN} and C_{BIAS} must be placed as close to the LTC4000-1 as possible. This allows as short a route as possible from C_{IN} to the IN and GND pins, as well as from C_{BIAS} to the BIAS and GND pins.

In a typical application, the LTC4000-1 is paired with an external DC/DC converter. The operation of this converter often involves high dV/dt switching voltage as well as high currents. Isolate these switching voltages and currents from the LTC4000-1 section of the board as much as possible by using good board layout practices. These include separating noisy power and signal grounds, having a good low impedance ground plane, shielding whenever necessary, and routing sensitive signals as short as possible and away from noisy sections of the board.

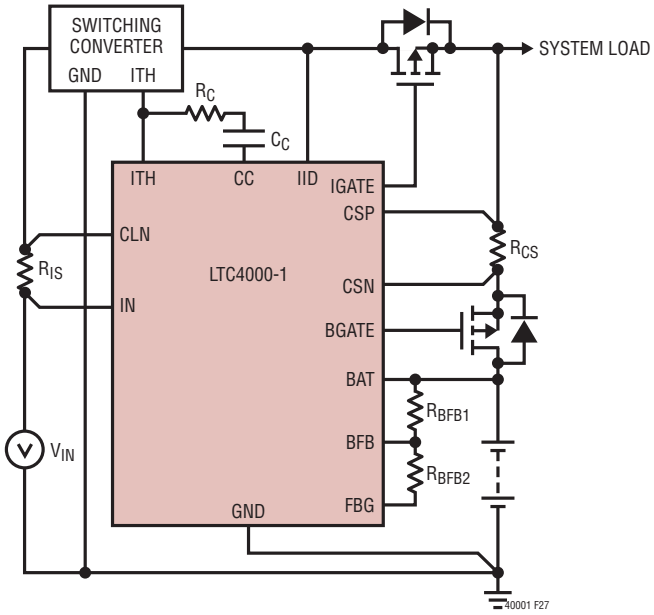

Figure 27. Kelvin Sense Lines Configuration for LTC4000-1

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APPENDIX—THE LOOP TRANSFER FUNCTIONS

When a series resistor (R_C) and capacitor (C_C) is used as the compensation network as shown in Figure 19, the transfer function from the input of A4-A7 to the ITH pin is simply as follows:

$$\frac{V_{ITH}}{V_{FB}}(s) = g_{m4\text{-}7}\left[\frac{\left(R_C - \frac{1}{g_{m10}}\right)C_C s + 1}{R_{O4\text{-}7} \bullet C_C s}\right]$$

where $g_{m4\text{-}7}$ is the transconductance of error amplifier A4-A7, typically 0.5mA/V; g_{m10} is the output amplifier (A10) transconductance, $R_{O4\text{-}7}$ is the output impedance of the error amplifier, typically 50MΩ; and R_{O10} is the effective output impedance of the output amplifier, typically 10MΩ with the ITH pin open circuit.

Note this simplification is valid when $g_{m10} \bullet R_{O10} \bullet R_{O4\text{-}7} \bullet C_C = A_{V10} \bullet R_{O4\text{-}7} \bullet C_C$ is much larger than any other poles or zeroes in the system. Typically $A_{V10} \bullet R_{O4\text{-}7} = 5 \bullet 10^{10}$ with the ITH pin open circuit. The exact value of g_{m10} and R_{O10} depends on the pull-up current and impedance connected to the ITH pin respectively.

In most applications, compensation of the loops involves picking the right values of R_C and C_C. Aside from picking the values of R_C and C_C, the value of g_{m10} may also be adjusted. The value of g_{m10} can be adjusted higher by increasing the pull-up current into the ITH pin and its value can be approximated as:

$$g_{m10} = \frac{I_{ITH} + 5\mu A}{50mV}$$

The higher the value of g_{m10}, the smaller the lower limit of the value of R_C would be. This lower limit is to prevent the presence of the right half plane zero.

Even though all the loops share this transfer function from the error amplifier input to the ITH pin, each of the loops has a slightly different dynamic due to differences in the feedback signal path.

The Input Voltage Regulation Loop

The feedback signal for the input voltage regulation loop is the voltage on the IFB pin, which is connected to the center node of the resistor divider between the input voltage (connected to the IN pin) and GND. This voltage is compared to an internal reference (1.000V typical) by the transconductance error amplifier A4. This amplifier then drives the output transconductance amplifier (A10) to appropriately adjust the voltage on the ITH pin driving the external DC/DC converter to regulate the output voltage observed by the IFB pin. This loop is shown in detail in Figure 28.

Assuming $R_{IS} << R_{IN} << (R_{IFB1} + R_{IFB2})$, the simplified loop transmission is as follows:

$$L_{IV}(s) = g_{m4}\left[\frac{\left(R_C - \frac{1}{g_{m10}}\right)C_C s + 1}{C_C s}\right] \bullet Gmi_p(s) \bullet$$

$$\left[\frac{R_{IN}}{R_{IN}\left(C_{IN} + C_{CLN}\right)s + 1}\right] \bullet \left[\frac{R_{IFB2}}{R_{IFB}}\right]$$

where $Gmi_p(s)$ is the transfer function from V_{ITH} to the input current of the external DC/DC converter, R_{IN} is the equivalent output impedance of the input source, and $R_{IFB} = R_{IFB1} + R_{IFB2}$.

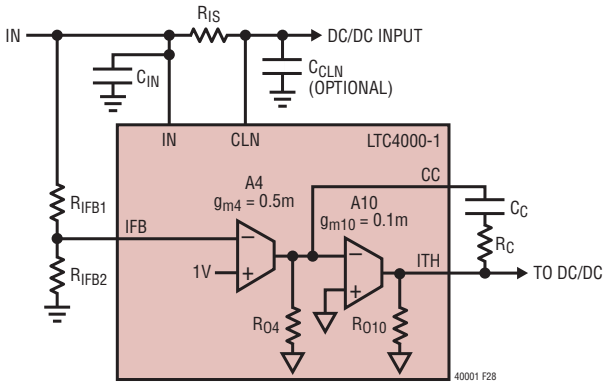


Figure 28. Simplified Linear Model of the Input Voltage Regulation Loop

TYPICAL APPLICATIONS

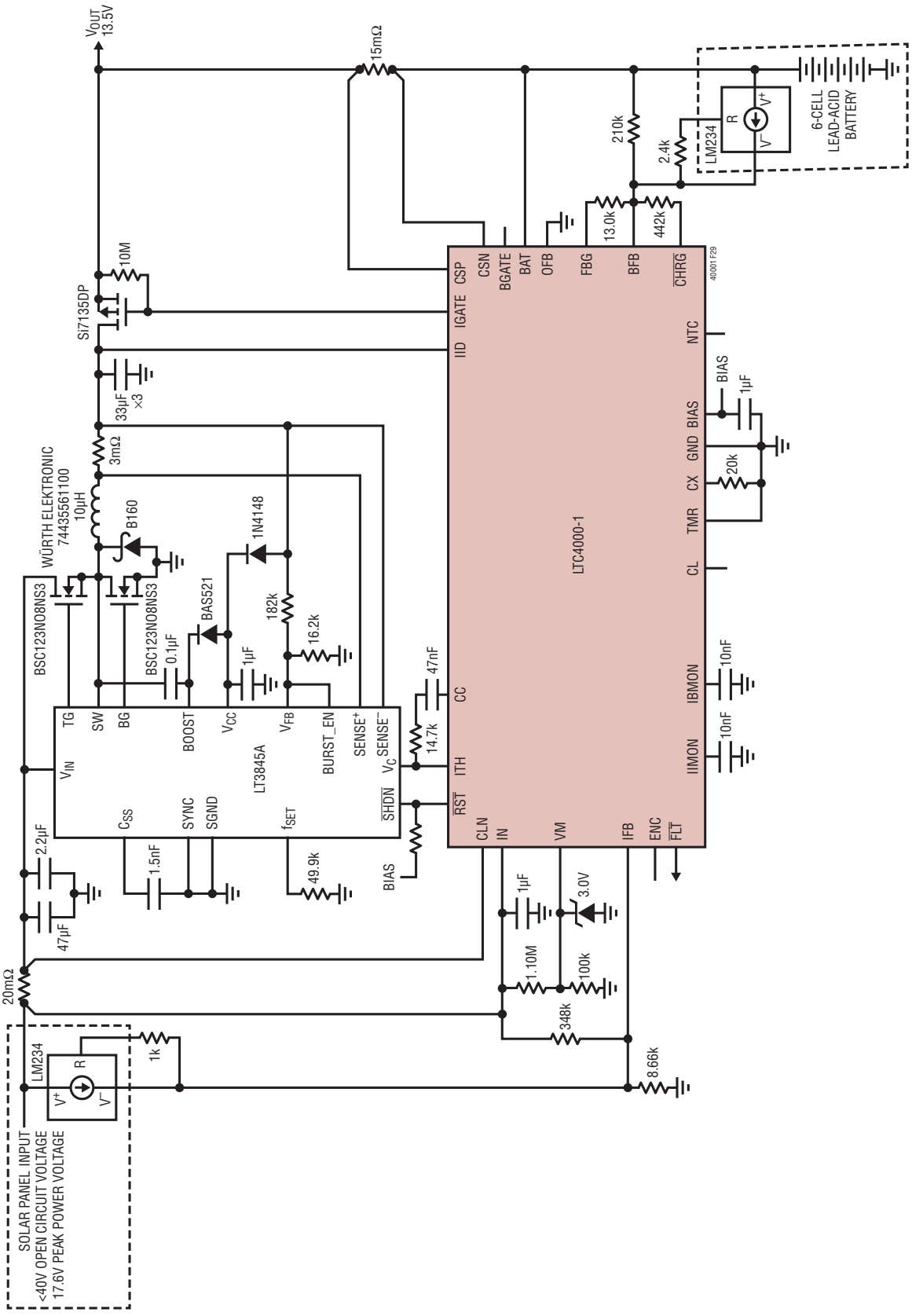


Figure 29. Solar Panel Input, 6-Cell Lead-Acid, 3-Step Battery Charger with 3.3A Bulk Charge Current, 14.1V at 25°C Absorption Voltage and 13.5V at 25°C Float Voltage. Temperature Compensation of Battery Float Voltage at –19.8mV/°C. Temperature Compensation of Solar Panel Input V_{MP} at –78mV/°C with V_{MP} = 17.6V at 25°C

TYPICAL APPLICATIONS

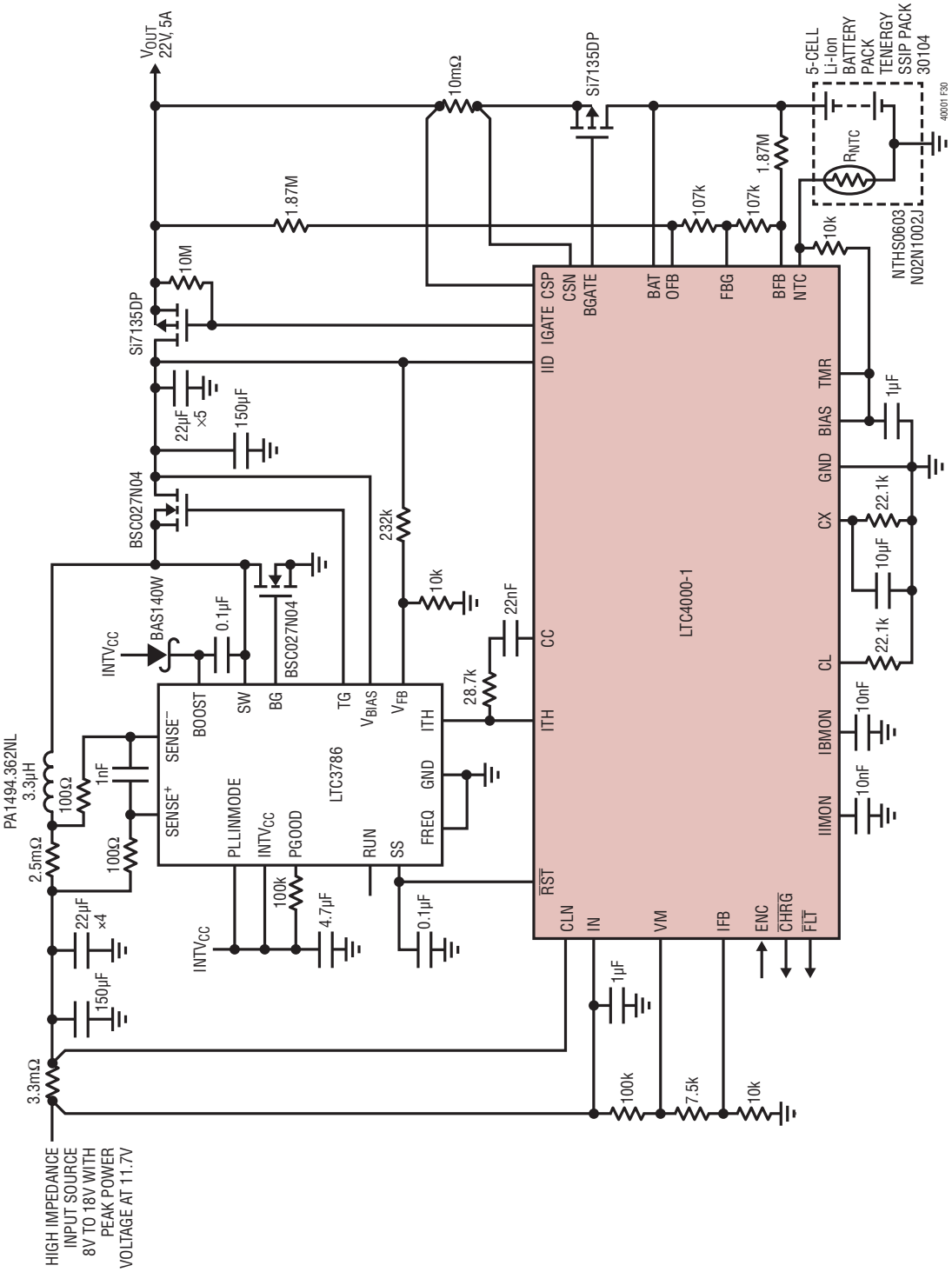


Figure 30. 21V at 5A Boost Converter 5-Cell Li-Ion Battery Charger for High Impedance Input Sources Such as Solar Cell, Fuel Cell or Wind Turbine Generator

TYPICAL APPLICATIONS

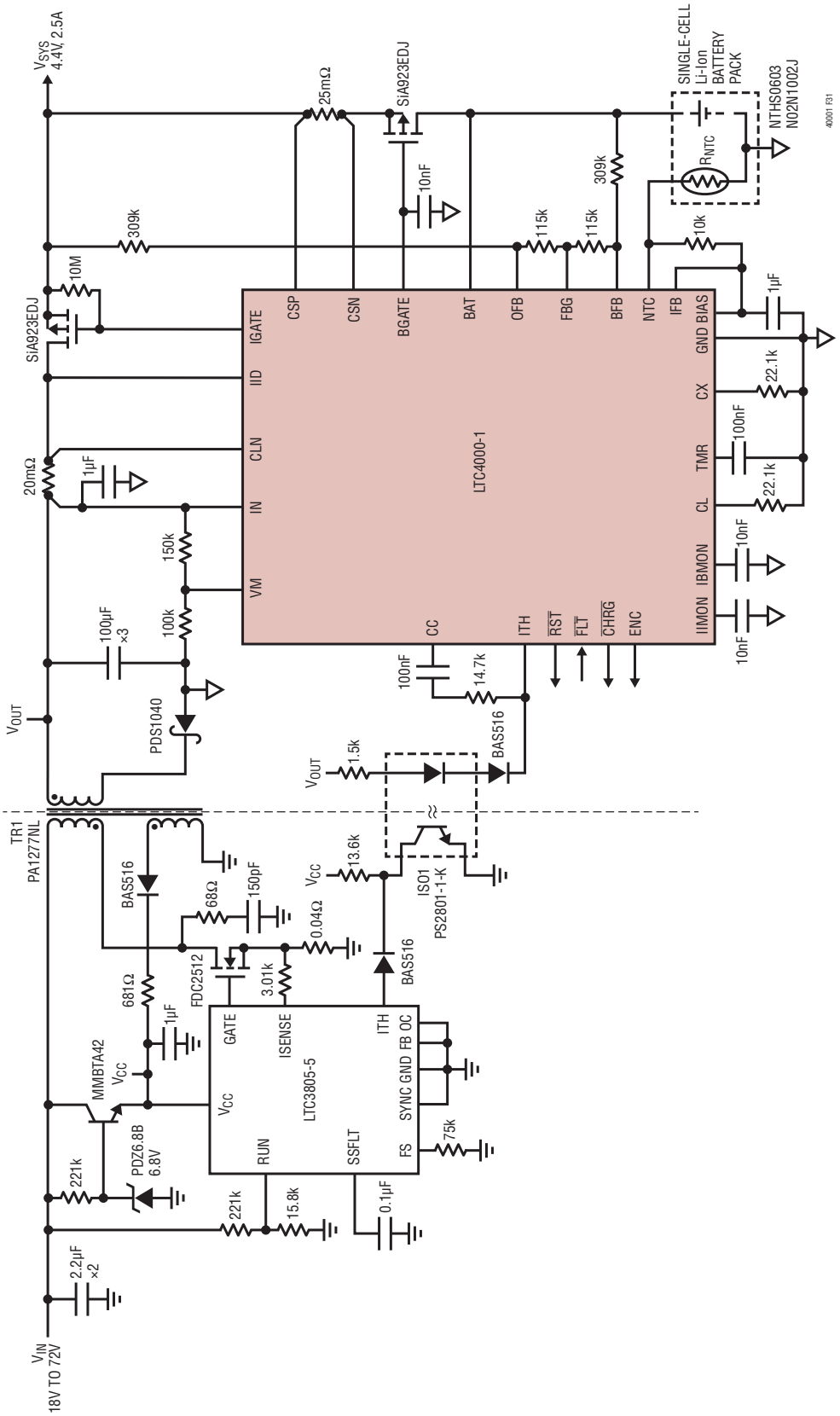
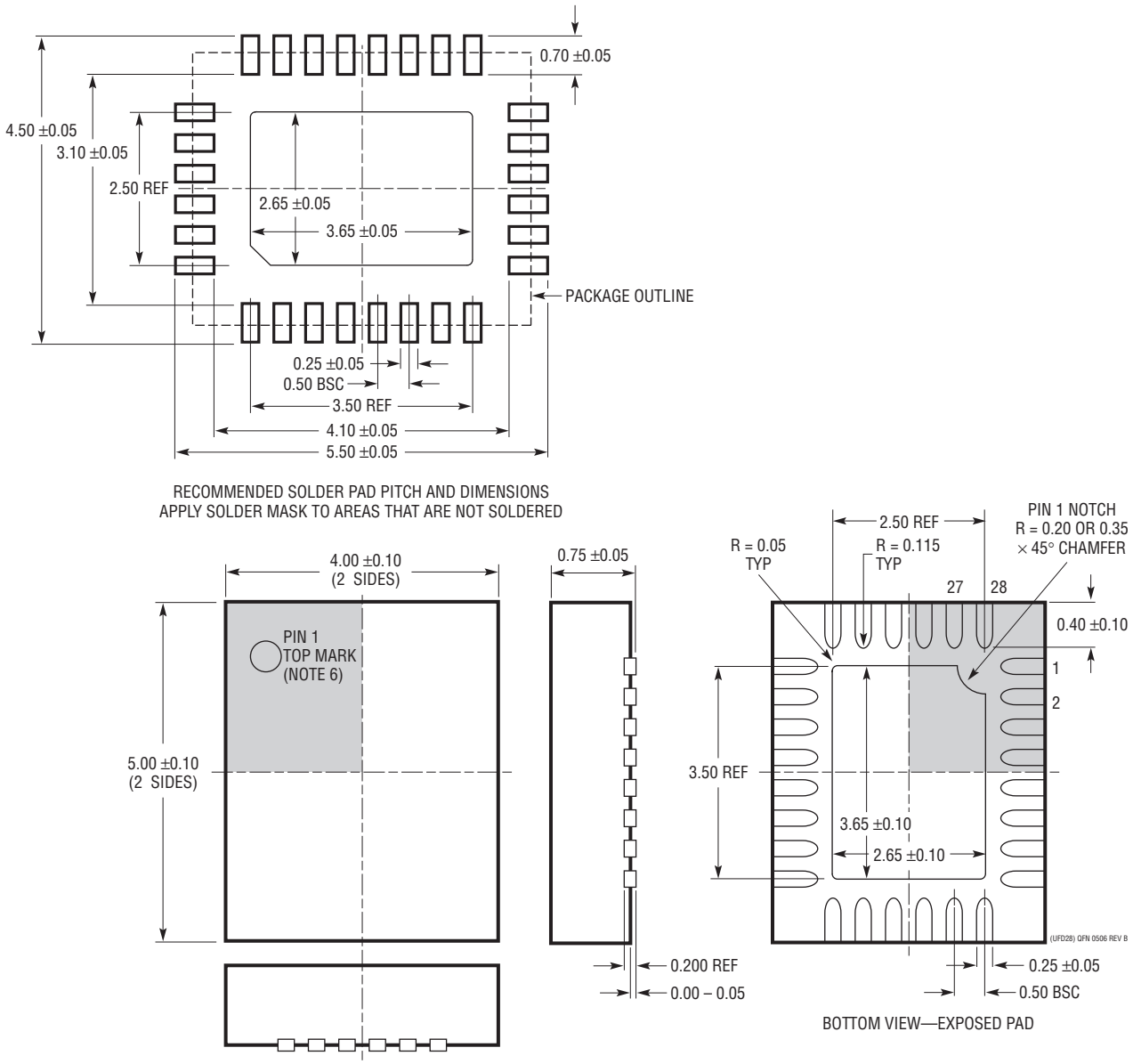


Figure 31. 18V to 72V$_{IN}$ to 4.2V at 2.0A Isolated Flyback Single-Cell Li-Ion Battery Charger with 2.9h Timer Termination and 0.22A Trickle Charge Current

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

UFD Package
28-Lead Plastic QFN (4mm × 5mm)
(Reference LTC DWG # 05-08-1712 Rev B)

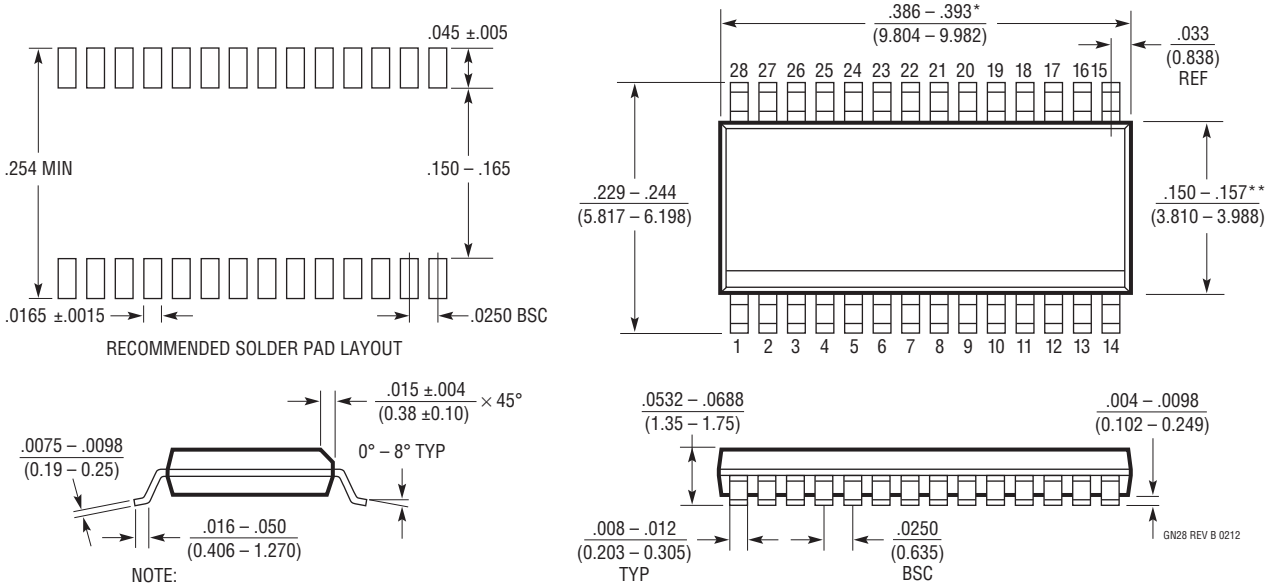


NOTE:
1. DRAWING PROPOSED TO BE MADE A JEDEC PACKAGE OUTLINE MO-220 VARIATION (WXXX-X).
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

GN Package
28-Lead Plastic SSOP (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1641 Rev B)



NOTE:
1. CONTROLLING DIMENSION: INCHES
2. DIMENSIONS ARE IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
3. DRAWING NOT TO SCALE
4. PIN 1 CAN BE BEVEL EDGE OR A DIMPLE

*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	6/13	Clarified IGATE pin functionality	10
		Clarified Input Ideal Diode functionality	12 to 13
		Clarified Input Ideal Diode PMOS Selection	15
		Clarified Input UVLO and Voltage Monitoring	16
		Revised R_{CX} C/X detection equation	18
		Revised Typical Application circuits (resistors)	11, 29, 34 to 36, 40

TYPICAL APPLICATION

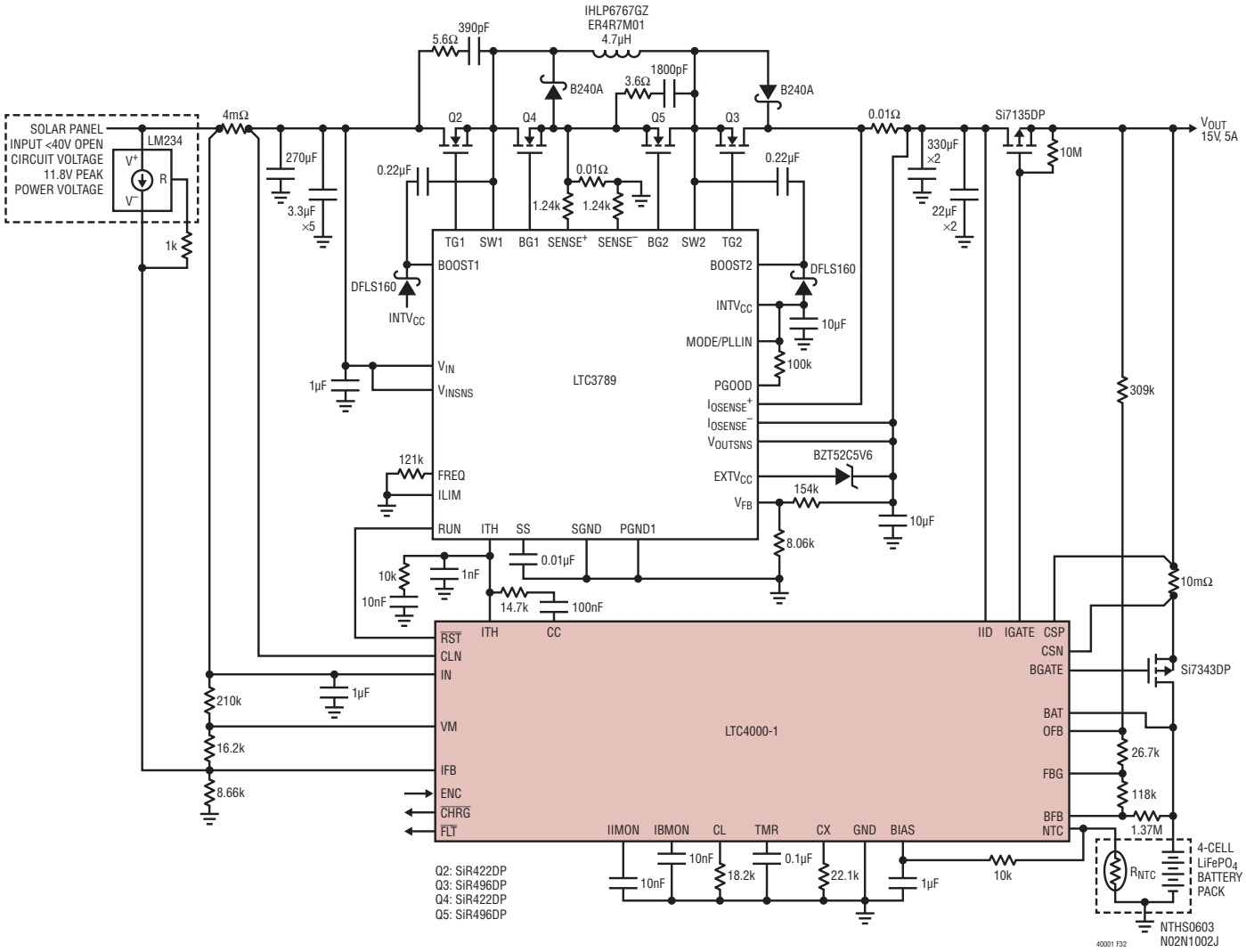


Figure 32. Solar Panel Input 6V to 36V_{IN} to 14.4V at 4.5A Buck Boost Converter 4-Cell $LiFePO_4$ Battery Charger with 2.9h Timer Termination and 0.22A Trickle Charge Current

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC4000	High Voltage High Current Controller for Battery Charging and Power Management	Similar to LTC4000-1 with Input Current Regulation
LTC3789	High Efficiency, Synchronous, 4 Switch Buck-Boost Controller	Improved LTC3780 with More Features
LT3845	High Voltage Synchronous Current Mode Step-Down Controller with Adjustable Operating Frequency	For Medium/High Power, High Efficiency Supplies
LT3650	High Voltage 2A Monolithic Li-Ion Battery Charger	3mm × 3mm DFN-12 and MSOP-12 Packages
LT3651	High Voltage 4A Monolithic Li-Ion Battery Charger	4A Synchronous Version of LT3650 Family
LT3652/LT3652HV	Power Tracking 2A Battery Chargers	Multi-Chemistry, Onboard Termination
LTC4009	High Efficiency, Multi-Chemistry Battery Charger	Low Cost Version of LTC4008, 4mm × 4mm QFN-20
LTC4012	High Efficiency, Multi-Chemistry Battery Charger with PowerPath Control	Similar to LTC4009 Adding PowerPath Control
LT3741	High Power, Constant Current, Constant Voltage, Step-Down Controller	Thermally Enhanced 4mm × 4mm QFN and 20-Pin TSSOP

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