THE DATASHEET OF

LTC6912IDE-1#PBF

www.win-source.net 0086-755-83957316

Dual Programmable Gain Amplifiers with Serial Digital Interface

FEATURES

- **2 Channels with Independent Gain Control**
  LTC6912-1: (0, 1, 2, 5, 10, 20, 50, and 100V/V)
  LTC6912-2: (0, 1, 2, 4, 8, 16, 32, and 64V/V)
- **Offset Voltage = 2mV Max (–40°C to 85°C)**
- **Channel-to-Channel Gain Matching of 0.1dB Max**
- **3-Wire SPI™ Interface**
- **Extended Gain-Bandwidth at High Gains**
- Wired-OR Outputs Possible (2:1 Analog MUX Function)
- Low Power Hardware Shutdown (GN-16 Only, 2µA Max at 2.7V)
- Rail-to-Rail Input Range
- Rail-to-Rail Output Swing
- Single or Dual Supply: 2.7V to 10.5V Total
- Input Noise: 12.6nV/√Hz
- Total System Dynamic Range to 115dB
- 16-Pin GN (SSOP) or 12-Pin DFN Package Options

APPLICATIONS

- Data Acquisition Systems
- Dynamic Gain Changing
- Automatic Ranging Circuits
- Automatic Gain Control

DESCRIPTION

The LTC®6912 is a family of dual channel, low noise, digitally programmable gain amplifiers (PGA) that are easy to use and occupy very little PC board space. The gains for both channels are independently programmable using a 3-wire SPI interface to select voltage gains of 0, 1, 2, 5, 10, 20, 50, and 100V/V (LTC6912-1); and 0, 1, 2, 4, 8, 16, 32, and 64V/V (LTC6912-2). All gains are inverting.

The LTC6912 family consists of 2 matched amplifiers with rail-to-rail outputs. When operated with unity gain, they will also process rail-to-rail input signals. A half-supply reference generated internally at the AGND pin supports single power supply applications. Operating from single or split supplies from 2.7V to 10.5V total, the LTC6912-X family is offered in tiny SSOP and DFN-12 Packages.

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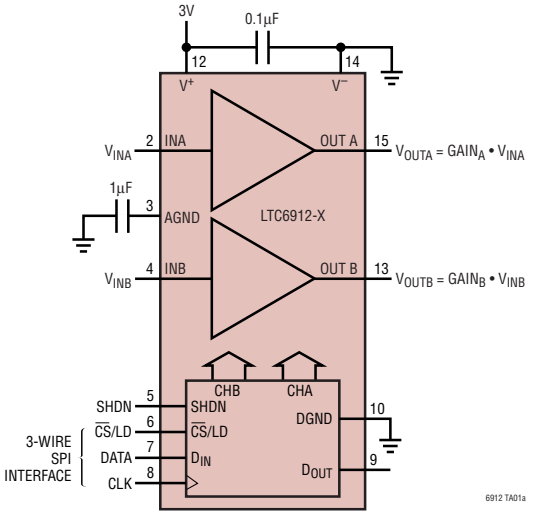
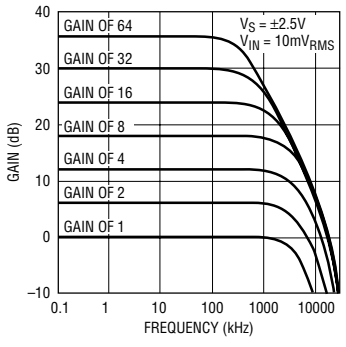
TYPICAL APPLICATION

A Dual, Matched Low Noise PGA (16-Lead SSOP Package)



LTC6912-2
Frequency Response

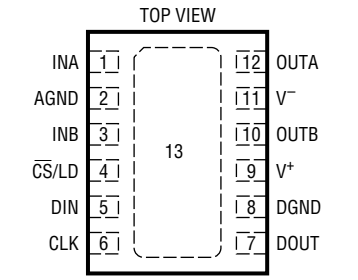


ABSOLUTE MAXIMUM RATINGS

(Note 1)

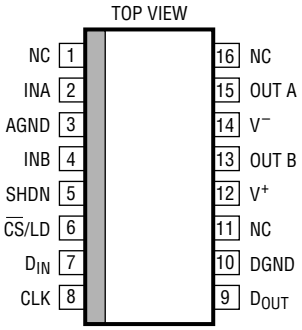
Total Supply Voltage (V^+ to V^-) 11V
Input Current ..... ±10mA
Operating Temperature Range (Note 2)
LTC6912C-1, LTC6912C-2 .....–40°C to 85°C
LTC6912I-1, LTC6912I-2.....–40°C to 85°C
LTC6912H-1, LTC6912H-2
(GN-16 Only) .....–40°C to 125°C
Specified Temperature Range (Note 3)
LTC6912C-1, LTC6912C-2 .....–40°C to 85°C
LTC6912I-1, LTC6912I-2.....–40°C to 85°C
LTC6912H-1, LTC6912H-2
(GN-16 Only) .....–40°C to 125°C
Storage Temperature Range .....–65°C to 150°C
UE Package .....–65°C to 125°C
Lead Temperature (Soldering, 10sec).....300°C

PACKAGE/ORDER INFORMATION



UE12 PACKAGE
12-LEAD (4mm × 3mm) PLASTIC DFN
EXPOSED PAD IS CONNECTED TO V^- (PIN 13),
MUST BE SOLDERED TO PCB

T_{JMAX} = 125°C, θ_{JA} = 160°C/W



GN PACKAGE
16-LEAD NARROW PLASTIC SSOP

T_{JMAX} = 150°C, θ_{JA} = 120°C/W

ORDER PART NUMBER	DFN PART* MARKING	ORDER PART NUMBER	GN PART MARKING
LTC6912CDE-1	69121	LTC6912CGN-1	69121
LTC6912IDE-1	69121	LTC6912IGN-1	6912I1
LTC6912CDE-2	69122	LTC6912HGN-1	6912H1
LTC6912IDE-2	69122	LTC6912CGN-2	69122
		LTC6912IGN-2	6912I2
		LTC6912HGN-2	6912H2

Order Options Tape and Reel: Add #TR Lead Free: Add #PBF Lead Free Tape and Reel: Add #TRPBF
Lead Free Part Marking: http://www.linear.com/leadfree/

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

GAIN SETTINGS AND PROPERTIES

Table 1. LTC6912-1 GAIN SETTINGS AND PROPERTIES

UPPER/LOWER NIBBLE				NOMINAL VOLTAGE GAIN		MAXIMUM LINEAR INPUT RANGE (V_{P-P})			NOMINAL INPUT IMPEDANCE (kΩ)	NOMINAL OUTPUT IMPEDANCE (Ω)
Q7	Q6	Q5	Q4			Dual 5V Supply	Single 5V Supply	Single 3V Supply		
Q3	Q2	Q1	Q0	Volts/Volt	dB					
0	0	0	0	0	–120	10	5	3	(Open)	0.4
0	0	0	1	–1	0	10	5	3	10	0.7
0	0	1	0	–2	6	5	2.5	1.5	5	3.4
0	0	1	1	–5	14	2	1	0.6	2	3.4
0	1	0	0	–10	20	1	0.5	0.3	1	3.4
0	1	0	1	–20	26	0.5	0.25	0.15	1	6.4
0	1	1	0	–50	34	0.2	0.1	0.06	1	15
0	1	1	1	–100	40	0.1	0.05	0.03	1	30
1	0	X	X	0	–120	10	5	3	(Open)	(Open)
1	1	X	X	Not Used (Note 11)					Not Used	

Table 2. LTC6912-2 GAIN SETTINGS AND PROPERTIES

UPPER/LOWER NIBBLE				NOMINAL VOLTAGE GAIN		MAXIMUM LINEAR INPUT RANGE (V_{P-P})			NOMINAL INPUT IMPEDANCE (kΩ)	NOMINAL OUTPUT IMPEDANCE (Ω)
Q7	Q6	Q5	Q4			Dual 5V Supply	Single 5V Supply	Single 3V Supply		
Q3	Q2	Q1	Q0	Volts/Volt	dB					
0	0	0	0	0	–120	10	5	3	(Open)	0.4
0	0	0	1	–1	0	10	5	3	10	0.7
0	0	1	0	–2	6	5	2.5	1.5	5	3.4
0	0	1	1	–4	12	2.5	1.25	0.75	2.5	3.4
0	1	0	0	–8	18.1	1.25	0.625	0.375	1.25	3.4
0	1	0	1	–16	24.1	0.625	0.3125	0.188	1.25	6.4
0	1	1	0	–32	30.1	0.3125	0.156	0.094	1.25	15
0	1	1	1	–64	36.1	0.156	0.078	0.047	1.25	30
1	0	X	X	0	–120	10	5	3	(Open)	(Open)
1	1	X	X	Not Used (Note 11)					Not Used	

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications that apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_S = 5V, AGND = 2.5V, Gain = 1, R_L = 10k to midsupply point, unless otherwise noted.

PARAMETER	CONDITIONS		C, I GRADES MIN	C, I GRADES TYP	C, I GRADES MAX	H GRADE MIN	H GRADE TYP	H GRADE MAX	UNITS
Specifications for Both the LTC6912-1 and the LTC6912-2									
Total Supply Voltage (V_S)		●	2.7		10.5	2.7		10.5	V
Supply Current per Channel	Both Amplifiers Active (Gain = 1)								
	V_S = 2.7V, V_{INA} = V_{INB} = V_{AGND}	●		1.75	2.75		1.75	3.0	mA
	V_S = 5V, V_{INA} = V_{INB} = V_{AGND}	●		2.0	3.0		2.0	3.25	mA
	V_S = ±5V, V_{INA} = V_{INB} = 0V	●		2.25	3.5		2.25	3.75	mA
Supply Current per Channel (Software Shutdown)	Both Amplifiers Inactive (State 1000)								
	V_S = 2.7V, V_{INA} = V_{INB} = V_{AGND}	●		150	255		150	280	µA
	V_S = 5V, V_{INA} = V_{INB} = V_{AGND}	●		200	325		200	350	µA
	V_S = ±5V, V_{INA} = V_{INB} = 0V	●		265	750		265	750	µA
Total-Supply Current (Hardware Shutdown, GN-16 Package Only)	V_S = 2.7V, V_{SHDN} = 2.43V	●		0.3	2		0.3	5	µA
	V_S = 5V, V_{SHDN} = 4.5V	●		3.6	10		3.6	10	µA
	V_S = ±5V, V_{SHDN} = 4.5V	●		20	50		20	50	µA
Output Voltage Swing LOW (Note 4)	V_S = 2.7V, R_L = 10k Tied to Midsupply Point	●		12	30		12	35	mV
	V_S = 2.7V, R_L = 500Ω Tied to Midsupply Point	●		60	110		50	125	mV
	V_S = 5V, R_L = 10k Tied to Midsupply Point	●		20	40		20	45	mV
	V_S = 5V, R_L = 500Ω Tied to Midsupply Point	●		100	170		90	190	mV
	V_S = ±5V, R_L = 10k Tied to 0V	●		30	50		30	60	mV
	V_S = ±5V, R_L = 500Ω Tied to 0V	●		190	260		80	290	mV
Output Voltage Swing HIGH (Note 4)	V_S = 2.7V, R_L = 10k Tied to Midsupply Point	●		10	20		10	25	mV
	V_S = 2.7V, R_L = 500Ω Tied to Midsupply Point	●		50	80		50	90	mV
	V_S = 5V, R_L = 10k Tied to Midsupply Point	●		15	30		15	35	mV
	V_S = 5V, R_L = 500Ω Tied to Midsupply Point	●		90	160		80	175	mV
	V_S = ±5V, R_L = 10k Tied to 0V	●		20	40		20	45	mV
	V_S = ±5V, R_L = 500Ω Tied to 0V	●		180	250		180	270	mV
Output Short-Circuit Current (Note 5)	V_S = 2.7V	●		±27			±27		mA
	V_S = ±5V	●		±35			±35		mA
AGND Open-Circuit Voltage (GN-16 Package Only)	V_S = Single 5V Supply, V_{SHDN} = 0.5V	●	2.45	2.5	2.55	2.45	2.5	2.55	V
	V_S = Single 5V Supply, V_{SHDN} = 4.5V			2.65			2.65		V
AGND (Common Mode) Input Voltage Range	V_S = Single 2.7V Supply	●	0.55		1.6	0.55		1.6	V
	V_S = Single 5V Supply	●	0.75		3.65	0.75		3.65	V
	V_S = ±5V	●	–4.3		3.2	–4.3		3.2	V
AGND Rejection (i.e., Common Mode Rejection or CMRR)	V_S = 2.7V, V_{AGND} = 1.1V to 1.6V	●	55	80		50	80		dB
	V_S = ±5V, V_{AGND} = –2.5V to 2.5V	●	55	75		50	75		dB
Power Supply Rejection Ratio (PSRR)	V_S =2.7V to ±5V	●	60	80		57	80		dB
Slew Rate	Gain = 1								
	V_S = 5V, V_{OUTA} = V_{OUTB} = 1.1V to 3.9V			12			12		V/µs
	V_S = ±5V, V_{OUTA} = V_{OUTB} = ±1.4V			16			16		V/µs
	Gain = 10 (–1), Gain = 8 (–2)								
	V_S = 5V, V_{OUTA} = V_{OUTB} = 1.1V to 3.9V			20			20		V/µs
	V_S = ±5V, V_{OUTA} = V_{OUTB} = ±1.4V			26			26		V/µs
Signal Attenuation at Gain = 0 Setting	Gain = 0 (Digital Inputs 0000), f = 200kHz	●		–120			–120		dB
Signal Attenuation in Software Shutdown	(State = 1000)	●		–120			–120		dB

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications that apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_S = 5V, AGND = 2.5V, Gain = 1, R_L = 10k to midsupply point, unless otherwise noted.

PARAMETER	CONDITIONS		C, I GRADES MIN	C, I GRADES TYP	C, I GRADES MAX	H GRADE MIN	H GRADE TYP	H GRADE MAX	UNITS
Specifications for Both the LTC6912-1 and the LTC6912-2									
SHDN Input High Voltage (GN-16 Package Only)	V_S = Single 2.7V	●	2.43			2.43			V
	V_S = Single 5V	●	4.5			4.5			V
	V_S = ±5V	●	4.5			4.5			V
SHDN Input Low Voltage (GN-16 Package Only)	V_S = Single 2.7V	●			0.27			0.27	V
	V_S = Single 5V	●			0.5			0.5	V
	V_S = ±5V	●			0.5			0.5	V
SHDN Pin 5, Input High Current (GN-16 Package Only)	V_S = Single 2.7V			0.2			0.2		µA
	V_S = Single 5V			1			1		µA
	V_S = ±5V			1			1		µA
SHDN Pin 5, Input Low Current (GN-16 Package Only)	V_S = Single 2.7V			0.2			0.2		µA
	V_S = Single 5V			1			1		µA
	V_S = ±5V			1			1		µA
Specifications for the LTC6912-1 ONLY									
Voltage Gain (Note 6)	V_S = 2.7V, Gain = 1, R_L = 10k	●	–0.07	0	0.07	–0.08	0	0.07	dB
	V_S = 2.7V, Gain = 1, R_L = 500Ω	●	–0.11	–0.02	0.07	–0.13	–0.02	0.07	dB
	V_S = 2.7V, Gain = 2, R_L = 10k	●	5.94	6.01	6.08	5.93	6.01	6.08	dB
	V_S = 2.7V, Gain = 5, R_L = 10k	●	13.85	13.95	14.05	13.8	13.95	14.05	dB
	V_S = 2.7V, Gain = 10, R_L =10k	●	19.7	19.93	20.1	19.65	19.93	20.1	dB
	V_S = 2.7V, Gain = 10, R_L = 500Ω	●	19.55	19.85	20.05	19.35	19.85	20.05	dB
	V_S = 2.7V, Gain = 20, R_L = 10k	●	25.75	25.94	26.1	25.65	25.94	26.1	dB
	V_S = 2.7V, Gain = 50, R_L = 10k	●	33.5	33.8	34.05	33.40	33.8	34.05	dB
	V_S = 2.7V, Gain = 100, R_L = 10k	●	39.2	39.6	40.0	39.0	39.6	40.0	dB
	V_S = 2.7V, Gain = 100, R_L = 500Ω	●	37.3	38.9	39.7	36.20	38.9	39.7	dB
	V_S = 5V, Gain = 1, R_L = 10k	●	–0.08	0.01	0.08	–0.09	0.01	0.08	dB
	V_S = 5V, Gain = 1, R_L = 500Ω	●	–0.11	–0.01	0.07	–0.13	–0.01	0.07	dB
	V_S = 5V, Gain = 2, R_L = 10k	●	5.95	6.02	6.09	5.94	6.02	6.09	dB
	V_S = 5V, Gain = 5, R_L = 10k	●	13.8	13.96	14.1	13.78	13.96	14.1	dB
	V_S = 5V, Gain = 10, R_L = 10k	●	19.8	19.94	20.1	19.75	19.94	20.1	dB
	V_S = 5V, Gain = 10, R_L = 500Ω	●	19.6	19.87	20.1	19.45	19.87	20.1	dB
	V_S = 5V, Gain = 20, R_L = 10k	●	25.78	25.94	26.08	25.75	25.94	26.08	dB
	V_S = 5V, Gain = 50, R_L = 10k	●	33.5	33.84	34.1	33.4	33.84	34.1	dB
	V_S = 5V, Gain = 100, R_L = 10k	●	39.3	39.7	40.1	39.1	39.7	40.1	dB
	V_S = 5V, Gain = 100, R_L = 500Ω	●	37.75	39.2	39.85	36.6	39.2	39.85	dB
	V_S = ±5V, Gain = 1, R_L = 10k	●	–0.06	0.01	0.08	–0.07	0.01	0.08	dB
	V_S = ±5V, Gain = 1, R_L = 500Ω	●	–0.10	0	0.08	–0.11	0	0.08	dB
	V_S = ±5V, Gain = 2, R_L = 10k	●	5.95	6.02	6.09	5.94	6.02	6.09	dB
	V_S = ±5V, Gain = 5, R_L = 10k	●	13.8	13.96	14.1	13.79	13.96	14.1	dB
	V_S = ±5V, Gain = 10, R_L = 10k	●	19.78	19.94	20.08	19.75	19.94	20.08	dB
	V_S = ±5V, Gain = 10, R_L = 500Ω	●	19.68	19.91	20.05	19.58	19.91	20.05	dB
	V_S = ±5V, Gain = 20, R_L = 10k	●	25.78	25.95	26.08	25.73	25.95	26.08	dB
	V_S = ±5V, Gain = 50, R_L = 10k	●	33.65	33.87	34.05	33.60	33.87	34.05	dB
	V_S = ±5V, Gain = 100, R_L = 10k	●	39.4	39.8	40.2	39.25	39.8	40.2	dB
	V_S = ±5V, Gain = 100, R_L = 500Ω	●	38.6	39.5	39.9	37.6	39.5	39.9	dB

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications that apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_S = 5V, AGND = 2.5V, Gain = 1, R_L = 10k to midsupply point, unless otherwise noted.

PARAMETER	CONDITIONS		C, I GRADES MIN	C, I GRADES TYP	C, I GRADES MAX	H GRADE MIN	H GRADE TYP	H GRADE MAX	UNITS
Specifications for the LTC6912-1 ONLY									
Channel-to-Channel Voltage Gain Match (Note 6)	V_S = 2.7V, Gain = 1, R_L = 10k	●	–0.1	±0.02	0.1	–0.1	±0.02	0.1	dB
	V_S = 2.7V, Gain = 1, R_L = 500Ω	●	–0.1	±0.02	0.1	–0.1	±0.02	0.1	dB
	V_S = 2.7V, Gain = 2, R_L = 10k	●	–0.1	±0.02	0.1	–0.1	±0.02	0.1	dB
	V_S = 2.7V, Gain = 5, R_L = 10k	●	–0.15	±0.02	0.15	–0.15	±0.02	0.15	dB
	V_S = 2.7V, Gain = 10, R_L = 10k	●	–0.15	±0.02	0.15	–0.15	±0.02	0.15	dB
	V_S = 2.7V, Gain = 10, R_L = 500Ω	●	–0.15	±0.02	0.15	–0.2	±0.02	0.2	dB
	V_S = 2.7V, Gain = 20, R_L = 10k	●	–0.15	±0.02	0.15	–0.15	±0.02	0.15	dB
	V_S = 2.7V, Gain = 50, R_L = 10k	●	–0.15	±0.02	0.15	–0.15	±0.02	0.15	dB
	V_S = 2.7V, Gain = 100, R_L = 10k	●	–0.2	±0.02	0.2	–0.2	±0.02	0.2	dB
	V_S = 2.7V, Gain = 100, R_L = 500Ω	●	–1.0	±0.02	1.0	–1.5	±0.02	1.5	dB
	V_S = 5V, Gain = 1, R_L = 10k	●	–0.1	±0.02	0.1	–0.1	±0.02	0.1	dB
	V_S = 5V, Gain = 1, R_L = 500Ω	●	–0.1	±0.02	0.1	–0.1	±0.02	0.1	dB
	V_S = 5V, Gain = 2, R_L = 10k	●	–0.1	±0.02	0.1	–0.1	±0.02	0.1	dB
	V_S = 5V, Gain = 5, R_L = 10k	●	–0.15	±0.02	0.15	–0.15	±0.02	0.15	dB
	V_S = 5V, Gain = 10, R_L = 10k	●	–0.15	±0.02	0.15	–0.15	±0.02	0.15	dB
	V_S = 5V, Gain = 10, R_L = 500Ω	●	–0.15	±0.02	0.15	–0.15	±0.02	0.15	dB
	V_S = 5V, Gain = 20, R_L = 10k	●	–0.15	±0.02	0.15	–0.15	±0.02	0.15	dB
	V_S = 5V, Gain = 50, R_L = 10k	●	–0.15	±0.02	0.15	–0.15	±0.02	0.15	dB
	V_S = 5V, Gain = 100, R_L = 10k	●	–0.2	±0.02	0.2	–0.2	±0.02	0.2	dB
	V_S = 5V, Gain = 100, R_L = 500Ω	●	–0.8	±0.02	0.8	–1.2	±0.02	1.2	dB
	V_S = ±5V, Gain = 1, R_L = 10k	●	–0.1	±0.02	0.1	–0.1	±0.02	0.1	dB
	V_S = ±5V, Gain = 1, R_L = 500Ω	●	–0.1	±0.02	0.1	–0.1	±0.02	0.1	dB
	V_S = ±5V, Gain = 2, R_L = 10k	●	–0.1	±0.02	0.1	–0.1	±0.02	0.1	dB
	V_S = ±5V, Gain = 5, R_L = 10k	●	–0.15	±0.02	0.15	–0.15	±0.02	0.15	dB
	V_S = ±5V, Gain = 10, R_L = 10k	●	–0.15	±0.02	0.15	–0.15	±0.02	0.15	dB
	V_S = ±5V, Gain = 10, R_L = 500Ω	●	–0.15	±0.02	0.15	–0.15	±0.02	0.15	dB
	V_S = ±5V, Gain = 20, R_L = 10k	●	–0.15	±0.02	0.15	–0.15	±0.02	0.15	dB
	V_S = ±5V, Gain = 50, R_L = 10k	●	–0.15	±0.02	0.15	–0.15	±0.02	0.15	dB
	V_S = ±5V, Gain = 100, R_L = 10k	●	–0.2	±0.02	0.2	–0.2	±0.02	0.2	dB
	V_S = ±5V, Gain = 100, R_L = 500Ω	●	–0.6	±0.02	0.6	–0.9	±0.02	0.9	dB
Gain Temperature Coefficient (Note 6)	V_S = 5V, Gain = 1, R_L = OPEN			2			2		ppm/°C
	V_S = 5V, Gain = 2, R_L = OPEN			–1.5			–1.5		ppm/°C
	V_S = 5V, Gain = 5, R_L = OPEN			–11			–11		ppm/°C
	V_S = 5V, Gain = 10, R_L = OPEN			–30			–30		ppm/°C
	V_S = 5V, Gain = 20, R_L = OPEN			–40			–40		ppm/°C
	V_S = 5V, Gain = 50, R_L = OPEN			–70			–70		ppm/°C
	V_S = 5V, Gain = 100, R_L = OPEN			–140			–140		ppm/°C
Channel-to-Channel Gain Temperature Coefficient Match (Gain Specified in dB's) (Note 6)	V_S = 5V, Gain = 1, R_L = OPEN			1			1		ppm/°C
	V_S = 5V, Gain = 2, R_L = OPEN			1			1		ppm/°C
	V_S = 5V, Gain = 5, R_L = OPEN			0.2			0.2		ppm/°C
	V_S = 5V, Gain = 10, R_L = OPEN			–1			–1		ppm/°C
	V_S = 5V, Gain = 20, R_L = OPEN			–1			–1		ppm/°C
	V_S = 5V, Gain = 50, R_L = OPEN			–3			–3		ppm/°C
	V_S = 5V, Gain = 100, R_L = OPEN			–3			–3		ppm/°C
Channel-to-Channel Isolation (Note 7)	f = 200kHz,								
	V_S = 5V, Gain = 1, R_L = 10k			113			113		dB
	V_S = 5V, Gain = 10, R_L = 10k			108			108		dB
	V_S = 5V, Gain = 100, R_L = 10k			89			89		dB

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications that apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_S = 5V, AGND = 2.5V, Gain = 1, R_L = 10k to midsupply point, unless otherwise noted.

PARAMETER	CONDITIONS		C, I SUFFIXES MIN	C, I SUFFIXES TYP	C, I SUFFIXES MAX	H SUFFIX MIN	H SUFFIX TYP	H SUFFIX MAX	UNITS
Specifications for the LTC6912-1 ONLY									
Offset Voltage Magnitude (Internal Op-Amp, Note 8)	Gain = 1	●		0.125	2		0.125	3.5	mV
Offset Voltage Magnitude Referred to INA or INB Pins (Note 8)	Gain = 1 Gain = 10	● ●		0.25 0.14	3.5 2		0.25 0.14	6.5 4	mV mV
Input Offset Voltage Drift, Internal Op Amp				6			10		µV/°C
DC Input Resistance at INA or INB Pins (Note 9)	DC V_{INA} or V_{INB} = 0V Gain = 0 State = 8, Software Shutdown Gain = 1 Gain = 2 Gain = 5 Gain > 5	 ● ● ● ● ● ●		 >10 >10 10 5 2 1			 >10 >10 10 5 2 1		 MΩ MΩ kΩ kΩ kΩ kΩ
DC Input Resistance Drift at INA or INB Pins (Note 9)	Gain = 1 Gain = 2 Gain = 5 Gain = 10 Gain = 20 Gain = 50 Gain = 100			85 90 100 120 130 150 190			95 100 110 130 140 160 200		ppm/°C ppm/°C ppm/°C ppm/°C ppm/°C ppm/°C ppm/°C
DC Input Resistance Match R_{INA}-R_{INB}	Gain = 1 Gain = 2 Gain = 5 Gain > 5	● ● ● ●		10 5 5 5			10 5 5 5		Ω Ω Ω Ω
DC Small Signal Output Resistance at OUT A or OUT B Pins	DC V_{INA} or V_{INB} = 0V Gain = 0 Gain = 1 Gain = 2 Gain = 5 Gain = 10 Gain = 20 Gain = 50 Gain = 100 State = 8, Software Shutdown	 ●		 0.4 0.7 1.0 1.9 3.4 6.4 15 30 >1			 0.4 0.7 1.0 1.9 3.4 6.4 15 30 >1		 Ω Ω Ω Ω Ω Ω Ω Ω MΩ
Gain Bandwidth Product	Gain = 100	●	18	33	50	16	33	50	MHz
Wideband Noise (Referred to Input)	f = 1kHz to 200kHz Gain = 0 (Output Noise only) Gain = 1 Gain = 2 Gain = 5 Gain = 10 Gain = 20 Gain = 50 Gain = 100			 8.9 15.6 11.1 8.3 7.4 7.0 6.7 6.3			 8.9 15.6 11.1 8.3 7.4 7.0 6.7 6.3		 μV_{RMS} μV_{RMS} μV_{RMS} μV_{RMS} μV_{RMS} μV_{RMS} μV_{RMS} μV_{RMS}

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications that apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_S = 5V, AGND = 2.5V, Gain = 1, R_L = 10k to midsupply point, unless otherwise noted.

PARAMETER	CONDITIONS		C, I GRADES MIN	C, I GRADES TYP	C, I GRADES MAX	H GRADE MIN	H GRADE TYP	H GRADE MAX	UNITS
Specifications for the LTC6912-1 ONLY									
Voltage Noise Density (Referred to Input)	f = 50kHz								
	Gain = 1			35.6			35.6		nV/√Hz
	Gain = 2			24.8			24.8		nV/√Hz
	Gain = 5			19.1			19.1		nV/√Hz
	Gain = 10			16.7			16.7		nV/√Hz
	Gain = 20			16			16		nV/√Hz
	Gain = 50			15.4			15.4		nV/√Hz
	Gain = 100			15.1			15.1		nV/√Hz
Total Harmonic Distortion	Gain = 10, f_{IN} = 10kHz, V_{OUT} = 1V_{RMS}			–90			–90		dB
				0.003			0.003		%
	Gain = 10, f_{IN} = 100kHz, V_{OUT} = 1V_{RMS}			–82			–82		dB
				0.008			0.008		%
Specifications for the LTC6912-2 ONLY									
Voltage Gain (Note 6)	V_S = 2.7V, Gain = 1, R_L = 10k	●	–0.07	0	0.07	–0.08	0	0.07	dB
	V_S = 2.7V, Gain = 1, R_L = 500Ω	●	–0.11	–0.02	0.07	–0.13	–0.02	0.07	dB
	V_S = 2.7V, Gain = 2, R_L = 10k	●	5.94	6.01	6.08	5.93	6.01	6.08	dB
	V_S = 2.7V, Gain = 4, R_L = 10k	●	11.9	12.02	12.12	11.88	12.02	12.12	dB
	V_S = 2.7V, Gain = 8, R_L = 10k	●	17.8	18.0	18.15	17.75	18.0	18.15	dB
	V_S = 2.7V, Gain = 8, R_L = 500Ω	●	17.65	17.94	18.15	17.50	17.94	18.15	dB
	V_S = 2.7V, Gain = 16, R_L =10k	●	23.8	24.01	24.25	23.75	24.01	24.25	dB
	V_S = 2.7V, Gain = 32, R_L = 10k	●	29.7	30.0	30.2	29.65	30.0	30.2	dB
	V_S = 2.7V, Gain = 64, R_L = 10k	●	35.4	35.8	36.2	35.15	35.8	36.2	dB
	V_S = 2.7V, Gain = 64, R_L = 500Ω	●	34.15	35.3	36.0	33.40	35.3	36.0	dB
	V_S = 5V, Gain = 1, R_L = 10k	●	–0.08	0	0.08	–0.09	0	0.08	dB
	V_S = 5V, Gain = 1, R_L = 500Ω	●	–0.1	–0.01	0.08	–0.12	–0.01	0.08	dB
	V_S = 5V, Gain = 2, R_L = 10k	●	5.95	6.02	6.09	5.94	6.02	6.09	dB
	V_S = 5V, Gain = 4, R_L = 10k	●	11.85	12.02	12.15	11.83	12.02	12.15	dB
	V_S = 5V, Gain = 8, R_L = 10k	●	17.85	18.01	18.15	17.83	18.01	18.15	dB
	V_S = 5V, Gain = 8, R_L = 500Ω	●	17.65	17.96	18.15	17.50	17.96	18.15	dB
	V_S = 5V, Gain = 16, R_L = 10k	●	23.85	24.02	24.15	23.80	24.02	24.15	dB
	V_S = 5V, Gain = 32, R_L = 10k	●	29.70	30.02	30.2	29.65	30.02	30.2	dB
	V_S = 5V, Gain = 64, R_L = 10k	●	35.5	35.9	36.25	35.40	35.9	36.25	dB
	V_S = 5V, Gain = 64, R_L = 500Ω	●	34.6	35.6	36.0	33.8	35.6	36.0	dB
	V_S = ±5V, Gain = 1, R_L = 10k	●	–0.06	0.01	0.08	–0.07	0.01	0.08	dB
	V_S = ±5V, Gain = 1, R_L = 500Ω	●	–0.1	0	0.08	–0.11	0	0.08	dB
	V_S = ±5V, Gain = 2, R_L = 10k	●	5.95	6.02	6.09	5.94	6.02	6.09	dB
	V_S = ±5V, Gain = 4, R_L = 10k	●	11.9	12.03	12.15	11.88	12.03	12.15	dB
	V_S = ±5V, Gain = 8, R_L = 10k	●	17.85	18.02	18.15	17.83	18.02	18.15	dB
	V_S = ±5V, Gain = 8, R_L = 500Ω	●	17.80	17.99	18.15	17.73	17.99	18.15	dB
	V_S = ±5V, Gain = 16, R_L = 10k	●	23.85	24.03	24.15	23.82	24.03	24.15	dB
	V_S = ±5V, Gain = 32, R_L = 10k	●	29.85	30.0	30.2	29.8	30.0	30.20	dB
	V_S = ±5V, Gain = 64, R_L = 10k	●	35.65	36.0	36.20	35.55	36.0	36.20	dB
	V_S = ±5V, Gain = 64, R_L = 500Ω	●	35.15	35.8	36.10	34.45	35.8	36.10	dB

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications that apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_S = 5V, AGND = 2.5V, Gain = 1, R_L = 10k to midsupply point, unless otherwise noted.

PARAMETER	CONDITIONS		C, I GRADES MIN	C, I GRADES TYP	C, I GRADES MAX	H GRADE MIN	H GRADE TYP	H GRADE MAX	UNITS
Specifications for the LTC6912-2 ONLY									
Channel-to-Channel Voltage Gain Match (Note 6)	V_S = 2.7V, Gain = 1, R_L = 10k	●	–0.1	±0.02	0.1	–0.1	±0.02	0.1	dB
	V_S = 2.7V, Gain = 1, R_L = 500Ω	●	–0.1	±0.02	0.1	–0.1	±0.02	0.1	dB
	V_S = 2.7V, Gain = 2, R_L = 10k	●	–0.1	±0.02	0.1	–0.1	±0.02	0.1	dB
	V_S = 2.7V, Gain = 4, R_L = 10k	●	–0.15	±0.02	0.15	–0.15	±0.02	0.15	dB
	V_S = 2.7V, Gain = 8, R_L = 10k	●	–0.15	±0.02	0.15	–0.15	±0.02	0.15	dB
	V_S = 2.7V, Gain = 8, R_L = 500Ω	●	–0.15	±0.02	0.15	–0.2	±0.02	0.2	dB
	V_S = 2.7V, Gain = 16, R_L = 10k	●	–0.15	±0.02	0.15	–0.15	±0.02	0.15	dB
	V_S = 2.7V, Gain = 32, R_L = 10k	●	–0.15	±0.02	0.15	–0.15	±0.02	0.15	dB
	V_S = 2.7V, Gain = 64, R_L = 10k	●	–0.2	±0.02	0.2	–0.2	±0.02	0.2	dB
	V_S = 2.7V, Gain = 64, R_L = 500Ω	●	–0.7	±0.02	0.7	–1.0	±0.02	1.0	dB
	V_S = 5V, Gain = 1, R_L = 10k	●	–0.1	±0.02	0.1	–0.1	±0.02	0.1	dB
	V_S = 5V, Gain = 1, R_L = 500Ω	●	–0.1	±0.02	0.1	–0.1	±0.02	0.1	dB
	V_S = 5V, Gain = 2, R_L = 10k	●	–0.1	±0.02	0.1	–0.1	±0.02	0.1	dB
	V_S = 5V, Gain = 4, R_L = 10k	●	–0.15	±0.02	0.15	–0.15	±0.02	0.15	dB
	V_S = 5V, Gain = 8, R_L = 10k	●	–0.15	±0.02	0.15	–0.15	±0.02	0.15	dB
	V_S = 5V, Gain = 8, R_L = 500Ω	●	–0.15	±0.02	0.15	–0.15	±0.02	0.15	dB
	V_S = 5V, Gain = 16, R_L = 10k	●	–0.15	±0.02	0.15	–0.15	±0.02	0.15	dB
	V_S = 5V, Gain = 32, R_L = 10k	●	–0.15	±0.02	0.15	–0.15	±0.02	0.15	dB
	V_S = 5V, Gain = 64, R_L = 10k	●	–0.15	±0.02	0.15	–0.15	±0.02	0.15	dB
	V_S = 5V, Gain = 64, R_L = 500Ω	●	–0.6	±0.02	0.6	–0.8	±0.02	0.8	dB
	V_S = ±5V, Gain = 1, R_L = 10k	●	–0.1	±0.02	0.1	–0.1	±0.02	0.1	dB
	V_S = ±5V, Gain = 1, R_L = 500Ω	●	–0.1	±0.02	0.1	–0.1	±0.02	0.1	dB
	V_S = ±5V, Gain = 2, R_L = 10k	●	–0.1	±0.02	0.1	–0.1	±0.02	0.1	dB
	V_S = ±5V, Gain = 4, R_L = 10k	●	–0.15	±0.02	0.15	–0.15	±0.02	0.15	dB
	V_S = ±5V, Gain = 8, R_L = 10k	●	–0.15	±0.02	0.15	–0.15	±0.02	0.15	dB
	V_S = ±5V, Gain = 8, R_L = 500Ω	●	–0.15	±0.02	0.15	–0.15	±0.02	0.15	dB
	V_S = ±5V, Gain = 16, R_L = 10k	●	–0.15	±0.02	0.15	–0.15	±0.02	0.15	dB
	V_S = ±5V, Gain = 32, R_L = 10k	●	–0.15	±0.02	0.15	–0.15	±0.02	0.15	dB
	V_S = ±5V, Gain = 64, R_L = 10k	●	–0.15	±0.02	0.15	–0.15	±0.02	0.15	dB
	V_S = ±5V, Gain = 64, R_L = 500Ω	●	–0.4	±0.02	0.4	–0.6	±0.02	0.6	dB
Gain Temperature Coefficient (Note 6)	V_S = 5V, Gain = 1, R_L = OPEN			2			2		ppm/°C
	V_S = 5V, Gain = 2, R_L = OPEN			–4			–4		ppm/°C
	V_S = 5V, Gain = 4, R_L = OPEN			–10			–10		ppm/°C
	V_S = 5V, Gain = 8, R_L = OPEN			–24			–24		ppm/°C
	V_S = 5V, Gain = 16, R_L = OPEN			–30			–30		ppm/°C
	V_S = 5V, Gain = 32, R_L = OPEN			–40			–40		ppm/°C
	V_S = 5V, Gain = 64, R_L = OPEN			–120			–120		ppm/°C
Channel-to-Channel Gain Temperature Coefficient Match (Note 6)	V_S = 5V, Gain = 1, R_L = OPEN			0			0		ppm/°C
	V_S = 5V, Gain = 2, R_L = OPEN			–0.5			–0.5		ppm/°C
	V_S = 5V, Gain = 4, R_L = OPEN			0			0		ppm/°C
	V_S = 5V, Gain = 8, R_L = OPEN			0			0		ppm/°C
	V_S = 5V, Gain = 16, R_L = OPEN			–1			–1		ppm/°C
	V_S = 5V, Gain = 32, R_L = OPEN			–4			–4		ppm/°C
	V_S = 5V, Gain = 64, R_L = OPEN			–4			–4		ppm/°C
Channel-to-Channel Isolation (Note 7)	f = 200kHz,								
	V_S = 5V, Gain = 1, R_L = 10k			117			117		dB
	V_S = 5V, Gain = 8, R_L = 10k			110			110		dB
	V_S = 5V, Gain = 64, R_L = 10k			92			92		dB
Offset Voltage Magnitude (Internal Op-Amp, Note 8)	Gain = 1	●		0.125	2		0.125	3.5	mV

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications that apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_S = 5V, AGND = 2.5V, Gain = 1, R_L = 10k to midsupply point, unless otherwise noted.

PARAMETER	CONDITIONS		C, I GRADES MIN	C, I GRADES TYP	C, I GRADES MAX	H GRADE MIN	H GRADE TYP	H GRADE MAX	UNITS
Specifications for the LTC6912-2 ONLY									
Offset Voltage Magnitude Referred to INA or INB Pins (Note 8)	Gain = 1	●		0.25	3.5		0.25	6.5	mV
	Gain = 8	●		0.14	2		0.14	4	mV
Input Offset Voltage Drift, Internal Op Amp				6			10		µV/°C
DC Input Resistance at INA or INB Pins (Note 9)	DC V_{INA} or V_{INB} = 0V								
	Gain = 0	●		>10			>10		MΩ
	State = 8, Software Shutdown	●		>10			>10		MΩ
	Gain = 1	●		10			10		kΩ
	Gain = 2	●		5			5		kΩ
	Gain = 4	●		2.5			2.5		kΩ
	Gain > 4	●		1.25			1.25		kΩ
DC Input Resistance Drift at INA or INB Pins (Note 9)	Gain = 1			85			95		ppm/°C
	Gain = 2			90			100		ppm/°C
	Gain = 4			95			105		ppm/°C
	Gain = 8			120			130		ppm/°C
	Gain = 16			130			140		ppm/°C
	Gain = 32			140			150		ppm/°C
	Gain = 64			170			180		ppm/°C
DC Input Resistance Match R_{INA}-R_{INB}	Gain = 1	●		10			10		Ω
	Gain = 2	●		5			5		Ω
	Gain = 4	●		5			5		Ω
	Gain > 4	●		5			5		Ω
DC Small Signal Output Resistance at OUT A or OUT B Pins	DC V_{INA} or V_{INB} = 0V								
	Gain = 0			0.4			0.4		Ω
	Gain = 1			0.7			0.7		Ω
	Gain = 2			1.0			1.0		Ω
	Gain = 4			1.9			1.9		Ω
	Gain = 8			3.4			3.4		Ω
	Gain = 16			6.4			6.4		Ω
	Gain = 32			15			15		Ω
	Gain = 64			30			30		Ω
	State = 8, Software Shutdown	●		>1			>1		MΩ
Gain Bandwidth Product	Gain = 64	●	17	30	50	15	30	50	MHz
Wideband Noise (Referred to Input)	f = 1kHz to 200kHz								
	Gain = 0 (Output Noise Only)			8.1			8.1		$µV_{RMS}$
	Gain = 1			13.8			13.8		$µV_{RMS}$
	Gain = 2			9.6			9.6		$µV_{RMS}$
	Gain = 4			7.5			7.5		$µV_{RMS}$
	Gain = 8			6.4			6.4		$µV_{RMS}$
	Gain = 16			6.0			6.0		$µV_{RMS}$
	Gain = 32			5.8			5.8		$µV_{RMS}$
	Gain = 64			5.6			5.6		$µV_{RMS}$

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications that apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_S = 5V, AGND = 2.5V, Gain = 1, R_L = 10k to midsupply point, unless otherwise noted.

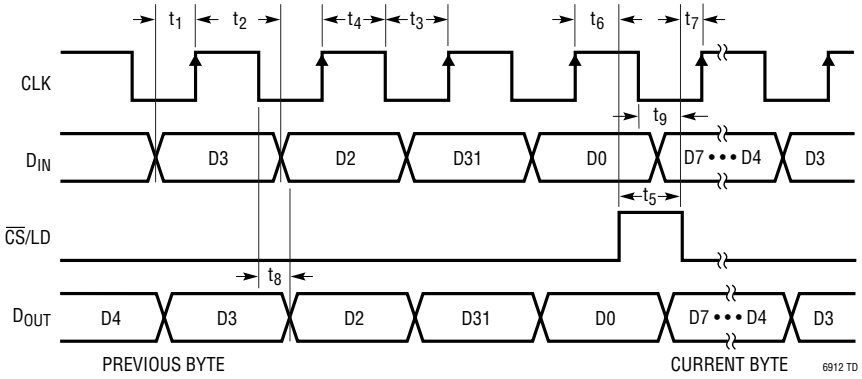
PARAMETER	CONDITIONS	C, I GRADES MIN	C, I GRADES TYP	C, I GRADES MAX	H GRADE MIN	H GRADE TYP	H GRADE MAX	UNITS
Specifications for the LTC6912-2 ONLY								
Voltage Noise Density (Referred to Input)	f = 50kHz							
	Gain = 1		31.1			31.1		nV/√Hz
	Gain = 2		22.8			22.8		nV/√Hz
	Gain = 4		17			17		nV/√Hz
	Gain = 8		14.6			14.6		nV/√Hz
	Gain = 16		13.2			13.2		nV/√Hz
	Gain = 32		12.9			12.9		nV/√Hz
	Gain = 64		12.6			12.6		nV/√Hz
Total Harmonic Distortion	Gain = 8, f_{IN} = 10kHz, V_{OUT} = $1V_{RMS}$		–84 0.006			–84 0.006		dB %
	Gain = 8, f_{IN} = 100kHz, V_{OUT} = $1V_{RMS}$		–82 0.008			–82 0.008		dB %

SERIAL INTERFACE SPECIFICATIONS

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Digital I/O Logic Levels, All Digital I/O Voltage Referenced to DGND							
V_{IH}	Digital Input High Voltage		●	2			V
V_{IL}	Digital Input Low Voltage		●			0.8	V
V_{OH}	Digital Output High Voltage	Sourcing 500µA	●	V^+ – 0.3			V
V_{OL}	Digital Output Low Voltage	Sinking 500µA	●			0.3	V
Serial Interface Timing, V^+ = 2.7V ~ 4.5V, V^- = 0V (Note 10)							
t_1	D_{IN} Valid to CLK Setup		●	60			ns
t_2	D_{IN} Valid to CLK Hold		●	0			ns
t_3	CLK Low		●	100			ns
t_4	CLK High		●	100			ns
t_5	$\overline{CS}$/LD Pulse Width		●	60			ns
t_6	LSB CLK to $\overline{CS}$/LD		●	60			ns
t_7	$\overline{CS}$/LD Low to CLK		●	30			ns
t_8	D_{OUT} Output Delay	C_L = 15pF	●			125	ns
t_9	CLK Low to $\overline{CS}$/LD Low		●	0			ns
Serial Interface Timing, V^+ = 4.5V ~ 5.5V, V^- = 0V (Note 10)							
t_1	D_{IN} Valid to CLK Setup		●	30			ns
t_2	D_{IN} Valid to CLK Hold		●	0			ns
t_3	CLK Low		●	50			ns
t_4	CLK High		●	50			ns
t_5	$\overline{CS}$/LD Pulse Width		●	40			ns
t_6	LSB CLK to $\overline{CS}$/LD		●	40			ns
t_7	$\overline{CS}$/LD Low to CLK		●	20			ns
t_8	D_{OUT} Output Delay	C_L = 15pF	●			85	ns
t_9	CLK Low to $\overline{CS}$/LD Low		●	0			ns

SERIAL INTERFACE SPECIFICATIONS

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Serial Interface Timing, Dual ±4.5V ~ ±5.5V Supplies (Note 10)							
t_1	D_{IN} Valid to CLK Setup		●	30			ns
t_2	D_{IN} Valid to CLK Hold		●	0			ns
t_3	CLK High		●	50			ns
t_4	CLK Low		●	50			ns
t_5	$\overline{CS}$/LD Pulse Width		●	40			ns
t_6	LSB CLK to $\overline{CS}$/LD		●	40			ns
t_7	$\overline{CS}$/LD Low to CLK		●	20			ns
t_8	D_{OUT} Output Delay	C_L = 15pF	●			85	ns
t_9	CLK Low to $\overline{CS}$/LD Low		●	0			ns



Note 1: Absolute Maximum Ratings are those values beyond which the life of the device may be impaired.

Note 2: The LTC6912-1C and LTC6912-1I are guaranteed functional over the operating temperature range of –40°C to 85°C. The LTC6912-1H is guaranteed functional over the operating temperature range of –40°C to 125°C.

Note 3: The LTC6912-1C is guaranteed to meet specified performance from 0°C to 70°C. The LTC6912-1C is designed, characterized and expected to meet specified performance from –40°C to 85°C but is not tested or QA sampled at these temperatures. The LTC6912-1I is guaranteed to meet specified performance from –40°C to 85°C. The LTC6912-1H is guaranteed to meet specified performance from –40°C to 125°C.

Note 4: Output voltage swings are measured as differences between the output and the respective supply rail.

Note 5: Extended operation with output shorted may cause junction temperature to exceed the 150°C limit for GN package and 125°C for a DFN package is not recommended.

Note 6: Gain is measured with a large signal DC test using an output excursion between approximately 30% and 70% of supply voltage.

Note 7: Channel-to-channel isolation is measured by applying a 200kHz input signal to one channel so that its output varies $1V_{RMS}$, and measuring the output voltage RMS of the other channel relative to AGND with its input tied to AGND. Isolation is calculated:

$Isolation_B = 20 \bullet \log^{10}(V_{OUTA}/V_{OUTB})$ or
$Isolation_A = 20 \bullet \log^{10}(V_{OUTB}/V_{OUTA})$

High channel-to-channel isolation is strongly dependent on proper circuit layout. See Applications Information.

Note 8: Offset voltage referred to the INA or INB input is (1 + 1/|GAIN|) times the offset voltage of the internal op amp, where GAIN is the nominal gain magnitude. The typical offset voltage values are for 25°C only. See Applications Information.

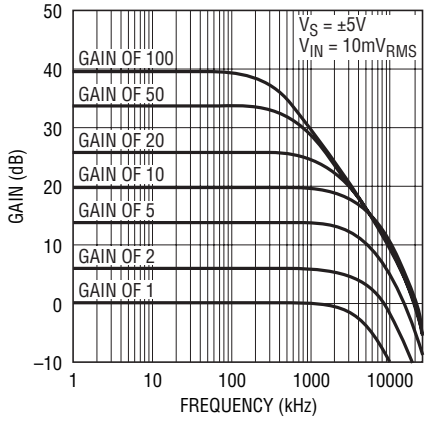
Note 9: Input resistance can vary by approximately ±30% part-to-part at a given gain setting.

Note 10: Guaranteed by design, not subject to test.

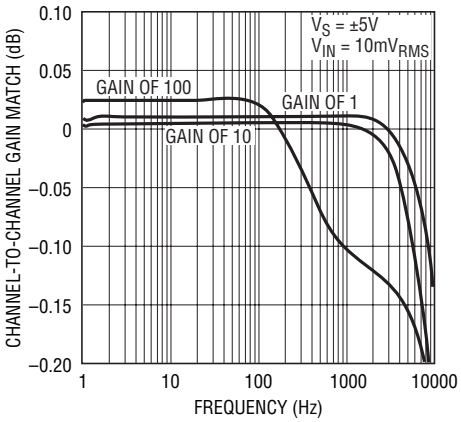
Note 11: States 13, 14 and 15 (binary 11xx) are not used. Programming a channel to states 8 or higher will configure that particular channel into a low power shutdown state. In addition, programming a channel into state 15 (binary 1111) will cause that particular channel to draw up to 20mA of supply current and is not recommended.

TYPICAL PERFORMANCE CHARACTERISTICS

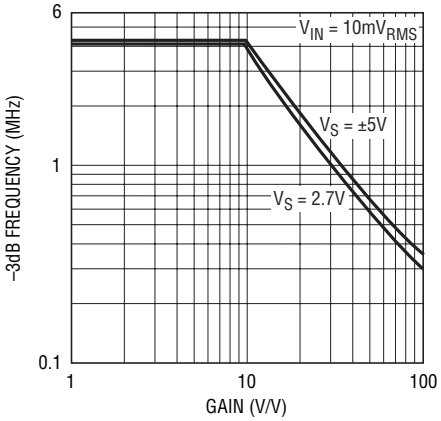
LTC6912-1 Frequency Response



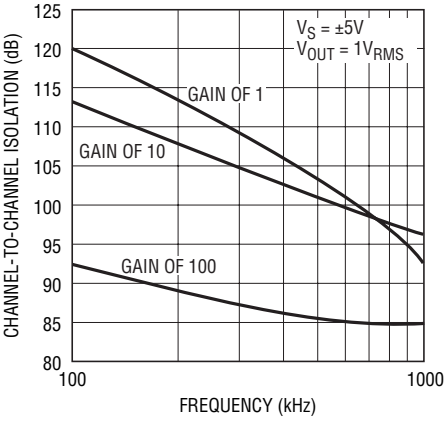
LTC6912-1 Channel Gain Matching vs Frequency



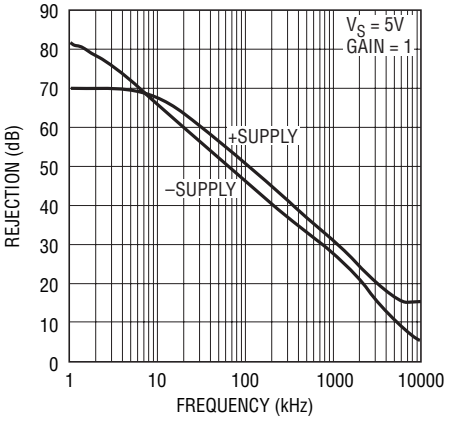
LTC6912-1 –3dB Bandwidth vs Gain Setting



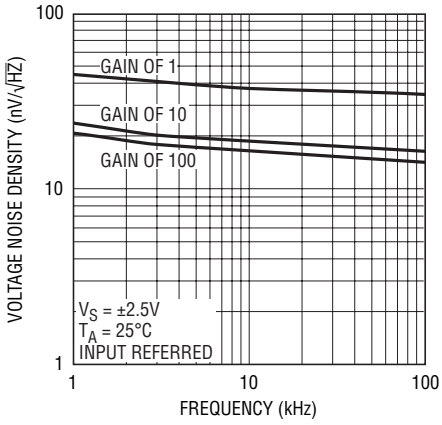
LTC6912-1 Channel Isolation vs Frequency



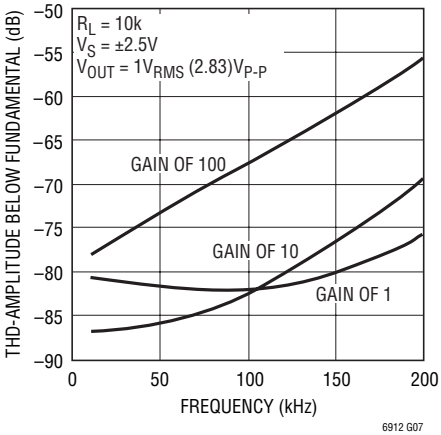
LTC6912-1 Power Supply Rejection vs Frequency



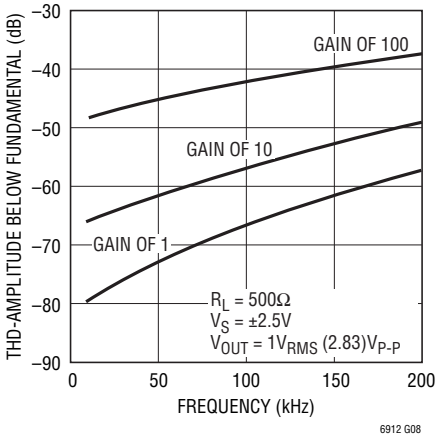
LTC6912-1 Noise Density vs Frequency



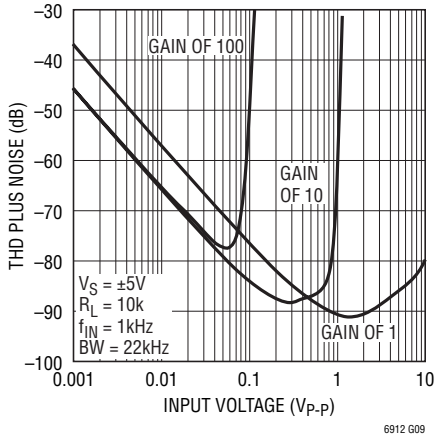
LTC6912-1 Distortion vs Frequency with Light Loading



LTC6912-1 Distortion vs Frequency with Heavy Loading

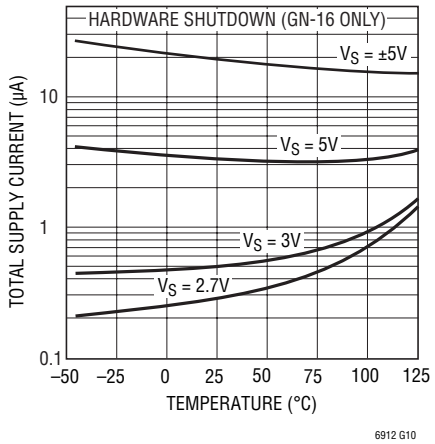


LTC6912-1 THD Plus Noise vs Input Voltage

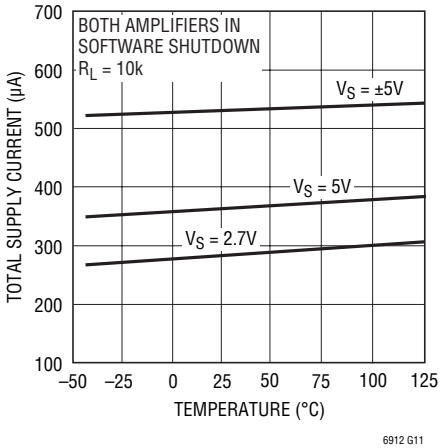


TYPICAL PERFORMANCE CHARACTERISTICS

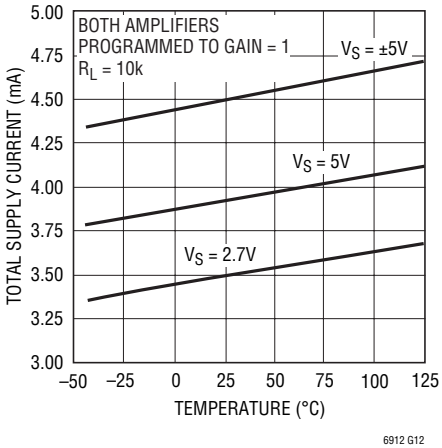
LTC6912-1 Hardware Shutdown Total Supply Current vs Temperature



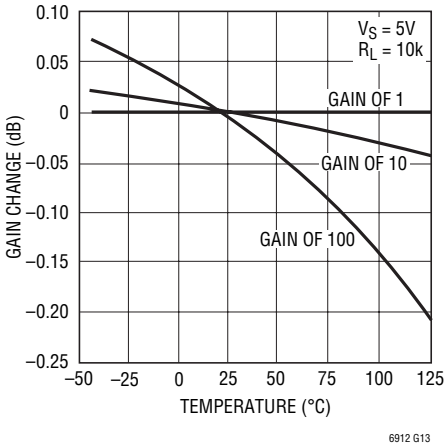
LTC6912-1 Software Shutdown Total Supply Current vs Temperature



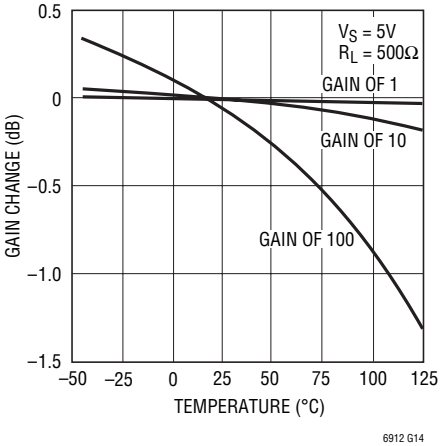
LTC6912-1 Total Supply Current vs Temperature (Both Amplifiers Active)



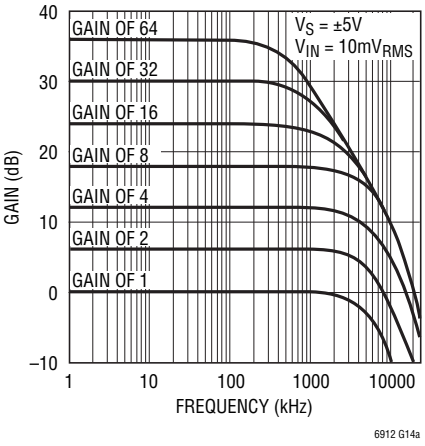
LTC6912-1 Gain Shift vs Temperature (Light Load)



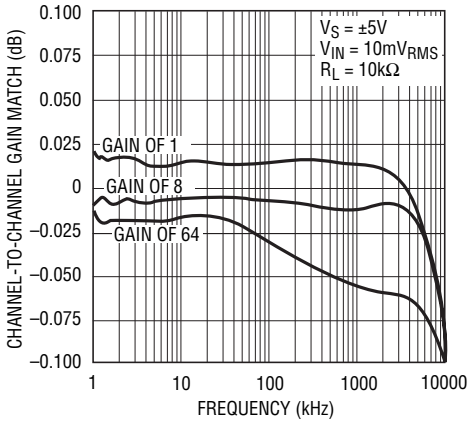
LTC6912-1 Gain Shift vs Temperature (Heavy Load)



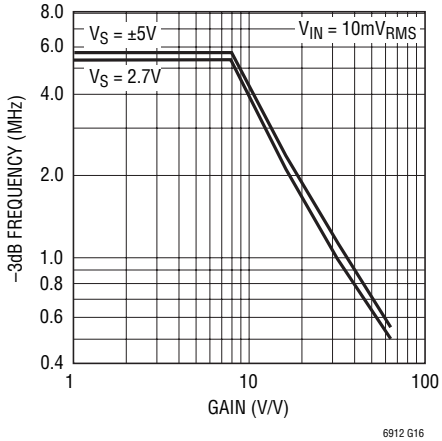
LTC6912-2 Frequency Response



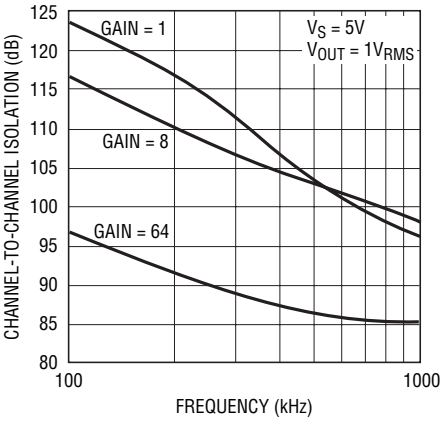
LTC6912-2 Channel Gain Matching vs Frequency



LTC6912-2 –3dB Bandwidth vs Gain Setting

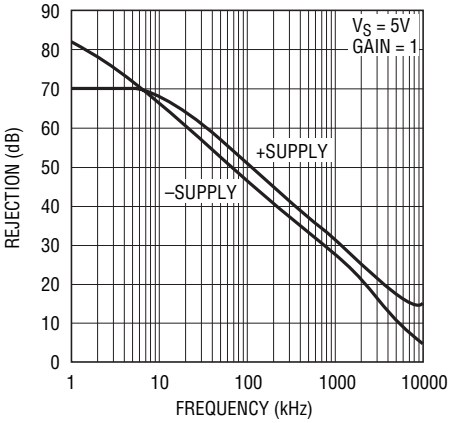


LTC6912-2 Channel Isolation vs Frequency

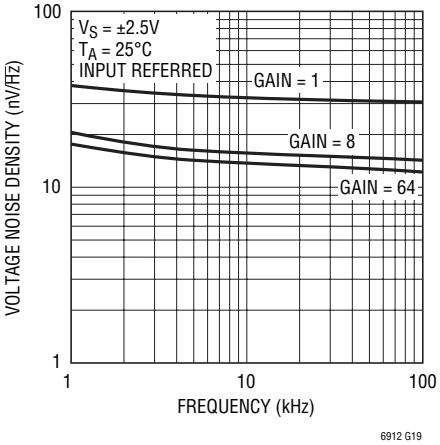


TYPICAL PERFORMANCE CHARACTERISTICS

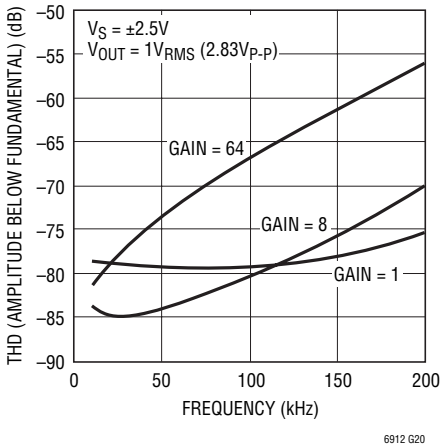
LTC6912-2 Power Supply Rejection vs Frequency



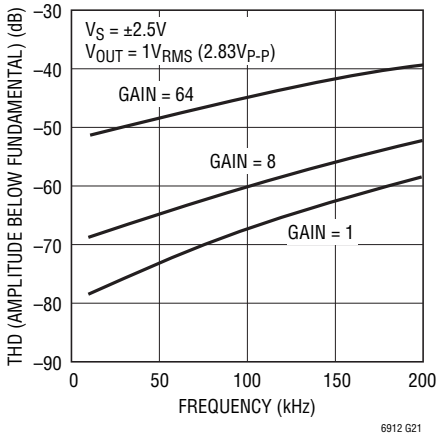
LTC6912-2 Noise Density vs Frequency



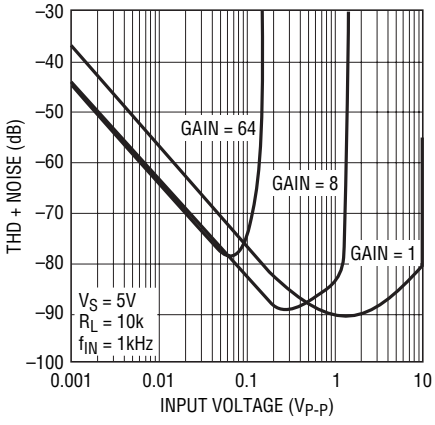
LTC6912-2 Distortion vs Frequency with Light Loading (R_L = 10k)



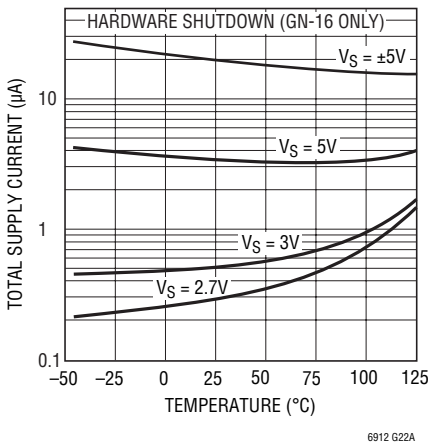
LTC6912-2 Distortion vs Frequency with Heavy Loading (R_L = 500Ω)



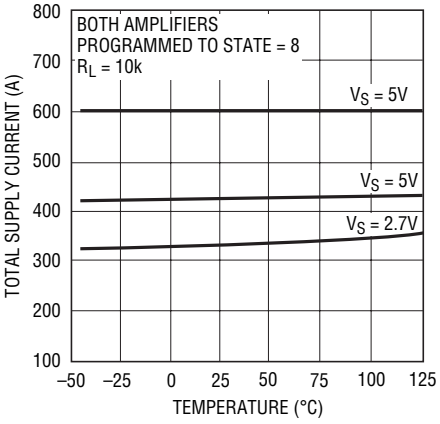
LTC6912-2 THD + Noise vs Input Voltage



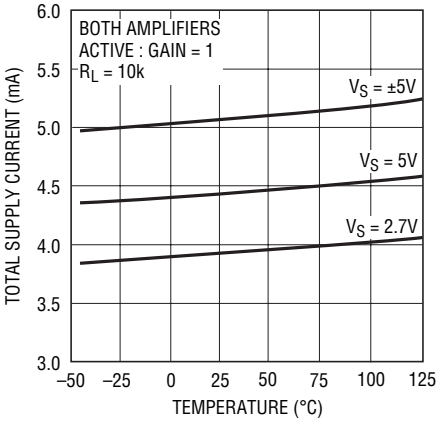
LTC6912-2 Hardware Shutdown Total Supply Current vs Temperature



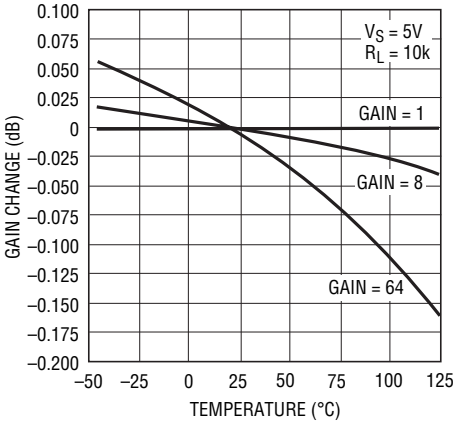
LTC6912-2 Software Shutdown Total Supply Current vs Temperature



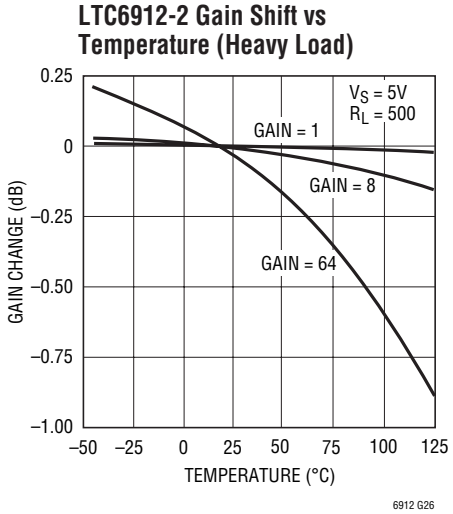
LTC6912-2 Total Supply Current vs Temperature (Both Amplifiers Active)



LTC6912-2 Gain Shift vs Temperature (Light Load)



TYPICAL PERFORMANCE CHARACTERISTICS



PIN FUNCTIONS

INA, INB: Analog Inputs. The input signal to the A channel amplifier of the LTC6912-X is the voltage difference between the INA pin and AGND pin. Likewise, the input signal to the B channel amplifier of the LTC6912-X is the voltage difference between the INB pin and AGND pin. The INA (or INB) pin connects internally to a digitally controlled resistance whose other end is a current summing point at the same potential as the AGND pin (Figure 1). At unity gain, the value of this input resistance is approximately 10kΩ and the INA (or INB) pin voltage range is rail-to-rail (V^+ to $V^–$). At gain settings above unity, the input resistance falls. The linear input range at INA and INB also falls inversely proportional to the programmed gain. Tables 1 and 2 summarize this behavior. The higher gains are designed to boost lower level signals with good noise performance. In the "zero" gain state (state = 0), or in software shutdown (state = 8) analog switches disconnect the INA or INB pin internally and this pin presents a very high input resistance. In the "zero" gain state (state = 0), the input may vary from rail to rail but the output is insensitive to it and is forced to the AGND potential. Circuitry driving the INA and INB pins must consider the LTC6912-X's input resistance, its process variance, and the variation of this resistance from gain setting to gain setting. Signal sources with significant output resistance may introduce a gain error as the source's output resistance and the LTC6912-X's input resistance forms a voltage divider. This is especially true at higher gain settings where the input resistance is the lowest.

In single supply voltage applications, the LTC6912-X's DC ground reference for both input and output is AGND, not $V^–$. With increasing gains, the LTC6912-X's input voltage range for an unclipped output is no longer rail-to-rail but diminishes inversely to gain, centered about the AGND potential.

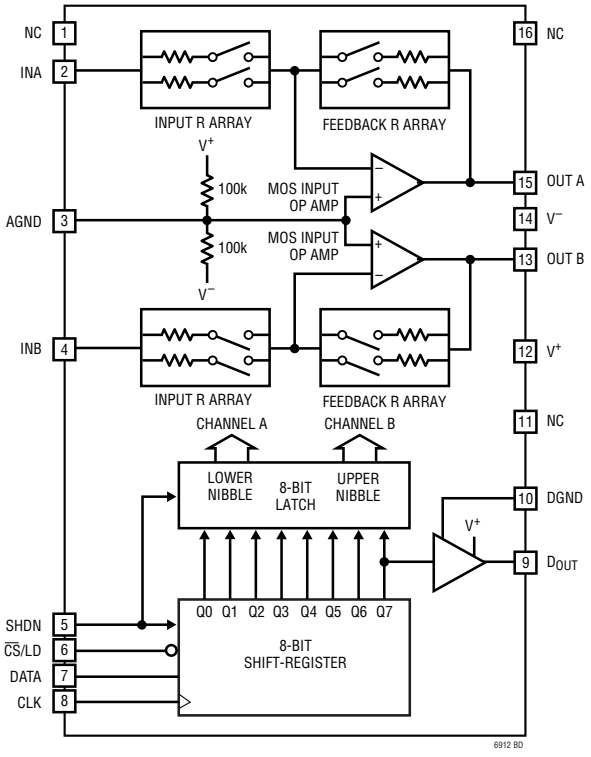


Figure 1. GN-16 Block Diagram

PIN FUNCTIONS

AGND: Analog Ground. The AGND pin is at the midpoint of an internal resistive voltage divider, developing a potential halfway between the V^+ and V^- pins. In normal operation, the AGND pin has an equivalent input resistance of nominally 50k (Figure 1). In order to reduce the quiescent supply current in hardware shutdown (SHDN pin pulled to V^+, GN-16 only), the equivalent series resistance of this pin significantly increases (to a value on the order of 800kΩ with 5V supplies, but is highly supply voltage, temperature, and process dependent). AGND is the noninverting input to both the internal channel A and channel B amplifiers. This makes AGND the ground reference voltage for the INA, INB, OUTA, and OUTB pins. Recommended analog ground plane connection depends on how power is applied to the LTC6912-X (See Figures 2, 3, and 4). Single power supply applications typically use V^- for the system signal ground. The analog ground plane in single-supply applications should therefore tie to V^-, and the AGND pin should be bypassed to this ground plane by a high quality capacitor of at least 0.1µF (Figure 2). The AGND pin provides an internal analog reference voltage at half the V^+ supply voltage. Dual supply applications with symmetrical supplies (such as ±5V) have a natural system ground plane potential of zero volts, in which the AGND pin can be directly tied to, making the zero volt ground plane the input and output reference voltage for the LTC6912-X (Figure 3). Finally, if dual asymmetrical power supplies are used, the supply ground is still the natural ground plane voltage. To maximize signal swing capability with an asymmetrical supply, however, it is often desirable to refer the LTC6912-X's analog input and output to a voltage equidistant from the two supply rails V^+ and V^-. The AGND pin will provide such a potential when open-circuited and bypassed with a capacitor (Figure 4). In noise sensitive applications where AGND does not tie directly to a ground plane, as in Figures 2 and 4, it is important to AC-bypass the AGND pin. Otherwise channel to channel isolation is degraded, and wideband noise will enter the signal path from the thermal noise of the internal voltage divider resistors which present a Thévenin equivalent resistance of approximately 50kΩ. This noise can reduce SNR by at least 15dB at high gain settings. An external capacitor from AGND to the ground plane, whose impedance is well below 50kΩ at frequencies of interest, will filter and suppress this noise. A 0.1µF high quality capacitor is effective for frequencies down to 1kHz. Larger capacitors will extend this suppression to lower frequencies. This issue does not arise in dual supply applications because the AGND pin ties directly to ground. In applications requiring an analog ground reference other than half the total supply voltage, the user can override the built-in analog ground reference by tying the AGND pin to a reference voltage with the AGND voltage range specified in the Electrical Characteristics Table. The AGND pin will load the external reference with approximately 50kΩ returned to the half-supply potential. AGND should still be capacitively bypassed to a ground plane as noted above. Do not connect the AGND pin to the V^- pin.

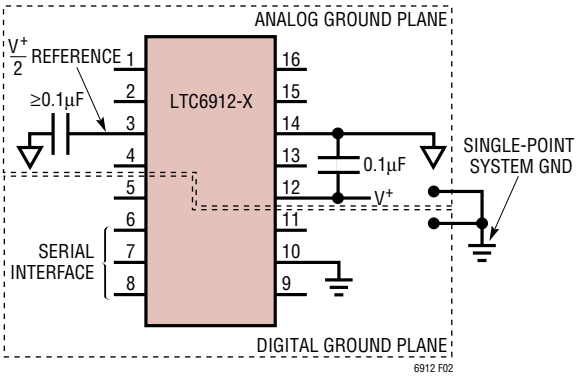


Figure 2. Single Supply Ground Plane Connection

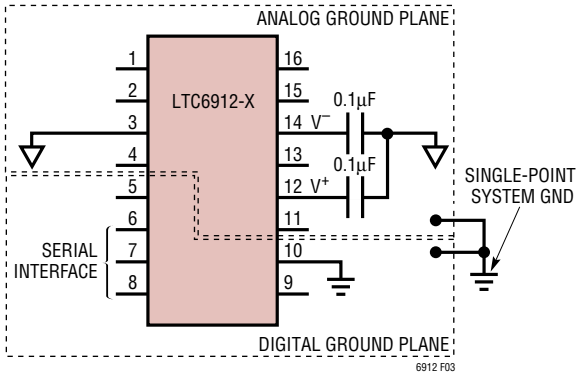


Figure 3. Symmetrical Dual Supply Ground Plane Connection

PIN FUNCTIONS

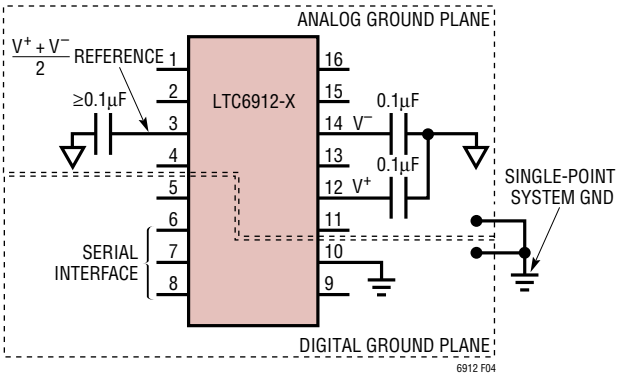


Figure 4. Asymmetrical Dual Supply Ground Plane Connection

SHDN (GN-16 ONLY): CMOS Compatible Logic Hardware Shutdown Input. The LTC6912-X has two shutdown modes. One is a software shutdown state which can be software programmed into either Channel A, Channel B, or both. The software shutdown, when programmed to a particular channel (state = 8), will disable that channel's amplifier and tri-state open its analog input and analog output. The serial interface, however is still active. A hardware shutdown occurs when the SHDN pin is pulled to the positive rail. In this condition, both amplifiers and serial interface are disabled. The SHDN pin is allowed to swing from V^- to 10.5V above V^-, regardless of V^+ so long as the logic levels meet the minimum requirements specified in the Electrical Characteristics table. The SHDN pin is a high impedance CMOS logic input, but has a small pull-down current source (<10µA) which will force SHDN low if the logic input is externally floated. On initial power up (with SHDN open), or coming out of the hardware shutdown mode (pulling SHDN to V^-), both amplifiers are reset into the power-on reset state (software shutdown mode, state = 8) for both channels.

$\overline{CS}$/LD: TTL/CMOS Compatible Logic Input. When this pin is asserted low, the CLK pin is enabled, and the 8-bit shift register serially shifts the shift register contents and whatever data is present on the D_{IN} pin into the shift register on the rising edge of CLK. On the rising edge of $\overline{CS}$/LD, the contents of the shift register data are loaded into the eight bit latch which configures the gain state of both channel A and channel B amplifiers. A logic high on $\overline{CS}$/LD inhibits the CLK signal internally to the IC.

D_{IN}: TTL/CMOS Compatible Logic Serial Data Input. The serial interface is synchronously loaded MSB first via D_{IN} on the rising edge of CLK with $\overline{CS}$/LD asserted low.

CLK: TTL/CMOS Compatible Logic Input. With $\overline{CS}$/LD asserted low, the clock synchronizes the loading of the serial shift register on its rising and falling edges. Data is shifted in at D_{IN} on the rising edge of CLK and is shifted out on D_{OUT} on the falling edge of CLK.

D_{OUT}: TTL/CMOS Compatible Logic Output. The MSB of the shift register contents is shifted out at D_{OUT} on the falling edge of CLK. The output at D_{OUT} swings between V^+ and DGND, and is rated to drive approximately 15pF.

DGND: Digital Ground: The DGND pin defines the potential from which LOGIC levels V_{IH} and V_{IL} for the 3-wire serial digital interface are referenced. The recommended connection of DGND depends on how power is applied to the LTC6912 (See Figures 2, 3, and 4). (CAVEAT: Under no conditions is DGND to exceed either supply pins V^+ and V^-, which could result in damage to the IC if not current limited.)

Single power supply applications typically use V^- for the system signal ground. The preferred connection for DGND is therefore V^- (See Figure 2).

Dual supply applications with symmetrical supplies (such as ±5V) have a natural system ground potential of zero volts, in which the DGND pin can be tied to, making the zero volt ground plane the logic reference (Figure 3).

Finally, if dual asymmetrical power supplies are used, the system ground is still the natural ground plane voltage.

V^-, V^+: Power Supply Pins. The V^+ and V^- pins should be bypassed with 0.1µF capacitors to an adequate analog ground plane using the shortest possible wiring. Electrically clean supplies and a low impedance ground are important for the high dynamic range available from the LTC6912 (see further details under the AGND pin description). Low noise linear power supplies are recommended. Switching power supplies require special care to prevent switching noise coupling into the signal path, reducing dynamic range.

PIN FUNCTIONS

OUT A, OUT B: Analog Output. These pins are the output of the A and B channel amplifiers respectively. Each operational amplifier can swing rail-to-rail (V^+ to V^-) as specified in the Electrical Characteristics table. For best performance, loading the output as lightly as possible will minimize signal distortion and gain error. The Electrical Characteristics table shows performance at output currents up to 10mA, and the current limits which occur when the output is shorted midsupply at 2.7V and ±5V supplies. Output current above 10mA is possible but current-limiting circuitry will begin to affect amplifier performance at approximately 20mA. Long-term operation above 20mA output is not recommended. Do not exceed maximum junction temperature of 150°C for a GN and 125°C for a DFN package. The output will drive capacitive loads up to 50pF. Capacitances higher than 50pF should be isolated by a series resistor (10Ω or higher).

APPLICATIONS INFORMATION

Functional Description

The LTC6912-X is a small outline, wideband, inverting two-channel amplifier with voltage gains that are independently programmable. Each delivers a choice of eight voltage gains, configurable through a 3-wire serial digital interface, which accepts TTL or CMOS logic levels (See Figure 5). Tables 1 and 2 list the nominal gains for the LTC6912-1 and LTC6912-2 respectively. Gain control within the amplifier occurs by switching resistors from a matched array in or out of a closed-loop op amp circuit using MOS analog switches (Figure 1). The bandwidths of the individual amplifiers depend on gain setting. The Typical Performance Characteristics section shows measured frequency responses.

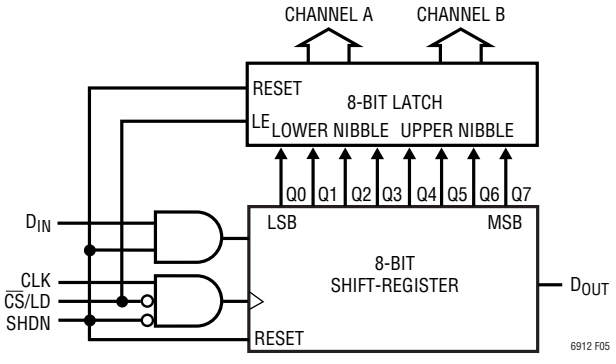


Figure 5. Serial Digital Interface Block Diagram

Description of the 3-Wire SPI Interface

Gain control of each amplifier is independently programmable using the 3-wire SPI interface (see Figure 5). Logic levels for the LTC6912 3-wire serial interface are TTL/CMOS compatible. When $\overline{CS}$/LD is low, the serial data on D_{IN} is shifted into an 8-bit shift-register on the rising edge of the clock, with the MSB transferred first. Serial data on D_{OUT} is shifted out on the clock's falling edge. A rising edge on $\overline{CS}$/LD will latch the shift-register's contents into an 8-bit D-latch and disable the clock internally on the IC. The upper nibble of the D-latch (4 most significant bits), configure the gain for the B-channel amplifier. The lower nibble of the D-latch (4 least significant bits), configures the gain for the A-channel amplifier. Tables 1 and 2 detail the nominal gains and respective gain codes. Care must be taken to ensure CLK is taken low before $\overline{CS}$/LD is pulled low to avoid an extra internal clock pulse to the input of the 8-bit shift-register (See Figure 5).

D_{OUT} is active in all states, therefore D_{OUT} cannot be "wire-OR'd" to other SPI outputs.

An LTC6912 may be daisy-chained with other LTC6912s or other devices having serial interfaces by connecting the D_{OUT} to the D_{IN} of the next chip while CLK and $\overline{CS}$/LD remain common to all chips in the daisy chain. The serial data is clocked to all the chips then the $\overline{CS}$/LD signal is pulled high to update all of them simultaneously. Figure 6 shows an example of two LTC6912s in a daisy chained SPI

APPLICATIONS INFORMATION

configuration. It is recommended the serial interface signals should remain idle in between data transfers in order to minimize digital noise coupling into the analog path.

Power On Reset

On the initial application of power, the power on reset state of both amplifiers is low power software shutdown (state = 8) (see Tables 1 and 2). In this state, both analog amplifiers are disabled and have their inputs and outputs opened. This will facilitate the application of using the device as a 2:1 analog MUX, in that the amplifier's outputs may be wired-OR together and the LTC6912 can alternately select between A and B channels. Care must be taken if the outputs are wired-OR'd to ensure the software shutdown state (state = 8) is always programmed in one of the two channels.

Timing Constraints

Settling time in the CMOS gain-control logic is typically several nanoseconds and is faster than the analog signal path. When the amplifier gain changes, the limiting timing is analog. As with any programmable-gain amplifier, each gain change causes an output transient as the amplifier's output moves, with finite speed, toward a differently scaled version of the input signal. The LTC6912-X analog path settles with a characteristic time constant or time scale, τ, that is roughly the standard value for a first order band limited response:

$$\tau = 0.35/f_{-3dB}$$

See the –3dB BW vs Gain Setting graph in the Typical Performance Characteristics section.

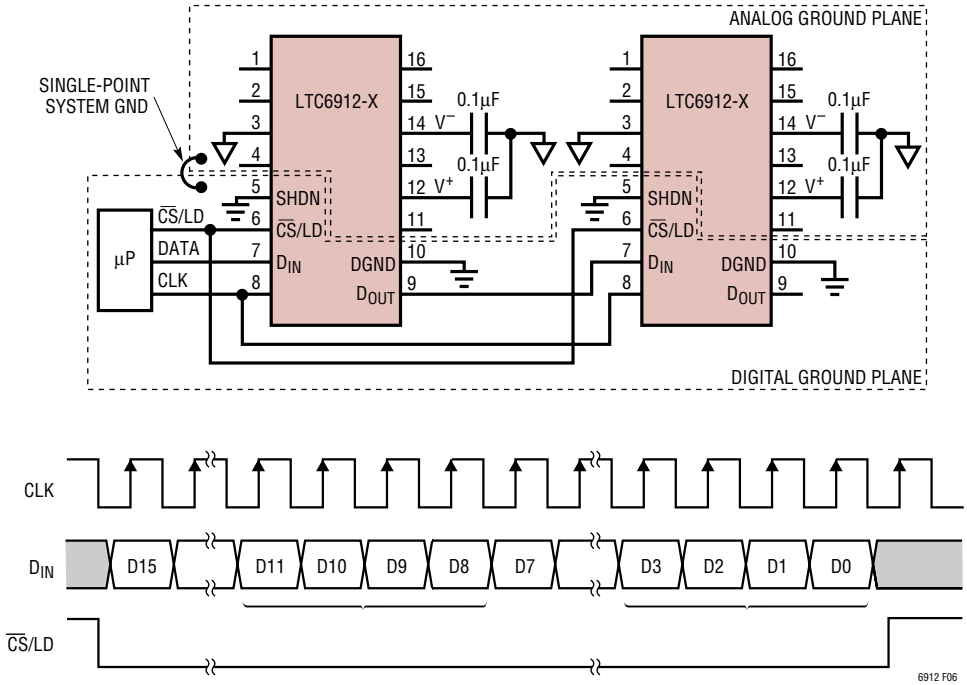


Figure 6. Two LTC6912s (Four PGAs) in Daisy Chain Configuration

APPLICATIONS INFORMATION

Offset Voltage vs Gain Setting

The electrical tables list DC offset (error), $V_{OS(OA)}$, at the inputs of the internal op amp (See Figure 1). The electrical tables also show the resulting, gain dependent offset voltage referred to the INA, or INB pins, $V_{OS(IN)}$. The two measures are related through the feedback/input resistor ratio, which equals the nominal gain-magnitude setting, |GAIN|:

$$V_{OS(IN)} = (1 + 1/|GAIN|)\ V_{OS(OA)}$$

Offset voltages at any gain setting can be inferred from this relationship. For example, an internal amplifier offset $V_{OS(OA)}$ of 1mV will appear referred to the INA, INB pins as 2mV at a gain setting of 1, or 1.5mV at a gain setting of 2. At high gains, $V_{OS(IN)}$ approaches $V_{OS(OA)}$. (Offset voltage is random and can have either polarity centered on 0V). The MOS input circuitry of the internal op amp in Figure 1 draws negligible input currents (less than 10µA), so only $V_{OS(OA)}$ and the GAIN affect the overall amplifier's offset.

AC-Coupled Operation

Adding capacitors in series with the INA and INB pins converts the LTC6912-X into a dual AC-coupled inverting amplifier, suppressing the input signal's DC level (and also adding the additional benefit of reducing the offset voltage from the LTC6912-X's amplifier itself). No further components are required because the input of the LTC6912-X biases itself correctly when a series capacitor is added. The INA and INB analog input pins connect internally to a resistor whose nominal value varies between 10kΩ and 1kΩ depending on the version of LTC6912 used (see the rightmost column of Tables 1 and 2). Therefore, the low frequency cutoff will vary with capacitor and gain setting. If, for example, a low frequency corner of 1kHz (or lower) on the LTC6912-1 is desired, use a series capacitor of 0.16µF or larger. 0.16µF has a reactance of 1kΩ at 1kHz, giving a 1kHz lower –3dB frequency for gain settings of 10V/V through 100V/V. If the LTC6912-1 is operated at lower gain settings with a 0.16µF capacitor, the higher input resistance will reduce the lower corner frequency down to 100Hz at a gain setting of 1V/V. These frequencies scale inversely with the value of input capacitor used.

Note that operating the LTC6912 family in "zero" gain mode (digital state 0000) open circuits both the INA and INB pins and this demands some care if employed with a series AC coupling input capacitor. When the chip enters the zero gain mode, the opened INA or INB pin tends to sample and freeze the voltage across the capacitor to the value it held just before the zero gain state. This can place the INA or INB pin at or near the DC potential of a supply rail. (The INA or INB pin may also drift to a supply potential in this state due to small leakage currents.) To prevent driving the INA or INB pin outside the supply limit and potentially damaging the chip, avoid AC input signals in the zero gain state with an AC coupling capacitor. Also, switching later to a non-zero gain value will cause a transient pulse at the output of the LTC6912-1 (with a time constant set by the capacitor value and the new LTC6912-1 input resistance value). This occurs because the INA and INB pins return to the AGND potential forcing transient current sourced by the amplifier output to charge the AC coupling capacitor to its proper DC blocking value.

SNR and Dynamic Range

The term "dynamic range" is much used (and abused) with signal paths. Signal-to-noise (SNR) is an unambiguous comparison of signal and noise levels, measured in the same way and under the same operating conditions. In a variable gain amplifier, however, further characterization is useful because both noise and maximum signal level in the amplifier will vary with the gain setting, in general. In the LTC6912-X, maximum output signal is independent of gain (and is near the full power supply voltage, as detailed in the swing sections of the Electrical Characteristics table). The maximum input level falls with increasing gain, and the input-referred noise falls as well (listed also in the table). To summarize the useful signal range in such an amplifier, we define dynamic range (DR) as the ratio of maximum input (at unity gain) to minimum input-referred noise (at maximum gain). This DR has a physical interpretation as the range of signal levels that will experience an SNR above unity V/V or 0dB. At a 10V total power supply, DR in the LTC6912-X (gains 0V/V to 100V/V), the DR is typically 115dB (the ratio of 9.9 V_{P-P}, or 3.5V_{RMS}, maximum input to the 6.3µV_{RMS} high gain input noise). The

APPLICATIONS INFORMATION

SNR from an amplifier is the ratio of input level to input-referred noise, and can be 108dB with the LTC6912 family at unity gain.

Construction and Instrumentation Cautions

Electrically clean construction is important in applications seeking the full dynamic range of the LTC6912 family of dual amplifiers. It is absolutely critical to have AGND either AC bypassed or wired directly using the shortest possible wiring, to a low impedance ground return for best channel-to-channel isolation. Short, direct wiring minimizes parasitic capacitance and inductance. High quality supply bypass capacitors of 0.1µF near the chip provide good decoupling from a clean, low inductance power source. But several centimeters of wire (i.e., a few µH of inductance) from the power supplies, unless decoupled by substantial capacitance (>10µF) near the chip, can create a parasitic high-Q LC resonant circuit in the hundreds of kHz range in the chip's supplies or ground reference. This may impair circuit performance at those frequencies. A compact, carefully laid out printed circuit board with a good ground plane makes a significant difference in minimizing distortion. Finally, equipment to measure performance can itself introduce distortion or noise floors. Checking for these limits with wired shorts from INA to OUTA and INB to OUTB in place of the chip is a prudent routine procedure.

TYPICAL APPLICATION

Low Noise AC Amplifier with Programmable Gain and Bandwidth

Analog data acquisition can exploit band limiting as well as gain to suppress unwanted signals or noise. Tailoring an analog front end to both the level and bandwidth of each source maximizes the resulting SNR. Figure 7 shows a block diagram for a low noise amplifier with gain and bandwidth independently programmable over a 100:1 range. Channels A and B of the LTC6912-1 are used to independently control the gain and bandwidth respectively over a 100:1 range. The LT1884 dual op amp forms an integrating lowpass loop with capacitor C2 to set the programmable upper corner frequency. The LT1884 also supports rail-to-rail output swings over the total supply voltage range of 2.7V to 10.5V. AC coupling through capacitor C1 establishes a fixed low frequency corner of 1Hz, which can be adjusted by changing C1. Alternatively, shorting C1 makes the amplifier DC coupled. If DC gain is not needed, the AC coupling cap C1 serves to suppress several error sources: any shift in DC levels, low frequency noise, and DC offset voltages (not including the LT1884's low internal offset).

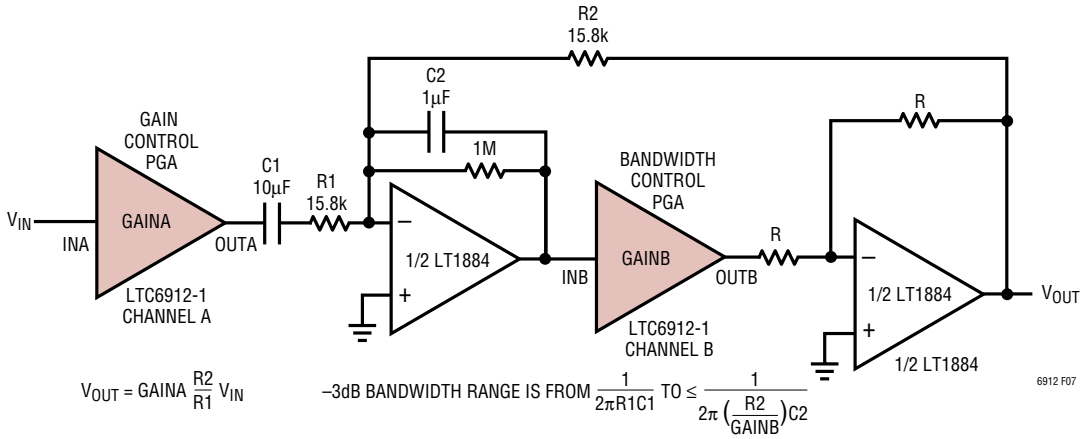
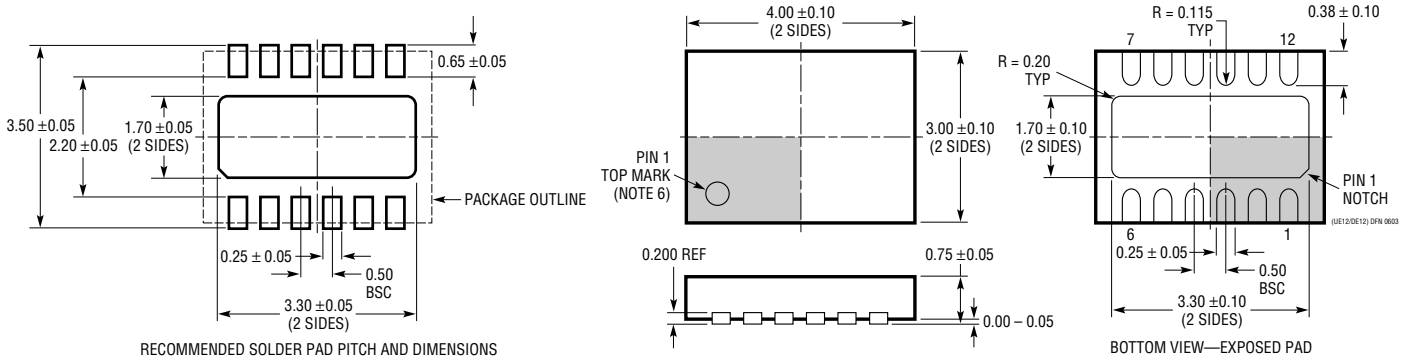


Figure 7. Block Diagram of an AC Amplifier with Programmable Gain and Bandwidth

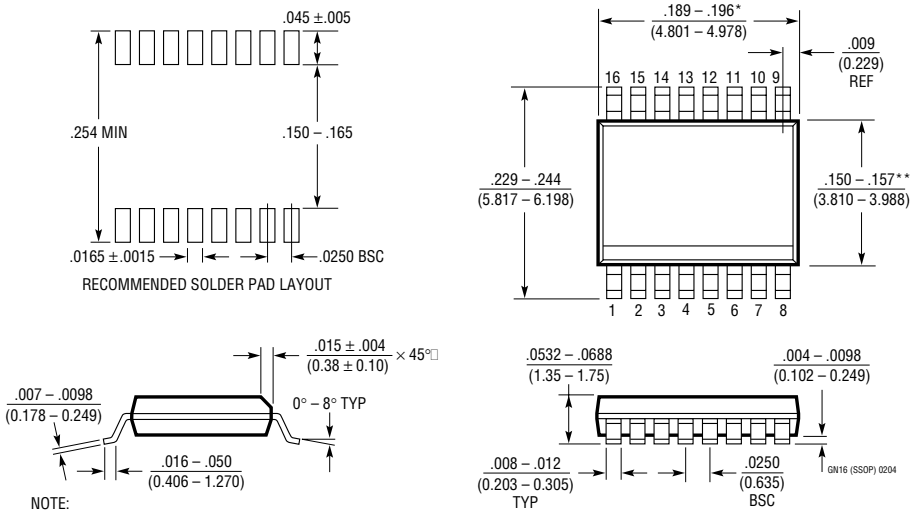
PACKAGE DESCRIPTION

DE/UE Package
12-Lead Plastic DFN (4mm × 3mm)
(Reference LTC DWG # 05-08-1695)



NOTE:
1. DRAWING PROPOSED TO BE A VARIATION OF VERSION (WGED) IN JEDEC PACKAGE OUTLINE M0-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

GN Package
16-Lead Plastic SSOP (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1641)



NOTE:
1. CONTROLLING DIMENSION: INCHES
2. DIMENSIONS ARE IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
3. DRAWING NOT TO SCALE

*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

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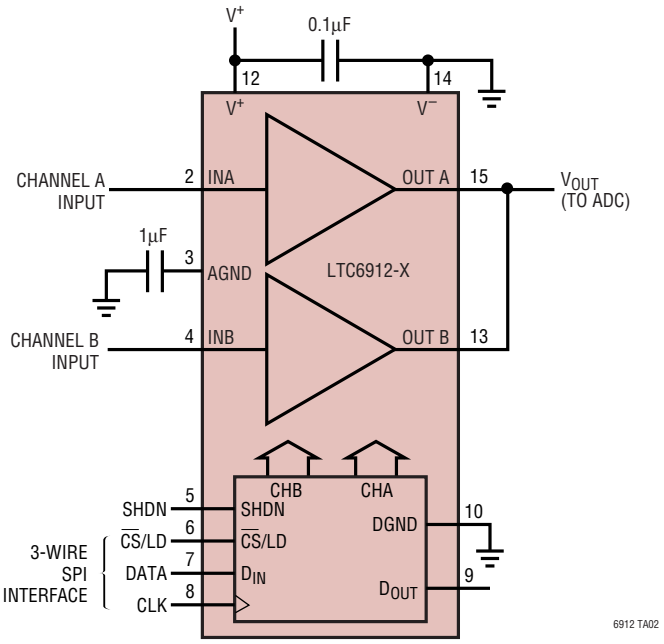
TYPICAL APPLICATION

A 2:1 PGA MUX



MUX OPERATION: IF THE LOWER NIBBLE (Q3, Q2, Q1, Q0) IS (1, 0, 0, 0) THEN OUTA IS IN TRI-STATE AND THE UPPER NIBBLE (Q7, Q6, Q5, Q4) CONTROLS THE ACTIVE CHANNEL B. IF THE UPPER NIBBLE IS (1, 0, 0, 0) THEN OUTB IS IN TRI-STATE AND THE LOWER NIBBLE CONTROLS ACTIVE CHANNEL A.

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1228	100MHZ Gain Controlled Transconductance Amplifier	Differential Input, Continuous Analog Gain Control
LT1251/LT1256	40Mhz Video Fader and Gain Controlled Amplifier	Two Input, One Output, Continuous Analog Gain Control
LTC1564	10kHz to 150kHz Digitally Controlled Filter and PGA	Continuous Time, Low Noise 8th Order Filter and 4-Bit PGA
LTC6910-1/-2/-3	Digitally Controlled Programmable Gain Amplifier in SOT-23	Single Programmable Gain Amplifier, 3-Bit Parallel Digital Interface
LTC6911-1/-2	Dual Digitally Controlled Programmable Gain Amplifier in MSOP-10	Dual Programmable Gain Amplifiers, 3-Bit Parallel Digital Interface
LTC6915	Zero Drift Instrumentation Amp with Digitally Programmable Gain	Gains 0 - 4096V/V, 116dB CMRR

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