THE DATASHEET OF

LYT4314L

LYT4211-4218/4311-4318
LYTSwitch™ High Power LED Driver IC Family

Single-Stage Accurate Primary-Side Constant Current (CC) Controller with PFC for Low-Line Applications, TRIAC Dimming and Non-Dimming Options

Product Highlights

- Better than ±5% CC regulation
- TRIAC dimmable to less than 5% output
- Fast start-up
  - <250 ms at full brightness
  - <1s at 10% brightness
- High power factor >0.9
- Easily meets EN61000-3-2
  - Less than 10% THD in optimized designs
- Up to 92% efficient
- 132 kHz switching frequency for small magnetics

High Performance, Combined Driver, Controller, Switch

The LYTSwitch family enables off-line LED drivers with high power factor which easily meet international requirements for THD and harmonics. Output current is tightly regulated with better than ±5% CC tolerance[1]. Efficiency of up to 92% is easily achieved in typical applications.

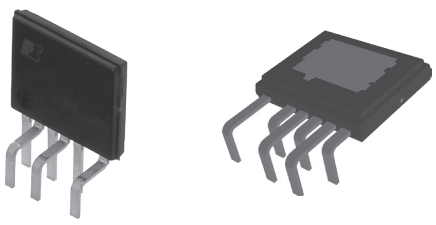
Supports a Wide Selection of TRIAC Dimmers

The LYTSwitch family provides excellent turn-on characteristics for leading-edge and trailing-edge TRIAC dimming applications. This results in drivers with a wide dimming range and fast start-up, even when turning-on from a low conduction angle. Large dimming ratio and low “pop-on” current.

Low Solution Cost and Long Lifetime

LYTSwitch ICs are highly integrated and employ a primary-side control technique that eliminates the optoisolator and reduces component count. This allows the use of low-cost single-sided printed circuit boards. Combining PFC and CC functions into a single-stage also helps reduce cost and increase efficiency. The 132 kHz switching frequency permits the use of small, low-cost magnetics.

LED drivers using the LYTSwitch family do not use primary-side aluminum electrolytic bulk capacitors. This means greatly extended driver lifetime, especially in bulb and other high temperature applications.



eSIP-7C (E Package) eSIP-7F (L Package)

Figure 2. Package Options.

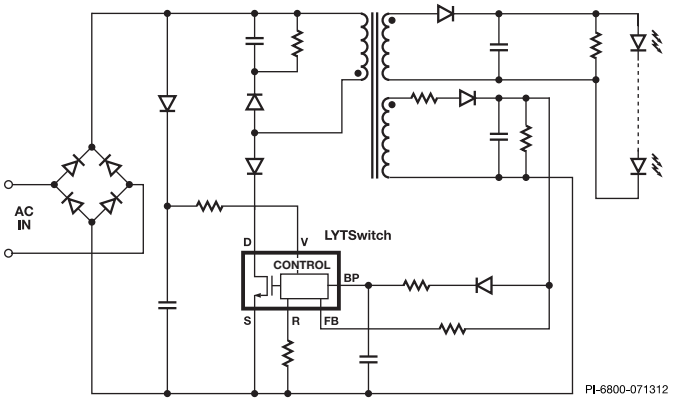


Figure 1. Typical Schematic.

Optimized for Different Applications and Power Levels

Part Number	Input Voltage Range	TRIAC Dimmable
LYT4211-LYT4218	85-132 VAC	No
LYT4311-LYT4318	85-132 VAC	Yes

Output Power Table[1,2]

Product[6]	Minimum Output Power[3]	Maximum Output Power[4]
LYT4x11E/L[5]	2.5 W	12 W
LYT4x12E/L	2.5 W	15 W
LYT4x13E/L	3.8 W	18 W
LYT4x14E/L	4.5 W	22 W
LYT4x15E/L	5.5 W	25 W
LYT4x16E/L	6.8 W	35 W
LYT4x17E/L	8.0 W	50 W
LYT4x18E/L	18 W	78 W

Table 1. Output Power Table.

Notes:

1. Performance for typical design. See Applications section.
2. Continuous power in an open-frame design with adequate heat sinking; device local ambient of 70 °C. Power level calculated assuming a typical LED string voltage and efficiency >80%.
3. Minimum output power requires C_{BP} = 47 µF.
4. Maximum output power requires C_{BP} = 4.7 µF.
5. LYT4311 C_{BP} = 47 µF, LYT4211 C_{BP} = 4.7 µF.
6. Package: eSIP-7C, eSIP-7F (see Figure 2).

Topology	Isolation	Efficiency	Cost	THD	Output Voltage
Isolated Flyback	Yes	88%	High	Best	Any
Buck	No	92%	Low	Good	Limited
Tapped Buck	No	89%	Middle	Best	Any
Buck-Boost	No	90%	Low	Best	High-Voltage

Table 2. Performance of Different Topologies in a Typical Non-Dimmable 10 W Low-Line Design.

Typical Circuit Schematic	Key Features

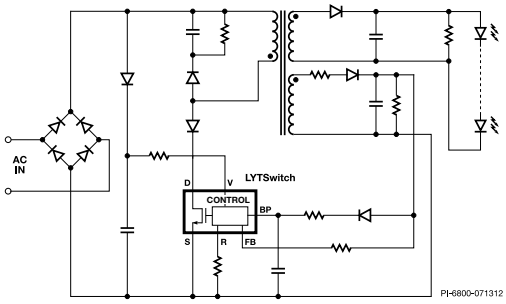
	**Flyback**
	Benefits
	• Provides isolated output
	• Supports widest range of output voltages
	• Very good THD performance
	Limitations
	• Flyback transformer
	  • Overall efficiency reduced by parasitic capacitance and inductance in the transformer
	  • Larger PCB area to meet isolation requirements
	• Requires additional components (primary clamp and bias)
	• Higher RMS switch and winding currents increases losses and lowers efficiency

Figure 3a. Typical Isolated Flyback Schematic.	

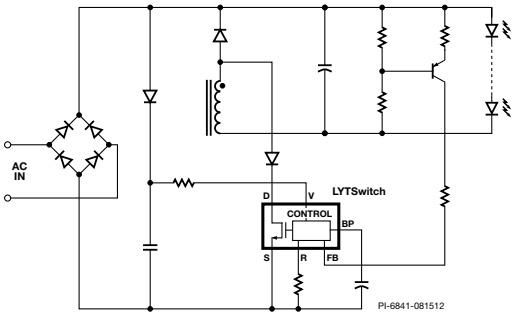
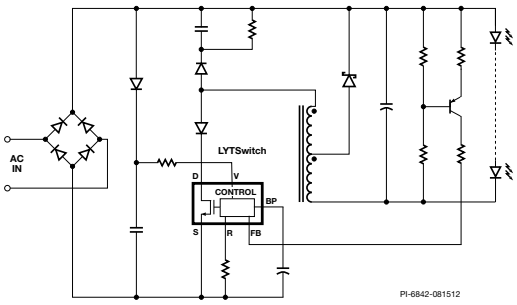
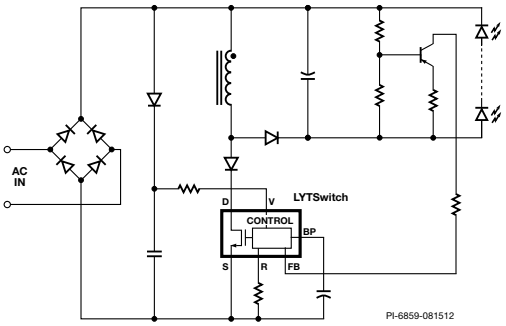
	**Buck**
	Benefits
	• Highest efficiency
	• Lowest component count – small size
	• Simple low-cost power inductor
	• Low drain source voltage stress
	• Best EMI/lowest component count for filter
	Limitations
	• Single input line voltage range
	  • Output voltage <0.6 × $V_{IN(AC)}$ × 1.41
	  • Output voltage for low THD designs
	  • Non-isolated

Figure 3b. Typical Buck Schematic.	
	**Tapped Buck** **Benefits** • Ideal for low output voltage designs (<20 V) • High efficiency • Low component count • Simple low-cost tapped inductor **Limitations** • Designs best suited for single input line voltage • Requires additional components (primary clamp) • Non-isolated
Figure 3c. Typical Tapped Buck Schematic.	
	**Buck-Boost** **Benefits** • Ideal for non-isolated high output voltage designs • High efficiency • Low component count • Simple common low-cost power inductor can be used • Lowest THD **Limitations** • Maximum V_{OUT} is limited by MOSFET breakdown voltage • Single input line voltage range • Non-isolated
Figure 3d. Typical Buck-Boost Schematic.	

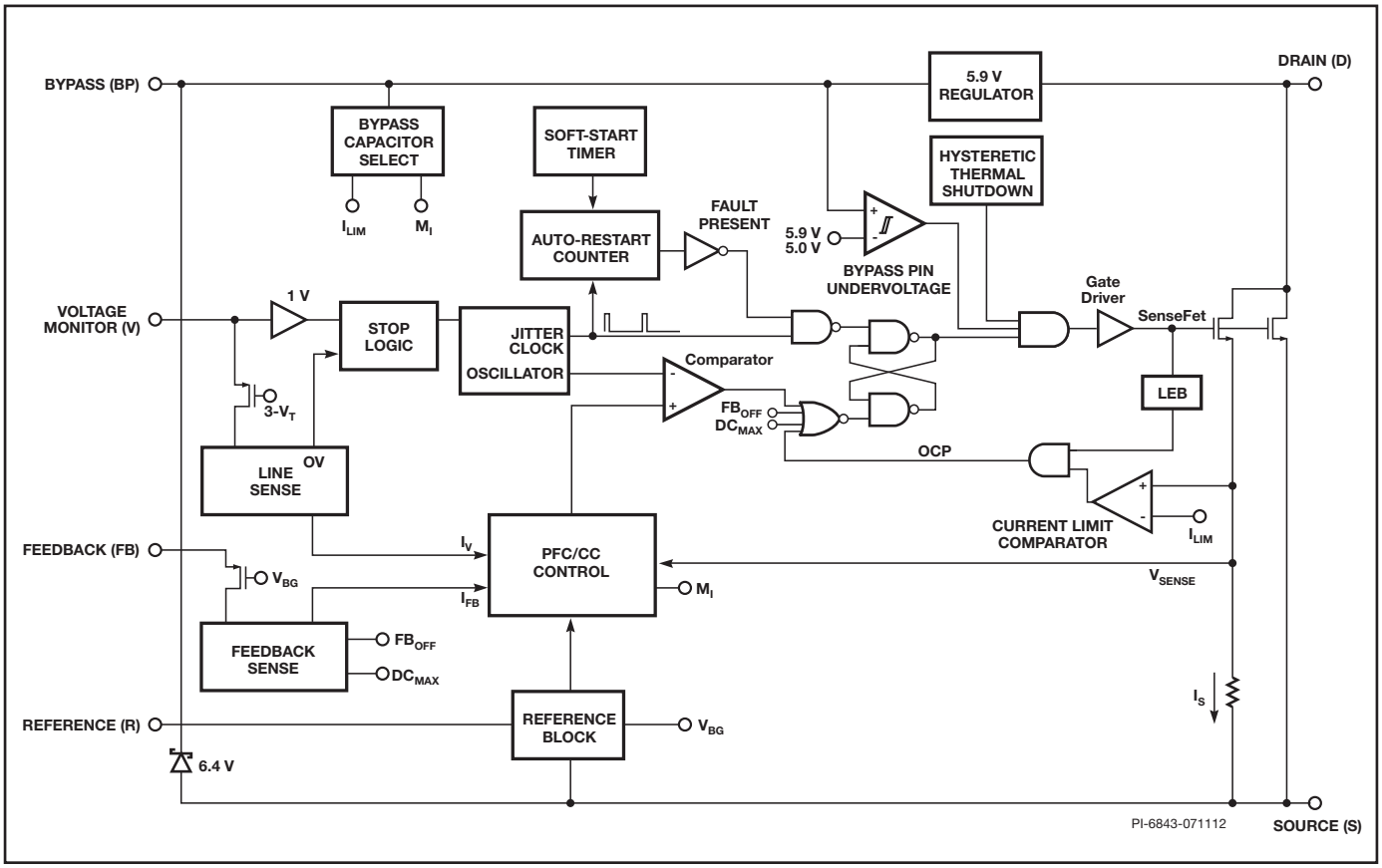


Figure 4. Functional Block Diagram.

Pin Functional Description

DRAIN (D) Pin:
This pin is the power FET drain connection. It also provides internal operating current for both start-up and steady-state operation.

SOURCE (S) Pin:
This pin is the power FET source connection. It is also the ground reference for the BYPASS, FEEDBACK, REFERENCE and VOLTAGE MONITOR pins.

BYPASS (BP) Pin:
This is the connection point for an external bypass capacitor for the internally generated 5.9 V supply. This pin also provides output power selection through choice of the BYPASS pin capacitor value.

FEEDBACK (FB) Pin:
The FEEDBACK pin is used for output voltage feedback. The current into the FEEDBACK pin is directly proportional to the output voltage. The FEEDBACK pin also includes circuitry to protect against open load and overload output conditions.

REFERENCE (R) Pin:
This pin is connected to an external precision resistor and is used to configure for dimming (LYT4311-4318) and non-TRIAC dimming (LYT4211-4218) modes of operation.

VOLTAGE MONITOR (V) Pin:
This pin interfaces with an external input line peak detector, consisting of a rectifier, filter capacitor and resistors. The applied current is used to control stop logic for overvoltage (OV), provide feed-forward to control the output current and the remote ON/OFF function.

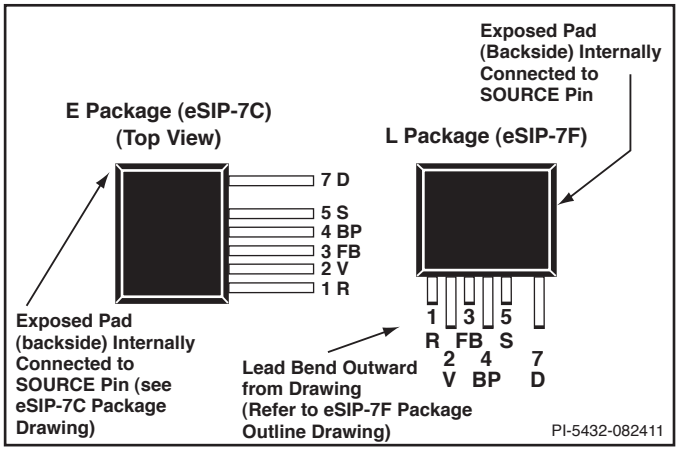


Figure 5. Pin Configuration.

Functional Description

A LYTSwitch device monolithically combines a controller and high-voltage power FET into one package. The controller provides both high power factor and constant current output in a single-stage. The LYTSwitch controller consists of an oscillator, feedback (sense and logic) circuit, 5.9 V regulator, hysteretic over-temperature protection, frequency jittering, cycle-by-cycle current limit, auto-restart, inductance correction, power factor and constant current control.

FEEDBACK Pin Current Control Characteristics

The figure shown below illustrates the operating boundaries of the FEEDBACK pin current. Above $I_{FB(SKIP)}$ switching is disabled and below $I_{FB(AR)}$ the device enters into auto-restart.

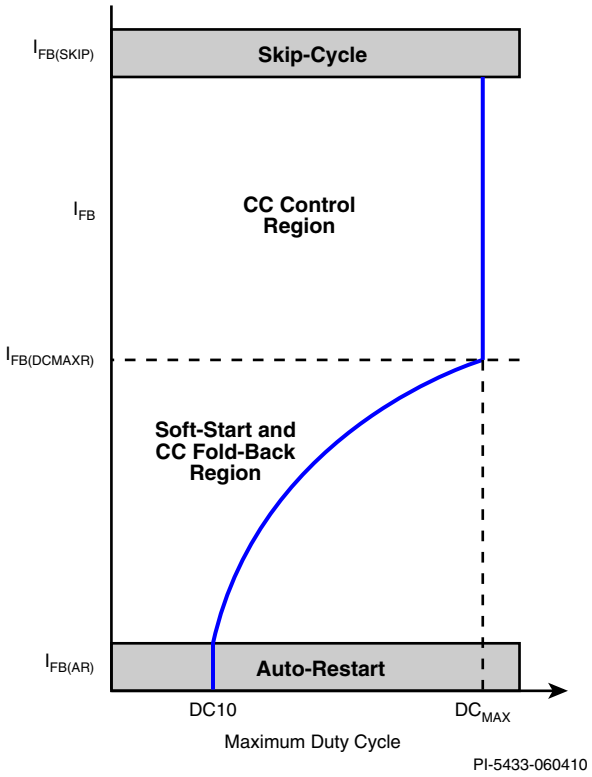


Figure 6. FEEDBACK Pin Current Characteristic.

The FEEDBACK pin current is also used to clamp the maximum duty cycle to limit the available output power for overload and open-loop conditions. This duty cycle reduction characteristic also promotes a monotonic output current start-up characteristic and helps preventing over-shoot.

REFERENCE Pin

The REFERENCE pin is tied to ground (SOURCE) via an external resistor. The value selected sets the internal references, determining the operating mode for dimming (LYT4311-4318) and non-dimming (LYT4211-4218) operation and the line overvoltage thresholds of the VOLTAGE MONITOR pin. For non-dimming or PWM dimming applications with LYT4211-4218, the external resistor should be a 24.9 kΩ ±1%. For phase angle AC dimming with LYT4311-4318, the external resistor should be a 49.9 kΩ ±1%. One percent resistors are recommended as the resistor tolerance directly affects the output tolerance. Other resistor values should not be used.

BYPASS Pin Capacitor Power Gain Selection

LYTSwitch devices have the capability to tailor the internal gain to either full or a reduced output power setting. This allows selection of a larger device to minimize dissipation for both thermal and efficiency reasons. The power gain is selected with the value of the BYPASS pin capacitor. The full power setting is selected with a 4.7 µF capacitor and the reduced power setting (for higher efficiency) is selected with a 47 µF capacitor. The BYPASS pin capacitor sets both the internal power gain as well as the over-current protection (OCP) threshold. Unlike the larger devices, the LYT4x11 power gain is not programmable. Use a 47 µF capacitor for the LYT4x11.

Switching Frequency

The switching frequency is 132 kHz during normal operation. To further reduce the EMI level, the switching frequency is jittered (frequency modulated) by approximately 2.6 kHz. During start-up the frequency is 66 kHz to reduce start-up time when the AC input is phase angle dimmed. Jitter is disabled in deep dimming.

Soft-Start

The controller includes a soft-start timing feature which inhibits the auto-restart protection feature for the soft-start period (t_{SOFT}) to distinguish start-up into a fault (short-circuit) from a large output capacitor. At start-up the LYTSwitch clamps the maximum duty cycle to reduce the output power. The total soft-start period is t_{SOFT}.

Remote ON/OFF and EcoSmart™

The VOLTAGE MONITOR pin has a 1 V threshold comparator connected at its input. This voltage threshold is used for remote ON/OFF control. When a signal is received at the VOLTAGE MONITOR pin to disable the output (VOLTAGE MONITOR pin tied to ground through an optocoupler photo-transistor) the LYTSwitch will complete its current switching cycle before the internal power FET is forced off.

The remote ON/OFF feature can also be used as an eco-mode or power switch to turn off the LYTSwitch and keep it in a very low power consumption state for indefinite long periods. When the LYTSwitch is remotely turned on after entering this mode, it will initiate a normal start-up sequence with soft-start the next time the BYPASS pin reaches 5.9 V. In the worst case, the delay from remote on to start-up can be equal to the full discharge/charge cycle time of the BYPASS pin. This reduced consumption remote off mode can eliminate expensive and unreliable in-line mechanical switches.

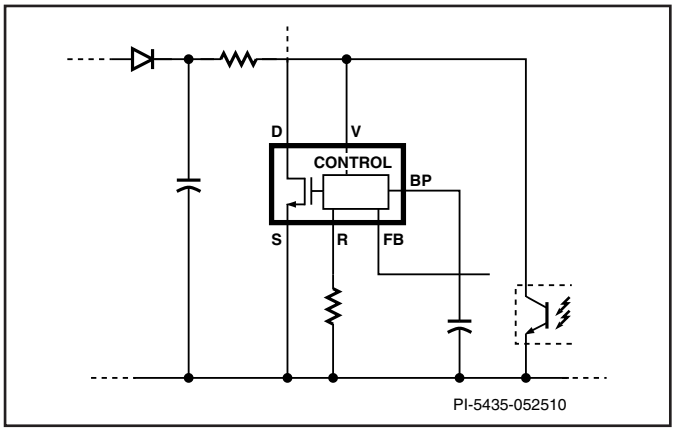


Figure 7. Remote ON/OFF VOLTAGE MONITOR Pin Control.

5.9 V Regulator/Shunt Voltage Clamp

The internal 5.9 V regulator charges the bypass capacitor connected to the BYPASS pin to 5.9 V by drawing a current from the voltage on the DRAIN pin whenever the power FET is off. The BYPASS pin is the internal supply voltage node. When the power FET is on, the device operates from the energy stored in the bypass capacitor. Extremely low power consumption of the internal circuitry allows LYTSwitch to operate continuously from current it takes from the DRAIN pin. A bypass capacitor value of 47 or 4.7 μF is sufficient for both high frequency decoupling and energy storage. In addition, there is a 6.4 V shunt regulator clamping the BYPASS pin at 6.4 V when current is provided to the BYPASS pin through an external resistor. This facilitates powering of LYTSwitch externally through a bias winding to increase operating efficiency. It is recommended that the BYPASS pin is supplied current from the bias winding for normal operation.

Auto-Restart

In the event of an open-loop fault (open FEEDBACK pin resistor or broken path to feedback winding), output short-circuits or an overload condition the controller enters into the auto-restart mode. The controller annunciates both short-circuit and open-loop conditions once the FEEDBACK pin current falls below the $I_{FB(AR)}$ threshold after the soft-start period. To minimize the power dissipation under this fault condition the shutdown/auto-restart circuit turns the power supply on (same as the soft-start period) and off at an auto-restart duty cycle of typically DC_{AR} for as long as the fault condition persists. If the fault is removed during the auto-restart off-time, the power supply will remain in auto-restart until the full off-time count is completed. Special consideration must be made to appropriately size the output capacitor to ensure that after the soft-start period (t_{SOFT}) the FEEDBACK pin current is above the $I_{FB(AR)}$ threshold to ensure successful power-supply start-up. After the soft-start time period, auto-restart is activated only when the FEEDBACK pin current falls below $I_{FB(AR)}$.

Over-Current Protection

The current limit circuit senses the current in the power FET. When this current exceeds the internal threshold (I_{LIMIT}), the power FET is turned off for the remainder of that cycle. A leading edge blanking circuit inhibits the current limit comparator for a short time (t_{LEB}) after the power FET is turned on. This leading edge blanking time has been set so that current spikes caused by capacitance and rectifier reverse recovery will not cause premature termination of the power FET conduction.

Line Overvoltage Protection

This device includes overvoltage detection to limit the maximum operating voltage detected through the VOLTAGE MONITOR pin. An external peak detector consisting of a diode and capacitor is required to provide input line peak voltage to the VOLTAGE MONITOR pin through a resistor.

The resistor sets line overvoltage (OV) shutdown threshold which, once exceeded, forces the LYTSwitch to stop switching. Once the line voltage returns to normal, the device resumes normal operation. A small amount of hysteresis is provided on the OV threshold to prevent noise-generated toggling. When the power FET is off, the rectified DC high voltage surge capability is increased to the voltage rating of the power FET (670 V), due to the absence of the reflected voltage and leakage spikes on the drain.

Hysteretic Thermal Shutdown

The thermal shutdown circuitry senses the controller die temperature. The threshold is set at 142 °C typical with a 75 °C hysteresis. When the die temperature rises above this threshold (142 °C) the power FET is disabled and remains disabled until the die temperature falls by 75 °C, at which point the power FET is re-enabled.

Safe Operating Area (SOA) Protection

The device also features a safe operating area (SOA) protection mode which disables FET switching for 40 cycles in the event the peak switch current reaches the I_{LIMIT} threshold and the switch on-time is less than $t_{ON(SOA)}$. This protection mode protects the device under short-circuited LED conditions and at start-up during the soft-start period when auto-restart protection is inhibited. The SOA protection mode remains active in normal operation.

Application Example

25 W TRIAC Dimmable High Power Factor LED Driver Design Example (DER-350)

The circuit schematic in Figure 8 shows a TRIAC dimmable high power factor LED driver based on LYT4317E from the LYTSwitch family of devices. The design is configurable for non-dimmable only applications by simple component value changes. It was optimized to drive an LED string at a voltage of 36 V with a constant current of 0.7 A ideal for Lumens PAR lamp retro-fit applications. The design operates over an input voltage range of 90 VAC to 132 VAC.

The key goals of this design were compatibility with standard leading edge TRIAC AC dimmers, very wide dimming range (1000:1, 700 mA:0.7 mA), high efficiency (>85%) and high power factor (>0.9). The design is fully protected from faults such as no-load (open load), overvoltage and output short-circuit or overload conditions and over temperature.

Circuit Description

The LYTSwitch device (U1- LYT4317E) integrates the power FET, controller and start-up functions into a single package reducing the component count versus typical implementations. Configured as part of an isolated continuous conduction mode flyback converter, U1 provides high power factor via its internal control algorithm together with the small input capacitance of the design. Continuous conduction mode operation results in reduced primary peak and RMS current. This both reduces EMI noise, allowing simpler, smaller EMI filtering components and improves efficiency. Output current regulation is maintained without the need for secondary-side sensing which eliminates current sense resistors and improves efficiency.

Input Stage

Fuse F1 provides protection from component failures while RV1 provides a clamp during differential line surges, keeping the peak drain voltage of U1 below the 725 V rating of the internal power FET. Bridge rectifier BR1 rectifies the AC line voltage. EMI filtering is provided by L1-L3, C1, C4, R2, R24 and R25 together with the safety rated Y class capacitor (CY1) that bridges the safety isolation barrier between primary and secondary. Resistor R2, R24 and R25 act to damp any resonances formed between L1, L2, L3, C1 and the AC line impedance. A small bulk capacitor (C4) is required to provide a low impedance source for the primary switching current. The maximum value of C2 and C4 is limited in order to maintain a power factor of greater than 0.9.

LYTSwitch Primary

To provide peak line voltage information to U1 the incoming rectified AC peak charges C6 via D2. This is then fed into the VOLTAGE MONITOR pin of U1 as a current via R10. This sensed current is also used by the device to set the line input overvoltage protection threshold. Resistor R9 provides a discharge path for C6 with a time constant much longer than that of the rectified AC to prevent generation of line frequency ripple.

The VOLTAGE MONITOR pin current and the FEEDBACK pin current are used internally to control the average output LED current. For TRIAC phase-dimming applications a 49.9 kΩ resistor (R14) is used on the REFERENCE pin and 2 MΩ (R10) on the VOLTAGE MONITOR pin to provide a linear relationship between input voltage and the output current and maximizing the dimming range.

Diode D3, R15 and C7 clamp the drain voltage to a safe level due to the effects of leakage inductance. Diode D4 is necessary to prevent reverse current from flowing through U1 for the period of the rectified AC input voltage that the voltage across C4 falls to below the reflected output voltage (V_{OR}).

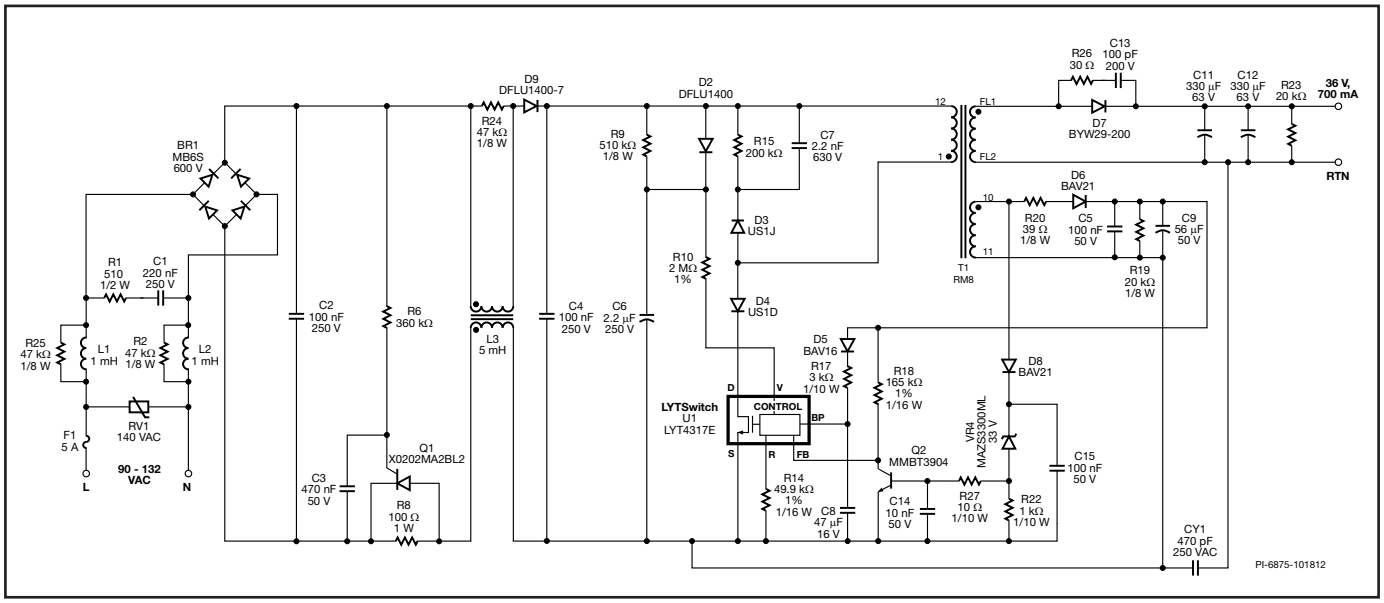


Figure 8. DER-350 Schematic of an Isolated, TRIAC Dimmable, High Power Factor, 90-132 VAC, 25 W / 36 V / 700 mA LED Driver.

Diode D6, C5, C9, R19 and R20 create the primary bias supply from an auxiliary winding on the transformer. Capacitor C8 provides local decoupling for the BYPASS pin of U1 which is the supply pin for the internal controller. During start-up C8 is charged to ~6 V from an internal high-voltage current source tied to the device DRAIN pin. This allows the part to start switching at which point the operating supply current is provided from the bias supply via R17. Capacitor C8 also selects the output power mode (47 μF for reduced power was selected to reduce dissipation in U1 and increase efficiency for this design).

Feedback

The bias winding voltage is proportional to the output voltage (set by the turns ratio between the bias and secondary windings). This allows the output voltage to be monitored without secondary-side feedback components. Resistor R18 converts the bias voltage into a current which is fed into the FEEDBACK pin of U1. The internal engine within U1 combines the FEEDBACK pin current, the VOLTAGE MONITOR pin current and drain current information to provide a constant output current over a 1.5:1 output voltage variation (LED string voltage variation of ±25%) at a fixed line input voltage.

To limit the output voltage at no-load an output overvoltage protection circuit is set by D8, C15, R22, VR4, R27, C14 and Q2. Should the output load be disconnected then the bias voltage will increase until VR4 conducts, turning on Q2 and reducing the current into the FEEDBACK pin. When this current drops below 10 μA the part enters auto-restart and switching is disabled for 300 ms allowing time for the output and bias voltages to fall.

Output Rectification

The transformer secondary winding is rectified by D7 and filtered by C11 and C12. An ultrafast TO-220 diode was selected for efficiency and the combined value of C11 and C12 were selected to give peak-to-peak LED ripple current equal to 30% of the mean value. For designs where lower ripple is desirable the output capacitance value can be increased.

A small pre-load is provided by R23 which discharges residual charge in output capacitors when turned off.

TRIAC Phase Dimming Control Compatibility

The requirement to provide output dimming with low-cost, TRIAC-based, leading edge phase dimmers introduces a number of trade-offs in the design.

Due to the much lower power consumed by LED based lighting the current drawn by the overall lamp is below the holding current of the TRIAC within the dimmer. This can cause undesirable behaviors such as limited dimming range and/or flickering as the TRIAC fires inconsistently. The relatively large impedance the LED lamp presents to the line allows significant ringing to occur due to the inrush current charging the input capacitance when the TRIAC turns on. This too can cause similar undesirable behavior as the ringing may cause the TRIAC current to fall to zero and turn off.

To overcome these issues simple two circuits, the SCR active damper and R-C passive bleeder, are incorporated. The drawback of these circuits is increased dissipation and therefore reduced efficiency of the supply. For non-dimming applications these components can simply be omitted.

The SCR active damper consists of components R6, C3, and Q1 in conjunction with R8. This circuit limits the inrush current that flows to charge C4 when the TRIAC turns on by placing R8 in series for the first ~1 ms of the TRIAC conduction. After approximately 1 ms, Q1 turns on and bypasses R8. This keeps the power dissipation on R8 low and allows a larger value during current limiting. Resistor R6 and C3 provide the delay on Q1 turn on after the TRIAC conducts. Diode D9 blocks the charge in capacitor C4 from flowing back after the TRIAC turns on which helps in dimming compatibility especially with high power dimmers.

The passive bleeder circuit is comprised of R1 and C1. This helps keep the input current above the TRIAC holding current while the input current corresponding to the effective driver resistance increases during each AC half-cycle.

Modified DER-350 25 W High Power Factor LED Driver for Non-Dimmable and Enhanced Line Regulation

The circuit schematic in Figure 9 shows a high power factor LED driver based on a LYT4317 from the LYTSwitch family of devices. It was optimized to drive an LED string at a voltage of 36 V with a constant current of 0.7 A, ideal for high lumen PAR lamp retro-fit applications. The design operates over the low-line input voltage range of 90 VAC to 132 VAC and is non-dimming application. A non-dimming application has tighter output current variation with changes in the line voltage than a dimming application. It's key to note that, although not specified for dimming, no circuit damage will result if the end user does operate the design with a phase controlled dimmer.

Modification for Non-Dimmable Configuration

The design is configurable for non-dimmable application by simply removing the component for SCR active damper (R6, R8, C3, and Q1), blocking diode D9 and R-C bleeder (R1, C1) changes and replacing the reference resistor R14 with 24.9 kΩ. (See Figure 9)

Key Application Considerations

Power Table

The data sheet power table (Table 1) represents the minimum and maximum practical continuous output power based on the following conditions:

- Efficiency of 80%
- Device local ambient of 70 °C
- Sufficient heat sinking to keep the device temperature below 100 °C
- For minimum output power column
  - Reflected output voltage (V_{OR}) of 120 V
  - FEEDBACK pin current of 135 µA
  - BYPASS pin capacitor value of 47 µF
- For maximum output power column
  - Reflected output voltage (V_{OR}) of 65 V
  - FEEDBACK pin current of 165 µA
  - BYPASS pin capacitor value of 4.7 µF (LYT4x11 = 4.7 µF)

Note that input line voltages above 85 VAC do not change the power delivery capability of LYTSwitch devices.

Device Selection

Select the device size by comparing the required output power to the values in Table 1. For thermally challenging designs, e.g., incandescent lamp replacement, where either the ambient temperature local to the LYTSwitch device is high and/or there is minimal space for heat sinking use the minimum output power column. This is selected by using a 47 µF BYPASS pin capacitor and results in a lower device current limit and therefore lower conduction losses. For open frame design or designs where space is available for heat sinking then refer to the maximum output power column. This is selected by using a 4.7 µF BYPASS pin capacitor for all but the LYT4x11 which has only one power setting. In all cases in order to obtain the best output current tolerance maintain the device temperature below 100 °C

Maximum Input Capacitance

To achieve high power factor, the capacitance used in both the EMI filter and for decoupling the rectified AC (bulk capacitor) must be limited in value. The maximum value is a function of the output power of the design and reduces as the output power reduces. For the majority of designs limit the total capacitance to less than 200 nF with a bulk capacitor value of 100 nF. Film capacitors are recommended compared to ceramic types as they minimize audible noise with operating with leading edge phase dimmers. Start with a value of 10 nF for the capacitance in the EMI filter and increase in value until there is sufficient EMI margin.

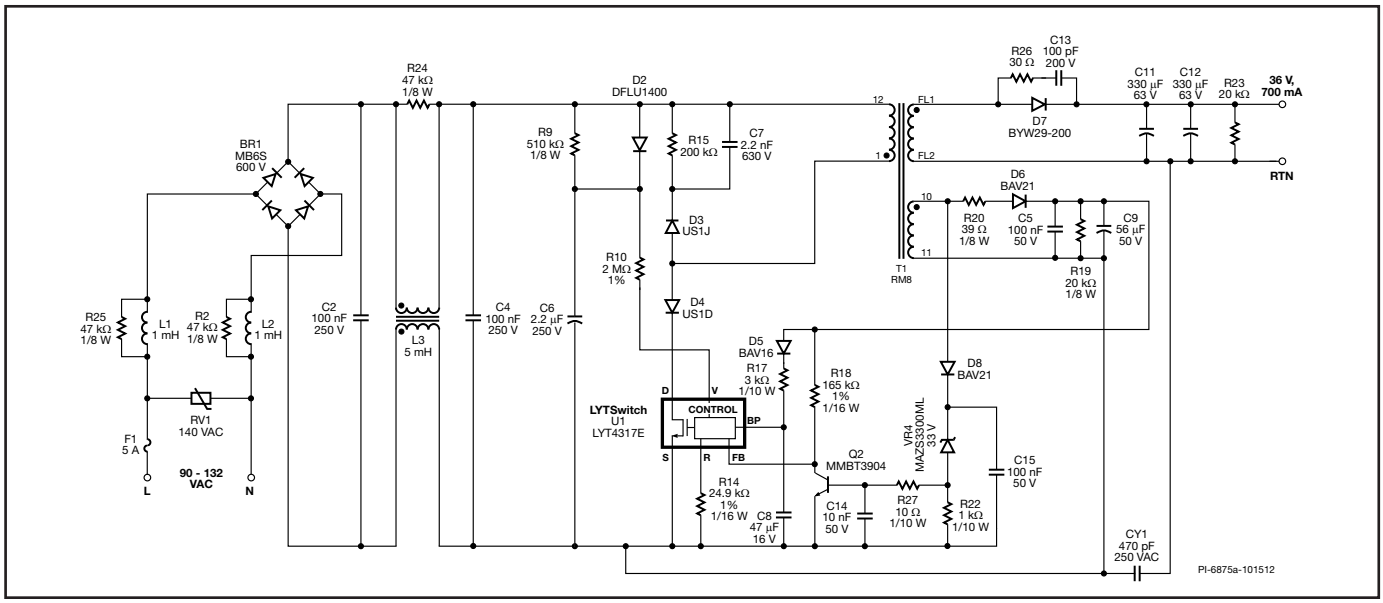


Figure 9. Modified Schematic of RD-350 for Non-Dimmable, Isolated, High Power Factor, 90-132 VAC, 25 W / 36 V LED Driver.

REFERENCE Pin Resistance Value Selection

The LYTSwitch family contains phase dimming devices, LYT4311-4318, and non-dimming devices, LYT4211-4218. The non-dimmable devices use a 24.9 kΩ ±1% REFERENCE pin resistor for best output current tolerance (over AC input voltage changes). The dimmable devices (i.e. LYT4311-4318) use 49.9 kΩ ±1% to achieve the widest dimming range.

VOLTAGE MONITOR Pin Resistance Network Selection

For widest AC phase angle dimming range with LYT4311-4318, use a 2 MΩ (1.7 MΩ for 100 VAC (Japan)) resistor connected to the line voltage peak detector circuit. Make sure that the resistor's voltage rating is sufficient for the peak line voltage. If necessary use multiple series connected resistors.

Primary Clamp and Output Reflected Voltage V_{OR}

A primary clamp is necessary to limit the peak drain to source voltage. A Zener clamp requires the fewest components and board space and gives the highest efficiency. RCD clamps are also acceptable however the peak drain voltage should be carefully verified during start-up and output short-circuits as the clamping voltage varies with significantly with the peak drain current.

For the highest efficiency, the clamping voltage should be selected to be at least 1.5 times the output reflected voltage, V_{OR}, as this keeps the leakage spike conduction time short. This will ensure efficient operation of the clamp circuit and will also keep the maximum drain voltage below the rated breakdown voltage of the FET. An RCD (or RCDZ) clamp provides tighter clamp voltage tolerance than a Zener clamp. The RCD clamp is more cost effective than the Zener clamp but requires more careful design to ensure that the maximum drain voltage does not exceed the power FET breakdown voltage. These V_{OR} limits are based on the BV_{DSS} rating of the internal FET, a V_{OR} of 60 V to 100 V is typical for most designs, giving the best PFC and regulation performance.

Series Drain Diode

An ultrafast or Schottky diode in series with the drain is necessary to prevent reverse current flowing through the device. The voltage rating must exceed the output reflected voltage, V_{OR}. The current rating should exceed two times the average primary current and have a peak rating equal to the maximum drain current of the selected LYTSwitch device.

Line Voltage Peak Detector Circuit

LYTSwitch devices use the peak line voltage to regulate the power delivery to the output. A capacitor value of 1 µF to 4.7 µF is recommended to minimize line ripple and give the highest power factor (>0.9), smaller values are acceptable but result in lower PF and higher line current distortion.

Operation with Phase Controlled Dimmers

Dimmer switches control incandescent lamp brightness by not conducting (blanking) for a portion of the AC voltage sine wave. This reduces the RMS voltage applied to the lamp thus reducing the brightness. This is called natural dimming and the LYTSwitch LYT4311-4318 devices when configured for dimming utilize natural dimming by reducing the LED current as the RMS line voltage decreases. By this nature, line regulation performance is purposely decreased to increase the dimming range and more closely mimic the operation of an incandescent lamp. Using a 49.9 kΩ REFERENCE pin resistance selects natural dimming mode operation.

Leading Edge Phase Controlled Dimmers

The requirement to provide flicker-free output dimming with low-cost, TRIAC-based, leading edge phase dimmers introduces a number of trade-offs in the design.

Due to the much lower power consumed by LED based lighting the current drawn by the overall lamp is below the holding current of the TRIAC within the dimmer. This causes undesirable behaviors such as limited dimming range and/or flickering. The relatively large impedance the LED lamp presents to the line allows significant ringing to occur due to the inrush current charging the input capacitance when the TRIAC turns on. This too can cause similar undesirable behavior as the ringing may cause the TRIAC current to fall to zero and turn off.

To overcome these issues two circuits, the active damper and passive bleeder, are incorporated. The drawback of these circuits is increased dissipation and therefore reduced efficiency of the supply so for non-dimming applications these components can simply be omitted.

Figure 10a shows the line voltage and current at the input of a leading edge TRIAC dimmer with Figure 10b showing the resultant rectified bus voltage. In this example, the TRIAC conducts at 90 degrees.

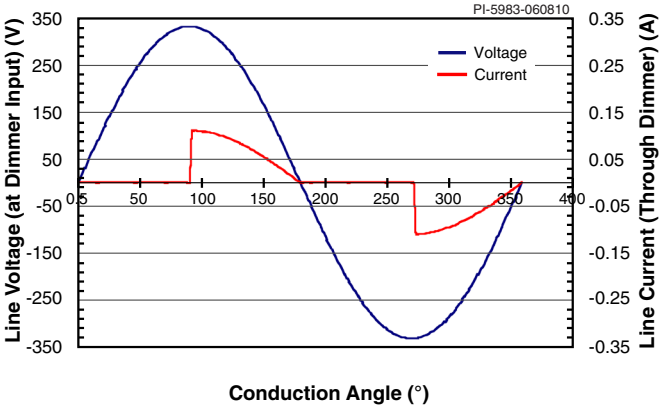


Figure 10a. Ideal Input Voltage and Current Waveform for a Leading Edge TRIAC Dimmer at 90°.

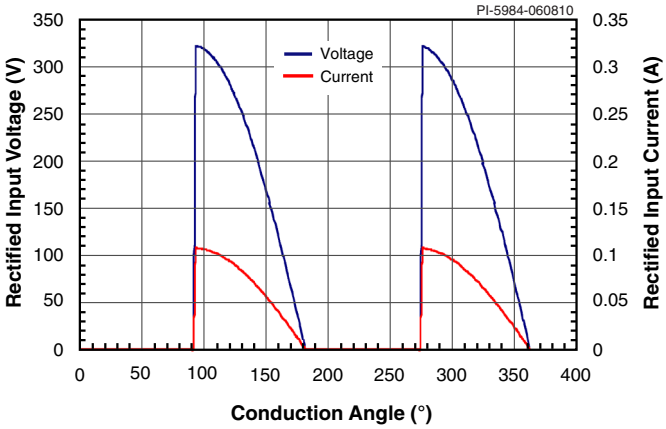


Figure 10b. Resultant Waveforms Following Rectification of TRIAC Dimmer Output.

Figure 11 shows undesired rectified bus voltage and current with the TRIAC turning off prematurely and restarting.

If the TRIAC is turning off before the end of the half-cycle erratically or alternate half AC cycles have different conduction angles then flicker will be observed in the LED light due to variations in the output current. This can be solved by including a bleeder and damper circuit.

Dimmers will behave differently based on manufacturer and power rating, for example a 300 W dimmer requires less dampening and requires less power loss in the bleeder than a 600 W or 1000 W dimmer due to different drive circuits and TRIAC holding current specifications. Multiple lamps in parallel driven from the same dimmer can introduce more ringing due to the increased capacitance of parallel units. Therefore, when testing dimmer operation verify on a number of models, different line voltages and with both a single driver and multiple drivers in parallel.

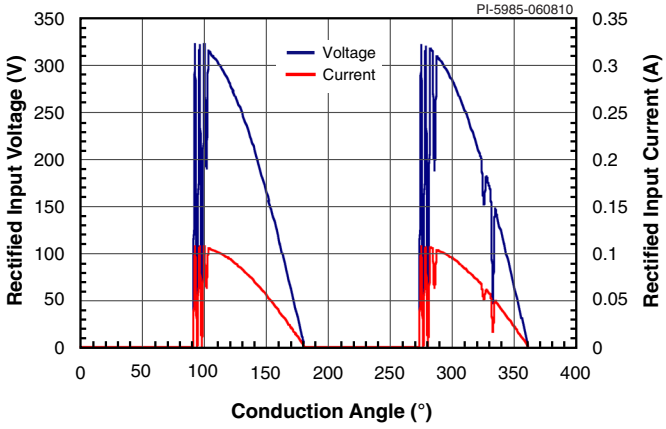


Figure 11. Example of Phase Angle Dimmer Showing Erratic Firing.

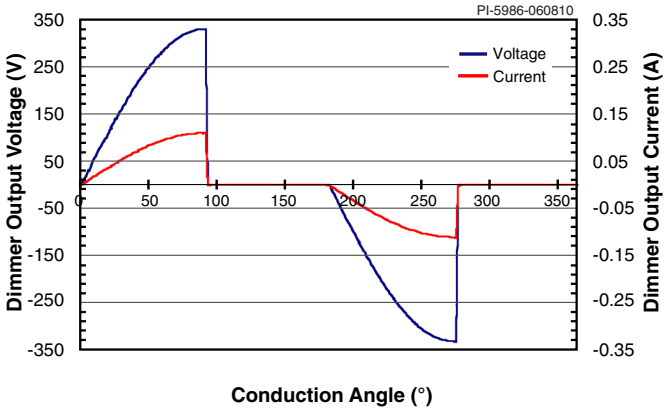


Figure 12. Ideal Dimmer Output Voltage and Current Waveforms for a Trailing Edge Dimmer at 90° Conduction Angle.

Start by adding a bleeder circuit. Add a 0.44 µF capacitor and 510 Ω 1 W resistor (components in series) across the rectified bus (C1 and R1 in Figure 8). If the results in satisfactory operation reduce the capacitor value to the smallest that result in acceptable performance to reduce losses and increase efficiency.

If the bleeder circuit does not maintain conduction in the TRIAC, then add an active damper as shown in Figure 12. This consists of components R6, C3, and Q1 in conjunction with R8. This circuit limits the inrush current that flows to charge C4 when the TRIAC turns on by placing R8 in series for the first 1 ms of the TRIAC conduction. After approximately 1 ms, Q1 turns on and shorts R8. This keeps the power dissipation on R8 low and allows a larger value to be used during current limiting. Increasing the delay before Q1 turns on by increasing the value of resistor R6 will improve dimmer compatibility but cause more power to be dissipated across R8. Monitor the AC line current and voltage at the input of the power supply as you make the adjustments. Increase the delay until the TRIAC operates properly but keep the delay as short as possible for efficiency.

As a general rule the greater the power dissipated in the bleeder and damper circuits, the more types of dimmers will work with the driver.

Trailing Edge Phase Controlled Dimmers

Figure 11 shows the line voltage and current at the input of the power supply with a trailing edge dimmer. In this example, the dimmer conducts at 90 degrees. Many of these dimmers use back-to-back connected power FETs rather than a TRIAC to control the load. This eliminates the holding current issue of TRIACs and since the conduction begins at the zero crossing, high current surges and line ringing are minimized. Typically these types of dimmers do not require damping and bleeder circuits.

Audible Noise Considerations for Use with Leading Edge Dimmers

Noise created when dimming is typically created by the input capacitors, EMI filter inductors and the transformer. The input capacitors and inductors experience high di/dt and dv/dt every AC half-cycle as the TRIAC fires and an inrush current flows to charge the input capacitance. Noise can be minimized by selecting film vs. ceramic capacitors, minimizing the capacitor value and selecting inductors that are physically short and wide.

The transformer may also create noise which can be minimized by avoiding cores with long narrow legs (high mechanical resonant frequency). For example, RM cores produce less audible noise than EE cores for the same flux density. Reducing the core flux density will also reduce the noise. Reducing the maximum flux density (BM) to 1500 Gauss usually eliminates any audible noise but must be balanced with the increased core size needed for a given output power.

Thermal and Lifetime Considerations

Lighting applications present thermal challenges to the driver. In many cases the LED load dissipation determines the working ambient temperature experienced by the drive so thermal evaluation should be performed with the driver inside the final enclosure. Temperature has a direct impact on driver and LED lifetime. For every 10 °C rise in temperature, component life is reduced by a factor of 2. Therefore it is important to properly heat sink and to verify the operating temperatures of all devices.

Layout Considerations

Primary-Side Connections

Use a single point (Kelvin) connection at the negative terminal of the input filter capacitor for the SOURCE pin and bias returns. This improves surge capabilities by returning surge currents from the bias winding directly to the input filter capacitor. The BYPASS pin capacitor should be located as close to the BYPASS pin and connected as close to the SOURCE pin as possible. The SOURCE pin trace should not be shared with the main power FET switching currents. All FEEDBACK pin components that connect to the SOURCE pin should follow the same rules as the BYPASS pin capacitor. It is critical that the main power FET switching currents return to the bulk capacitor with the shortest path as possible. Long high current paths create excessive conducted and radiated noise.

Secondary-Side Connections

The output rectifier and output filter capacitor should be as close as possible. The transformer's output return pin should have a short trace to the return side of the output filter capacitor.

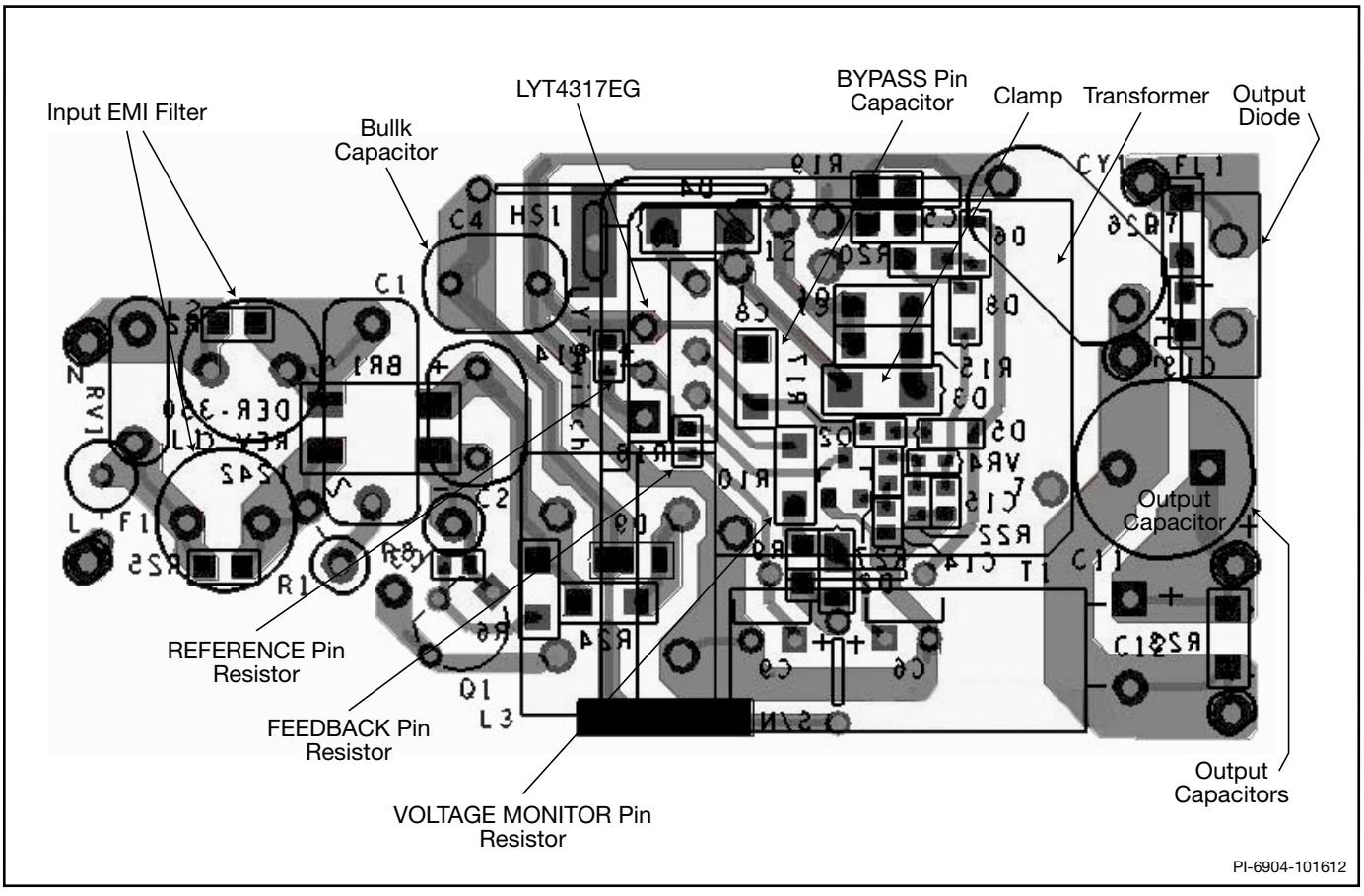


Figure 13. DER-350 25 W Layout Example, Top Silk / Bottom Layer.

Quick Design Checklist

Maximum Drain Voltage
Verify that the peak V_{DS} does not exceed 670 V under all operating conditions including start-up and fault conditions.

Maximum Drain Current
Measure the peak drain current under all operation conditions including start-up and fault conditions. Look for signs of transformer saturation (usually occurs at highest operating ambient temperatures). Verify that the peak current is less than the stated Absolute Maximum Rating in the data sheet.

Thermal Check
At maximum output power, both minimum and maximum line voltage and ambient temperature; verify that temperature specifications are not exceeded for the LYTSwitch, transformer, output diodes, output capacitors and drain clamp components.

Absolute Maximum Ratings[1,4]

DRAIN Pin Peak Current[5]: LYT4x11 ..... 1.37 A
LYT4x12 ..... 2.08 A
LYT4x13 ..... 2.72 A
LYT4x14 ..... 4.08 A
LYT4x15 ..... 5.44 A
LYT4x16 ..... 6.88 A
LYT4x17 ..... 7.73 A
LYT4x18 ..... 9.00 A
DRAIN Pin Voltage ..... -0.3 to 670 V
BYPASS Pin Voltage ..... -0.3 to 9 V
BYPASS Pin Current ..... 100 mA
VOLTAGE MONITOR Pin Voltage..... -0.3 to 9 V
FEEDBACK Pin Voltage ..... -0.3 to 9 V
REFERENCE Pin Voltage ..... -0.3 to 9 V
Lead Temperature[3] .....260 °C
Storage Temperature ..... -65 to 150 °C
Operating Junction Temperature[2]..... -40 to 150 °C

Notes:
1. All voltages referenced to SOURCE, T_A = 65 °C.
2. Normally limited by internal circuitry.
3. 1/16 in. from case for 5 seconds.
4. Absolute Maximum Ratings specified may be applied, one at a time without causing permanent damage to the product. Exposure to Absolute Maximum Ratings for extended periods of time may affect product reliability.
5. Peak DRAIN current is allowed while the DRAIN voltage is simultaneously less than 400 V. See also Figure 13.

Thermal Resistance

Thermal Resistance: E or L Package
(θ_{JA}) .....105 °C/W[1]
(θ_{JC})..... 2 °C/W[2]

Notes:
1. Free standing with no heat sink.
2. Measured at back surface tab.

Parameter	Symbol	Conditions SOURCE = 0 V; T_J = -20 °C to 125 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Control Functions							
Switching Frequency	f_{OSC}	T_J = 65 °C	Average	124	132	140	kHz
			Peak-Peak Jitter		5.4		
Frequency Jitter Modulation Rate	f_M	T_J = 65 °C See Note B			2.6		kHz
BYPASS Pin Charge Current	I_{CH1}	V_{BP} = 0 V, T_J = 65 °C	LYT4x11	-4.1	-3.4	-2.7	mA
			LYT4x12	-7.3	-6.1	-4.9	
			LYT4x13-4x17	-12	-9.5	-7.0	
			LYT4x18	-13.3	-10.8	-8.3	
	I_{CH2}	V_{BP} = 5 V, T_J = 65 °C	LYT4x11	-0.81	-0.62	-0.43	
			LYT4x12	-3.1	-2.4	-1.7	
			LYT4x13-4x17	-5.6	-4.35	-3.1	
			LYT4x18	-6.75	-5.5	-4.25	
Charging Current Temperature Drift		See Note A, B			0.7		%/°C
BYPASS Pin Voltage	V_{BP}	0 °C < T_J < 100 °C		5.75	5.95	6.15	V
BYPASS Pin Voltage Hysteresis	$V_{BP(H)}$	0 °C < T_J < 100 °C			0.85		V
BYPASS Pin Shunt Voltage	$V_{BP(SHUNT)}$	I_{BP} = 4 mA 0 °C < T_J < 100 °C		6.1	6.4	6.6	V
Soft-Start Time	t_{SOFT}	T_J = 65 °C V_{BP} = 5.9 V		55	76		ms

Parameter	Symbol	Conditions SOURCE = 0 V; T_J = -20 °C to 125 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Control Functions (cont.)							
Drain Supply Current	I_{CD2}	0 °C < T_J < 100 °C FET Not Switching		0.5	0.8	1.2	mA
	I_{CD1}	0 °C < T_J < 100 °C FET Switching at f_{OSC}		1	2.5	4	
VOLTAGE MONITOR Pin							
Line Overvoltage Threshold	I_{OV}	T_J = 65 °C R_R = 24.9 kΩ R_R = 49.9 kΩ	Threshold	115	123	131	µA
			Hysteresis		6		
VOLTAGE MONITOR Pin Voltage	V_V	0 °C < T_J < 100 °C I_V < I_{OV}		2.75	3.0	3.25	V
VOLTAGE MONITOR Pin Short-Circuit Current	$I_{V(SC)}$	V_V = 5 V T_J = 65 °C		165	185	205	µA
Remote ON/OFF Threshold	$V_{V(REM)}$	T_J = 65 °C		0.5			V
FEEDBACK Pin							
FEEDBACK Pin Current at Onset of Maximum Duty Cycle	$I_{FB(DCMAXR)}$	0 °C < T_J < 100 °C				90	µA
FEEDBACK Pin Current Skip Cycle Threshold	$I_{FB(SKIP)}$	0 °C < T_J < 100 °C		220			µA
Maximum Duty Cycle	DC_{MAX}	$I_{FB(DCMAXR)}$ < I_{FB} < $I_{FB(SKIP)}$ 0 °C < T_J < 100 °C		90		99.9	%
FEEDBACK Pin Voltage	V_{FB}	I_{FB} = 150 µA 0 °C < T_J < 100 °C		2.1	2.3	2.56	V
FEEDBACK Pin Short-Circuit Current	$I_{FB(SC)}$	V_{FB} = 5 V T_J = 65 °C		320	400	480	µA
Duty Cycle Reduction	DC10	I_{FB} = $I_{FB(AR)}$, T_J = 65 °C, See Note B		17			%
	DC40	I_{FB} = 40 µA, T_J = 65 °C			34		
	DC60	I_{FB} = 60 µA, T_J = 65 °C			55		
Auto-Restart							
Auto-Restart ON-Time	t_{AR}	T_J = 65 °C V_{BP} = 5.9 V		55	76		ms
Auto-Restart Duty Cycle	DC_{AR}	T_J = 65 °C See Note B			25		%
SOA Minimum Switch ON-Time	$t_{ON(SOA)}$	T_J = 65 °C See Note B				1.75	µs
FEEDBACK Pin Current During Auto-Restart	$I_{FB(AR)}$	0 °C < T_J < 100 °C			6.5	10	µA

Parameter	Symbol	Conditions SOURCE = 0 V; T_J = -20 °C to 125 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
REFERENCE Pin							
REFERENCE Pin Voltage	V_R	R_R = 24.9 kΩ 0 °C < T_J < 100 °C		1.223	1.245	1.273	V
REFERENCE Pin Current	I_R			48.69	49.94	51.19	µA
Current Limit/Circuit Protection							
Full Power Current Limit (C_{BP} = 4.7 µF)	$I_{LIMIT(F)}$ T_J = 65 °C	di/dt = 174 mA/µs	LYT4x12	1.00		1.17	A
		di/dt = 174 mA/µs	LYT4x13	1.24		1.44	
		di/dt = 225 mA/µs	LYT4x14	1.46		1.70	
		di/dt = 320 mA/µs	LYT4x15	1.76		2.04	
		di/dt = 350 mA/µs	LYT4x16	2.43		2.83	
		di/dt = 426 mA/µs	LYT4x17	3.26		3.79	
Reduced Power Current Limit (C_{BP} = 47 µF)	$I_{LIMIT(R)}$ T_J = 65 °C	di/dt = 133 mA/µs	LYT4x11	0.74		0.86	A
		di/dt = 195 mA/µs	LYT4x12	0.81		0.95	
		di/dt = 192 mA/µs	LYT4x13	1.00		1.16	
		di/dt = 240 mA/µs	LYT4x14	1.19		1.38	
		di/dt = 335 mA/µs	LYT4x15	1.43		1.66	
		di/dt = 380 mA/µs	LYT4x16	1.76		2.05	
		di/dt = 483 mA/µs	LYT4x17	2.35		2.73	
		di/dt = 930 mA/µs	LYT4x18	4.90		5.70	
Minimum ON-Time Pulse	$t_{LEB} + t_{IL(D)}$	T_J = 65 °C		300	500	700	ns
Leading Edge Blanking Time	t_{LEB}	T_J = 65 °C See Note B		150		500	ns
Current Limit Delay	$t_{IL(D)}$	T_J = 65 °C See Note B			150		ns
Thermal Shutdown Temperature		See Note B		135	142	150	°C
Thermal Shutdown Hysteresis		See Note B			75		°C
BYPASS Pin Power-Up Reset Threshold Voltage	$V_{BP(RESET)}$	0 °C < T_J < 100 °C		2.25	3.30	4.25	V

Parameter	Symbol	Conditions SOURCE = 0 V; T_J = -20 °C to 125 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Output							
ON-State Resistance	$R_{DS(ON)}$	LYT4x11 I_D = 100 mA	T_J = 65 °C		11.5	13.2	Ω
			T_J = 100 °C		13.5	15.5	
		LYT4x12 I_D = 100 mA	T_J = 65 °C		6.9	8.0	
			T_J = 100 °C		8.4	9.7	
		LYT4x13 I_D = 150 mA	T_J = 65 °C		5.3	6.0	
			T_J = 100 °C		6.3	7.3	
		LYT4x14 I_D = 150 mA	T_J = 65 °C		3.4	3.9	
			T_J = 100 °C		3.9	4.5	
		LYT4x15 I_D = 200 mA	T_J = 65 °C		2.5	2.9	
			T_J = 100 °C		3.0	3.4	
		LYT4x16 I_D = 250 mA	T_J = 65 °C		1.9	2.2	
			T_J = 100 °C		2.3	2.7	
		LYT4x17 I_D = 350 mA	T_J = 65 °C		1.7	2.0	
			T_J = 100 °C		2.0	2.4	
		LYT4x18 I_D = 600 mA	T_J = 65 °C		1.3	1.5	
			T_J = 100 °C		1.6	1.8	
OFF-State Drain Leakage Current	I_{DSS}	V_{BP} = 6.4 V, V_{DS} = 560 V, T_J = 100 °C				50	µA
Breakdown Voltage	BV_{DSS}	V_{BP} = 6.4 V, T_J = 65 °C		670			V
Minimum Drain Supply Voltage		T_J < 100 °C		36			V
Rise Time	t_R	Measured in a Typical Flyback See Note B			100		ns
Fall Time	t_F				50		ns

NOTES:

A. For specifications with negative values, a negative temperature coefficient corresponds to an increase in magnitude with increasing temperature and a positive temperature coefficient corresponds to a decrease in magnitude with increasing temperature.

B. Guaranteed by characterization. Not tested in production.

Typical Performance Characteristics

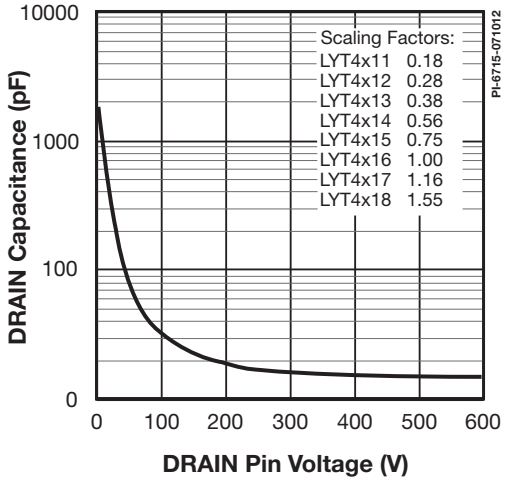


Figure 14. Drain Capacitance vs. Drain Pin Voltage.

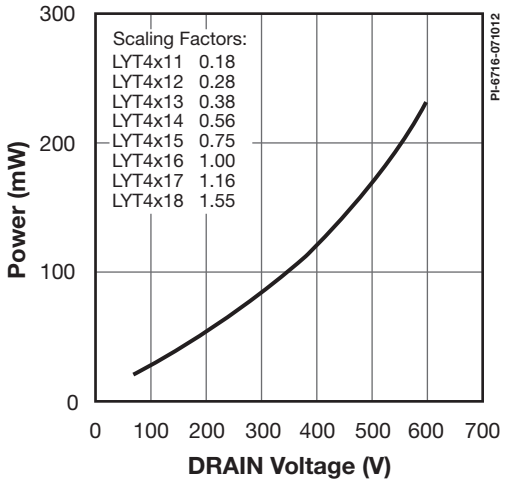


Figure 15. Power vs. Drain Voltage.

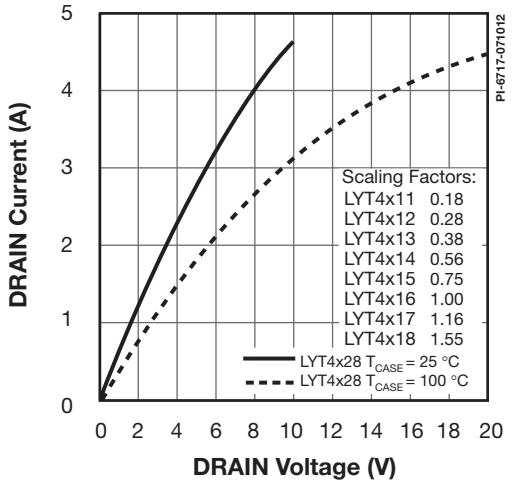


Figure 16. Drain Current vs. Drain Voltage.

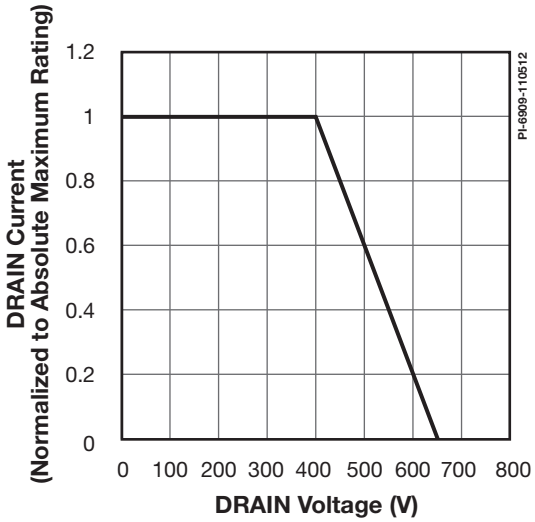
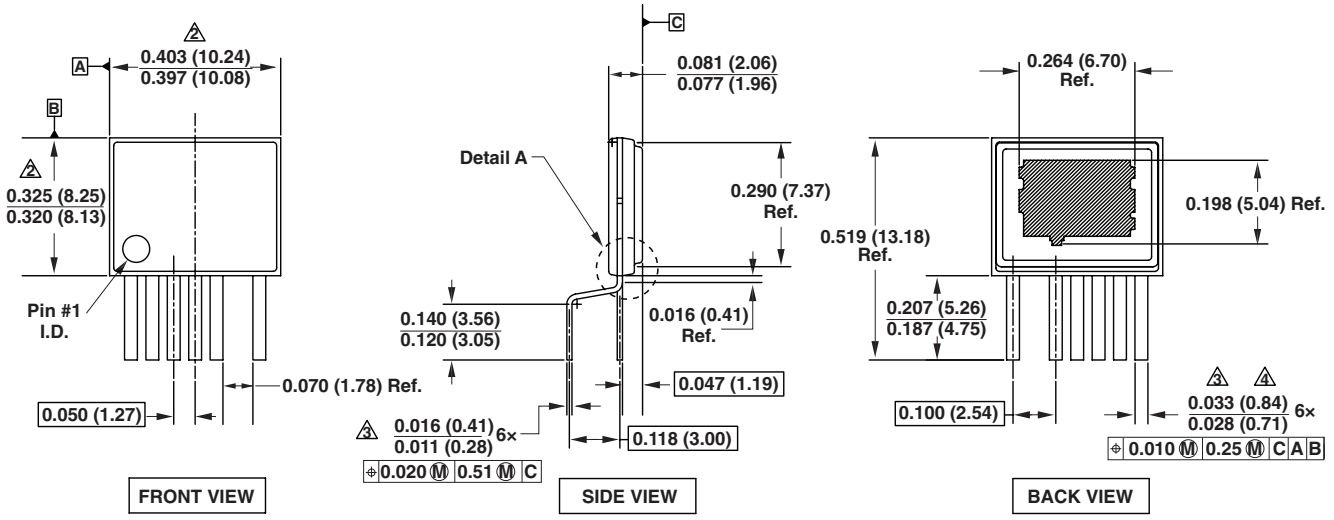
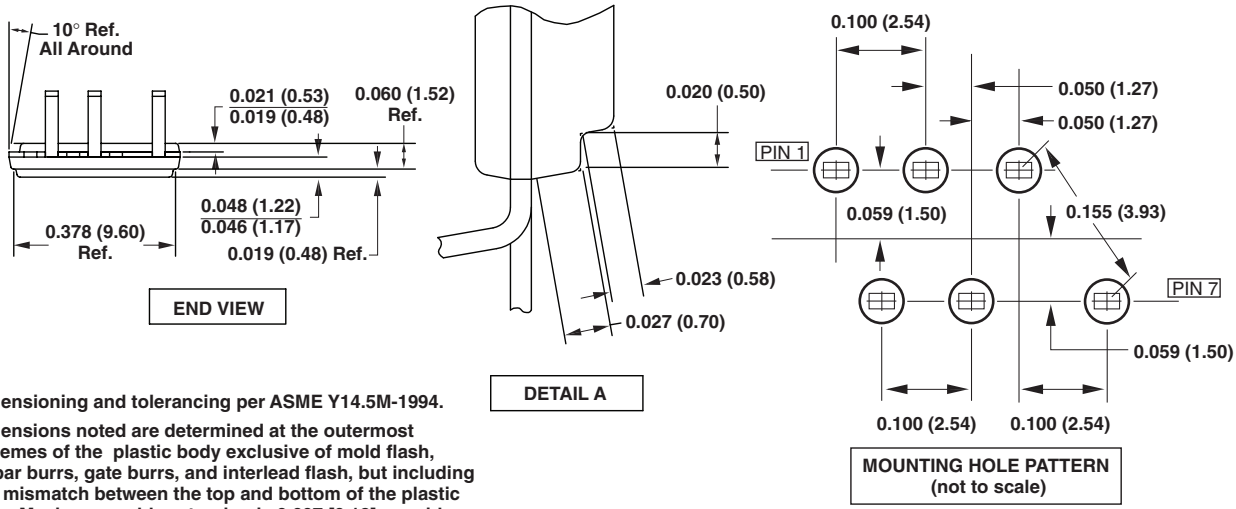


Figure 17. Maximum Allowable Drain Current vs. Drain Voltage.

eSIP-7C (E Package)



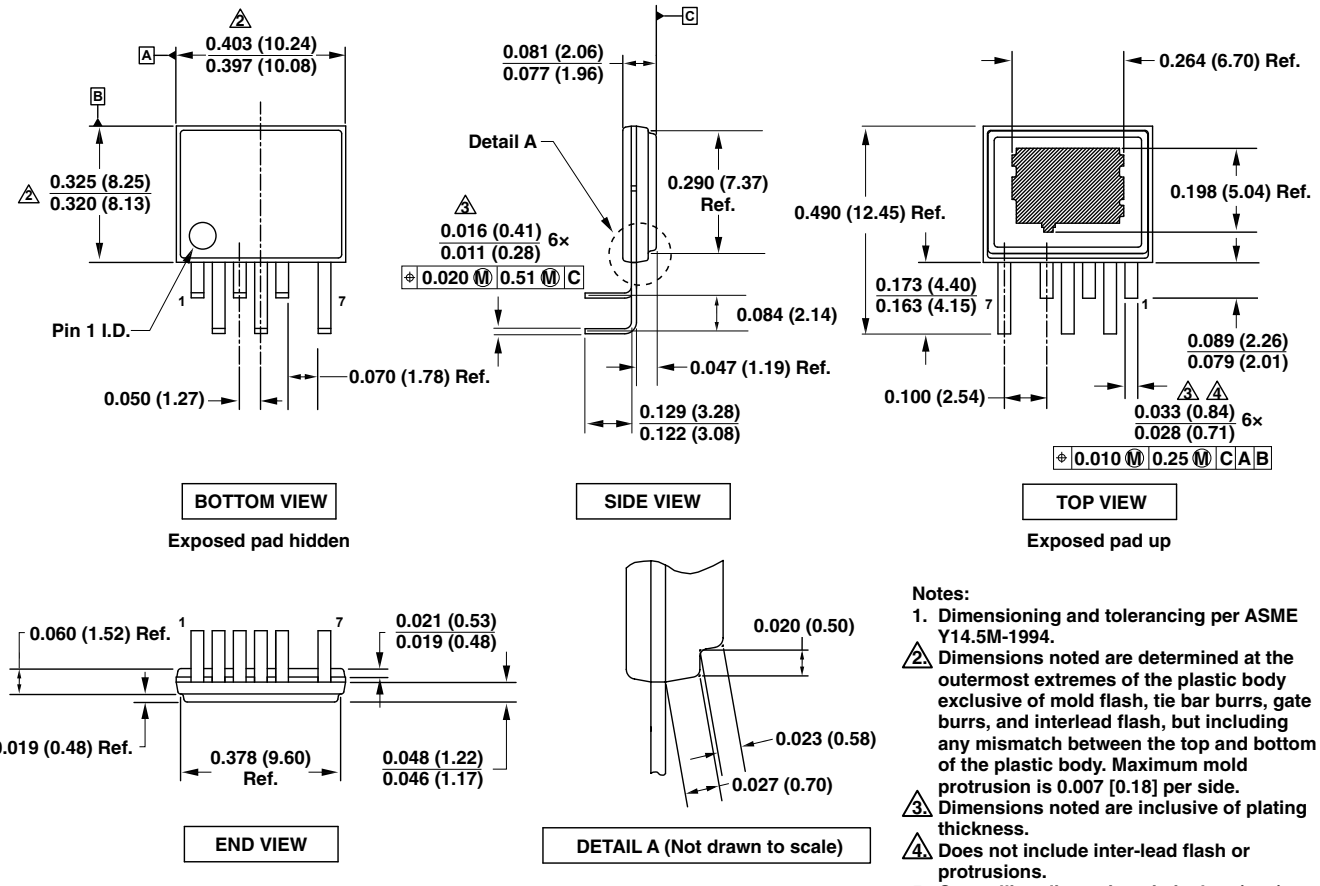


Notes:

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimensions noted are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs, and interlead flash, but including any mismatch between the top and bottom of the plastic body. Maximum mold protrusion is 0.007 [0.18] per side.
3. Dimensions noted are inclusive of plating thickness.
4. Does not include inter-lead flash or protrusions.
5. Controlling dimensions in inches (mm).

PI-4917-061510

eSIP-7F (L Package)

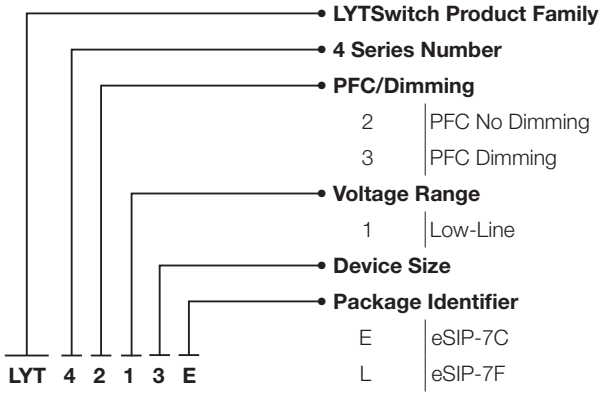


Notes:

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimensions noted are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs, and interlead flash, but including any mismatch between the top and bottom of the plastic body. Maximum mold protrusion is 0.007 [0.18] per side.
3. Dimensions noted are inclusive of plating thickness.
4. Does not include inter-lead flash or protrusions.
5. Controlling dimensions in inches (mm).

PI-5204-061510

Part Ordering Information



Revision	Notes	Date
A	Initial Release.	11/12
B	Corrected Min and Typ parameter table values on pages 13 and 14.	02/13
B	Updated parameters I_{CH1}, I_{CH2}, I_{CD1}, DC_{AR}, $I_{LIMIT(F)}$, $I_{LIMIT(R)}$, on pages 13, 14 and 15.	02/20/13

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