



THE DATASHEET OF MAX125CEAX+TD





2x4-Channel, Simultaneous-Sampling 14-Bit DAS

MAX125/MAX126

General Description

The MAX125/MAX126 are high-speed, multichannel, 14-bit data-acquisition systems (DAS) with simultaneous track/holds (T/Hs). These devices contain a 14-bit, 3 μ s, successive-approximation analog-to-digital converter (ADC), a +2.5V reference, a buffered reference input, and a bank of four simultaneous-sampling T/H amplifiers that preserve the relative phase information of the sampled inputs. The MAX125/MAX126 have two multiplexed inputs for each T/H, allowing a total of eight inputs. In addition, the converter is overvoltage tolerant to ± 17 V; a fault condition on any channel will not harm the IC. Available input ranges are ± 5 V (MAX125) and ± 2.5 V (MAX126).

An on-board sequencer converts one to four channels per $\overline{\text{CONVST}}$ pulse. In the default mode, one T/H output (CH1A) is converted. An interrupt signal ($\overline{\text{INT}}$) is provided after the last conversion is complete. Convert two, three, or four channels by reprogramming the MAX125/MAX126 through the bidirectional parallel interface. Once programmed, the MAX125/MAX126 continue to convert the specified number of channels per $\overline{\text{CONVST}}$ pulse until they are reprogrammed. The channels are converted sequentially, beginning with CH1. The $\overline{\text{INT}}$ signal always follows the end of the last conversion in a conversion sequence. The ADC converts each assigned channel in 3 μ s and stores the result in an internal 14x4 RAM. Upon completion of the conversions, data can be accessed by applying successive pulses to the $\overline{\text{RD}}$ pin. Four successive reads access four data words sequentially.

The parallel interface's data-access and bus-release timing specifications are compatible with most popular digital signal processors and 16-bit/32-bit microprocessors, so the MAX125/MAX126 conversion results can be accessed without resorting to wait states.

Applications

Multiphase Motor Control
Power-Grid Synchronization
Power-Factor Monitoring
Digital Signal Processing
Vibration and Waveform Analysis

Features

- ◆ Four Simultaneous-Sampling T/H Amplifiers with Two Multiplexed Inputs (eight single-ended inputs total)
- ◆ 3 μ s Conversion Time per Channel
- ◆ Throughput: 250ksps (1 channel)
142ksps (2 channels)
100ksps (3 channels)
76ksps (4 channels)
- ◆ Input Range: ± 5 V (MAX125)
 ± 2.5 V (MAX126)
- ◆ Fault-Protected Input Multiplexer (± 17 V)
- ◆ ± 5 V Supplies
- ◆ Internal +2.5V or External Reference Operation
- ◆ Programmable On-Board Sequencer
- ◆ High-Speed Parallel DSP Interface

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	INL (LSB)
MAX125CCAX	0°C to +70°C	36 SSOP	± 4
MAX125CEAX	-40°C to +85°C	36 SSOP	± 4
MAX126CCAX	0°C to +70°C	36 SSOP	± 4
MAX126CEAX	-40°C to +85°C	36 SSOP	± 4

Typical Operating Circuit appears at end of data sheet.

Pin Configuration appears at end of data sheet.

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ABSOLUTE MAXIMUM RATINGS

AV _{DD} to AGND	-0.3V to 6V	Continuous Power Dissipation (T _A = +70°C)	
AV _{SS} to AGND	0.3V to -6V	SSOP (derate 11.8mW/°C above +70°C)	941mW
DV _{DD} to DGND	-0.3V to 6V	Operating Temperature Ranges	
AGND to DGND	-0.3V to 0.3V	MAX125CCAX/MAX126CCAX	0°C to +70°C
CH_ _ to AGND	±17V	MAX125CEAX/MAX126CEAX	-40°C to +85°C
REFIN, REFOUT to AGND	-0.3V to 6V	Storage Temperature Range	-65°C to +150°C
Digital Inputs/Outputs to DGND	-0.3V to (DV _{DD} + 0.3V)	Lead Temperature (soldering, 10sec).....	300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(AV_{DD} = +5V ±5%, AV_{SS} = -5V ±5%, DV_{DD} = +5V ±5%, V_{REFIN} = 2.5V, AGND = DGND = 0V, 4.7µF capacitor from REFOUT to AGND, 0.1µF capacitor from REFIN to AGND, f_{CLK} = 16MHz, external clock, 50% duty cycle, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC ACCURACY (Note 1)						
Resolution	N	All channels	14			Bits
Integral Nonlinearity	INL	(Note 2)		±2	±4	LSB
No Missing Codes			13			Bits
Bipolar Zero Error		T _A = +25°C		±5	±15	mV
		T _A = T _{MIN} to T _{MAX}			±25	
Bipolar Zero-Error Match		Between all channels		1.2	5	mV
Zero-Code Tempco				±5		ppm/°C
Gain Error		T _A = +25°C		±5	±10	mV
		T _A = T _{MIN} to T _{MAX}			±15	
Gain-Error Match		Between all channels		1.2	5	mV
Gain-Error Tempco				±5		ppm/°C
DYNAMIC PERFORMANCE (f_{CLK} = 16MHz, f_{IN} = 10.06kHz (Notes 1, 3))						
Signal-to-Noise Plus Distortion	SINAD	Single-channel mode, channel 1A, 250ksps (Note 4)	MAX125	72	75	dB
			MAX126	70	72	
Total Harmonic Distortion	THD	Single-channel mode, channel 1A, 250ksps (Notes 4, 5)		-89	-80	dB
Spurious-Free Dynamic Range	SFDR	Single-channel mode, channel 1A, 250ksps (Note 4)	80	90		dB
Channel-to-Channel Isolation		Single-channel mode, channel 1A, 250ksps (Note 6)		80		dB

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ELECTRICAL CHARACTERISTICS (continued)

(AVDD = +5V ±5%, AVSS = -5V ±5%, DVDD = +5V ±5%, VREFIN = 2.5V, AGND = DGND = 0V, 4.7µF capacitor from REFOUT to AGND, 0.1µF capacitor from REFIN to AGND, fCLK = 16MHz, external clock, 50% duty cycle, TA = TMIN to TMAX, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ANALOG INPUT						
Input Voltage Range	VIN	MAX125			±5	V
		MAX126			±2.5	
Input Current	IIN	MAX125, VIN = ±5V			±667	µA
		MAX126, VIN = ±2.5V				
Input Capacitance	CIN	(Note 7)			16	pF
TRACK/HOLD						
Acquisition Time	tACQ		1			µs
Small-Signal Bandwidth				8		MHz
Full-Power Bandwidth				0.5		MHz
Droop Rate				2		mV/ms
Aperture Delay				5		ns
Aperture Jitter				30		psRMS
Aperture-Delay Matching				500		ps
REFERENCE OUTPUT (Note 8)						
Output Voltage	VREFOUT	TA = +25°C	2.475	2.500	2.525	V
External Load Regulation		0mA < ILOAD < 1mA		±1		%
REFOUT Tempco		(Note 9)		30		ppm/°C
External Capacitive Bypass at REFIN			0.1			µF
External Capacitive Bypass at REFOUT			4.7		22	µF
REFERENCE INPUT						
Input Voltage Range			2.50 ±10%			V
Input Current		REFIN = 2.5V			±10	µA
Input Resistance		(Note 10)		10		kΩ
Input Capacitance		(Note 7)			10	pF
EXTERNAL CLOCK						
External Clock Frequency			0.1		16	MHz
DIGITAL INPUTS (CONVST, RD, WR, CS, CLK, A0–A3) (Note 1)						
Input High Voltage	VIH		2.4			V
Input Low Voltage	VIL				0.8	V
Input Current	IIN	CONVST, RD, WR, CS, CLK			±1	µA
		A0–A3			±10	
Input Capacitance	CIN	(Note 7)			15	pF

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ELECTRICAL CHARACTERISTICS (continued)

(AVDD = +5V ±5%, AVSS = -5V ±5%, DVDD = +5V ±5%, VREFIN = 2.5V, AGND = DGND = 0V, 4.7µF capacitor from REFOUT to AGND, 0.1µF capacitor from REFIN to AGND, fCLK = 16MHz, external clock, 50% duty cycle, TA = TMIN to TMAX, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL OUTPUTS (D0–D13, INT) (Note 1)						
Output High Voltage	VOH	IOUT = 1mA	4			V
Output Low Voltage	VOL	IOUT = -1.6mA			0.4	V
Three-State Leakage Current		D0–D13			±10	µA
Three-State Output Capacitance		(Note 7)			10	pF
POWER REQUIREMENTS						
Positive Supply Voltage	AVDD		4.75	5	5.25	V
Negative Supply Voltage	AVSS		-5.25	-5	-4.75	V
Digital Supply Voltage	DVDD		4.75	5	5.25	V
Positive Supply Current	I(AVDD)			17	25	mA
Negative Supply Current	I(AVSS)		-17	-13		mA
Digital Supply Current	I(DVDD)			3	5	mA
Shutdown Positive Current					3	mA
Shutdown Negative Current			-1			mA
Shutdown Digital Current					3	mA
Positive Supply Rejection	PSRR+	(Note 11)		±1	±2	LSB
Negative Supply Rejection	PSRR-	(Note 11)			±2	LSB
Power Dissipation		(Note 12)		165	250	mW

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TIMING CHARACTERISTICS (Figure 4)

(AV_{DD} = +5V, AV_{SS} = -5V, DV_{DD} = +5V, AGND = DGND = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{\text{CONVST}}$ Pulse Width	t _{cw}		30			ns
$\overline{\text{CS}}$ to $\overline{\text{WR}}$ Setup Time	t _{cws}		0			ns
$\overline{\text{CS}}$ to $\overline{\text{WR}}$ Hold Time	t _{cwh}		0			ns
$\overline{\text{WR}}$ Low Pulse Width	t _{wr}		30			ns
$\overline{\text{CS}}$ to $\overline{\text{CONVST}}$ Delay	t _{cSD}		125			ns
Address Setup Time	t _{AS}		30			ns
Address Hold Time	t _{AH}		0			ns
$\overline{\text{RD}}$ to $\overline{\text{INT}}$ Delay	t _{iD}	25pF load			30	ns
Delay Time Between Reads	t _{RD}		40			ns
$\overline{\text{CS}}$ to $\overline{\text{RD}}$ Setup Time	t _{CRS}		0			ns
$\overline{\text{CS}}$ to $\overline{\text{RD}}$ Hold Time	t _{CRH}		0			ns
$\overline{\text{RD}}$ Low Pulse Width	t _{rD}		30			ns
Data-Access Time	t _{DA}	25pF load (Note 13)			30	ns
Bus-Relinquish Time	t _{DH}	25pF load (Note 14)	5		45	ns
Conversion Time	t _{CONV}	Mode 1, 1 channel			3	μs
		Mode 2, 2 channel			6	
		Mode 3, 3 channel			9	
		Mode 4, 4 channel			12	
Conversion Rate/Channel		Mode 1, 1 channel			250	ksps
		Mode 2, 2 channel			142	
		Mode 3, 3 channel			100	
		Mode 4, 4 channel			76	
Start-Up Time		Exiting shutdown		5		μs

Note 1: AV_{DD} = +5V, AV_{SS} = -5V, DV_{DD} = +5V, V_{REFIN} = 2.500V (external), V_{IN} = ±5V (MAX125) or ±2.5V (MAX126).

Note 2: Relative accuracy is the analog value's deviation at any code from its theoretical value after the full-scale range has been calibrated.

Note 3: CLK synchronized with $\overline{\text{CONVST}}$.

Note 4: f_{IN} = 10.06kHz, V_{IN} = ±5V (MAX125) or ±2.5V (MAX126).

Note 5: First five harmonics.

Note 6: All inputs except CH1A driven with ±5V (MAX125) or ±2.5V (MAX126) 10kHz signal; CH1A connected to AGND and digitized.

Note 7: Guaranteed by design. Not production tested.

Note 8: AV_{DD} = +5V, AV_{SS} = -5V, DV_{DD} = +5V, V_{IN} = 0V (all channels).

Note 9: Temperature drift is defined as the change in output voltage from +25°C to T_{MIN} or T_{MAX}. It is calculated as TC = [ΔREFOUT/REFOUT] / ΔT.

Note 10: See Figure 2.

Note 11: Defined as the change in positive full scale caused by a ±5% variation in the nominal supply voltage. Tested with one input at full scale and all others at AGND. V_{REFIN} = 2.5V (internal).

Note 12: Tested with V_{IN} = AGND on all channels, V_{REFIN} = 2.5V (internal).

Note 13: The data-access time is defined as the time required for an output to cross 0.8V or 2.0V. It is measured using the circuit of Figure 1. The measured number is then extrapolated back to determine the value with a 25pF load.

Note 14: The bus-relinquish time is derived from the measured time taken for the data outputs to change 0.5V when loaded with the circuit of Figure 1. The measured number is then extrapolated back to remove the effects of charging/discharging the 120pF capacitor. Thus, the time given is the part's true bus-relinquish time, independent of the external bus loading capacitance.

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Pin Description

PIN	NAME	FUNCTION
1, 2	CH2B, CH2A	Channel 2 Multiplexed Inputs, single-ended
3, 4	CH1B, CH1A	Channel 1 Multiplexed Inputs, single-ended
5	AV _{DD}	+5V ±5% Analog Supply Voltage
6	REFIN	External Reference Input/Internal Reference Output. Bypass with a 0.1µF capacitor to AGND.
7	REFOUT	Reference-Buffer Output. Bypass with a 4.7µF capacitor to AGND.
8, 36	AGND	Analog Ground. Both pins must be tied to ground.
9–16	D13–D6	Data Bits. D13 = MSB.
17	DV _{DD}	+5V ±5% Digital Supply Voltage
18	DGND	Digital Ground
19, 20	D5, D4	Data Bits
21–24	D3/A3–D0/A0	Bidirectional Data Bits/Address Bits. D0/A0 = LSB.
25	CLK	Clock Input (duty cycle must be 30% to 70%).
26	$\overline{\text{CS}}$	Chip-Select Input (active-low)
27	$\overline{\text{WR}}$	Write Input (active-low)
28	$\overline{\text{RD}}$	Read Input (active-low)
29	$\overline{\text{CONVST}}$	Conversion-Start Input. Rising edge initiates sampling and conversion sequence.
30	$\overline{\text{INT}}$	Interrupt Output. Falling edge indicates the end of a conversion sequence.
31	AV _{SS}	-5V ±5% Analog Supply Voltage
32, 33	CH4A, CH4B	Channel 4 Multiplexed Inputs, single-ended
34, 35	CH3A, CH3B	Channel 3 Multiplexed Inputs, single-ended

Detailed Description

The MAX125/MAX126 use a successive-approximation conversion technique and four simultaneous-sampling track/hold (T/H) amplifiers to convert analog signals into 14-bit digital outputs. Each T/H has two multiplexed inputs, allowing a total of eight inputs. Each T/H output is converted and stored in memory to be accessed sequentially by the parallel interface with successive read cycles. The MAX125/MAX126 internal micro-sequencer can be programmed to digitize one, two, three, or four inputs sampled simultaneously from either of the two banks of four inputs (see Figure 2).

The conversion timing and control sequences are derived from a 16MHz external clock, the $\overline{\text{CONVST}}$

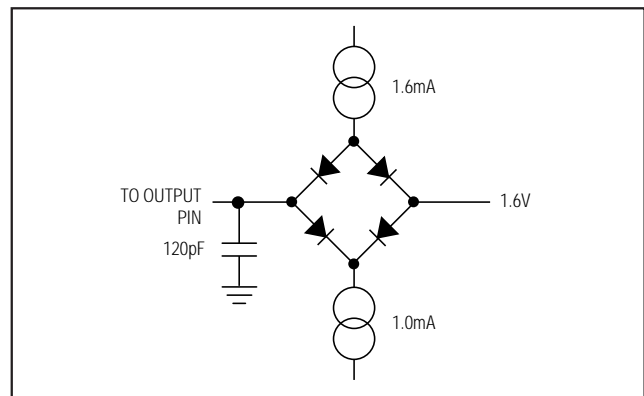


Figure 1. Load Circuit for Access Time and Bus Relinquish Time

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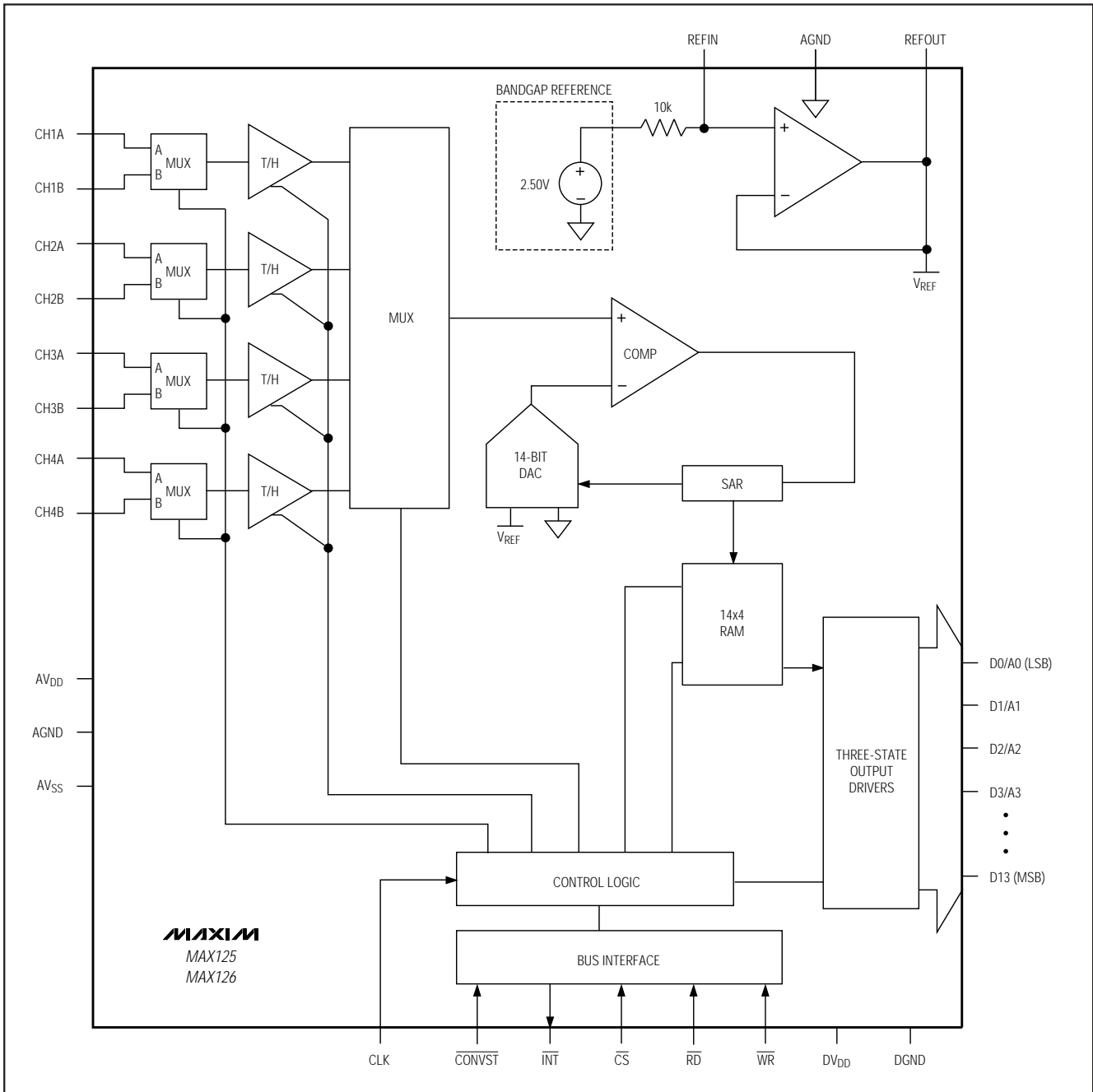


Figure 2. Functional Diagram

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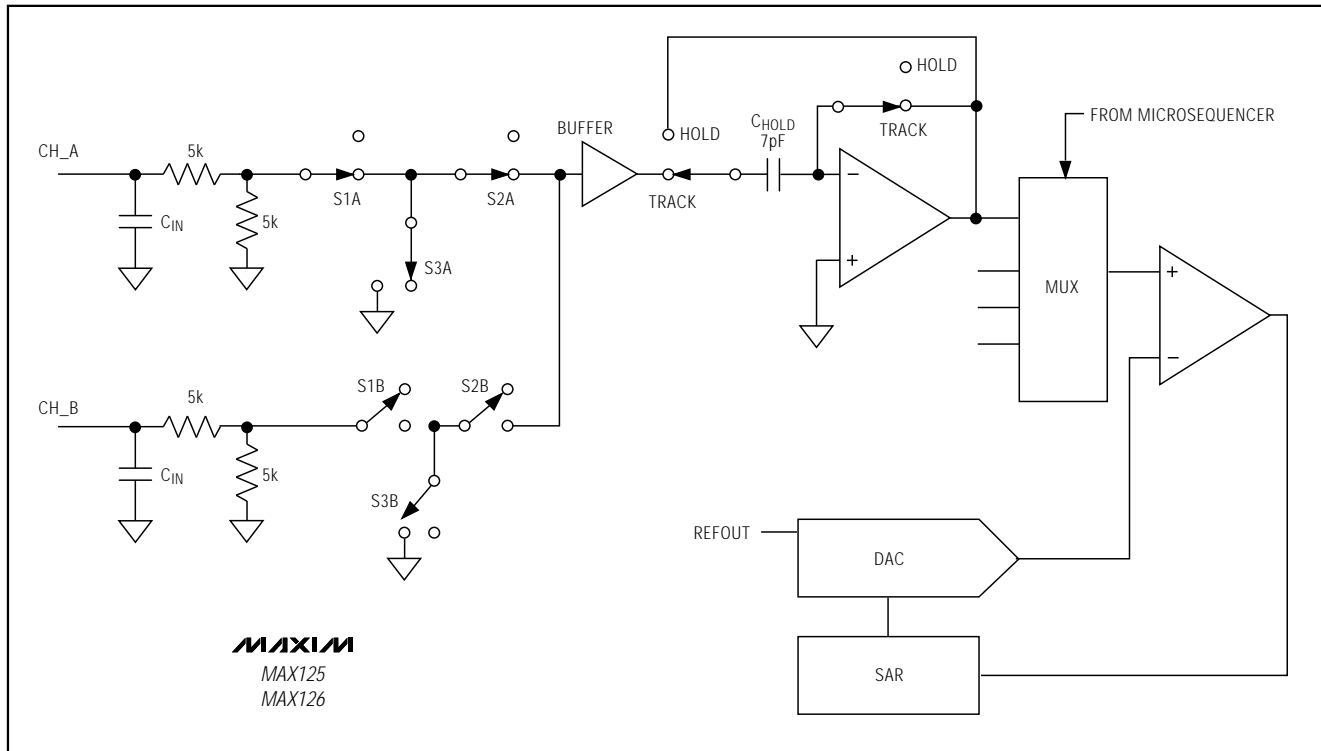


Figure 3. Equivalent Input Circuit

signal, and the programmed mode. The T/H amplifiers hold the input voltages at the $\overline{\text{CONVST}}$ rising edge. Additional $\overline{\text{CONVST}}$ pulses are ignored until the last conversion for the sample is complete. The ADC converts each assigned channel in $3\mu\text{s}$ and stores the result in an internal 4x14-bit memory.

At the end of the last conversion, $\overline{\text{INT}}$ goes low and the T/H amplifiers begin to track the inputs again. The data can be accessed by applying successive pulses to the $\overline{\text{RD}}$ pin. Successive reads access data words sequentially. The memory is *not* random-access; data from CH1 is always read first. After accessing all programmed channels, the address pointer selects CH1 again. Additional read pulses cycle through the data words. $\overline{\text{CS}}$ can be held low during successive reads.

Input Bandwidth

The T/H's input tracking circuitry has an 8MHz small-signal bandwidth, so it is possible to digitize high-speed transient events and measure periodic signals with bandwidths exceeding the ADC's sampling rate by using undersampling techniques. To avoid high-frequency signals being aliased into the frequency band of interest, anti-alias filtering is recommended.

Analog Input Range and Input Protection
The MAX125's input range is $\pm 5\text{V}$, and the MAX126's input range is $\pm 2.5\text{V}$. The input resistance for both parts is $10\text{k}\Omega$. An input protection structure allows input voltages to $\pm 17\text{V}$ without harming the IC. This protection is also active in shutdown mode.

Track/Holds

The MAX125/MAX126 feature four simultaneous T/Hs. Each T/H has two multiplexed inputs. A T-switch input configuration provides excellent hold-mode isolation. Allow $1\mu\text{s}$ acquisition time for 14-bit accuracy.

The T/H aperture delay is typically 10ns. The 500ps aperture-delay mismatch between the T/Hs allows the relative phase information of up to four different inputs to be preserved. Figure 3 shows the equivalent input circuit, illustrating the ADC's sampling architecture. Only one of four T/H stages with its two multiplexed inputs (CH_A and CH_B) is shown. All switches are in track configuration for channel A. An internal buffer charges the hold capacitor to minimize the required acquisition time between conversions. The analog input appears as a $10\text{k}\Omega$ resistor in parallel with a 16pF capacitor.

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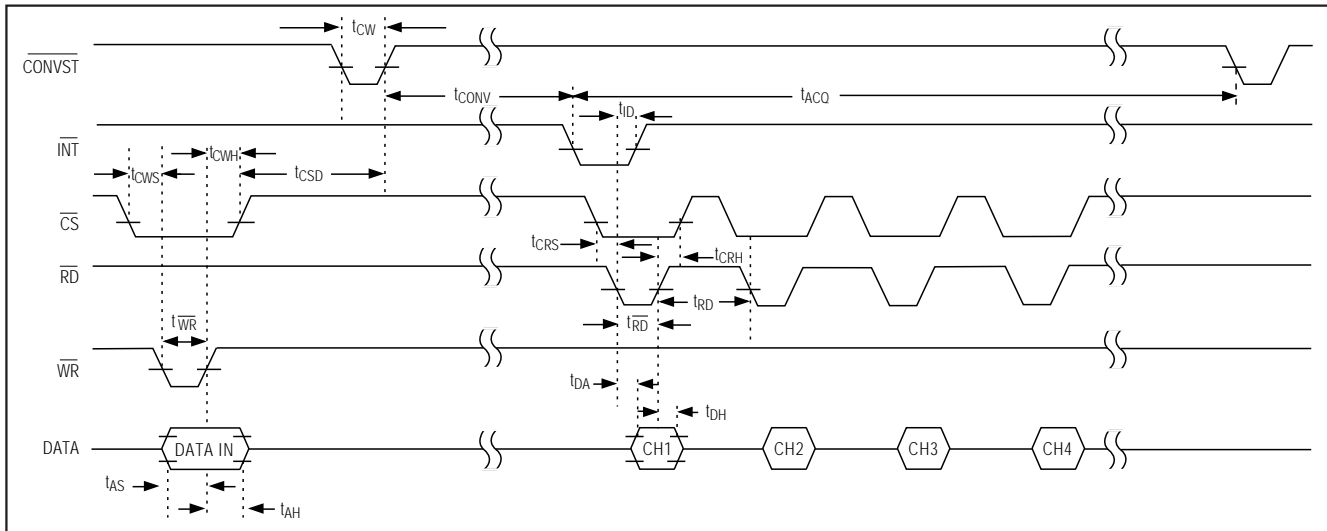


Figure 4. Timing Diagram

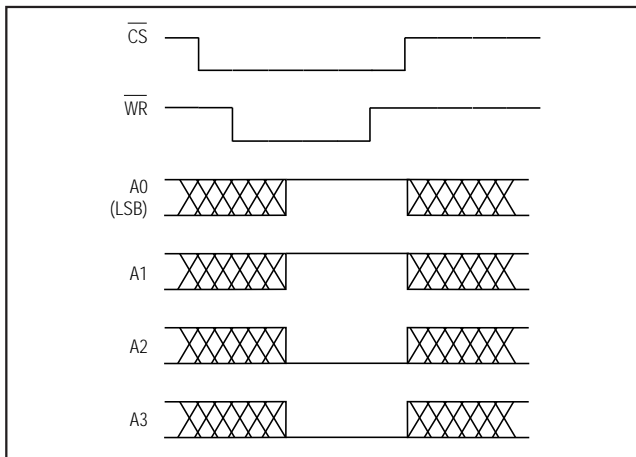


Figure 5. Programming a Four-Channel Conversion, Input Mux A

Between conversions, the buffer input is connected to channel 1 of the selected track/hold bank. When a channel is not selected, switches S1, S2, and S3 are placed in hold mode to improve channel-to-channel isolation.

Digital Interface

Input data (A0–A3) and output data (D0–D13) are multiplexed on a three-state bidirectional interface. This parallel I/O can easily be interfaced with a microprocessor (μ P) or DSP. \overline{CS} , \overline{WR} , and \overline{RD} control the write and read operations. \overline{CS} is the standard chip-select signal, which enables the controller to address the MAX125/MAX126 as an I/O port. When \overline{CS} is high, it disables the \overline{WR} and

\overline{RD} inputs and forces the interface into a high-Z state. Figure 4 details the interface timing.

Programming Modes

The MAX125/MAX126 have eight conversion modes plus power-down, which are programmed through a bidirectional parallel interface. At power-up, the devices default to the mode *Input Mux A/Single-Channel Conversion*. The user can select between two banks (mux inputs A or mux inputs B) of four simultaneous-sampled input channels, as illustrated in Figure 2. An internal microsequencer can be programmed to convert one, two, three, or four channels of the selected bank per sample. For a single-channel conversion, CH1 is digitized, and then INT goes low to indicate completion of the conversion. For multichannel conversions, INT goes low after the last channel has been digitized.

To input data into the MAX125/MAX126, pull \overline{CS} low, program the bidirectional pins A0–A3 (Table 1), and pulse \overline{WR} low. Data is latched into the devices on the \overline{WR} or \overline{CS} rising edge. The ADC is now ready to convert. Once programmed, the ADCs continue operating in the same mode until they are reprogrammed or until power is removed. Figure 5 shows an example of programming a four-channel conversion using Input Mux A.

Starting a Conversion

After programming the MAX125/MAX126 as outlined in the *Programming Modes* section, pulse \overline{CONVST} low to initiate a conversion sequence. The analog inputs are sampled at the \overline{CONVST} rising edge. Do not start a new conversion while the conversion is in progress. Monitor the \overline{INT} output. A falling edge indicates the end of a conversion sequence.

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Table 1. Modes of Operation

A3	A2	A1	A0	CONVERSION TIME (μ s)	MODE
0	0	0	0	3	Input Mux A/Single-Channel Conversion (default at power-up)
0	0	0	1	6	Input Mux A/Two-Channel Conversion
0	0	1	0	9	Input Mux A/Three-Channel Conversion
0	0	1	1	12	Input Mux A/Four-Channel Conversion
0	1	0	0	3	Input Mux B/Single-Channel Conversion
0	1	0	1	6	Input Mux B/Two-Channel Conversion
0	1	1	0	9	Input Mux B/Three-Channel Conversion
0	1	1	1	12	Input Mux B/Four-Channel Conversion
1	X	X	X	—	Power-Down

X = Don't care

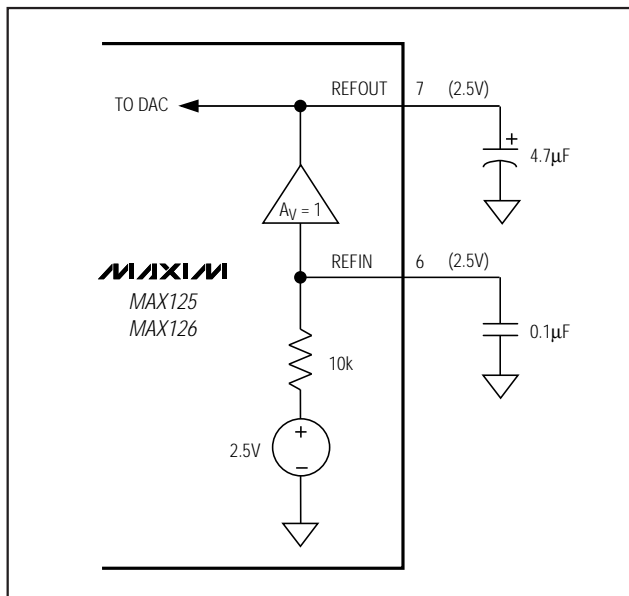


Figure 6. Internal Reference

Reading a Conversion

Digitized data from up to four channels are stored in memory to be read out through the parallel interface. After receiving an $\overline{\text{INT}}$ signal, the user can access up to four conversion results by performing up to four read operations.

With $\overline{\text{CS}}$ low, the conversion result from CH_1 is accessed, and $\overline{\text{INT}}$ is reset high on the first $\overline{\text{RD}}$ falling edge. On the $\overline{\text{RD}}$ rising edge, the internal address pointer is advanced. If a single conversion is programmed, only one $\overline{\text{RD}}$ pulse is required, and the

address pointer is reset to CH_1. For multichannel conversions, up to four $\overline{\text{RD}}$ falling edges sequentially access the data for channels 1 through 4. For n channels converted ($1 < n \leq 4$), the address pointer is reset to CH_1 after n $\overline{\text{RD}}$ pulses. Do not perform a read operation during conversion, as it will corrupt the conversion's accuracy.

Applications Information

External Clock

The MAX125/MAX126 require a TTL-compatible clock up to 16MHz for proper operation. The clock duty cycle's range is between 30% and 70%.

Internal and External Reference

The MAX125/MAX126 can be used with an internal or external reference voltage. An external reference can be connected directly at REFIN. An internal buffer with a gain of +1 provides 2.5V at REFOUT.

Internal Reference

The full-scale range with the internal reference is $\pm 5V$ for the MAX125 and $\pm 2.5V$ for the MAX126. Bypass REFIN with a $0.1\mu\text{F}$ capacitor to AGND and bypass the REFOUT pin with a $4.7\mu\text{F}$ (min) capacitor to AGND (Figure 6). The maximum value to compensate the reference buffer is $22\mu\text{F}$. Larger values are acceptable if low-ESR capacitors are used.

External Reference

For operation over a wide temperature range, an external 2.5V reference with tighter specifications improves accuracy. The MAX6325 is an excellent choice to match the MAX125/MAX126 accuracy over the commercial and extended temperature ranges with a

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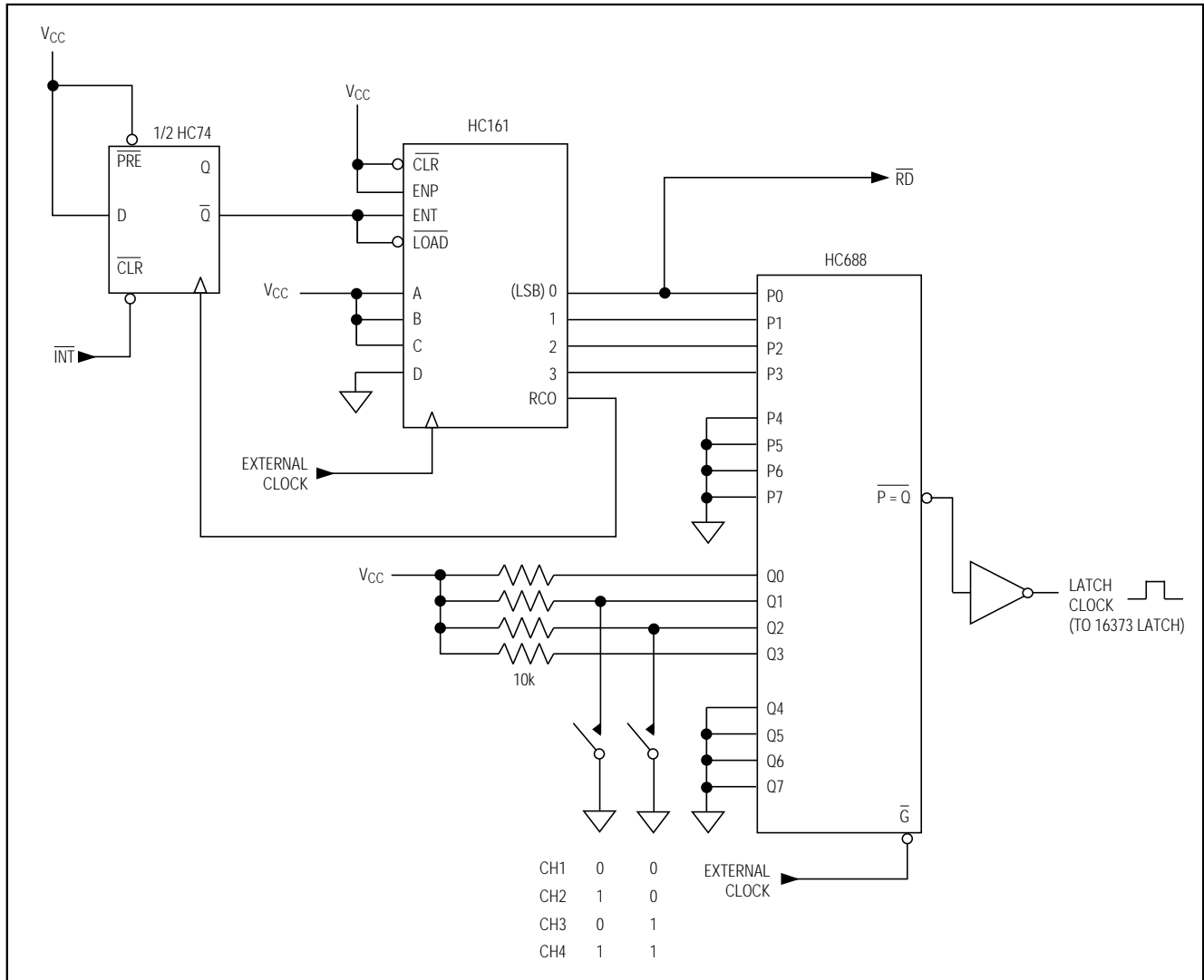


Figure 9. Output Demultiplexer Circuit

The circuit of Figure 10 shows a typical vector motor-control application using all available inputs of the MAX125/MAX126. CH1A and CH2A are connected to two isolated Hall-effect current sensors and are a part of the current (torque) feedback loop. The MAX125/MAX126 digitize the currents and deliver raw data to the following DSP and controller stages, where the vector processing takes place. Sensorless vector control uses a computer model for the motor and an algorithm to split each output current into its magnetizing (stator current) and torque-producing (rotor current) components.

If a 2- to 3-phase conversion is not practical, three currents can be sampled simultaneously with the addition of a third sensor (not shown). Optional voltage (position) feedback can be derived by measuring two phase voltages (CH3A, CH4A). Typically, an isolated differential amplifier is used between the motor and the MAX125/MAX126. Again, the third phase voltage can be derived from the magnitude (phase voltage) and its relative phase.

For optimum speed control and good load regulation close to zero speed, additional velocity and position feedback are derived from an encoder or resolver and

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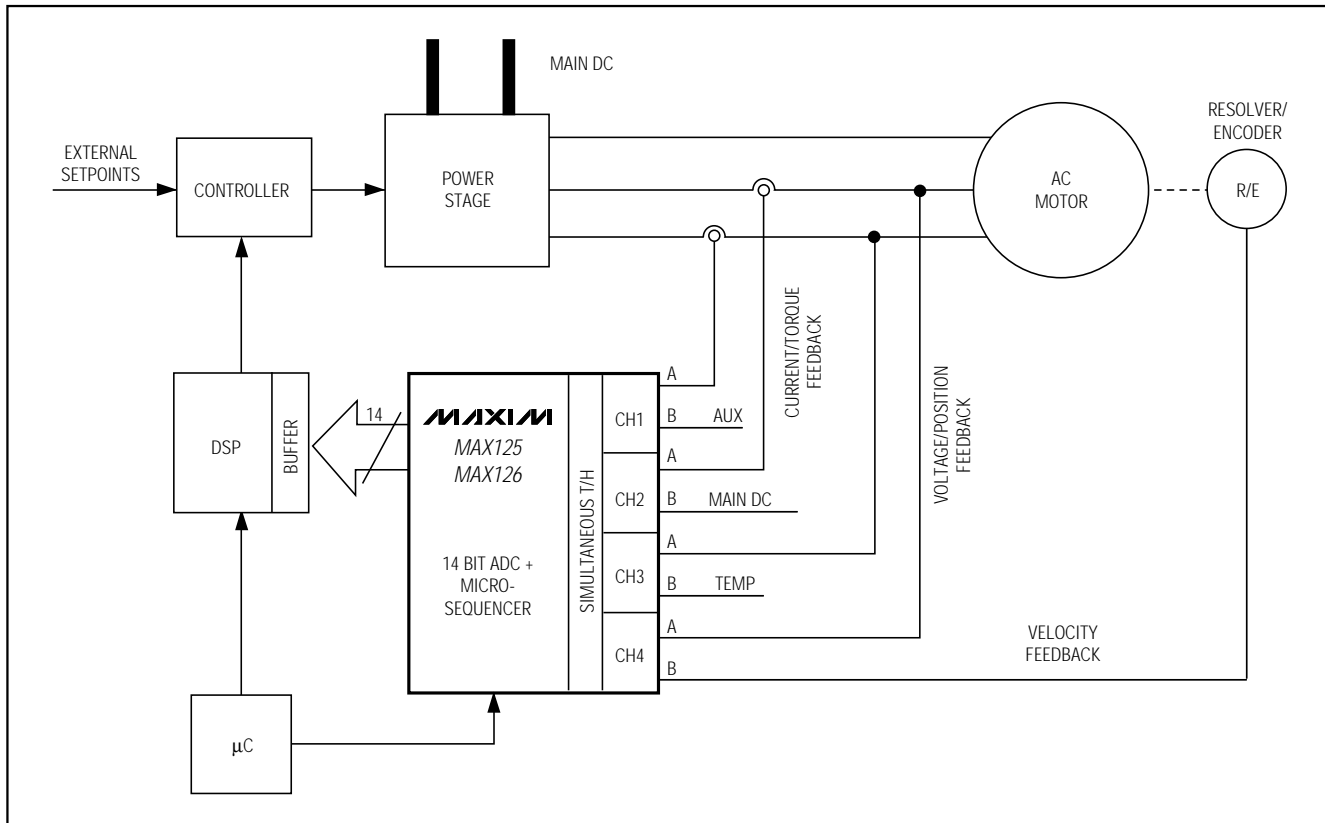


Figure 10. Vector Motor Control

brought to the MAX125/MAX126 at CH4B. The additional channels can be used to evaluate slower analog inputs, such as the main DC bus voltage (CH2B), temperature sensors (CH3B), or other analog inputs (AUX, CH1B).

Power-Supply Bypassing and Ground Management

For optimum system performance, use printed circuit boards with separate analog and digital ground planes. Wire-wrapped boards are not recommended. Connect the two ground planes together at the low-impedance power-supply source. Connect DGND and AGND together at the IC. For the best ground connection, connect the DGND and AGND pins together and

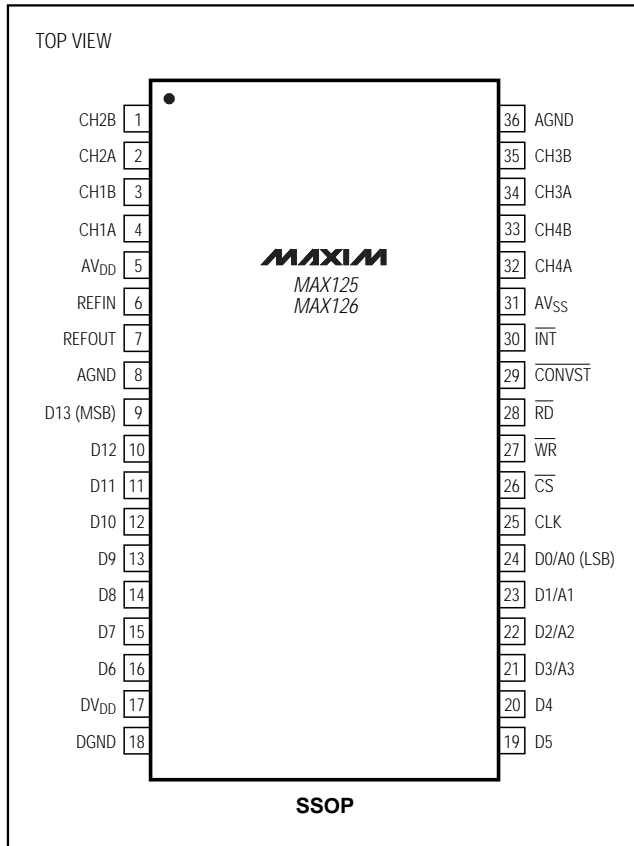
connect that point to the system analog ground plane to avoid interference from other digital noise sources. If DGND is connected to the system digital ground, digital noise may get through to the ADC's analog portion.

The AGND pins must be connected directly to a low-impedance ground plane. Extra impedance between the pins and the ground plane increases crosstalk and degrades INL.

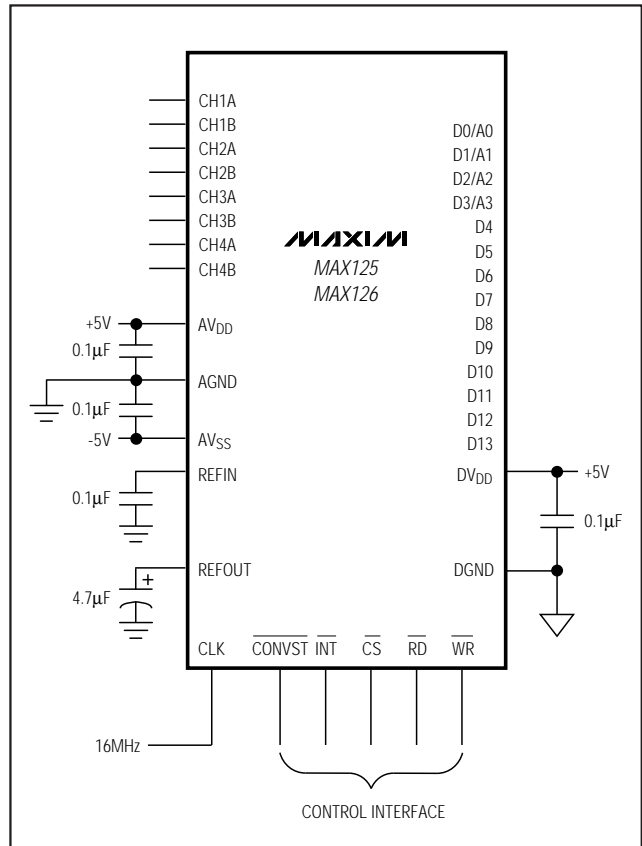
Bypass AVDD and AVSS with 0.1μF ceramic capacitors to AGND. Mount them with short leads close to the device. Ferrite beads may also be used to further isolate the analog and digital power supplies. Bypass DVDD with a 0.1μF ceramic capacitor to DGND.

2x4-Channel, Simultaneous-Sampling 14-Bit DAS

Pin Configuration



Typical Operating Circuit



Chip Information

TRANSISTOR COUNT: 4219
SUBSTRATE CONNECTED TO AV_{SS}

Package Information

For the latest package outline information and land patterns, go to www.maxim-ic.com/packages.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
36 SSOP	A36-4	21-0040

2x4-Channel, Simultaneous-Sampling 14-Bit DAS

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
2	6/07	Updated <i>Ordering Information</i> section	1, 2, 15
3	7/08	Added line to DC Accuracy section of EC table	2

MAX125/MAX126

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