WINSOURCE
ELECTRONICS

THE DATASHEET OF

MAX15014BATX+

EVALUATION KIT AVAILABLE

MAX15014–MAX15017

1A, 4.5V to 40V Input Buck Converters with 50mA Auxiliary LDO Regulators

General Description

The MAX15014–MAX15017 combine a step-down DC-DC converter and a 50mA, low-quiescent-current low-dropout (LDO) regulator. The LDO regulator is ideal for powering always-on circuitry. The DC-DC converter input voltage range is 4.5V to 40V for the MAX15015/MAX15016, and 7.5V to 40V for the MAX15014/MAX15017.

The DC-DC converter output is adjustable from 1.26V to 32V and can deliver up to 1A of load current. These devices utilize a feed-forward voltage-mode-control scheme for good noise immunity in the high-voltage switching environment and offer external compensation allowing for maximum flexibility with a wide selection of inductor values and capacitor types. The switching frequency is internally fixed at 135kHz and 500kHz, depending on the version chosen. Moreover, the switching frequency can be synchronized to an external clock signal through the SYNC input. Light-load efficiency is improved by automatically switching to a pulse-skip mode. The soft-start time is adjustable with an external capacitor. The DC-DC converter can be disabled independent of the LDO, thus reducing the quiescent current to 47μA (typ).

The LDO linear regulators operate from 5V to 40V and deliver a guaranteed 50mA load current. The devices feature a preset output voltage of 5V (MAX1501_A) or 3.3V (MAX1501_B). Alternatively, the output voltage can be adjusted from 1.5V to 11V by using an external resistive divider. The LDO section also features a $\overline{\text{RESET}}$ output with adjustable timeout period.

Protection features include cycle-by-cycle current limit, hiccup-mode output short-circuit protection, and thermal shutdown. All devices are available in a space-saving, high-power (2.86W), 36-pin TQFN package and are rated for operation over the -40°C to +125°C automotive temperature range.

Applications

- Mobile Radios
- Navigation Systems

Features

- Combined DC-DC Converters and Low-Quiescent-Current LDO Regulators
- 1A DC-DC Converters Operate from 4.5V to 40V (MAX15015/MAX15016) or 7.5V to 40V (MAX15014/MAX15017)
- Switching Frequency of 135kHz (MAX15014/MAX15016) or 500kHz (MAX15015/MAX15017)
- 50mA LDO Regulator Operates from 5V to 40V Independent of the DC-DC Converter
- 47μA Quiescent Current with DC-DC Converter Off and LDO On
- 6μA System Shutdown Current
- Frequency Synchronization Input
- Shutdown/Enable Inputs
- Adjustable Soft-Start Time
- Active-Low Open-Drain $\overline{\text{RESET}}$ Output with Programmable Timeout Delay
- Thermal Shutdown and Output Short-Circuit Protection
- Space-Saving (6mm x 6mm) Thermally Enhanced 36-Pin TQFN Package

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX15014AATX+	-40°C to +125°C	36 TQFN-EP*
MAX15014BATX+	-40°C to +125°C	36 TQFN-EP*
MAX15015AATX+	-40°C to +125°C	36 TQFN-EP*
MAX15015BATX+	-40°C to +125°C	36 TQFN-EP*
MAX15016AATX+	-40°C to +125°C	36 TQFN-EP*
MAX15016BATX+	-40°C to +125°C	36 TQFN-EP*
MAX15017AATX+	-40°C to +125°C	36 TQFN-EP*
MAX15017BATX+	-40°C to +125°C	36 TQFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*

19-0734; Rev 1; 11/14

Absolute Maximum Ratings

IN_SW, IN_LDO, DRAIN, EN_SYS, EN_SW
to SGND .... -0.3V to +45V
IN_LDO to IN_SW .... -0.3V to +0.3V
LX to SGND .... -0.3V to (V_{IN_SW} + 0.3V)
LX to PGND .... -0.3V to (V_{IN_SW} + 0.3V)
BST to SGND .... -0.3V to (V_{IN_SW} + 12V)
BST to LX .... -0.3V to +12V
PGND to SGND .... -0.3V to +0.3V
REG, DVREG, SYNC, $\overline{\text{RESET}}$, CT to SGND .... -0.3V to +12V
FB, COMP_SW, SS to SGND .... -0.3V to (V_{REG} + 0.3V)
SET_LDO, LDO_OUT to SGND .... -0.3V to +12V
C+ to PGND
(MAX15015/MAX15016 only) .... (V_{DVREG} - 0.3V) to 12V
C- to PGND
(MAX15015/MAX15016 only) .... -0.3V to (V_{DVREG} + 0.3V)

LDO_OUT Output Current .... Internally Limited
Switch DC Current (DRAIN and LX pins combined)
T_J = +125°C 1.9A
T_J = +150°C 1.25A
$\overline{\text{RESET}}$ Sink Current 5mA
Continuous Power Dissipation (T_A = +70°C)
36-Pin TQFN (derate 26.3mW/°C above +70°C)
Single-Layer Board 2105mW
36-Pin TQFN (derate 35.7mW/°C above +70°C)
Multilayer Board 2857mW
Operating Temperature Range .... -40°C to +125°C
Maximum Junction Temperature .... +150°C
Storage Temperature Range .... -60°C to +150°C
Lead Temperature (soldering, 10s) .... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(V_{IN_SW} = V_{IN_LDO} = V_{DRAIN} = 14V, V_{EN_SYS} = V_{EN_SW} = 2.4V, V_{REG} = V_{DVREG}, V_{SYNC} = V_{SET_LDO} = V_{SGND} = V_{PGND} = 0V, C_{REG} = 1µF, C_{IN_SW} = 0.1µF, C_{IN_LDO} = 0.1µF, C_{LDO_OUT} = 10µF, C_{DRAIN} = 0.22µF, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
System Supply Current (Not Switching)	I_{SYS}	No load	V_{FB} = 1.3V, MAX15014/MAX15017		0.7	1.8	mA
			V_{FB} = 1.3V, MAX15015/MAX15016		0.85	1.8	
Switching System Supply Current	I_{SW}	No load	V_{FB} = 0V, MAX15014/ MAX15017		5.6		mA
			V_{FB} = 0V, MAX15015/ MAX15016		8.6		
LDO Quiescent Current	I_{LDO}	V_{EN_SYS} = 14V, V_{EN_SW} = 0V	I_{LDO_OUT} = 100µA		47	63	µA
			I_{LDO_OUT} = 50mA		130	200	
System Shutdown Current	I_{SHDN}	V_{EN_SYS} = 0V, V_{EN_SW} = 0V			6	10	µA
System Enable Voltage	V_{EN_SYSH}	EN_SYS = high, system on		2.4			V
	V_{EN_SYSL}	EN_SYS = low, system off				0.8	
System Enable Hysteresis					220		mV
System Enable Input Current	I_{EN_SYS}	V_{EN_SYS} = 2.4V			0.5	2	µA
		V_{EN_SYS} = 14V			0.6	2	
BUCK CONVERTER							
Input Voltage Range	V_{IN_SW}	MAX15014/MAX15017		7.5		40.0	V
		MAX15015/MAX15016		4.5		40.0	

Electrical Characteristics (continued)

(V_{IN_SW} = V_{IN_LDO} = V_{DRAIN} = 14V, V_{EN_SYS} = V_{EN_SW} = 2.4V, V_{REG} = V_{DVREG}, V_{SYNC} = V_{SET_LDO} = V_{SGND} = V_{PGND} = 0V, C_{REG} = 1µF, C_{IN_SW} = 0.1µF, C_{IN_LDO} = 0.1µF, C_{LDO_OUT} = 10µF, C_{DRAIN} = 0.22µF, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Undervoltage Lockout Threshold	$UVLO_{TH}$	V_{IN_SW} and IN_LDO rising, MAX15014/MAX15017	6.7	7.0	7.4	V
		V_{IN_SW} and IN_LDO rising, MAX15015/MAX15016	3.90	4.08	4.25	
Undervoltage Lockout Hysteresis	$UVLO_{HYST}$	MAX15014/MAX15017		0.54		V
		MAX15015/MAX15016		0.3		
Output Voltage Range	V_{OUT}	Minimum output		1.26		V
		Maximum output		32		
Output Current	I_{OUT}			1		A
EN_SW Input Voltage Threshold	V_{EN_SWH}	EN_SW = high, switching power supply is on	2.4			V
	V_{EN_SWL}	EN_SW = low, switching power supply is off			0.8	
EN_SW Hysteresis				220		mV
Switching Enable Input Current	I_{EN_SW}	V_{EN_SW} = 2.4V		0.5	2	µA
		V_{EN_SW} = 14V		0.6	2	
INTERNAL VOLTAGE REGULATOR						
Output Voltage	V_{REG}	MAX15014/MAX15017, V_{IN_SW} = 9V to 40V	7.6		8.4	V
		MAX15015/MAX15016, V_{IN_SW} = 5.5V to 40V	4.75		5.25	
Line Regulation		V_{IN_SW} = 9.0V to 40V, MAX15014/MAX15017		1		mV/V
		V_{IN_SW} = 5.5V to 40V, MAX15015/MAX15016		1		
Load Regulation		I_{REG} = 0 to 20mA			0.25	V
Dropout Voltage		V_{IN_SW} = 7.5V (MAX15014/MAX15017), V_{IN_SW} = 4.5V (MAX15015/MAX15016), I_{REG} = 20mA			0.5	V
OSCILLATOR						
Frequency Range	f_{CLK}	V_{SYNC} = 0V, MAX15014/MAX15016	122	136	150	kHz
		V_{SYNC} = 0V, MAX15015/MAX15017	425	500	575	
Maximum Duty Cycle	D_{MAX}	V_{SYNC} = 0V, V_{IN_SW} = 7.5V, MAX15014 (135kHz)	90		98	%
		V_{SYNC} = 0V, V_{IN_SW} = 4.5V, MAX15016 (135kHz)	90		98	
		V_{SYNC} = 0V, V_{IN_SW} = 4.5V, MAX15015 (500kHz)	90		96	
		V_{SYNC} = 0V, V_{IN_SW} = 7.5V, MAX15017 (500kHz)	90		98	
Minimum LX Low Time		V_{SYNC} = 0V	94			ns
SYNC High-Level Voltage			2.2			V
SYNC Low-Level Voltage					0.8	

Electrical Characteristics (continued)

(V_{IN_SW} = V_{IN_LDO} = V_{DRAIN} = 14V, V_{EN_SYS} = V_{EN_SW} = 2.4V, V_{REG} = V_{DVREG}, V_{SYNC} = V_{SET_LDO} = V_{SGND} = V_{PGND} = 0V, C_{REG} = 1µF, C_{IN_SW} = 0.1µF, C_{IN_LDO} = 0.1µF, C_{LDO_OUT} = 10µF, C_{DRAIN} = 0.22µF, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SYNC Frequency Range	f_{SYNC}	MAX15014/MAX15016	100		200	kHz
		MAX15015/MAX15017	400		600	
Ramp Level Shift (Valley)				0.3		V
ERROR AMPLIFER						
Soft-Start Reference Voltage	V_{SS}		1.210	1.235	1.260	V
Soft-Start Current	I_{SS}	V_{SS} = 0V	7	12	17	µA
FB Regulation Voltage	V_{FB}		1.210	1.235	1.260	V
FB Input Range	V_{FB}		0		1.5	V
FB Input Current	I_{FB}	V_{FB} = 1.244V	-250		+250	nA
COMP Voltage Range		I_{COMP} = -500µA to +500µA	0.25		4.5	V
Open-Loop Gain				80		dB
Unity-Gain Bandwidth				1.8		MHz
PWM Modulator Gain		f_{SYNC} = 500kHz, MAX15015/MAX15017		10		V/V
		f_{SYNC} = 135kHz, MAX15014/MAX15016		10		
CURRENT-LIMIT COMPARATOR						
Pulse Skip Threshold	IPFM		100	200	300	mA
Cycle-by-Cycle Current Limit	I_{ILIM}		1.3	2	2.6	A
Number of Consecutive ILIM Events to Hiccup				7		—
Hiccup Timeout				512		Clock periods
POWER SWITCH						
Switch On-Resistance		V_{BST} - V_{LX} = 6V	0.15	0.4	0.80	Ω
Switch Gate Charge		V_{BST} - V_{LX} = 6V		4		nC
Switch Leakage Current		V_{IN_SW} = V_{IN_LDO} = V_{LX} = V_{DRAIN} = 40V, V_{FB} = 0V			10	µA
BST Quiescent Current		V_{BST} = 40V, V_{DRAIN} = 40V, V_{FB} = 0V, DVREG = 5V		400	600	µA
BST Leakage Current		V_{BST} = V_{DRAIN} = V_{LX} = V_{IN_SW} = V_{IN_LDO} = 40V, EN_SW = 0V			1	µA
CHARGE PUMP (MAX15015/MAX15016)						
C- Output Voltage Low		Sinking 10mA			0.1	V
C- Output Voltage High		Relative to DVREG, sourcing 10mA			0.1	V
DVREG to C+ On-Resistance		Sourcing 10mA			10	Ω
LX to PGND On-Resistance		Sinking 10mA			12	Ω
LDO						
Input Voltage Range	V_{IN_LDO}		5		40	V
Undervoltage Lockout Threshold	$UVLO\_LDO_{TH}$	V_{IN_LDO} rising	3.90	4.1	4.25	V

Electrical Characteristics (continued)

(V_{IN_SW} = V_{IN_LDO} = V_{DRAIN} = 14V, V_{EN_SYS} = V_{EN_SW} = 2.4V, V_{REG} = V_{DVREG}, V_{SYNC} = V_{SET_LDO} = V_{SGND} = V_{PGND} = 0V, C_{REG} = 1µF, C_{IN_SW} = 0.1µF, C_{IN_LDO} = 0.1µF, C_{LDO_OUT} = 10µF, C_{DRAIN} = 0.22µF, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Undervoltage Lockout Hysteresis	$UVLO\_LDO_{HYST}$				0.3		V
Output Current	I_{OUT}	V_{IN} = 6V (Note 2)		65		200	mA
Output Voltage	V_{LDO_OUT}	SET_LDO = SGND, MAX1501_A	I_{LDO_OUT} = 100µA	4.90	5	5.06	V
			I_{LDO_OUT} = 1mA	4.90	5	5.06	
			6V ≤ V_{IN_LDO} ≤ 40V, I_{LDO_OUT} = 1mA	4.85	5	5.15	
			1mA ≤ I_{OUT} ≤ 50mA, V_{IN_LDO} = 14V	4.85	5	5.15	
		SET_LDO = SGND, MAX1501_B	I_{LDO_OUT} = 100µA	3.22	3.3	3.35	
			I_{LDO_OUT} = 1mA	3.22	3.3	3.35	
			6V ≤ V_{IN_LDO} ≤ 40V, I_{LDO_OUT} = 1mA	3.2	3.3	3.4	
			1mA ≤ I_{LDO_OUT} ≤ 50mA, V_{IN_LDO} = 14V	3.2	3.3	3.4	
Adjustable Output Voltage Range	V_{ADJ}	V_{SET_LDO} ≥ 0.25V		1.5		11.0	V
Dropout Voltage	ΔV_{DO}	V_{IN_LDO} = 5V, MAX1501_A	I_{OUT} = 10mA			0.6	V
			I_{OUT} = 50mA			0.82	
		V_{IN_LDO} = 4.0V, MAX1501_B	I_{OUT} = 10mA			0.1	
			I_{OUT} = 50mA			0.4	
Startup Response Time		From EN_SYS high to LDO_OUT rise, R_L = 500Ω, SET_LDO = SGND			400		µs
SET_LDO Reference Voltage	V_{SET_LDO}			1.220	1.241	1.265	V
Minimum SET_LDO Threshold		(Note 3)			185		mV
SET_LDO Input Leakage Current	I_{SET_LDO}	V_{SET_LDO} = 11V			0.5	100	nA
Power-Supply Rejection Ratio	PSRR	I_{OUT} = 10mA, f = 100Hz, 500mV_{P-P}, V_{LDO_OUT} = 5V			78		dB
		I_{OUT} = 10mA, f = 1MHz, 500mV_{P-P}, V_{LDO_OUT} = 5V			24		
Short-Circuit Current	I_{SC}			125	185	300	mA

Electrical Characteristics (continued)

(V_{IN_SW} = V_{IN_LDO} = V_{DRAIN} = 14V, V_{EN_SYS} = V_{EN_SW} = 2.4V, V_{REG} = V_{DVREG}, V_{SYNC} = V_{SET_LDO} = V_{SGND} = V_{PGND} = 0V, C_{REG} = 1µF, C_{IN_SW} = 0.1µF, C_{IN_LDO} = 0.1µF, C_{LDO_OUT} = 10µF, C_{DRAIN} = 0.22µF, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

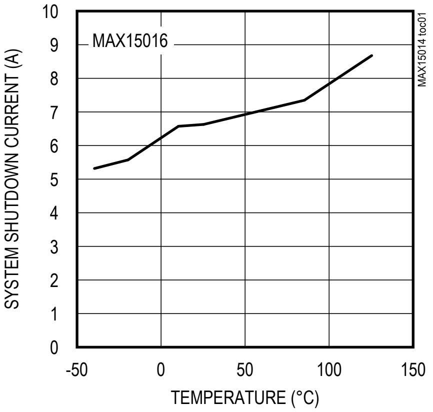
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{\text{RESET}}$ OUTPUT						
$\overline{\text{RESET}}$ Threshold	$V_{\overline{RESET}}$	$\overline{\text{RESET}}$ goes high after rising V_{LDO_OUT} crosses this threshold	90	92.5	95	%V_{OUT}
$\overline{\text{RESET}}$ Output Low Voltage	V_{RL}	(V_{LDO_OUT} – $V_{\overline{RESET}}$) / $I_{\overline{RESET}}$ = 4kΩ			0.4	V
$\overline{\text{RESET}}$ Output High Leakage Current	I_{RH}	$V_{\overline{RESET}}$ = 3.3V (For MAX15_ _ _B), $V_{\overline{RESET}}$ = 5V (For MAX15_ _ _A)			1	µA
$\overline{\text{RESET}}$ Output Minimum Timeout Period		When LDO_OUT reaches $\overline{\text{RESET}}$ threshold, CT = unconnected		50		µs
ENABLE to $\overline{\text{RESET}}$ Minimum Timeout Period		When EN_SYS goes high, C_{LDO_OUT} = 10µF, I_{LDO_OUT} = 50mA, V_{LDO_OUT} = 3.3V, CT = unconnected		650		µs
Delay Comparator Threshold (Rising)	V_{CT-TH}		1.220	1.241	1.265	V
Delay Comparator Threshold Hysteresis	$V_{CTTH-HYST}$			100		mV
CT Charge Current	I_{CT-CHQ}	V_{CT} = 0V	1.5	2	3	µA
CT Discharge Current	I_{CT-DIS}			18		mA
THERMAL SHUTDOWN						
Thermal Shutdown Temperature		Temperature rising		+160		°C
Thermal Shutdown Hysteresis				20		°C

Note 1: Limits at -40°C are guaranteed by design and not production tested.
Note 2: Maximum output current is limited by package power dissipation.
Note 3: This is the minimum voltage needed at SET_LDO for the system to recognize that the user wants an adjustable LDO_OUT.

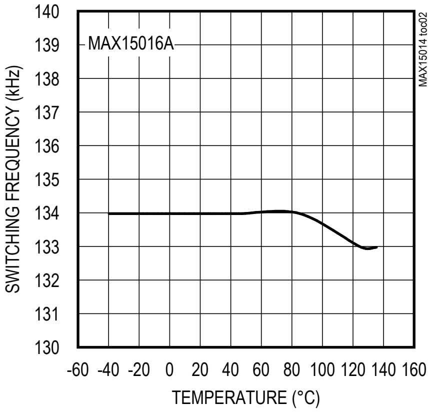
Typical Operating Characteristics

($V_{IN\_SW} = V_{IN\_LDO} = V_{DRAIN} = 14V$, $V_{EN\_SYS} = V_{EN\_SW} = 2.4V$, $V_{REG} = V_{DVREG}$, $V_{SYNC} = V_{SET\_LDO} = V_{SGND} = V_{PGND} = 0V$, $C_{REG} = 1\mu F$, $C_{IN\_SW} = 0.1\mu F$, $C_{IN\_LDO} = 0.1\mu F$, $C_{LDO\_OUT} = 10\mu F$, $C_{DRAIN} = 0.22\mu F$, see Figures 6 and 7, $T_A = +25°C$, unless otherwise noted.)

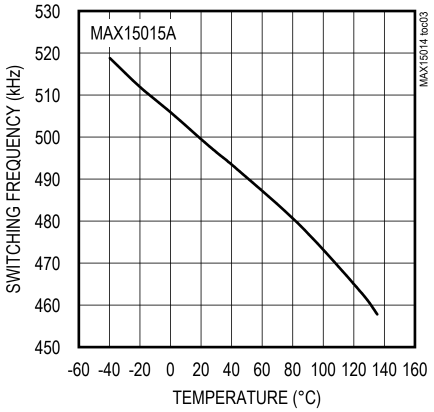
SYSTEM SHUTDOWN CURRENT vs. TEMPERATURE



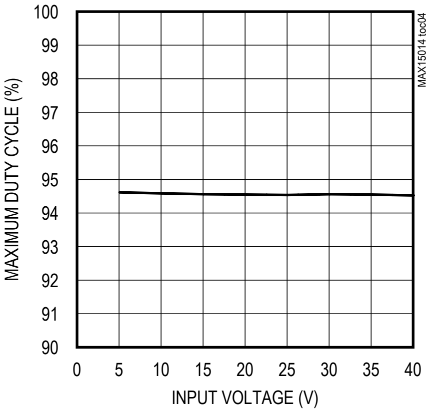
SWITCHING FREQUENCY vs. TEMPERATURE



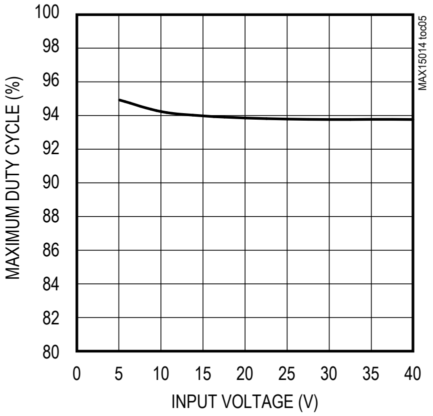
SWITCHING FREQUENCY vs. TEMPERATURE



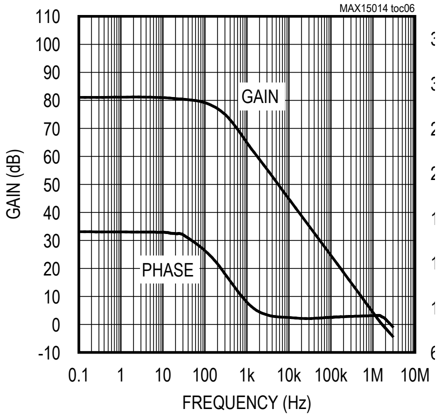
MAXIMUM DUTY CYCLE vs. INPUT VOLTAGE (MAX15016A)



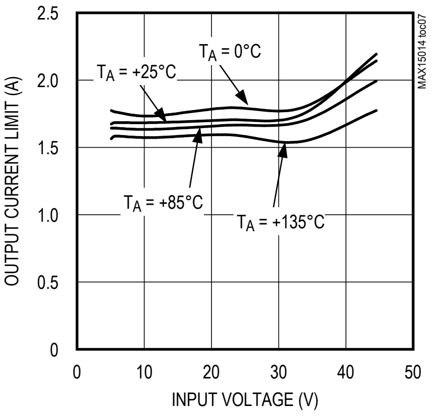
MAXIMUM DUTY CYCLE vs. INPUT VOLTAGE (MAX15015A)



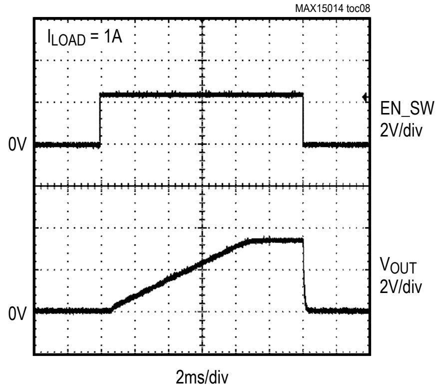
ERROR AMPLIFIER OPEN-LOOP GAIN AND PHASE vs. FREQUENCY



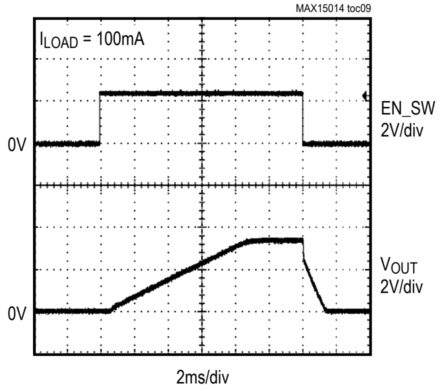
OUTPUT CURRENT LIMIT vs. INPUT VOLTAGE



TURN-ON/-OFF WAVEFORM



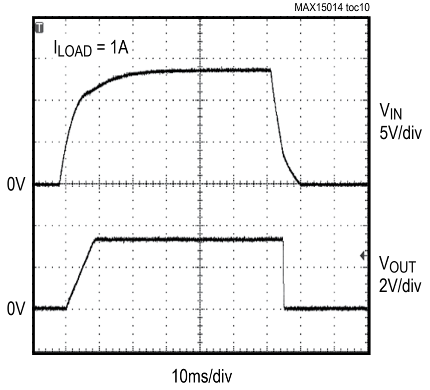
TURN-ON/-OFF WAVEFORM



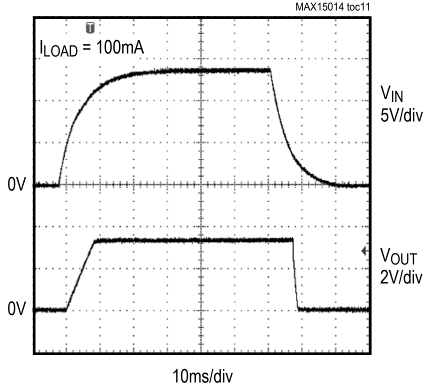
Typical Operating Characteristics (continued)

(V_{IN_SW} = V_{IN_LDO} = V_{DRAIN} =14V, V_{EN_SYS} = V_{EN_SW} = 2.4V, V_{REG} = V_{DVREG}, V_{SYNC} = V_{SET_LDO} = V_{SGND} = V_{PGND} = 0V, C_{REG} = 1µF, C_{IN_SW} = 0.1µF, C_{IN_LDO} = 0.1µF, C_{LDO_OUT} = 10µF, C_{DRAIN} = 0.22µF, see Figures 6 and 7, T_A = +25°C, unless otherwise noted.)

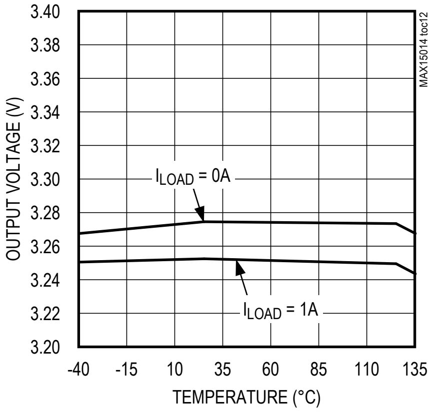
TURN-ON/-OFF WAVEFORM
INCREASING V_{IN}



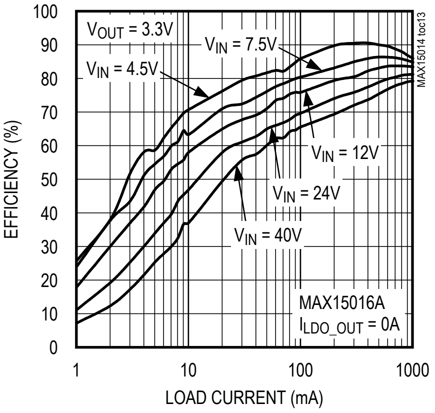
TURN-ON/-OFF WAVEFORM
INCREASING V_{IN}



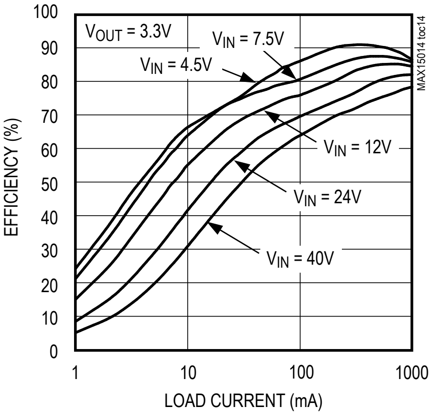
OUTPUT VOLTAGE vs. TEMPERATURE



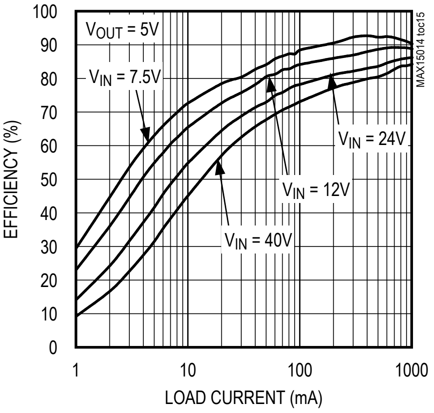
EFFICIENCY vs. LOAD CURRENT



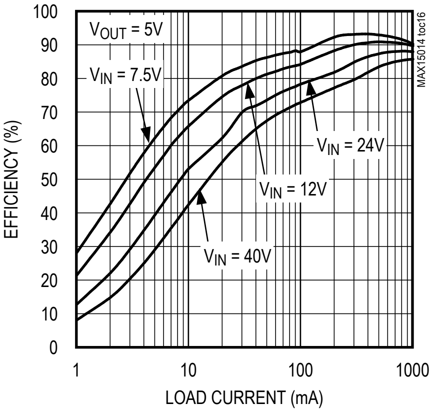
EFFICIENCY vs. LOAD CURRENT
(MAX15015A)



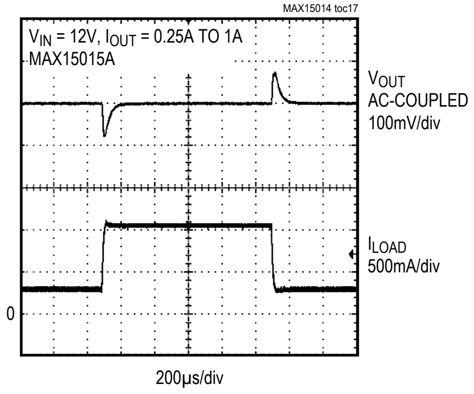
EFFICIENCY vs. LOAD CURRENT
(MAX15014)



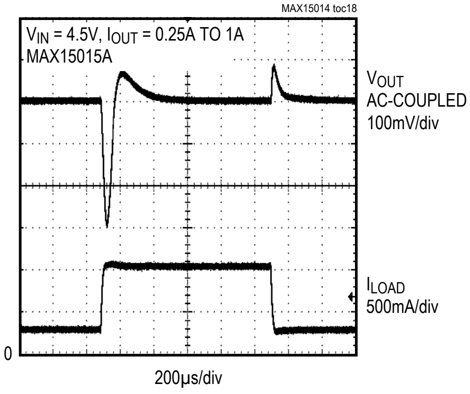
EFFICIENCY vs. LOAD CURRENT
(MAX15017A)



LOAD-TRANSIENT RESPONSE



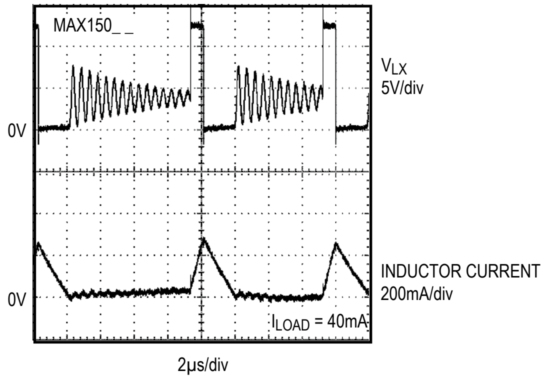
LOAD-TRANSIENT RESPONSE



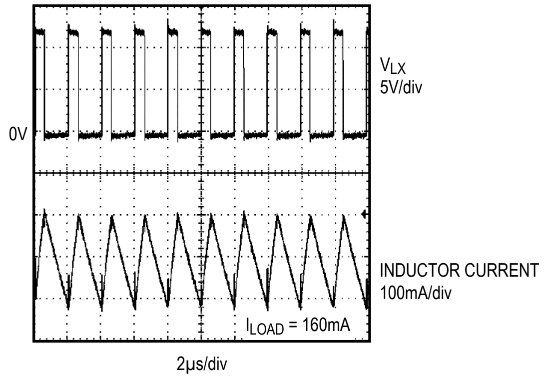
Typical Operating Characteristics (continued)

(V_{IN_SW} = V_{IN_LDO} = V_{DRAIN} =14V, V_{EN_SYS} = V_{EN_SW} = 2.4V, V_{REG} = V_{DVREG}, V_{SYNC} = V_{SET_LDO} = V_{SGND} = V_{PGND} = 0V, C_{REG} = 1µF, C_{IN_SW} = 0.1µF, C_{IN_LDO} = 0.1µF, C_{LDO_OUT} = 10µF, C_{DRAIN} = 0.22µF, see Figures 6 and 7, T_A = +25°C, unless otherwise noted.)

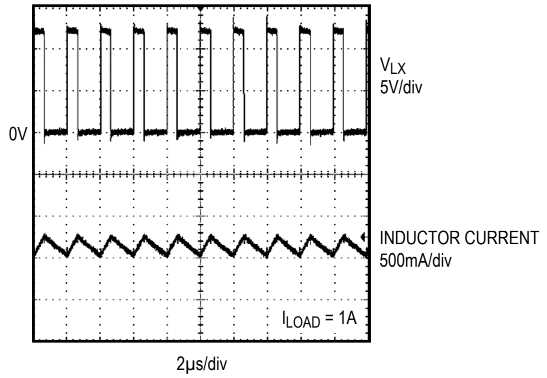
LX VOLTAGE AND INDUCTOR CURRENT



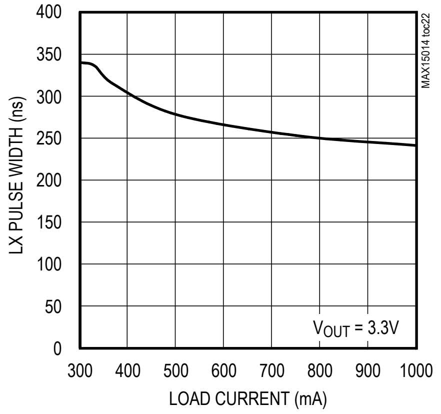
LX VOLTAGE AND INDUCTOR CURRENT



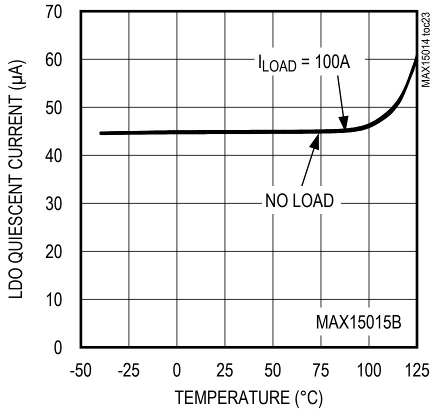
LX VOLTAGE AND INDUCTOR CURRENT



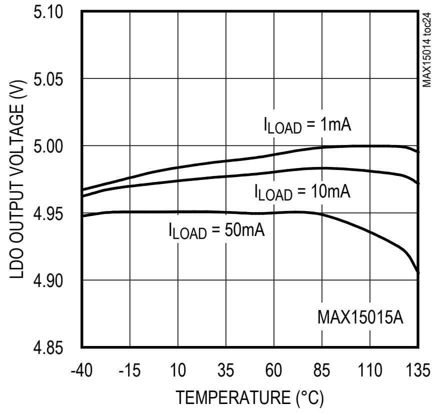
MINIMUM LX PULSE WIDTH vs. LOAD CURRENT



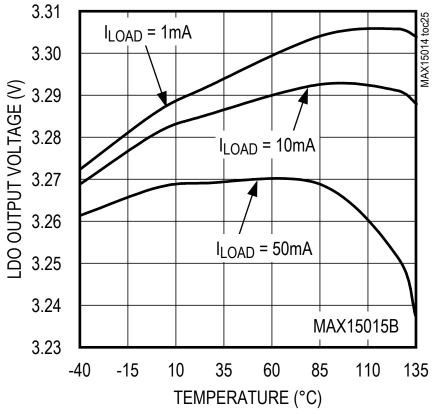
LDO QUIESCENT CURRENT vs. TEMPERATURE



OUTPUT VOLTAGE vs. TEMPERATURE

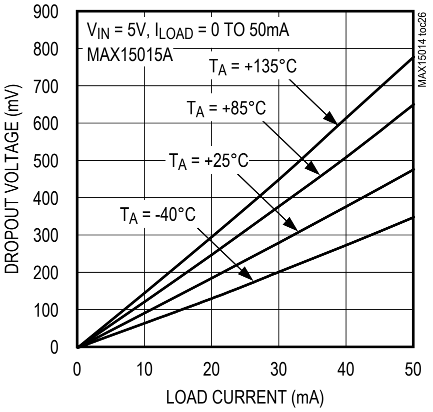


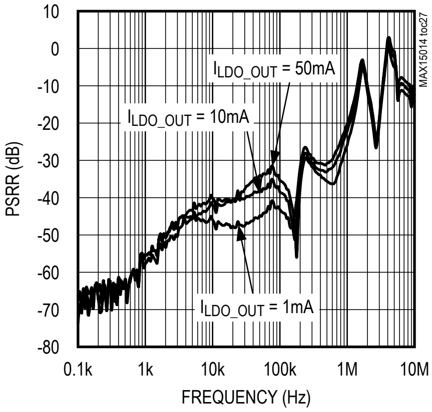
OUTPUT VOLTAGE vs. TEMPERATURE

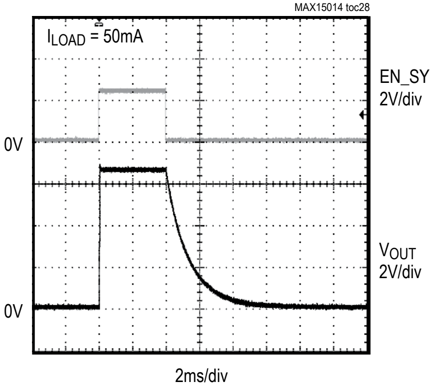


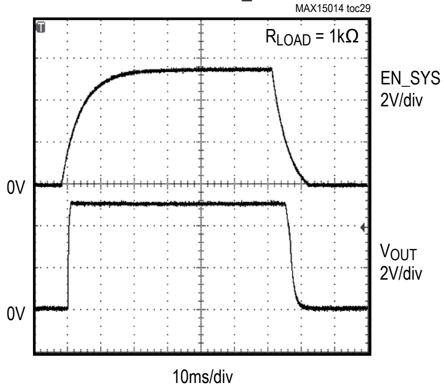
Typical Operating Characteristics (continued)

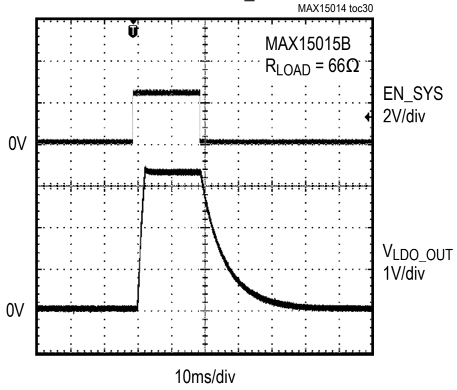
(V_{IN_SW} = V_{IN_LDO} = V_{DRAIN} =14V, V_{EN_SYS} = V_{EN_SW} = 2.4V, V_{REG} = V_{DVREG}, V_{SYNC} = V_{SET_LDO} = V_{SGND} = V_{PGND} = 0V, C_{REG} = 1µF, C_{IN_SW} = 0.1µF, C_{IN_LDO} = 0.1µF, C_{LDO_OUT} = 10µF, C_{DRAIN} = 0.22µF, see Figures 6 and 7, T_A = +25°C, unless otherwise noted.)

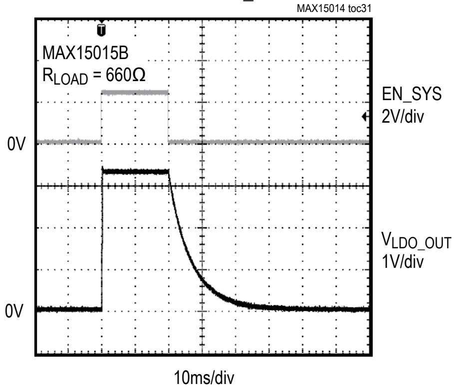

DROPOUT VOLTAGE vs. LOAD CURRENT

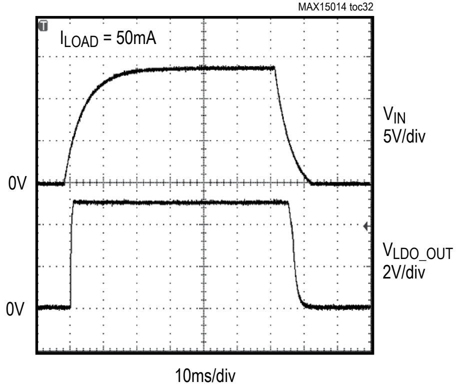

POWER-SUPPLY REJECTION RATIO


TURN-ON/-OFF WAVEFORM
TOGGLING EN_SYS


TURN-ON/-OFF WAVEFORM
TOGGLING EN_SYS


TURN-ON/-OFF WAVEFORM
TOGGLING EN_SYS

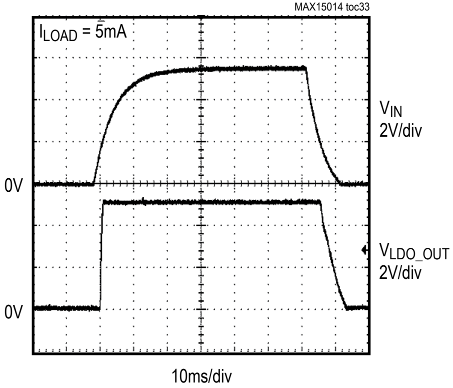

TURN-ON/-OFF WAVEFORM
TOGGLING EN_SYS


TURN-ON/-OFF WAVEFORM
INCREASING V_{IN}

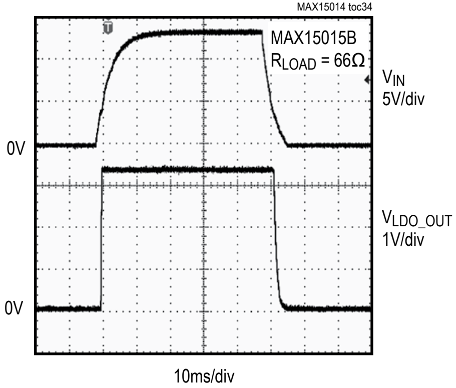
Typical Operating Characteristics (continued)

(V_{IN_SW} = V_{IN_LDO} = V_{DRAIN} =14V, V_{EN_SYS} = V_{EN_SW} = 2.4V, V_{REG} = V_{DVREG}, V_{SYNC} = V_{SET_LDO} = V_{SGND} = V_{PGND} = 0V, C_{REG} = 1µF, C_{IN_SW} = 0.1µF, C_{IN_LDO} = 0.1µF, C_{LDO_OUT} = 10µF, C_{DRAIN} = 0.22µF, see Figures 6 and 7, T_A = +25°C, unless otherwise noted.)

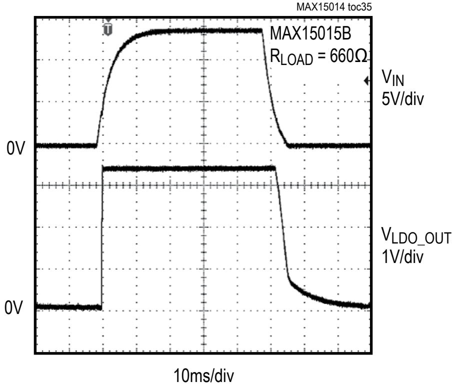
LDO TURN-ON/-OFF WAVEFORM WITH INCREASING V_{IN}



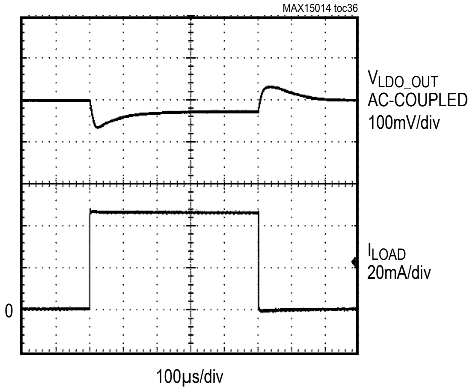
TURN-ON/-OFF WAVEFORM INCREASING V_{IN}



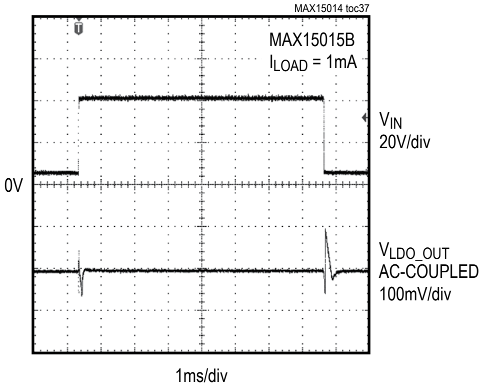
TURN-ON/-OFF WAVEFORM INCREASING V_{IN}



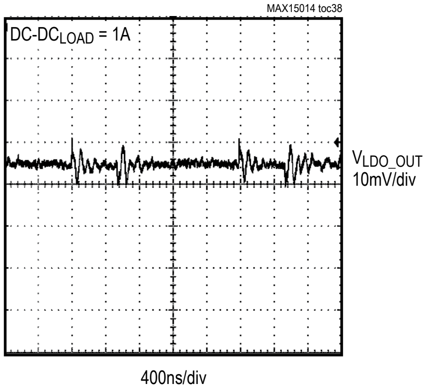
LOAD-TRANSIENT RESPONSE



INPUT-VOLTAGE STEP RESPONSE



RESIDUAL SWITCHING NOISE ON THE LDO OUTPUT



Pin Description

PIN		NAME	FUNCTION
MAX15014/ MAX15017	MAX15015/ MAX15016		
1–3, 9, 12, 14, 16, 19, 24, 26, 27, 30, 35	1–3, 9, 12, 14, 16, 19, 24, 26, 27, 30, 35	N.C.	No Connection. Not internally connected. Leave unconnected or connect to SGND.
23, 28	—	I.C.	Internally Connected. Leave unconnected.
4	4	$\overline{\text{RESET}}$	Active-Low Reset Output. When the rising V_{LDO_OUT} voltage crosses the reset threshold, $\overline{\text{RESET}}$ goes high after an adjustable delay. Pull up $\overline{\text{RESET}}$ to LDO_OUT with at least 4kΩ. $\overline{\text{RESET}}$ is an active-low open-drain output.
5	5	SGND	Signal Ground Connection. Connect SGND and PGND together at one point near the input bypass capacitor negative terminal.
6	6	CT	Reset Timeout Delay Capacitor Connection. CT is pulled low during reset. When out of reset, CT is pulled up to an internal 3.6V rail with a 2µA current source. When the rising CT voltage reaches the trip threshold (typically 1.24V), $\overline{\text{RESET}}$ is deasserted. When EN_SYS is low or in thermal shutdown, CT is low.
7	7	EN_SW	Switching Regulator Enable Input (Active High). If EN_SW is high and EN_SYS is high, the switching power supply is enabled. EN_SW is internally pulled down to SGND through a 0.5µA current sink.
8	8	EN_SYS	Active-High System Enable Input. Connect EN_SYS high to turn on the system. The LDO is active if EN_SYS is high; once EN_SYS is high, the switching regulator can be turned on if EN_SW is high. EN_SYS is internally pulled down to SGND through a 0.5µA current sink.
10	10	SET_LDO	LDO Feedback Input/Output Voltage Setting. Connect SET_LDO to SGND to select the preset output voltage (5V or 3.3V). Connect SET_LDO to an external resistor-divider network for adjustable output operation.
11	11	LDO_OUT	Linear Regulator Output. Bypass with at least 10µF low-ESR capacitor from LDO_OUT to SGND. In the 5V LDO versions (A), the LDO operates in dropout below 6V down to the UVLO trip point.
13	13	IN_LDO	LDO Input Voltage. The input voltage range for the LDO extends from 5V to 40V. Bypass with a 0.1µF ceramic capacitor to SGND.
15	15	BST	High-Side Gate Driver Supply. Connect BST to the cathode of the bootstrap diode and to the positive terminal of the bootstrap capacitor.
17, 18	17, 18	LX	Source Connection of Internal High-Side Switch. Connect both LX pins to the inductor and the cathode of the freewheeling diode.
20, 21	20, 21	DRAIN	Drain Connection of the Internal High-Side Switch. Connect both DRAIN inputs together.
22	22	PGND	Power Ground Connection. Connect the input bypass capacitor negative terminal, the anode of the freewheeling diode, and the output filter capacitor negative terminal to PGND. Connect PGND to SGND together at a single point near the input bypass capacitor negative terminal.

Pin Description (continued)

PIN		NAME	FUNCTION
MAX15014/ MAX15017	**MAX15015/ MAX15016**		
—	23	C-	Charge-Pump Flying Capacitor Negative Connection (MAX15015/MAX15016 only)
25	25	DVREG	Gate Drive Supply for the High-Side MOSFET Driver. Connect to REG and to the anode of the bootstrap diode for MAX15014/MAX15017. Connect to REG for MAX15015/MAX15016.
—	28	C+	Charge-Pump Flying Capacitor Positive Connection (MAX15015/MAX15016 only). Connect to the positive terminal of the external pump capacitor and to the anode of the bootstrap diode.
29	29	SYNC	Oscillator Synchronization Input. SYNC can be driven by an external clock to synchronize the switching frequency. Connect SYNC to SGND when not used.
31	31	COMP	Error Amplifier Output. Connect COMP to the compensation feedback network.
32	32	FB	Feedback Regulation Point. Connect to the center tap of a resistive divider from converter output to SGND to set the output voltage. The FB voltage regulates to the voltage present at SS (1.235V).
33	33	SS	Soft-Start and Reference Output. Connect a capacitor from SS to SGND to set the soft-start time. See the *Applications Information* section to calculate the value of the C_{SS} capacitor.
34	34	REG	Internal Regulator Output. 5V output for the MAX15015/MAX15016 and 8V output for the MAX15014/MAX15017. Bypass to SGND with at least a 1µF ceramic capacitor.
36	36	IN_SW	Supply Input Connection. Connect to IN_LDO and an external voltage source from 4.5V to 40V. EN_SW and EN_SYS must be high and IN_SW must be above its UVLO threshold for operation of the switching regulator.
—	—	EP	Exposed Pad. The exposed pad must be electrically connected to SGND. For an effective heatsinking, solder the exposed pad to a large copper plane.

Detailed Description

The MAX15014–MAX15017 combine a voltage-mode buck converter with an internal 0.5Ω power-MOSFET switch and a low-quiescent-current LDO regulator. The buck converter of the MAX15015/MAX15016 has a wide input voltage range of 4.5V to 40V. The MAX15014/MAX15017's input voltage range is 7.5V to 40V. Fixed switching frequencies of 135kHz and 500kHz are available. The internal low R_{DS_ON} switch allows for up to 1A of output current, and the output voltage can be adjusted from 1.26V to 32V. External compensation and voltage feed-forward simplify loop-compensation design and allow for a wide variety of L and C filter components. All devices offer an automatic switchover to pulse-skipping (PFM) mode, providing low-quiescent current and high efficiency at light loads. Under no load, PFM mode operation reduces the current consumption to 5.6mA for the MAX15014/MAX15017 and 8.6mA for the MAX15015/MAX15016. In shutdown (DC-DC and LDO regulator off), the supply current falls to 6µA. Additional features include a programmable soft-start, cycle-by-cycle current limit, hiccup-mode output short-circuit protection, and thermal shutdown.

The LDO linear regulator operates from 5V to 40V and delivers a guaranteed 50mA load current. The devices feature a preset output voltage of 5.0V (MAX1501_A) or 3.3V (MAX1501_B). Alternatively, the output voltage can be adjusted from 1.5V to 11V using an external resistive divider. The LDO section also features a $\overline{\text{RESET}}$ output with adjustable timeout period.

Enable Inputs and UVLO

The MAX15014–MAX15017 feature two logic inputs, EN_SW (active-high) and EN_SYS (active-high) that can be used to enable the switching power supply and the LDO_OUT outputs. When V_{EN_SW} is higher than the threshold and EN_SYS is high, the switching power supply is enabled. When EN_SYS is high, the LDO is

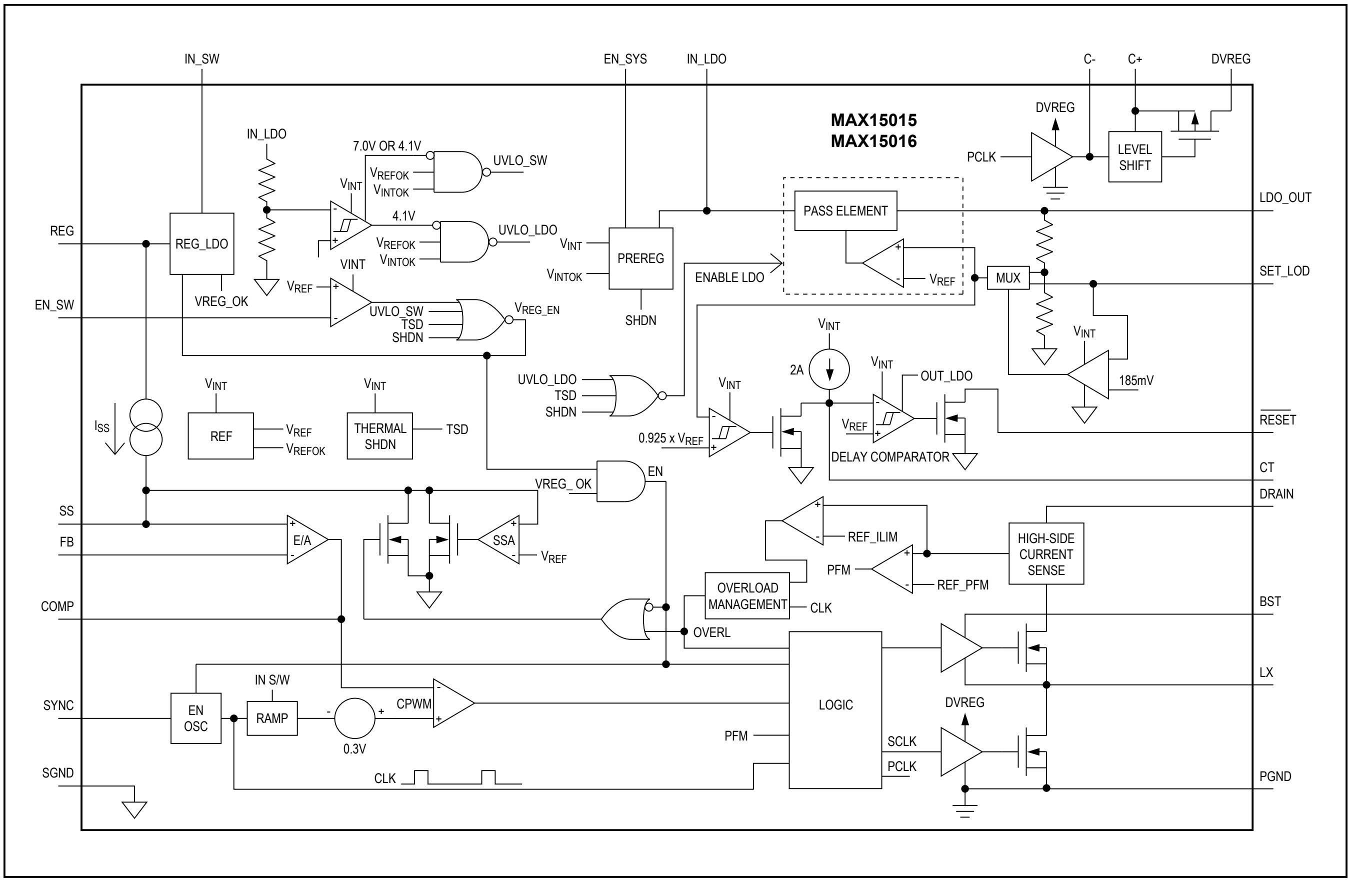


Figure 1. MAX15015/MAX15016 Simplified Block Diagram

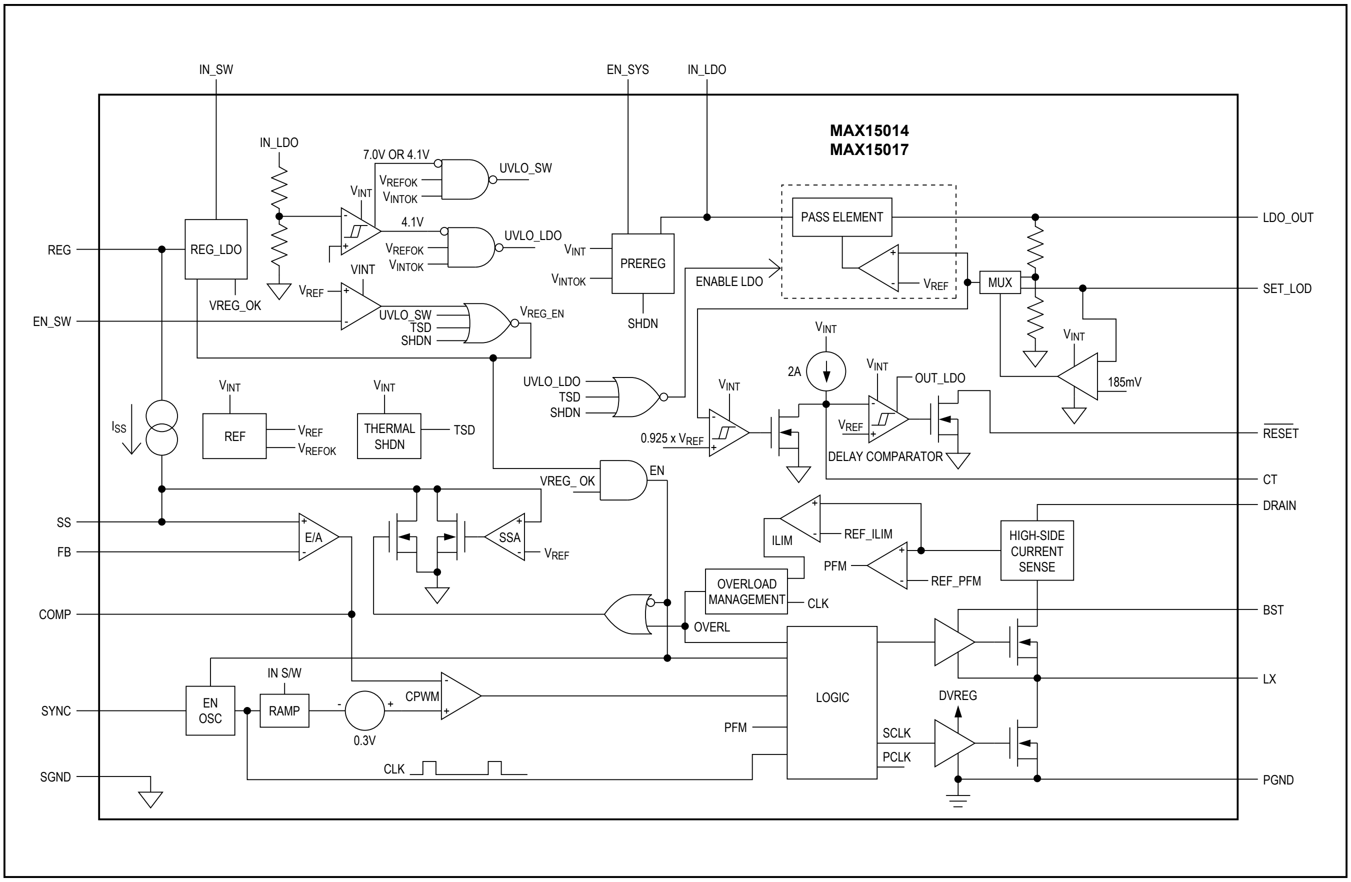


Figure 2. MAX15014/MAX15017 Simplified Block Diagram

Table 1. Enable Inputs Configuration

EN_SYS	EN_SW	LDO REGULATOR	DC-DC SWITCHING CONVERTER
Low	Low	Off	Off
Low	High	Off	Off
High	Low	On	Off
High	High	On	On

active. When EN_SYS is low, the entire chip is off (see Table 1).

The MAX15014–MAX15017 provide undervoltage lockout (UVLO). The UVLO monitors the input voltage (V_{IN_LDO}) and is fixed at 4.1V (MAX15015/MAX15016) or 7V (MAX15014/MAX15017).

Internal Linear Regulator (REG)

REG is the output terminal of a 5V (MAX15015/MAX15016), or 8V (MAX15014/MAX15017) LDO that is powered from IN_SW and provides power to the IC. Connect REG externally to DVREG to provide power for the high-side MOSFET gate driver. Bypass REG to SGND with a ceramic capacitor (C_{REG}) of at least 1µF. Place the capacitor physically close to the MAX15014–MAX15017 to provide good bypassing. During normal operation, REG is intended for powering up only the internal circuitry and should not be used to supply power to external loads.

Soft-Start and Reference (SS)

SS is the 1.235V reference bypass connection for the MAX15014–MAX15017 and also controls the soft-start period. At startup, after input voltage is applied at IN_SW, IN_LDO and the UVLO thresholds are reached, the device enters soft-start. During soft-start, 14µA is sourced into the capacitor (C_{SS}) connected from SS to SGND causing the reference voltage to ramp up slowly. When V_{SS} reaches 1.244V, the output becomes fully active. Set the soft-start time (t_{SS}) using following equation:

$$t_{SS} = \frac{V_{SS} \times C_{SS}}{I_{SS}}$$

where V_{SS} = soft-start reference voltage = 1.235V (typ), I_{SS} = soft-start current = 14 x 10^{-6}A (typ), t_{SS} is in seconds and C_{SS} is in Farads.

Internal Charge Pump (MAX15015/MAX15016)

The MAX15015/MAX15016 feature an internal charge pump to enhance the turn-on of the internal MOSFET, allowing for operation with input voltages down to 4.5V. Connect a flying capacitor (C_F) between C+ and C-, a boost diode from C+ to BST, as well as a bootstrap capacitor (C_{BST}) between BST and LX to provide the gate-drive voltage for the high-side n-channel DMOS switch. During the on-time, the flying capacitor is charged to V_{DVREG}. During the off-time, the positive terminal of the flying capacitor (C+) is pumped to two times V_{DVREG}, and charge is dumped onto C_{BST} to provide twice the regulator voltage across the high-side DMOS driver. Use a ceramic capacitor of at least 0.1µF for C_{BST} and C_F, located as close as possible to the device.

Gate-Drive Supply (DVREG)

DVREG is the supply input for the internal high-side MOSFET driver. The power for DVREG is derived from the output of the internal regulator (REG). Connect DVREG to REG externally. To filter the switching noise, the use of an RC filter (1Ω and 0.47µF) from REG to DVREG is recommended. In the MAX15015/MAX15016, the high-side drive supply is generated using the internal charge pump along with the bootstrap diode and capacitor. In the MAX15014/MAX15017, the high-side MOSFET driver supply is generated using only the bootstrap diode and capacitor.

Error Amplifier

The output of the internal error amplifier (COMP) is available for frequency compensation (see the *Compensation Design* section). The inverting input is FB, the noninverting input SS, and the output COMP. The error amplifier has an 80dB open-loop gain and a 1.8MHz GBW product. See the *Typical Operating Characteristics* for the Gain and Phase vs. Frequency graph.

Oscillator/Synchronization Input (SYNC)

With SYNC connected to SGND, the MAX15014–MAX15017 use their internal oscillator and switch at a fixed frequency of 135kHz and 500kHz. The MAX15014/MAX15016 are the 135kHz options and MAX15015/MAX15017 are the 500kHz options. For external synchronization, drive SYNC with an external clock from 400kHz to 600kHz (MAX15015/MAX15017), or 100kHz to 200kHz (MAX15014/MAX15016). When driven with an external clock, the device synchronizes to the rising edge of SYNC.

PWM Comparator/Voltage Feed-Forward

An internal ramp generator clocked by the internal oscillator is compared against the output of the error amplifier to generate the PWM signal. The maximum amplitude of the ramp (V_{RAMP}) automatically adjusts to compensate for input voltage and oscillator frequency changes. This causes the V_{IN_SW}/V_{RAMP} to be a constant 10V/V across the input voltage range of 4.5V to 40V (MAX15015/MAX15016), or 7.5V to 40V (MAX15014/MAX15017), and the SYNC frequency range of 400kHz to 600kHz (MAX15015/MAX15017), or 100kHz to 200kHz (MAX15014/MAX15016).

Output Short-Circuit Protection (Hiccup Mode)

The MAX15014–MAX15017 protect against an output short circuit by utilizing hiccup-mode protection. In hiccup mode, a series of sequential cycle-by-cycle current-limit events cause the part to shut down and restart with a soft-start sequence. This allows the device to operate with a continuous output short circuit.

During normal operation, the current is monitored at the drain of the internal power MOSFET. When the current limit is exceeded, the internal power MOSFET turns off until the next on-cycle and a counter increments. If the counter counts seven consecutive current-limit events, the device discharges the soft-start capacitor and shuts down for 512 clock periods before restarting with a soft-start sequence. Each time the power MOSFET turns on and the device does not exceed the current limit, the counter is reset.

LDO Regulator

The LDO regulator operates over an input voltage from 5V to 40V, and can be enabled independently of the DC-DC converter section. Its quiescent current is as low as 47μA with a load current of 100μA. All devices feature a preset output voltage of 5V (MAX1501_A) or 3.3V (MAX1501_B). Alternatively, the output voltage can be adjusted using an external resistive-divider network connected between LDO_OUT, SET_LDO, and SGND. See Figure 5.

$\overline{\text{RESET}}$ Output

The $\overline{\text{RESET}}$ output is typically connected to the reset input of a microprocessor (μP). A μP's reset input starts or restarts the μP in a known state. The MAX15014–MAX15017 supervisory circuits provide the reset logic to prevent code-execution errors during power-up, power-down, and brownout conditions. $\overline{\text{RESET}}$ changes from high to low whenever the monitored voltage drops below the $\overline{\text{RESET}}$ threshold voltage. Once the monitored voltage exceeds its respective $\overline{\text{RESET}}$ threshold voltage(s), $\overline{\text{RESET}}$ remains low for the $\overline{\text{RESET}}$ timeout period, then goes high. The $\overline{\text{RESET}}$ timeout period is adjustable with an external capacitor (C_{CT}) connected to CT.

Thermal-Shutdown Protection

The MAX15014–MAX15017 feature thermal-shutdown protection that limits the total power dissipation in the device and protects it in the event of an extended thermal-fault condition. When the die temperature exceeds +160°C, an internal thermal sensor shuts down the part, turning off the DC-DC converter and the LDO regulator, and allowing the IC to cool. After the die temperature falls by 20°C, the part restarts with a soft-start sequence.

Applications Information

Setting the Output Voltage

Connect a resistive divider (R3 and R4, see Figures 6 and 7) from OUT to FB to SGND to set the output voltage. Choose R3 and R4 so that DC errors due to the FB input bias current do not affect the output-voltage setting precision. For the most common output-voltage settings (3.3V or 5V), R3 values in the 10kΩ range are adequate. Select R3 first and calculate R4 using the following equation:

$$R4 = \frac{R3}{\left[\frac{V_{OUT}}{V_{FB}} - 1\right]}$$

where V_{FB} = 1.235V.

Inductor Selection

Three key inductor parameters must be specified for operation with the MAX15014–MAX15017: inductance value (L), peak inductor current (I_{PEAK}), and inductor saturation current (I_{SAT}). The minimum required inductance is a function of operating frequency, input-to-output voltage differential, and the peak-to-peak inductor current (ΔI_{P-P}). Higher ΔI_{P-P} allows for a lower inductor value, while a lower ΔI_{P-P} requires a higher inductor value. A lower inductor value minimizes size and cost and improves large-signal and transient response, but reduces efficiency due to higher peak currents and higher peak-to-peak output-voltage ripple for the same output capacitor. On the other hand, higher inductance increases efficiency by reducing the ΔI_{P-P}. Resistive losses due to extra wire turns can exceed the benefit gained from lower ΔI_{P-P} levels, especially when the inductance is increased without also allowing for larger inductor dimensions. A good compromise is to choose ΔI_{P-P} equal to 40% of the full load current. Calculate the inductor using the following equation:

$$L = \frac{V_{OUT}(V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times \Delta I_{P-P}}$$

V_{IN} and V_{OUT} are typical values so that efficiency is optimum for typical conditions. The switching frequency (f_{SW}) is internally fixed at 135kHz (MAX15014/MAX15016) or 500kHz (MAX15015/MAX15017) and can vary when synchronized to an external clock (see the *Oscillator/Synchronization Input (SYNC)* section). The ΔI_{P-P}, which reflects the peak-to-peak output ripple, is worst at the maximum input voltage. See the *Output Capacitor Selection* section to verify that the worst-case output ripple is acceptable. The inductor current (I_{SAT}) is also important to avoid current runaway during continuous output short circuit. Select an inductor with an I_{SAT} specification higher than the maximum peak current limit of 2.6A.

Input Capacitor Selection

The discontinuous input current of the buck converter causes large input ripple currents and therefore the input capacitor must be carefully chosen to keep the input voltage ripple within design requirements. The input voltage ripple is comprised of ΔV_Q (caused by the capacitor discharge) and ΔV_{ESR} (caused by the ESR of the input capacitor). The total voltage ripple is the sum of ΔV_Q and ΔV_{ESR}. Calculate the input capacitance and ESR required for a specified ripple using the following equations:

$$ESR = \frac{\Delta V_{ESR}}{I_{OUT\_MAX} + \frac{\Delta I_{P-P}}{2}}$$

$$C_{IN} = \frac{I_{OUT\_MAX} \times D}{\Delta V_Q \times f_{SW}}$$

where C_{IN} is the sum of C_{DRAIN} and additional decoupling capacitance at the buck converter input,

$$\Delta I_{P-P} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN} \times f_{SW} \times L} \text{ and}$$

$$D = \frac{V_{OUT}}{V_{IN}}$$

I_{OUT_MAX} is the maximum output current, D is the duty cycle, and f_{SW} is the switching frequency.

The MAX15014–MAX15017 include UVLO hysteresis and soft-start to avoid chattering during turn-on. However, use additional bulk capacitance if the input source impedance is high. Use enough input capacitance at lower input voltages to avoid possible undershoot below the undervoltage-lockout threshold during transient loading.

Output Capacitor Selection

The allowable output-voltage ripple and the maximum deviation of the output voltage during load steps determine the output capacitance (C_{OUT}) and its equivalent series resistance (ESR). The output ripple is mainly composed of ΔV_Q (caused by the capacitor discharge) and ΔV_{ESR} (caused by the voltage drop across the ESR of the output capacitor). The equations for calculating the peak-to-peak output-voltage ripple are:

$$\Delta V_Q = \frac{\Delta I_{P-P}}{8 \times C_{OUT} \times f_{SW}}$$

$$\Delta V_{ESR} = ESR \times \Delta I_{P-P}$$

Normally, a good approximation of the output-voltage ripple is $\Delta V_{RIPPLE} = \Delta V_{ESR} + \Delta V_Q$. If using ceramic capacitors, assume the contribution to the output-voltage ripple from ESR and the capacitor discharge to be equal to 20% and 80%, respectively. ΔI_{P-P} is the peak-to-peak inductor current (see the *Input Capacitor Selection* section) and f_{SW} is the converter's switching frequency.

The allowable deviation of the output voltage during fast-load transients also determines the output capacitance, its ESR, and its equivalent series inductance (ESL). The output capacitor supplies the load current during a load step until the controller responds with a greater duty cycle. The response time ($t_{RESPONSE}$) depends on the closed-loop bandwidth of the converter (see the *Compensation Design* section). The resistive drop across the output capacitor's ESR, the drop across the capacitor's ESL (ΔV_{ESL}), and the capacitor discharge causes a voltage droop during the load step.

Use a combination of low-ESR tantalum/aluminum electrolytic and ceramic capacitors for better transient load and voltage-ripple performance. Non-leaded capacitors and capacitors in parallel help reduce the ESL. Keep the maximum output-voltage deviation below the tolerable limits of the electronics being powered. Use the following equations to calculate the required ESR, ESL, and capacitance value during a load step:

$$ESR = \frac{\Delta V_{ESR}}{I_{STEP}}$$

$$C_{OUT} = \frac{I_{STEP} \times t_{RESPONSE}}{\Delta V_Q}$$

$$ESL = \frac{\Delta V_{ESL} \times t_{STEP}}{I_{STEP}}$$

$$t_{RESPONSE} \cong \frac{1}{3 f_C}$$

where I_{STEP} is the load step, t_{STEP} is the rise time of the load step, $t_{RESPONSE}$ is the response time of the controller, and f_C is the closed-loop crossover frequency.

Compensation Design

The MAX15014–MAX15017 use a voltage-mode-control scheme that regulates the output voltage by comparing the error-amplifier output (COMP) with an internal ramp to produce the required duty cycle. The output lowpass LC filter creates a double pole at the resonant frequency, which has a gain drop of -40dB/decade. The error amplifier must compensate for this gain drop and phase shift to achieve a stable closed-loop system.

The basic regulator loop consists of a power modulator, an output feedback-divider, and a voltage error amplifier. The power modulator has a DC gain set by V_{IN}/V_{RAMP}, with a double pole and a single zero set by the output inductance (L), the output capacitance (C_{OUT}), and its ESR. The power modulator incorporates a voltage feed-forward feature, which automatically adjusts for variations in the input voltage, resulting in a DC gain of 10.

The following equations define the power modulator:

$$G_{MOD\_DC} = \frac{V_{IN}}{V_{RAMP}} = 10$$

$$f_{LC} = \frac{1}{2 \times \pi \times \sqrt{L \times C_{OUT}}}$$

$$f_{ZESR} = \frac{1}{2 \times \pi \times C_{OUT} \times ESR}$$

The switching frequency is internally set at 500kHz for MAX15015/MAX15017 and can vary from 400kHz to 600kHz when driven with an external SYNC signal. The switching frequency is internally set at 135kHz for MAX15014/MAX15016 and can vary from 100kHz to 200kHz when driven with an external SYNC signal. The crossover frequency (f_C), which is the frequency when the closed-loop gain is equal to unity, should be set to around 1/10 of the switching frequency or below.

The crossover frequency occurs above the LC double-pole frequency, and the error amplifier must provide a gain and phase bump to compensate for the rapid gain and phase loss from the LC double pole, which exhibits little damping.

This is accomplished by utilizing a Type 3 compensator that introduces two zeroes and three poles into the control loop. The error amplifier has a low-frequency pole (f_{P1}) near the origin so that tight voltage regulation at DC can be achieved.

The two zeroes are at:

$$f_{ZI} = \frac{1}{2\pi \times R5 \times C7}$$

and

$$f_{Z2} = \frac{1}{2\pi \times (R3 + R6) \times C6}$$

and the higher frequency poles are at:

$$f_{P2} = \frac{1}{2\pi \times R6 \times C6}$$

and

$$f_{P3} = \frac{1}{2\pi \times R5 \times \frac{C7 \times C8}{C7 + C8}}$$

The compensation design primarily depends on the type of output capacitor. Ceramic capacitors exhibit very low ESR, and are well suited for high-switching-frequency applications, but are limited in capacitance value and tend to be more expensive. Aluminum electrolytic capacitors have much larger ESR but can reach much larger capacitance values.

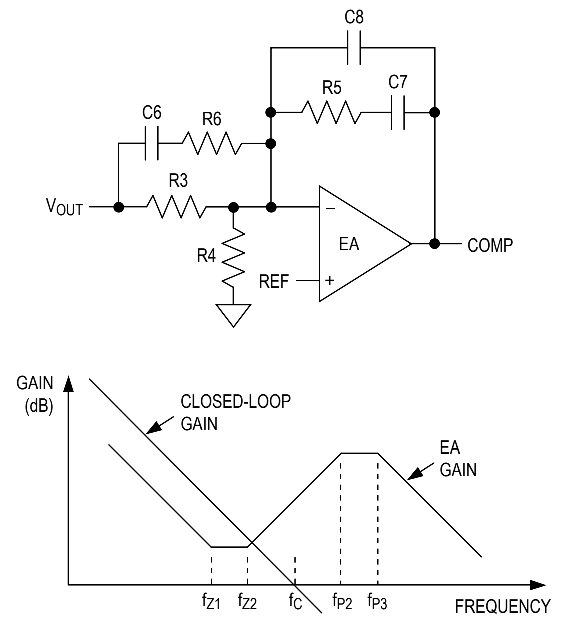


Figure 3. Error Amplifier Compensation Circuit (Closed-Loop and Error-Amplifier Gain Plot) for Ceramic Capacitors

Compensation when $f_C < f_{ZESR}$

This is usually the case when a ceramic capacitor is selected. In this case, f_{ZESR} occurs after f_C. Figure 3 shows the error amplifier feedback as well as its gain response.

f_{Z1} is set to 0.5 to 0.8 x f_{LC} and f_{Z2} is set to f_{LC} to compensate for the gain and phase loss due to the double pole. To achieve a 0dB crossover with -20dB/decade slope, poles f_{P2} and f_{P3} are set above the crossover frequency (f_C).

The values for R3 and R4 are already determined in the *Setting the Output Voltage* section. The value of R3 is also used in the following calculations.

Since $f_{Z2} < f_C < f_{P2}$, then R3 >> R6, and R3 + R6 can be approximated as R3.

Now we can calculate C6 for zero f_{Z2}:

$$C6 = \frac{1}{2\pi \times f_{LC} \times R3}$$

f_C occurs between f_{Z2} and f_{P2}. In this region, the compensatorgain (G_{EA}) at f_C is due primarily to C6 and R5. Therefore, $G_{EA}(f_C) = 2\pi \times f_C \times C6 \times R5$ and the modulator gain at f_C is:

$$G_{MOD}(f_C) = \frac{G_{MOD\_DC}}{(2\pi \times f_C)^2 \times L \times C_{OUT}}$$

Since $G_{EA}(f_C) \times G_{MOD}(f_C) = 1$, R5 is calculated by:

$$R5 = \frac{f_C \times L \times C_{OUT} \times 2\pi}{C6 \times G_{MOD\_DC}}$$

The frequency of f_{Z1} is set to $0.5 \times f_{LC}$ and now we can calculate C7 by:

$$C7 = \frac{1}{0.5 \times 2\pi \times R5 \times f_{LC}}$$

f_{P2} is set at 1/2 the switching frequency (f_{SW}). R6 is then calculated by:

$$R6 = \frac{1}{2\pi \times C6 \times (0.5 \times f_{SW})}$$

Note that if the crossover frequency has been chosen as 1/10 of the switching frequency, then $f_{P2} = 5xf_C$.

The purpose of f_{P3} is to further attenuate the residual switching ripple at the COMP pin.

If the ESR zero (f_{ZESR}) occurs in a region between f_C and $f_{SW}/2$, then f_{P3} can be used to cancel it. This way, the Bode plot of the loop-gain plot does not flatten out soon after the 0dB crossover, and maintains its -20dB/decade slope up to 1/2 of the switching frequency.

If the ESR zero well exceeds $f_{SW}/2$ (or even f_{SW}), f_{P3} should in any case be set high enough not to erode the phase margin at the crossover frequency. For example, it can be set between $5 \times f_C$ and $10 \times f_C$.

The value for C8 is calculated from:

$$C8 = \frac{C7}{(2\pi \times C7 \times R5 \times f_{P3} - 1)}$$

Compensation when $f_C > f_{ZESR}$

For larger ESR capacitors such as tantalum and aluminum electrolytic, f_{ZESR} can occur before f_C. If $f_{ZESR} < f_C$, then f_C occurs between f_{P2} and f_{P3}. f_{Z1} and f_{Z2} remain the same as before; however, f_{P2} is now set equal to f_{ZESR}. The output capacitor's ESR zero frequency is higher than f_{LC} but lower than the closed-loop crossover frequency. The equations that define the error amplifier's poles and zeros (f_{Z1}, f_{Z2}, f_{P2}, and f_{P3}) are the same as before; however, f_{P2} is now lower than the closed-loop crossover frequency. Figure 4 shows the error-amplifier feedback as well as its gain response for circuits that use higher-ESR output capacitors (tantalum or aluminum electrolytic).

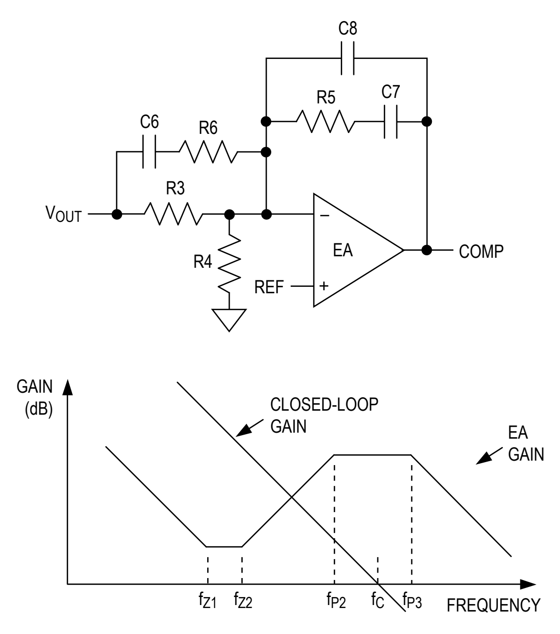


Figure 4. Error Amplifier Compensation Circuit (Closed-Loop and Error-Amplifier Gain Plot) for Higher ESR Output Capacitors

Again, starting from R3, calculate C6 for zero f_{Z2}:

$$C6 = \frac{1}{2\pi \times f_{LC} \times R3}$$

and then place f_{P2} to cancel the ESR zero. R6 is calculated as:

$$R6 = \frac{C_{OUT} \times ESR}{C6}$$

If the value obtained here for R6 is not considerably smaller than R3, recalculate C6 using (R3 + R6) in place of R3. Then use the new value of C6 to obtain a better approximation for R6. The process can be further iterated, and convergence is ensured as long as $f_{LC} < f_{ZESR}$.

The error-amplifier gain between f_{P2} and f_{P3} is approximately equal to R5/(R6 || R3).

The ESR zero frequency (f_{ZESR}) might not be very much higher than the double-pole frequency f_{LC}; therefore, the value of R5 can be calculated as:

$$R5 = \frac{R3 \times R6}{R3 + R6} \times \frac{f_C{}^2}{G_{MOD\_DC} \times f_{LC}{}^2}$$

C7 can still be calculated as:

$$C7 = \frac{1}{0.5 \times 2\pi \times R5 \times f_{LC}}$$

f_{P3} is set at $5xf_C$. Therefore, C8 is calculated as:

$$C8 = \frac{C7}{2\pi \times C7 \times R5 \times f_{P3} - 1}$$

Setting the LDO Linear Regulator Output Voltage

The MAX15014–MAX15017 LDO regulator features Dual Mode™ operation: it can operate in either a preset voltage mode or an adjustable mode. In preset-voltage mode, internal trimmed feedback resistors set the internal linear regulator to 3.3V or 5V (see the *Selector Guide*). Select preset-voltage mode by connecting SET_LDO to ground. In adjustable mode, select an output voltage between 1.5V and 11V using two external resistors connected as a voltage-divider to SET_LDO (see Figure 5). Set the output voltage using the following equation:

$$V_{OUT} = V_{SET\_LDO}\left(1 + \frac{R1}{R2}\right)$$

where V_{SET_LDO} = 1.241V and the recommended value for R2 is around 50kΩ.

Setting the $\overline{\text{RESET}}$ Timeout Delay

The $\overline{\text{RESET}}$ timeout period is adjustable to accommodate a variety of µP applications. Adjust the $\overline{\text{RESET}}$ timeout period by connecting a capacitor (C_{CT}) between CT and SGND.

$$t_{RP} = \frac{C_{CT} \times V_{CT\text{-}TH}}{I_{CT\text{-}THQ}}$$

where $V_{CT\text{-}TH}$ = delay-comparator threshold (rising) = 1.241V (typ), $I_{CT\text{-}THQ}$ = CT charge current = 2 x 10^{-6}A (typ), t_{RP} is in seconds and C_{CT} is in Farads.

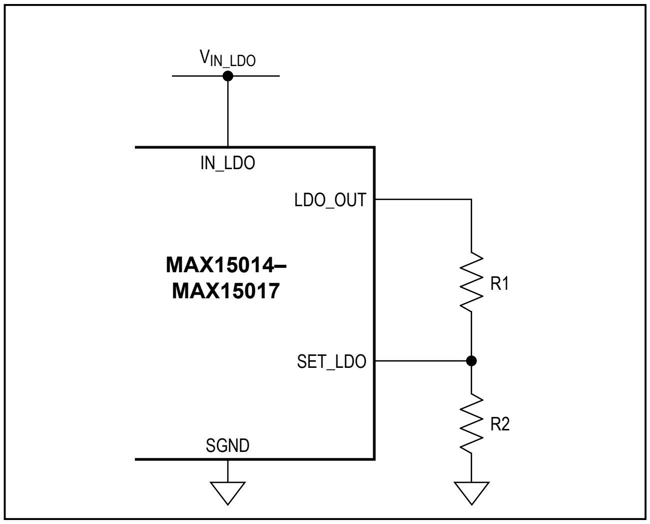


Figure 5. Setting the Output Voltage Using a Resistive Divider

Connect CT to LDO_OUT to select the internally fixed timeout period. C_{CT} must be a low-leakage-type capacitor. Ceramic capacitors are recommended; do not use capacitors lower than 200pF to avoid the influence of parasitic capacitances.

Capacitor Selection and Regulator Stability

For stable operation over the full temperature range and with load currents up to 50mA, use a 10µF (min) output capacitor (C_{LDO_OUT}) with a maximum ESR of 0.4Ω. To reduce noise and improve load-transient response, stability, and power-supply rejection, use larger output capacitor values. Some ceramic dielectrics such as Z5U and Y5V exhibit very large capacitance and ESR variation with temperature and are not recommended. With X7R or X5R dielectrics, 15µF should be sufficient for operation over their rated temperature range. For higher ESR tantalum capacitors (up to 1Ω), use 22µF or more to maintain stability. To improve power-supply rejection and transient response, use a minimum 0.1µF capacitor between IN_LDO and SGND.

Power Dissipation

The MAX15014–MAX15017 are available in a thermally enhanced package and can dissipate up to 2.86W at T_A = +70°C. When the die temperature reaches +160°C, the part shuts down and is allowed to cool. After the die cools by 20°C, the device restarts with a soft-start. The power dissipated in the device is the sum of the power dissipated in the LDO, power dissipated from supply current (P_Q), transition losses due to switching the internal power MOSFET (P_{SW}), and the power

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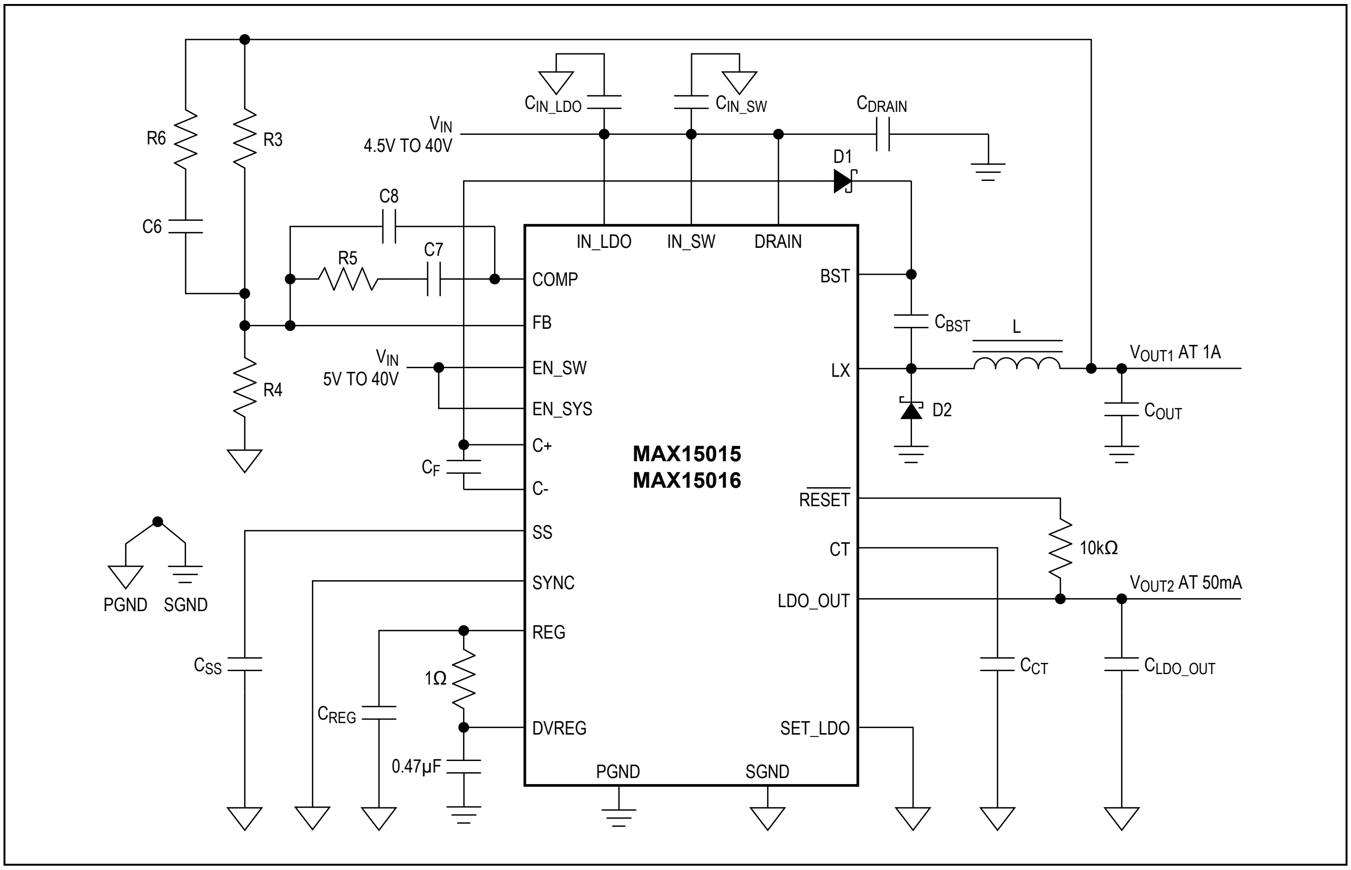


Figure 6. MAX15015/MAX15016 Typical Application Circuit (4.5V to 40V Input Operation)

dissipated due to the RMS current through the internal power MOSFET (P_{MOSFET}). The total power dissipated in the package must be limited such that the junction temperature does not exceed its absolute maximum rating of +150°C at maximum ambient temperature. Calculate the power lost in the MAX15014–MAX15017 using the following equations:

The power loss through the switch:

$$P_{MOSFET} = (I_{RMS\_MOSFET})^2 \times R_{ON}$$

$$I_{RMS\_MOSFET} = \sqrt{\frac{D}{3} \times \left[I^2_{PK} + (I_{PK} \times I_{DC}) + I^2_{DC}\right]}$$

$$I_{PK} = I_{OUT} + \frac{\Delta I_{P-P}}{2}$$

$$I_{DC} = I_{OUT} - \frac{\Delta I_{P-P}}{2}$$

$$D = \frac{V_{OUT}}{V_{IN}}$$

R_{ON} is the on-resistance of the internal power MOSFET (see the *Electrical Characteristics*).

The power loss due to switching the internal MOSFET:

$$P_{SW} = \frac{V_{IN} \times I_{OUT} \times (t_R + t_F) \times f_{SW}}{4}$$

t_R and t_F are the rise and fall times of the internal power MOSFET measured at LX.

The power loss due to the switching supply current (I_{SW}):

$$P_Q = V_{IN\_SW} \times I_{SW}$$

The power loss due to the LDO regulator:

$$P_{LDO} = (V_{IN\_LDO} - V_{LDO\_OUT}) \times I_{LDO\_OUT}$$

The total power dissipated in the device will be:

$$P_{TOTAL} = P_{MOSFET} + P_{SW} + P_Q + P_{LDO}$$

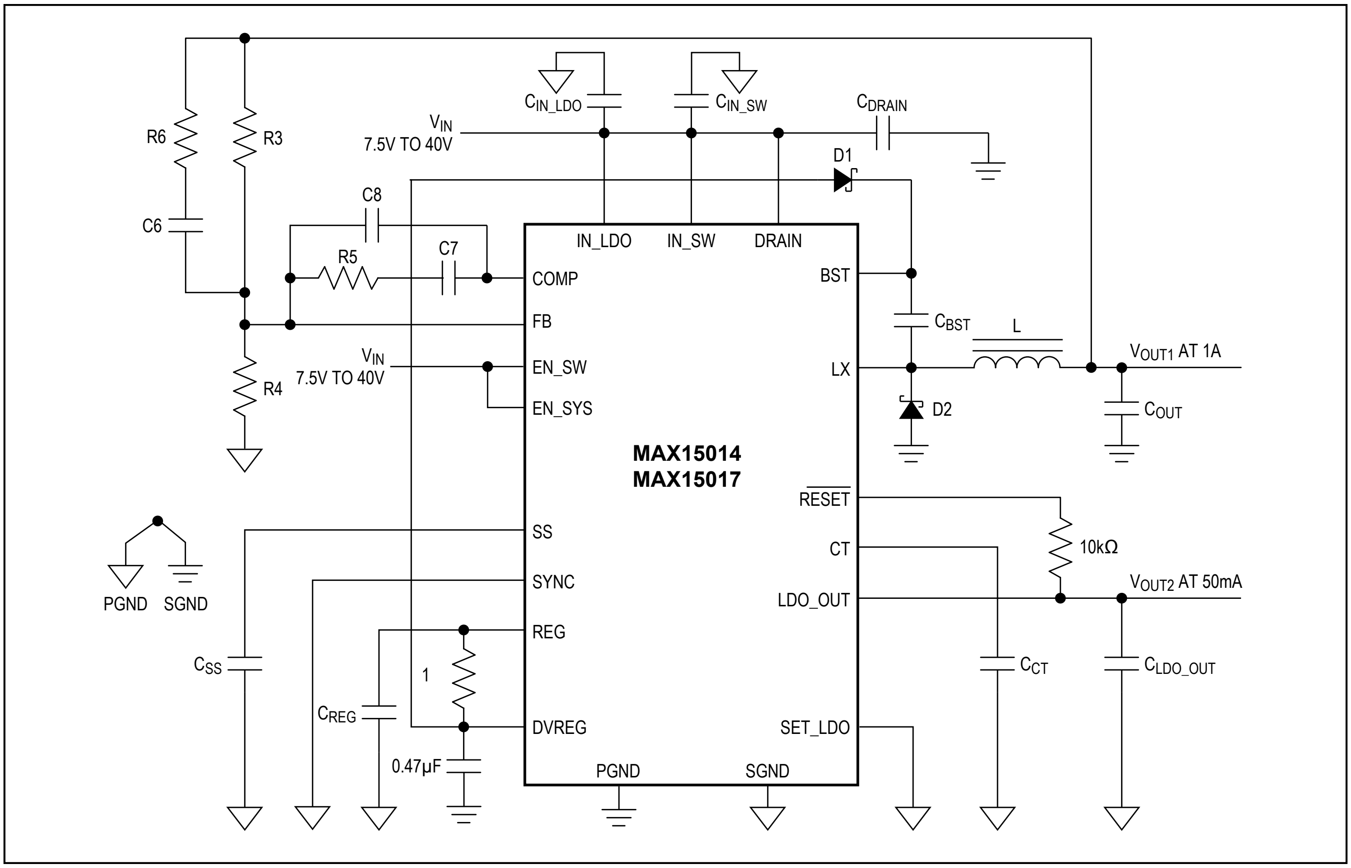
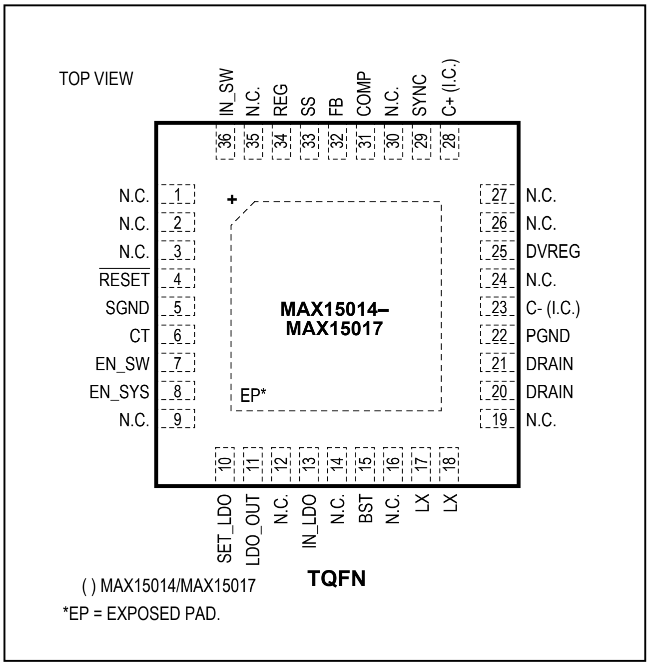


Figure 7. MAX15014/MAX15017 Typical Application Circuit (7.5V to 40V Input-Voltage Operation)

Pin Configuration



( ) MAX15014/MAX15017

*EP = EXPOSED PAD.

Chip Information

PROCESS: BiCMOS/DMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
36 TQFN	T3666+3	**21-0141**	**90-0050**

Selector Guide

PART	SWITCHING FREQUENCY (kHz)	DC-DC MINIMUM INPUT VOLTAGE (V)	CHARGE PUMP	LDO OUTPUT		
				5V	3.3V	ADJUSTABLE OUTPUT
MAX15014A	135	7.5	—	X	—	X
MAX15014B	135	7.5	—	—	X	X
MAX15015A	500	4.5	X	X	—	X
MAX15015B	500	4.5	X	—	X	X
MAX15016A	135	4.5	X	X	—	X
MAX15016B	135	4.5	X	—	X	X
MAX15017A	500	7.5	—	X	—	X
MAX15017B	500	7.5	—	—	X	X

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	1/07	Initial release	—
1	11/14	No /V OPNs in *Ordering Information*; deleted automotive reference in *Applications* section; update *Packaging Information*	1, 25