



**THE DATASHEET OF  
MAX16808AUI+**



## MAX16807

## Integrated 8-Channel LED Driver with Switch-Mode Boost and SEPIC Controller

### General Description

The MAX16807 is an integrated, high-efficiency white or RGB LED driver. It is designed for LCD backlighting and other LED lighting applications with multiple strings of LEDs. The MAX16807 current-mode PWM controller regulates the necessary voltage to the LED array. Depending on the input voltage and LED voltage range, it can be used with boost or buck-boost (SEPIC) topologies. The MAX16807 features an 8V to 26.5V input voltage range. A wide range of adjustable frequency (20kHz to 1MHz) allows design optimization for efficiency and minimum board space.

The MAX16807 LED driver includes eight open-drain, constant-current-sinking LED driver outputs rated for 36V continuous operation. The LED current-control circuitry achieves  $\pm 3\%$  current matching among strings and enables paralleling of outputs for LED string currents higher than 55mA. The output-enable pin is used for simultaneous PWM dimming of all output channels. Dimming frequency range is 50Hz to 30kHz and dimming ratio is up to 5000:1. The constant-current outputs are single resistor programmable and the LED current can be adjusted up to 55mA per output channel.

The MAX16807 operates either in stand-alone mode or with a microcontroller ( $\mu\text{C}$ ) using an industry-standard, 4-wire serial interface.

The MAX16807 includes overtemperature protection, operates over the full  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  temperature range, and is available in a thermally enhanced, 28-pin TSSOP exposed pad package.

### Features

- Eight Constant-Current Output Channels (Up to 55mA Each)
- $\pm 3\%$  Current Matching Among Outputs
- Paralleling Channels Allows Higher Current per LED String
- Output Rated for 36V Continuous Voltage
- Output-Enable Pin for PWM Dimming (Up to 30kHz)
- One Resistor Sets LED Current for All Channels
- Wide Dimming Ratio Up to 5000:1
- Low Current-Sense Reference (300mV) for High Efficiency
- 8V to 26.5V Input Voltage or Higher with External Biasing Devices
- 4-Wire Serial Interface to Control Individual Output Channels

### Applications

- LCD White or RGB LED Backlighting: LCD TVs, Desktop and Notebook Panels, Industrial and Medical Displays
- Ambient, Mood, and Accent Lighting

### Ordering Information

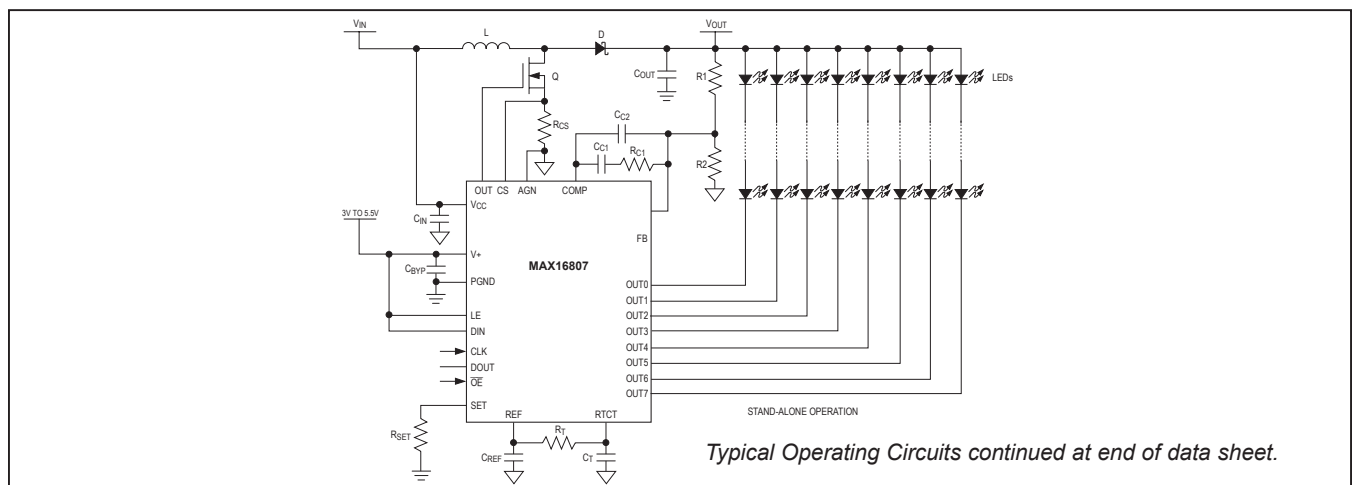
| PART          | TEMP RANGE                                      | PIN-PACKAGE  |
|---------------|---|--------------|
| MAX16807AU I+ | $-40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$ | 28 TSSOP-EP* |

+Denotes lead(Pb)-free/RoHS-compliant package.

\*EP = Exposed pad.

Pin Configuration appears at end of data sheet.

### Typical Operating Circuits



**Absolute Maximum Ratings**

|   |                                   |   |                 |
|---|-----------------------------------|---|-----------------|
| V <sub>CC</sub> to AGND.....                              | -0.3V to +30V                     | OUT0–OUT7 Sink Current.....                           | 60mA            |
| Current into V <sub>CC</sub> (V <sub>CC</sub> > 24V)..... | ±30mA                             | Total PGND Current .....                              | 480mA           |
| V+ to PGND.....   | -0.3V to +6V                      | Continuous Power Dissipation (T <sub>A</sub> = +70°C) |                 |
| OUT to AGND.....  | -0.3V to (V <sub>CC</sub> + 0.3V) | 28-Pin TSSOP (derate 27mW/°C* above +70°C).....       | 2162mW          |
| OUT Current (10µs duration).....                          | ±1A                               | Operating Temperature Range.....                      | -40°C to +125°C |
| FB, COMP, CS, RTCT, REF to AGND.....                      | -0.3V to +6V                      | Junction Temperature.....                             | +150°C          |
| COMP Sink Current.....                                    | 10mA                              | Storage Temperature Range .....                       | -65°C to +150°C |
| OUT0–OUT7 to PGND.....                                    | -0.3V to +40V                     | Lead Temperature (soldering, 10s) .....               | +300°C          |
| DIN, CLK, LE, OE, SET to PGND.....                        | -0.3V to (V+ + 0.3V)              |   |                 |
| DOUT Current.....   | ±10mA                             |   |                 |

\*Per JEDEC51 Standard (Multilayer Board).

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Electrical Characteristics (PWM Controller)**

(V<sub>CC</sub> = +15V, V+ = +3V to +5.5V referenced to PGND, R<sub>T</sub> = 10kΩ, C<sub>T</sub> = 3.3nF, REF = open, COMP = open, C<sub>REF</sub> = 0.1µF, V<sub>FB</sub> = 2V, CS = AGND, V<sub>AGND</sub> = V<sub>PGND</sub> = 0V; all voltages are measured with respect to AGND, unless otherwise noted. T<sub>J</sub> = T<sub>A</sub> = -40°C to +125°C, unless otherwise noted. Typical values are at T<sub>A</sub> = +25°C.) (Note 1)

| PARAMETER                      | SYMBOL              | CONDITIONS   | MIN   | TYP   | MAX   | UNITS |
|--------------------------------|---------------------|--|-------|-------|-------|-------|
| <b>REFERENCE</b>               |                     |  |       |       |       |       |
| Output Voltage                 | V <sub>REF</sub>    | I <sub>REF</sub> = 1mA, T <sub>J</sub> = +25°C                       | 4.95  | 5     | 5.05  | V     |
| Line Regulation                | ΔV <sub>LINE</sub>  | 12V < V <sub>CC</sub> < 25V, I <sub>REF</sub> = 1mA                  |       | 0.4   | 4     | mV    |
| Load Regulation                | ΔV <sub>LOAD</sub>  | 1mA < I <sub>REF</sub> < 20mA  |       | 6     | 50    | mV    |
| Total Output-Voltage Variation | V <sub>REFT</sub>   | (Note 2)   | 4.875 |       | 5.125 | V     |
| Output Noise Voltage           | V <sub>NOISE</sub>  | 10Hz < f < 10kHz   |       | 50    |       | µV    |
| Output Short-Circuit Current   | I <sub>SHORT</sub>  | V <sub>REF</sub> = 0V  | 30    |       | 180   | mA    |
| <b>OSCILLATOR</b>              |                     |  |       |       |       |       |
| Initial Accuracy               |                     | T <sub>J</sub> = +25°C   | 51    | 54    | 57    | kHz   |
| Voltage Stability              |                     | 12V < V <sub>CC</sub> < 25V  |       | 0.2   | 0.5   | %     |
| Temperature Stability          |                     |  |       | 1     |       | %     |
| RTCT Ramp Peak-to-Peak         |                     |  |       | 1.7   |       | V     |
| RTCT Ramp Valley               |                     |  |       | 1.1   |       | V     |
| Discharge Current              | I <sub>DIS</sub>    | V <sub>RTCT</sub> = 2V, T <sub>J</sub> = +25°C                       | 7.9   | 8.3   | 8.7   | mA    |
|                                |                     | V <sub>RTCT</sub> = 2V, -40°C ≤ T <sub>J</sub> ≤ +125°C              | 7.5   | 8.3   | 9.0   |       |
| Frequency Range                | f <sub>OSC</sub>    |  | 20    |       | 1000  | kHz   |
| <b>ERROR AMPLIFIER</b>         |                     |  |       |       |       |       |
| FB Input Voltage               | V <sub>FB</sub>     | FB shorted to COMP   | 2.45  | 2.50  | 2.55  | V     |
| Input Bias Current             | I <sub>B(FB)</sub>  |  |       | -0.01 | -0.1  | µA    |
| Open-Loop Gain                 | A <sub>VOL</sub>    | 2V ≤ V <sub>COMP</sub> ≤ 4V  |       | 100   |       | dB    |
| Unity-Gain Bandwidth           | f <sub>GBW</sub>    |  |       | 1     |       | MHz   |
| Power-Supply Rejection Ratio   | PSRR                | 12V ≤ V <sub>CC</sub> ≤ 25V  | 60    | 80    |       | dB    |
| COMP Sink Current              | I <sub>SINK</sub>   | V <sub>FB</sub> = 2.7V, V <sub>COMP</sub> = 1.1V                     | 2     | 6     |       | mA    |
| COMP Source Current            | I <sub>SOURCE</sub> | V <sub>FB</sub> = 2.3V, V <sub>COMP</sub> = 5V                       | 0.5   | 1.2   | 1.8   | mA    |
| COMP Output-Voltage High       | V <sub>OH</sub>     | V <sub>FB</sub> = 2.3V, R <sub>COMP</sub> = 15kΩ to AGND             | 5     | 5.8   |       | V     |
| COMP Output-Voltage Low        | V <sub>OL</sub>     | V <sub>FB</sub> = 2.7V, R <sub>COMP</sub> = 15kΩ to V <sub>REF</sub> |       | 0.1   | 1.1   | V     |

**Electrical Characteristics (PWM Controller) (continued)**

( $V_{CC} = +15V$ ,  $V_+ = +3V$  to  $+5.5V$  referenced to PGND,  $R_T = 10k\Omega$ ,  $C_T = 3.3nF$ , REF = open, COMP = open,  $C_{REF} = 0.1\mu F$ ,  $V_{FB} = 2V$ , CS = AGND,  $V_{AGND} = V_{PGND} = 0V$ ; all voltages are measured with respect to AGND, unless otherwise noted.  $T_J = T_A = -40^\circ C$  to  $+125^\circ C$ , unless otherwise noted. Typical values are at  $T_A = +25^\circ C$ .) (Note 1)

| PARAMETER                               | SYMBOL          | CONDITIONS                 | MIN   | TYP   | MAX   | UNITS   |          |
|---|-----------------|----------------------------|---|-------|-------|---------|----------|
| <b>CURRENT-SENSE AMPLIFIER</b>          |                 |                            |   |       |       |         |          |
| Current-Sense Gain                      | $A_{CS}$        | (Notes 3, 4)               | 2.85  | 3.00  | 3.40  | V/V     |          |
| Maximum Current-Sense Signal            | $V_{CS\_MAX}$   | (Note 3)                   | 0.275   | 0.300 | 0.325 | V       |          |
| Power-Supply Rejection Ratio            | PSRR            | $12V \leq V_{CC} \leq 25V$ |   | 70    |       | dB      |          |
| Current-Sense Input Bias Current        | $I_{CS}$        | $V_{COMP} = 0V$            |   | -1    | -2.5  | $\mu A$ |          |
| Current Sense to OUT Delay              | $t_{PWM}$       | 50mV overdrive             |   | 60    |       | ns      |          |
| <b>MOSFET DRIVER</b>                    |                 |                            |   |       |       |         |          |
| OUT Low-Side On-Resistance              | $V_{RDS\_ONL}$  | $I_{SINK} = 200mA$         | $T_J = -40^\circ C$ to $+85^\circ C$ (Note 2) |       | 4.5   | 10      | $\Omega$ |
|   |                 |                            | $T_J = -40^\circ C$ to $+125^\circ C$         |       | 4.5   | 12      |          |
| OUT High-Side On-Resistance             | $V_{RDS\_ONH}$  | $I_{SOURCE} = 100mA$       | $T_J = -40^\circ C$ to $+85^\circ C$ (Note 2) |       | 3.5   | 7.5     | $\Omega$ |
|   |                 |                            | $T_J = -40^\circ C$ to $+125^\circ C$         |       | 3.5   | 10      |          |
| Source Current (Peak)                   | $I_{SOURCE}$    | $C_{LOAD} = 10nF$          |   | 2     |       | A       |          |
| Sink Current (Peak)                     | $I_{SINK}$      | $C_{LOAD} = 10nF$          |   | 1     |       | A       |          |
| Rise Time                               | $t_R$           | $C_{LOAD} = 1nF$           |   | 15    |       | ns      |          |
| Fall Time                               | $t_F$           | $C_{LOAD} = 1nF$           |   | 22    |       | ns      |          |
| <b>UNDERVOLTAGE LOCKOUT/STARTUP</b>     |                 |                            |   |       |       |         |          |
| Startup Voltage Threshold               | $V_{CC\_START}$ |                            | 7.98  | 8.4   | 8.82  | V       |          |
| Minimum Operating Voltage After Turn-On | $V_{CC\_MIN}$   |                            | 7.1   | 7.6   | 8.0   | V       |          |
| Undervoltage-Lockout Hysteresis         | $UVLO_{HYST}$   |                            |   | 0.8   |       | V       |          |
| <b>PULSE-WIDTH MODULATION (PWM)</b>     |                 |                            |   |       |       |         |          |
| Maximum Duty Cycle                      | $D_{MAX}$       |                            | 94.5  | 96    | 97.5  | %       |          |
| Minimum Duty Cycle                      | $D_{MIN}$       |                            |   |       | 0     | %       |          |
| <b>SUPPLY CURRENT</b>                   |                 |                            |   |       |       |         |          |
| Startup Supply Current                  | $I_{START}$     | $V_{CC} = 7.5V$            |   | 32    | 65    | $\mu A$ |          |
| Operating Supply Current                | $I_{CC}$        | $V_{FB} = V_{CS} = 0V$     |   | 3     | 5     | mA      |          |
| $V_{CC}$ Zener Voltage                  | $V_Z$           | $I_{CC} = 25mA$            | 24  | 26.5  |       | V       |          |

**Electrical Characteristics (LED Driver)**

(V+ = +3V to +5.5V, V<sub>AGND</sub> = V<sub>PGND</sub> = 0V; all voltages are measured with respect to PGND, unless otherwise noted. T<sub>A</sub> = T<sub>J</sub> = -40°C to +125°C, unless otherwise noted. Typical values are at T<sub>A</sub> = +25°C.) (Note 1)

| PARAMETER   | SYMBOL            | CONDITIONS   | MIN          | TYP         | MAX  | UNITS |
|---|-------------------|--|--------------|-------------|------|-------|
| Operating Supply Voltage  | V+                |  | 3.0          |             | 5.5  | V     |
| Output Voltage  | V <sub>OUT_</sub> |  |              |             | 36   | V     |
| Standby Current (Interface Idle, All Output Ports High Impedance)   |                   | R <sub>SET</sub> = 360Ω, DIN, LE, CLK = PGND or V+,<br>OE = V+, DOUT unconnected                     |              | 3.6         | 4.5  | mA    |
| Standby Current (Interface Active, All Output Ports High Impedance) |                   | R <sub>SET</sub> = 360Ω, f <sub>CLK</sub> = 5MHz, OE = V+,<br>DIN, LE = PGND or V+, DOUT unconnected |              | 3.8         | 4.8  | mA    |
| Supply Current (Interface Idle, All Output Ports Active Low)        | I+                | R <sub>SET</sub> = 360Ω, OE = PGND, DIN,<br>LE = V+, DOUT unconnected                                |              | 17          | 30   | mA    |
| <b>INTERFACE (DIN, CLK, DOUT, LE, OE)</b>                           |                   |  |              |             |      |       |
| Input-Voltage High (DIN, CLK, LE, OE)                               | V <sub>IH</sub>   |  | 0.7<br>x V+  |             |      | V     |
| Input-Voltage Low (DIN, CLK, LE, OE)                                | V <sub>IL</sub>   |  |              | 0.3<br>x V+ |      | V     |
| Hysteresis Voltage (DIN, CLK, LE, OE)                               | V <sub>HYST</sub> |  |              | 0.8         |      | V     |
| Input Leakage Current (DIN, CLK)                                    | I <sub>LEAK</sub> |  | -1           |             | +1   | μA    |
| OE Pullup Current to V+   | I <sub>OE</sub>   | V+ = 5.5V, OE = PGND   | 0.25         | 1.5         | 25.0 | μA    |
| LE Pulldown Current to PGND   | I <sub>LE</sub>   | V+ = 5.5V, LE = V+   | 0.25         | 1.5         | 25.0 | μA    |
| Output-Voltage High (DOUT)  | V <sub>OH</sub>   | I <sub>SOURCE</sub> = 4mA  | V+<br>- 0.5V |             |      | V     |
| Output-Voltage Low (DOUT)   | V <sub>OL</sub>   | I <sub>SINK</sub> = 4mA  |              |             | 0.5  | V     |
| OUT_ Output Current   | I <sub>OUT_</sub> | 0°C ≤ T <sub>A</sub> ≤ +125°C, V <sub>OUT</sub> = 1V to 2.5V,<br>R <sub>SET</sub> = 360Ω             | 46.5         | 50          | 53.5 | mA    |
|   |                   | T <sub>A</sub> = -40°C, V <sub>OUT</sub> = 1V to 2.5V,<br>R <sub>SET</sub> = 360Ω                    | 43           |             | 57   |       |
| OUT_ Leakage Current  |                   | OE = V+  |              |             | 1    | μA    |

**5V Timing Characteristics**

(V+ = +4.5V to +5.5V, V<sub>AGND</sub> = V<sub>PGND</sub> = 0V; all voltages are measured with respect to PGND, unless otherwise noted. T<sub>A</sub> = T<sub>J</sub> = -40°C to +125°C, unless otherwise noted. Typical values are at T<sub>A</sub> = +25°C.) (Notes 1, 5)

| PARAMETER                                     | SYMBOL                                    | CONDITION                            | MIN | TYP | MAX | UNITS |
|---|---|--------------------------------------|-----|-----|-----|-------|
| <b>INTERFACE TIMING CHARACTERISTICS</b>       |   |                                      |     |     |     |       |
| CLK Clock Period                              | t <sub>CP</sub>                           |                                      | 40  |     |     | ns    |
| CLK Pulse-Width High                          | t <sub>CH</sub>                           |                                      | 19  |     |     | ns    |
| CLK Pulse-Width Low                           | t <sub>CL</sub>                           |                                      | 19  |     |     | ns    |
| DIN Setup Time                                | t <sub>DS</sub>                           |                                      | 4   |     |     | ns    |
| DIN Hold Time                                 | t <sub>DH</sub>                           |                                      | 8   |     |     | ns    |
| DOUT Propagation Delay                        | t <sub>DO</sub>                           |                                      | 12  |     | 50  | ns    |
| DOUT Rise Time                                | t <sub>DR</sub>                           | C <sub>DOUT</sub> = 10pF, 20% to 80% |     |     | 10  | ns    |
| DOUT Fall Time                                | t <sub>DF</sub>                           | C <sub>DOUT</sub> = 10pF, 80% to 20% |     |     | 10  | ns    |
| LE Pulse-Width High                           | t <sub>LW</sub>                           |                                      | 20  |     |     | ns    |
| LE Setup Time                                 | t <sub>LS</sub>                           |                                      | 15  |     |     | ns    |
| LE Rising to OUT_ Rising Delay                | t <sub>LRR</sub>                          | (Note 6)                             |     |     | 110 | ns    |
| LE Rising to OUT_ Falling Delay               | t <sub>LRF</sub>                          | (Note 6)                             |     |     | 325 | ns    |
| CLK Rising to OUT_ Rising Delay               | t <sub>CRR</sub>                          | (Note 6)                             |     |     | 110 | ns    |
| CLK Rising to OUT_ Falling Delay              | t <sub>CRF</sub>                          | (Note 6)                             |     |     | 325 | ns    |
| $\overline{OE}$ Rising to OUT_ Rising Delay   | t <sub>OEER</sub>                         | (Note 6)                             |     |     | 110 | ns    |
| $\overline{OE}$ Falling to OUT_ Falling Delay | t <sub>OE<math>\overline{E}</math>F</sub> | (Note 6)                             |     |     | 325 | ns    |
| OUT_ Turn-On Fall Time                        | t <sub>F</sub>                            | 80% to 20% (Note 6)                  |     |     | 210 | ns    |
| OUT_ Turn-Off Rise Time                       | t <sub>R</sub>                            | 20% to 80% (Note 6)                  |     |     | 130 | ns    |

### 3.3V Timing Characteristics

( $V_+ = +3V$  to  $< +4.5V$ ,  $V_{AGND} = V_{PGND} = 0V$ ; all voltages are measured with respect to PGND, unless otherwise noted.  $T_A = T_J = -40^\circ C$  to  $+125^\circ C$ , unless otherwise noted. Typical values are at  $T_A = +25^\circ C$ .) (Notes 1, 5)

| PARAMETERS                                    | SYMBOL    | CONDITIONS                     | MIN | TYP | MAX | UNITS |
|---|-----------|--------------------------------|-----|-----|-----|-------|
| <b>INTERFACE TIMING CHARACTERISTICS</b>       |           |                                |     |     |     |       |
| CLK Clock Period                              | $t_{CP}$  |                                | 52  |     |     | ns    |
| CLK Pulse-Width High                          | $t_{CH}$  |                                | 24  |     |     | ns    |
| CLK Pulse-Width Low                           | $t_{CL}$  |                                | 24  |     |     | ns    |
| DIN Setup Time                                | $t_{DS}$  |                                | 4   |     |     | ns    |
| DIN Hold Time                                 | $t_{DH}$  |                                | 8   |     |     | ns    |
| DOUT Propagation Delay                        | $t_{DO}$  |                                | 12  |     | 70  | ns    |
| DOUT Rise Time                                | $t_{DR}$  | $C_{DOUT} = 10pF$ , 20% to 80% |     |     | 12  | ns    |
| DOUT Fall Time                                | $t_{DF}$  | $C_{DOUT} = 10pF$ , 80% to 20% |     |     | 12  | ns    |
| LE Pulse-Width High                           | $t_{LW}$  |                                | 20  |     |     | ns    |
| LE Setup Time                                 | $t_{LS}$  |                                | 15  |     |     | ns    |
| LE Rising to OUT_ Rising Delay                | $t_{LRR}$ | (Note 6)                       |     |     | 140 | ns    |
| LE Rising to OUT_ Falling Delay               | $t_{LRF}$ | (Note 6)                       |     |     | 350 | ns    |
| CLK Rising to OUT_ Rising Delay               | $t_{CRR}$ | (Note 6)                       |     |     | 140 | ns    |
| CLK Rising to OUT_ Falling Delay              | $t_{CRF}$ | (Note 6)                       |     |     | 350 | ns    |
| $\overline{OE}$ Rising to OUT_ Rising Delay   | $t_{OER}$ | (Note 6)                       |     |     | 140 | ns    |
| $\overline{OE}$ Falling to OUT_ Falling Delay | $t_{OEF}$ | (Note 6)                       |     |     | 350 | ns    |
| OUT_ Turn-On Fall Time                        | $t_F$     | 80% to 20% (Note 6)            |     |     | 275 | ns    |
| OUT_ Turn-Off Rise Time                       | $t_R$     | 20% to 80% (Note 6)            |     |     | 150 | ns    |

**Note 1:** All devices are 100% production tested at  $T_J = +25^\circ C$  and  $T_J = +125^\circ C$ . Limits to  $T_A = -40^\circ C$  are guaranteed by design.

**Note 2:** Guaranteed by design, not production tested.

**Note 3:** Parameter is measured at trip point of latch with  $V_{FB} = 0V$ .

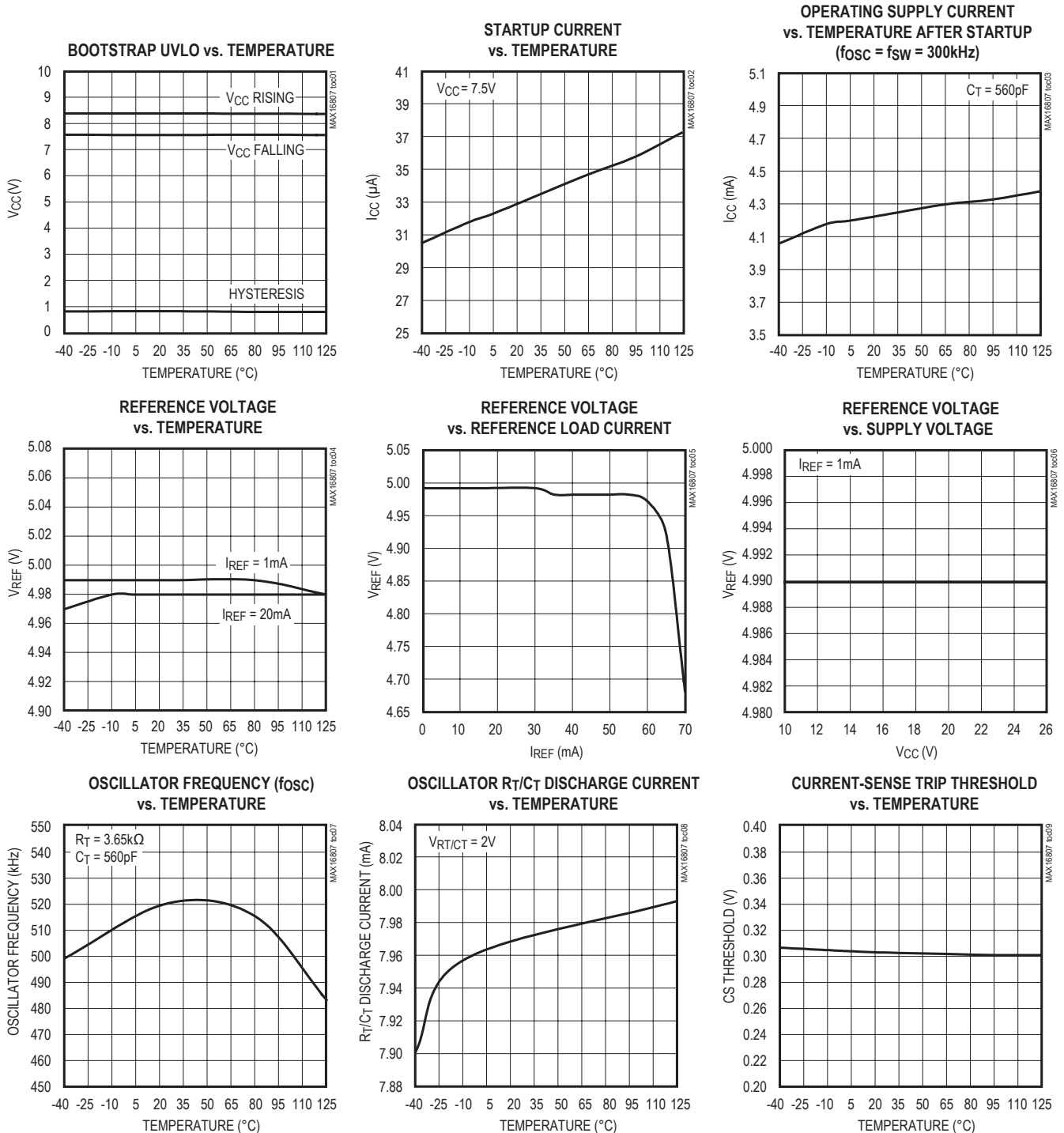
**Note 4:** Gain is defined as  $A = \Delta V_{COMP} / \Delta V_{CS}$ ,  $0.05V \leq V_{CS} \leq 0.25V$ .

**Note 5:** See Figures 3 and 4.

**Note 6:** A  $65\Omega$  pullup resistor is connected from OUT\_ to 5.5V. Rising refers to  $V_{OUT_}$  when current through OUT\_ is turned off and falling refers to  $V_{OUT_}$  when current through OUT\_ is turned on.

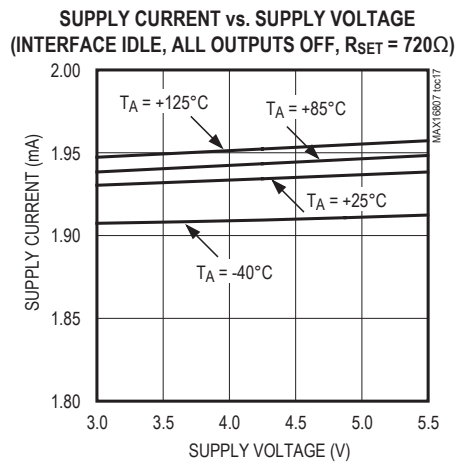
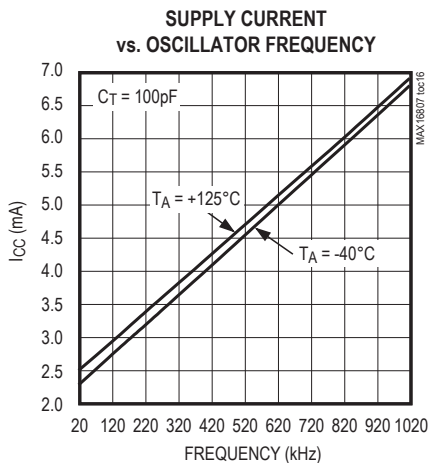
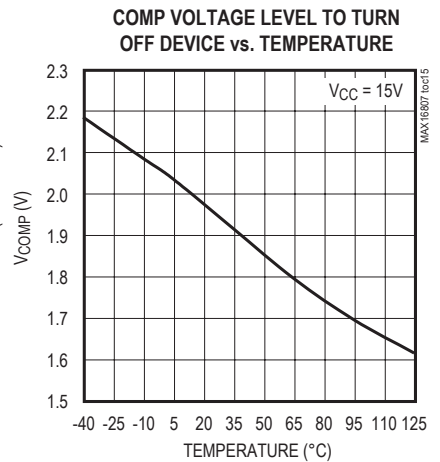
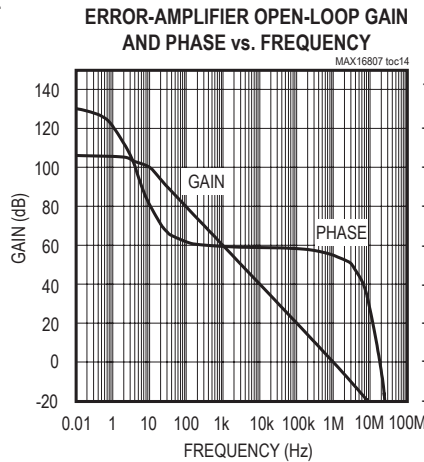
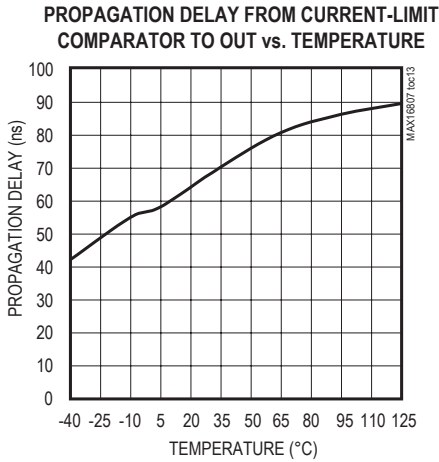
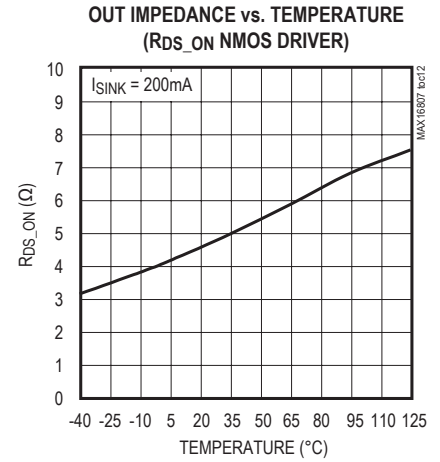
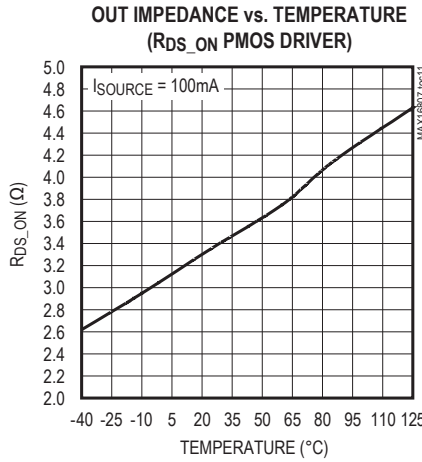
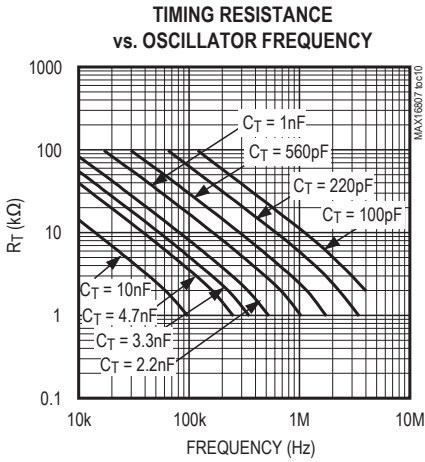
Typical Operating Characteristics

( $V_{CC} = +15V$ ,  $V^+ = 3V$  to  $5.5V$ ,  $R_T = 10k\Omega$ ,  $C_T = 3.3nF$ ,  $V_{REF} = COMP = open$ ,  $C_{REF} = 0.1\mu F$ ,  $V_{FB} = 2V$ ,  $V_{CS} = V_{AGND} = V_{PGND} = 0V$ . Typical values are at  $T_A = +25^\circ C$ , unless otherwise noted.)



Typical Operating Characteristics (continued)

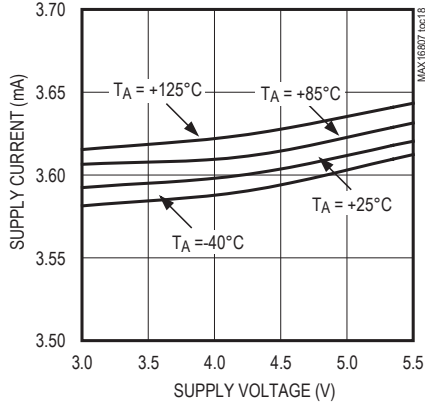
( $V_{CC} = +15V$ ,  $V_+ = 3V$  to  $5.5V$ ,  $R_T = 10k\Omega$ ,  $C_T = 3.3nF$ ,  $V_{REF} = COMP = open$ ,  $C_{REF} = 0.1\mu F$ ,  $V_{FB} = 2V$ ,  $V_{CS} = V_{AGND} = V_{PGND} = 0V$ . Typical values are at  $T_A = +25^\circ C$ , unless otherwise noted.)



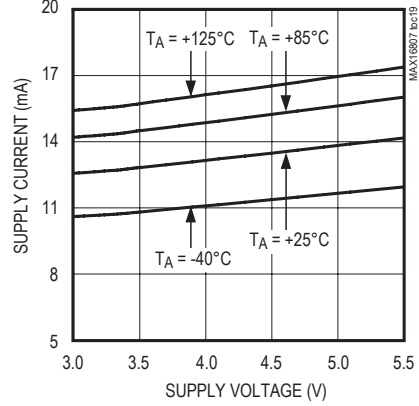
Typical Operating Characteristics (continued)

( $V_{CC} = +15V$ ,  $V+ = 3V$  to  $5.5V$ ,  $R_T = 10k\Omega$ ,  $C_T = 3.3nF$ ,  $V_{REF} = COMP = open$ ,  $C_{REF} = 0.1\mu F$ ,  $V_{FB} = 2V$ ,  $V_{CS} = V_{AGND} = V_{PGND} = 0V$ . Typical values are at  $T_A = +25^\circ C$ , unless otherwise noted.)

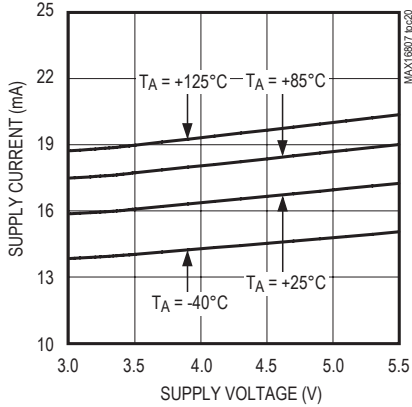
SUPPLY CURRENT vs. SUPPLY VOLTAGE  
(INTERFACE IDLE, ALL OUTPUTS OFF,  $R_{SET} = 360\Omega$ )



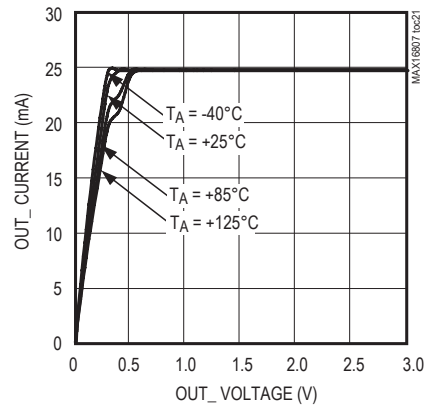
SUPPLY CURRENT vs. SUPPLY VOLTAGE  
(INTERFACE IDLE, ALL OUTPUTS ON,  $R_{SET} = 720\Omega$ )



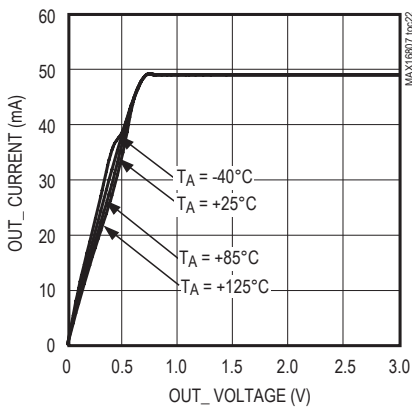
SUPPLY CURRENT vs. SUPPLY VOLTAGE  
(INTERFACE IDLE, ALL OUTPUTS ON,  $R_{SET} = 360\Omega$ )



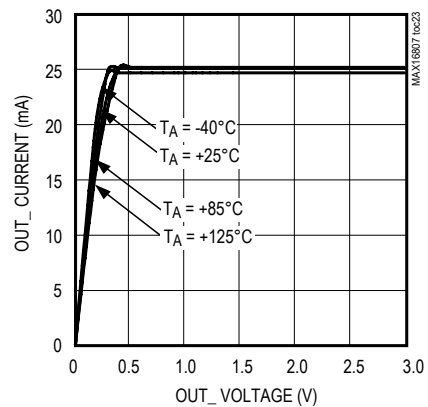
OUT\_ CURRENT vs. OUT\_ VOLTAGE  
( $R_{SET} = 720\Omega$ ,  $V+ = 3.3V$ )



OUT\_ CURRENT vs. OUT\_ VOLTAGE  
( $R_{SET} = 360\Omega$ ,  $V+ = 3.3V$ )

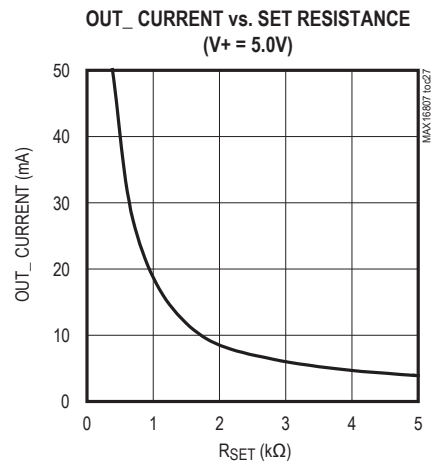
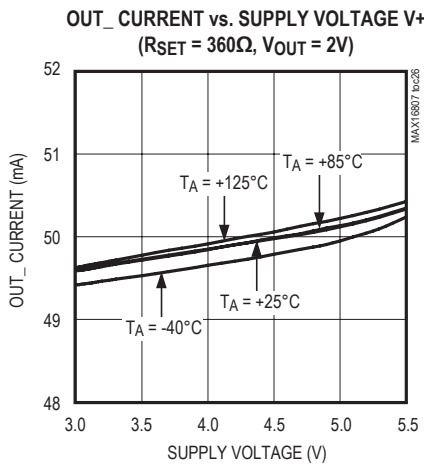
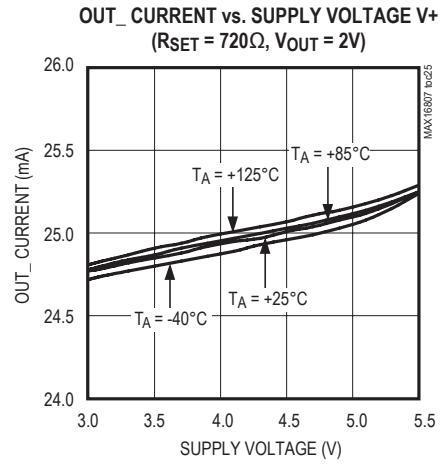
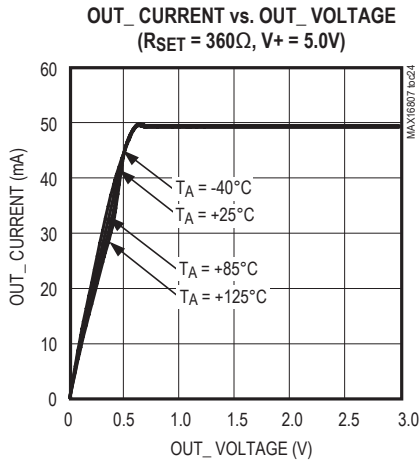


OUT\_ CURRENT vs. OUT\_ VOLTAGE  
( $R_{SET} = 720\Omega$ ,  $V+ = 5.0V$ )



Typical Operating Characteristics (continued)

( $V_{CC} = +15V$ ,  $V+ = 3V$  to  $5.5V$ ,  $R_T = 10k\Omega$ ,  $C_T = 3.3nF$ ,  $V_{REF} = COMP = open$ ,  $C_{REF} = 0.1\mu F$ ,  $V_{FB} = 2V$ ,  $V_{CS} = V_{AGND} = V_{PGND} = 0V$ . Typical values are at  $T_A = +25^\circ C$ , unless otherwise noted.)



## Pin Description

| PIN       | NAME            | FUNCTION   |
|-----------|-----------------|--|
| 1, 13, 28 | N.C.            | No Connection. Not internally connected. Leave unconnected.  |
| 2         | AGND            | Analog Ground  |
| 3         | OUT             | MOSFET Driver Output OUT. Connects to the gate of the external n-channel MOSFET.   |
| 4         | V <sub>CC</sub> | Power-Supply Input. Bypass V <sub>CC</sub> to AGND with a 0.1μF ceramic capacitor or a parallel combination of a 0.1μF and a higher value ceramic capacitor.   |
| 5         | REF             | 5V Reference Output. Bypass REF to AGND with a 0.1μF ceramic capacitor.  |
| 6–9       | OUT4–OUT7       | LED Driver Outputs. OUT4–OUT7 are open-drain, constant-current-sinking outputs rated for 36V.  |
| 10        | $\overline{OE}$ | Active-Low Output Enable Input. Drive $\overline{OE}$ low to PGND to enable the OUT0–OUT7. Drive $\overline{OE}$ high to disable OUT0–OUT7.  |
| 11        | DOUT            | Serial-Data Output. Data is clocked out of the 8-bit internal shift register to DOUT on CLK's rising edge.   |
| 12        | SET             | LED Current Setting. Connect R <sub>SET</sub> from SET to PGND to set the LED current.   |
| 14        | V+              | LED Driver Positive Supply Voltage. Bypass V+ to PGND with a 0.1μF ceramic capacitor.  |
| 15, 16    | PGND            | Power Ground   |
| 17        | DIN             | Serial-Data Input  |
| 18        | CLK             | Serial-Clock Input   |
| 19        | LE              | Latch-Enable Input. Data is loaded transparently from the internal shift register(s) to the output latch(es) while LE is high. Data is latched into the output latch(es) on LE's falling edge, and retained while LE is low. |
| 20–23     | OUT0–OUT3       | LED Driver Outputs. OUT0–OUT3 are open-drain, constant-current-sinking outputs rated for 36V.  |
| 24        | COMP            | Error-Amplifier Output   |
| 25        | FB              | Error-Amplifier Inverting Input  |
| 26        | CS              | PWM Controller Current-Sense Input   |
| 27        | RTCT            | PWM Controller Timing Resistor/Capacitor Connection. A resistor R <sub>T</sub> from RTCT to REF and a capacitor C <sub>T</sub> from RTCT to AGND set the oscillator frequency.   |
| —         | EP              | Exposed Pad. Connect to the ground plane for improved power dissipation. Do not use as the only ground connection for the part.  |

## Detailed Description

The MAX16807 LED driver includes an internal switch-mode controller that can be used as boost or buck-boost (SEPIC) converters to generate the voltage necessary to drive the multiple strings of LEDs. This device incorporates an integrated low-side driver, programmable oscillator (20kHz to 1MHz), error amplifier, low-voltage (300mV) current sense for higher efficiency, and a 5V reference to power up external circuitry (see Figures 1a and 1b).

The MAX16807 LED driver includes a 4-wire serial interface and a current-mode PWM controller to generate the necessary voltage for driving eight open-drain, constant-current-sinking output ports. The driver uses current-

sensing feedback circuitry (not simple current mirrors) to ensure very small current variations over the full allowed range of output voltage (see the *Typical Operating Characteristics*). The 4-wire serial interface comprises an 8-bit shift register and an 8-bit transparent latch. The shift register is written through a clock input (CLK) and a data input (DIN), and the data propagates to a data output (DOUT). The data output allows multiple drivers to be cascaded and operated together. The contents of the 8-bit shift register are loaded into the transparent latch through a latch-enable input (LE). The latch is transparent to the shift-register outputs when high and latches the current state on the falling edge of LE. Each driver output is an open-drain, constant-current sink that should be connected to the cathode of a string of LEDs con-

# MAX16807

## Integrated 8-Channel LED Driver with Switch-Mode Boost and SEPIC Controller

nected in series. The constant-current capability is up to 55mA per output, set for all eight outputs by an external resistor ( $R_{SET}$ ). The device can operate in stand-alone mode (see the *Typical Operating Circuits*.)

The number of channels can be expanded by using the MAX6970 and MAX6971 family in conjunction with the MAX16807.

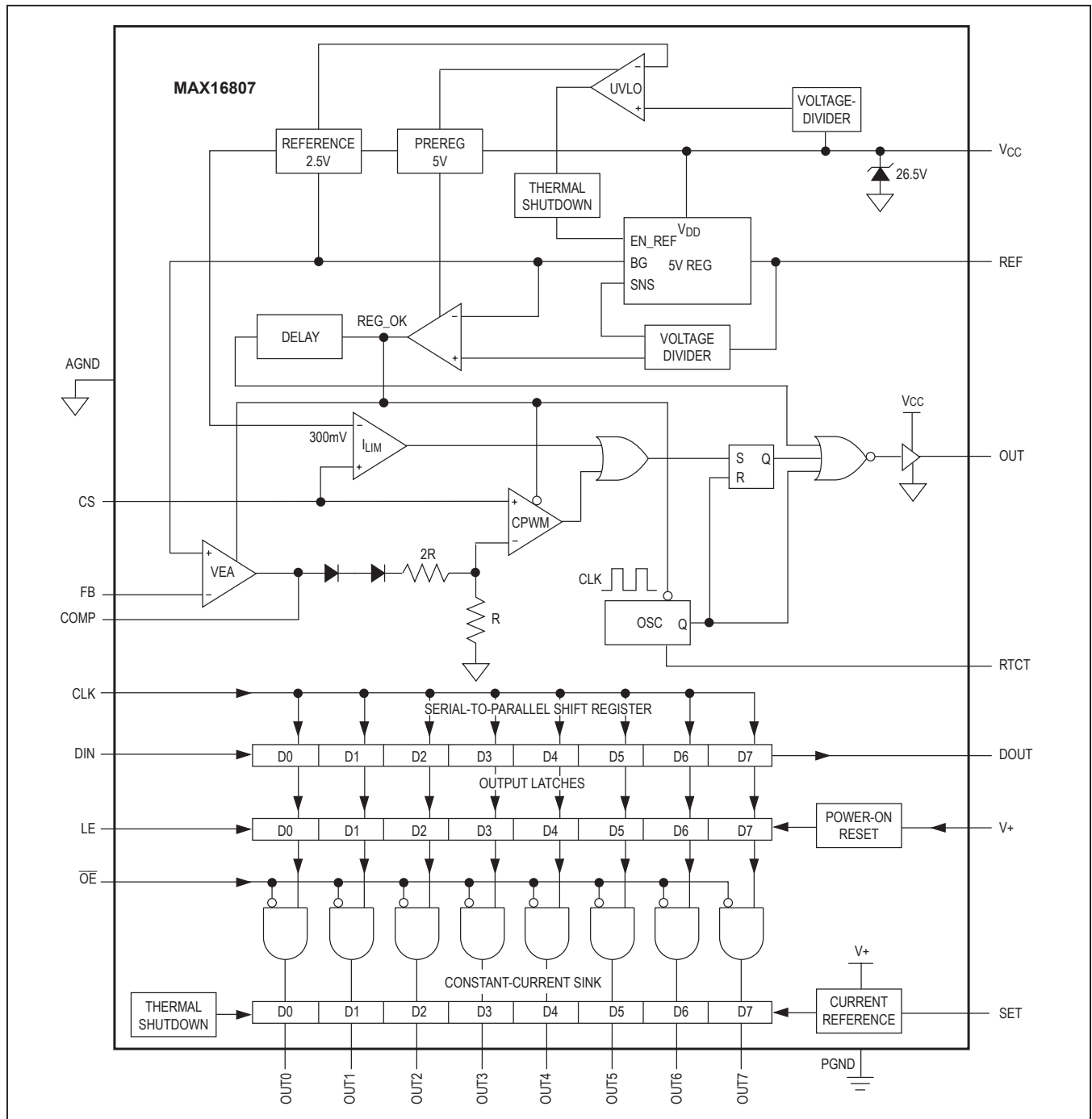


Figure 1a. Internal Block Diagram (MAX16807)

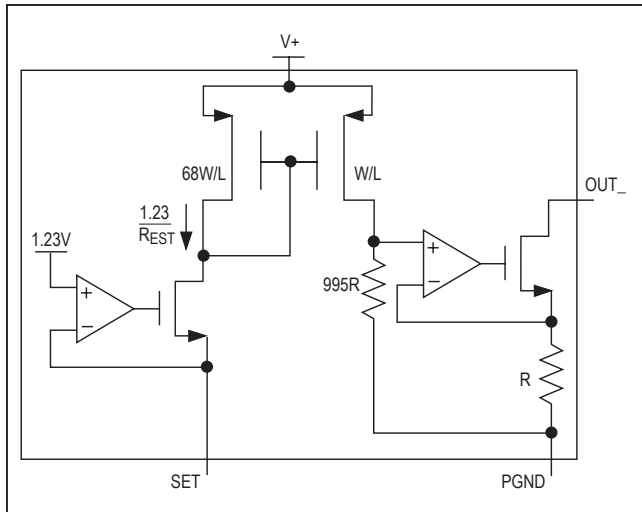


Figure 1b. OUT\_ Driver Internal Diagram

## Switch-Mode Controller

### Current-Mode Control Loop

The advantages of current-mode control over voltage-mode control are twofold. First, there is the feed-forward characteristic brought on by the controller's ability to adjust for variations in the input voltage on a cycle-by-cycle basis. Second, the stability requirements of the current-mode controller are reduced to that of a single-pole system, unlike the double pole in the voltage-mode control scheme. The MAX16807 uses a current-mode control loop where the output of the error amplifier is compared to the current-sense voltage ( $V_{CS}$ ). When the current-sense signal is lower than the inverting input of the CPWM comparator, the output of the comparator is low and the switch is turned on at each clock pulse. When the current-sense signal is higher than the inverting input of the CPWM comparator, the output is high and the switch is turned off.

### Undervoltage Lockout (UVLO)

The turn-on supply voltage for the MAX16807 is 8.4V (typ). Once  $V_{CC}$  reaches 8.4V, the reference powers up. There is 0.8V of hysteresis from the turn-on voltage to the UVLO threshold. Once  $V_{CC}$  reaches 8.4V, the MAX16807 operates with  $V_{CC}$  down to 7.6V (typ). Once  $V_{CC}$  goes below 7.6V, the device is in UVLO. When in UVLO, the quiescent supply current into  $V_{CC}$  falls back to 32 $\mu$ A (typ), and OUT and REF are pulled low.

### MOSFET Driver

OUT drives an external n-channel MOSFET and swings from AGND to  $V_{CC}$ . Ensure that  $V_{CC}$  remains below the

absolute maximum  $V_{GS}$  rating of the external MOSFET. OUT is a push-pull output with the on-resistance of the pMOS (typically 3.5 $\Omega$ ) and the on-resistance of the nMOS (typically 4.5 $\Omega$ ). The driver can source 2A and sink 1A (typ). This allows for the MAX16807 to quickly turn on and off high gate-charge MOSFETs. Bypass  $V_{CC}$  with one or more 0.1 $\mu$ F ceramic capacitors to AGND, placed close to the  $V_{CC}$  pin. The average current sourced to drive the external MOSFET depends on the total gate charge ( $Q_G$ ) and operating frequency of the converter. The power dissipation in the device is a function of the average output drive current ( $I_{DRIVE}$ ). Use the following equation to calculate the power dissipation in the device due to  $I_{DRIVE}$ :

$$I_{DRIVE} = (Q_G \times f_{SW})$$

$$PD = (I_{DRIVE} + I_{CC}) \times V_{CC}$$

where  $I_{CC}$  is the operating supply current. See the *Typical Operating Characteristics* for the operating supply current at a given frequency.

### Error Amplifier

The MAX16807 includes an internal error amplifier. The inverting input is at FB and the noninverting input is internally connected to a 2.5V reference. Set the output voltage using a resistive divider between the output of the converter ( $V_{OUT}$ , FB, and AGND). Use the following formula to set the output voltage:

$$V_{OUT} = \left(1 + \frac{R1}{R2}\right) \times V_{FB}$$

where  $V_{FB} = 2.5V$ .

### Oscillator

The oscillator frequency is programmable using an external capacitor and a resistor at RTCT (see  $R_T$  and  $C_T$  in the *Typical Operating Circuits*).  $R_T$  is connected from RTCT to the 5V reference (REF), and  $C_T$  is connected from RTCT to AGND. REF charges  $C_T$  through  $R_T$  until its voltage reaches 2.8V.  $C_T$  then discharges through an 8.3mA internal current sink until  $C_T$ 's voltage reaches 1.1V, at which time  $C_T$  is allowed to charge through  $R_T$  again. The oscillator's period is the sum of the charge and discharge times of  $C_T$ . Calculate the charge time as follows:

$$t_C = 0.57 \times R_T \times C_T$$

where  $t_C$  is in seconds,  $R_T$  in ohms ( $\Omega$ ), and  $C_T$  in Farads (F).

The discharge time is then:

$$t_D = (R_T \times C_T \times 1000) / [(4.88 \times R_T) - (1.8 \times 1000)]$$

where  $t_D$  is in seconds,  $R_T$  in ohms ( $\Omega$ ), and  $C_T$  in Farads (F).

The oscillator frequency is then:

$$OSC = \frac{1}{(t_C + t_D)}$$

$$R_{CS} = \frac{V_{CS}}{I_{P-P}}$$

**Reference Output (REF)**

REF is a 5V reference output that can source 20mA. Bypass REF to AGND with a 0.1µF capacitor.

**Current Limit**

The MAX16807 includes a fast current-limit comparator to terminate the on-cycle during an overload or a fault condition. The current-sense resistor ( $R_{CS}$ ) connected between the source of the external MOSFET and AGND, sets the current limit. The CS input has a voltage trip level ( $V_{CS}$ ) of 0.3V. Use the following equation to calculate  $R_{CS}$ :

$I_{P-P}$  is the peak current that flows through the MOSFET. When the voltage produced by this current (through the current-sense resistor) exceeds the current-limit comparator threshold, the MOSFET driver (OUT) turns the switch off within 60ns. In most cases, a small RC filter is required to filter out the leading-edge spike on the sense waveform. Set the time constant of the RC filter at 50ns.

**Buck-Boost (SEPIC) Operation**

Figure 2 shows a buck-boost application circuit using the MAX16807 in stand-alone mode of operation. SEPIC topology is necessary when the total forward voltage of the LEDs in a string is such that  $V_{OUT}$  can be below or above  $V_{IN}$ .

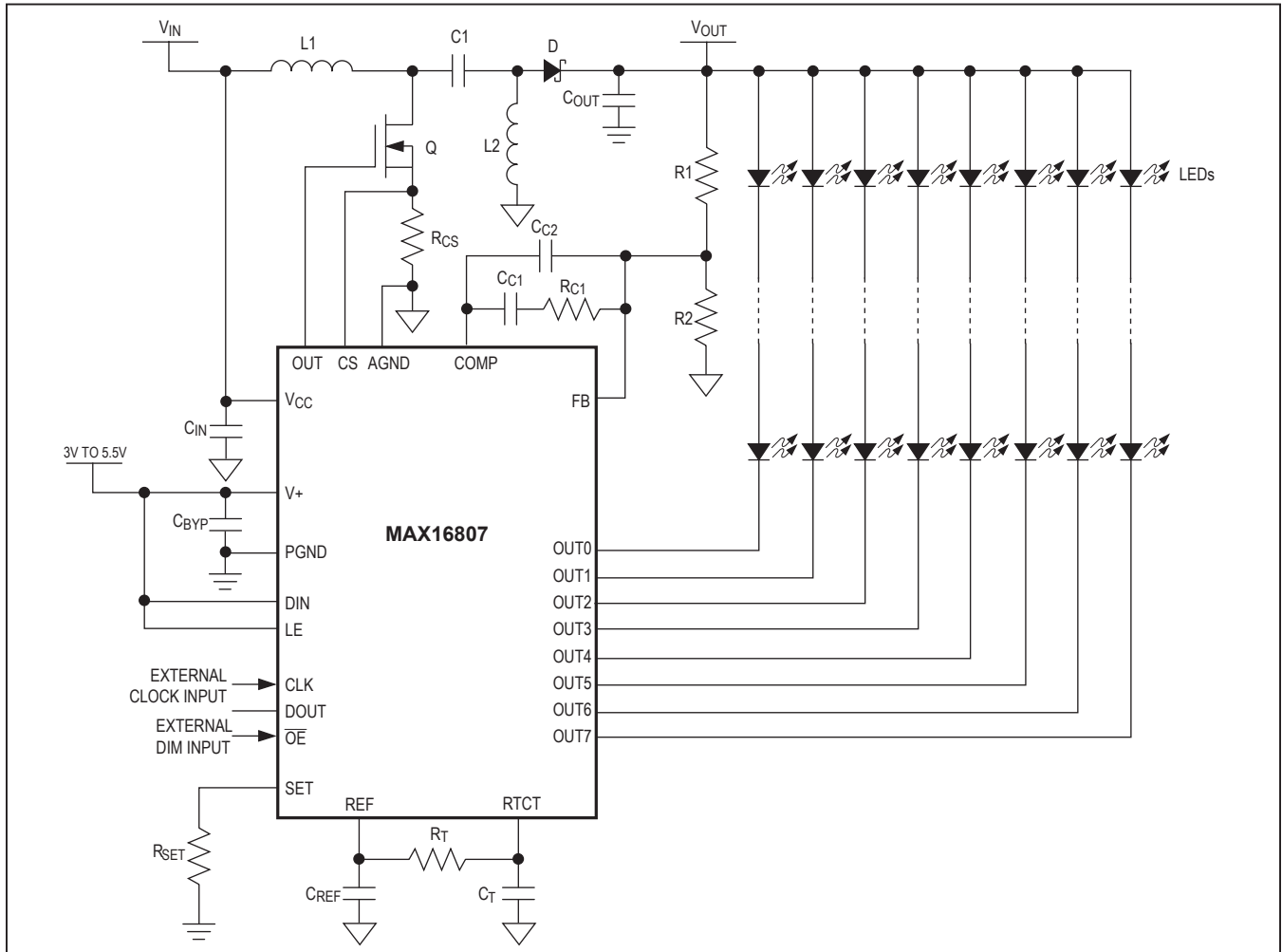


Figure 2. Buck-Boost (SEPIC) Configuration

**LED Driver**

**4-Wire Interface**

The MAX16807 also operates in stand-alone mode (see the *Typical Operating Circuits*). For use with a microcontroller, the MAX16807 features a 4-wire serial interface using DIN, CLK, LE,  $\overline{OE}$  inputs and DOUT as a data output. This interface is used to write the LED channels' data to the MAX16807. The serial-interface data word length is 8 bits (D0–D7). See Figure 3.

The functions of the five interface pins are as follows:

DIN is the serial-data input, and must be stable when it is sampled on the rising edge of CLK. Data is shifted in MSB first. This means that data bit D7 is clocked in first, followed by seven more data bits, finishing with the LSB (D0).

CLK is the serial-clock input that shifts data at DIN into the MAX16807's 8-bit shift register on its rising edge.

LE is the latch-enable input of the MAX16807 that transfers data from the 8-bit shift register to its 8-bit output latch (transparent latch). The data is latched on the falling edge of LE (Figure 4). The fourth input ( $\overline{OE}$ ) provides output-enable control of the output drivers. When  $\overline{OE}$  is driven high, the outputs (OUT0–OUT7) are forced to high impedance without altering the contents of the output latches. Driving  $\overline{OE}$  low enables the outputs to follow the state of the output latches.  $\overline{OE}$  is independent of the operation of the serial interface operation. Data can be shifted into the serial-interface shift register and latched, regardless of the state of  $\overline{OE}$ . DOUT is the serial-data output that

shifts data out from the MAX16807's 8-bit shift register on the rising edge of CLK. Data at DIN propagates through the shift register and appears at DOUT eight clock cycles later. Table 1 shows the 4-wire serial-interface truth table.

**Selecting External Component R<sub>SET</sub> to Set LED Output Current**

The MAX16807 uses an external resistor (R<sub>SET</sub>) to set the LED current for outputs OUT0–OUT7. The minimum allowed value of R<sub>SET</sub> is 330Ω, which sets the output currents to 55mA. The maximum allowed value of R<sub>SET</sub> is 5kΩ (I<sub>OUT\_</sub> = 3.6mA) and the maximum allowed capacitance at SET is 100pF.

Use the following formula to set the output current:

$$R_{SET} = \frac{18,000}{I_{OUT_}}$$

where I<sub>OUT\_</sub> is the desired output current in milliamps and the value for R<sub>SET</sub> is in ohms.

**Overtemperature Cutoff**

The MAX16807 contains an internal temperature sensor that turns off all outputs when the die temperature exceeds +165°C. The outputs are enabled again when the die temperature drops below +140°C. Register contents are not affected, so when a driver is overdissipating, the external symptom is the load LEDs cycling on and off as the driver repeatedly overheats and cools, alternately turning itself off and then back on again.

**Table 1. 4-Wire Serial-Interface Truth Table**

| SERIAL DATA INPUT DIN | CLOCK INPUT | SHIFT REGISTER CONTENTS |    |    |     |      |      | LOAD INPUT | LATCH CONTENTS |    |    |     |      |    | BLANKING INPUT  | OUTPUT CONTENTS CURRENT AT OUT <sub>_</sub> |    |    |     |      |    |
|-----------------------|-------------|-------------------------|----|----|-----|------|------|------------|----------------|----|----|-----|------|----|-----------------|---|----|----|-----|------|----|
|                       | CLK         | D0                      | D1 | D2 | ... | Dn-1 | Dn   | LE         | D0             | D1 | D2 | ... | Dn-1 | Dn | $\overline{OE}$ | D0  | D1 | D2 | ... | Dn-1 | Dn |
| H                     |             | H                       | R0 | R1 | ... | Rn-2 | Rn-1 |            |                |    |    |     |      |    |                 |   |    |    |     |      |    |
| L                     |             | L                       | R0 | R1 | ... | Rn-2 | Rn-1 |            |                |    |    |     |      |    |                 |   |    |    |     |      |    |
| X                     |             | R0                      | R1 | R2 | ... | Rn-1 | Rn   |            |                |    |    |     |      |    |                 |   |    |    |     |      |    |
|                       |             | X                       | X  | X  | ... | X    | X    | L          | R0             | R1 | R2 | ... | Rn-1 | Rn |                 |   |    |    |     |      |    |
|                       |             | P0                      | P1 | P2 | ... | Pn-1 | Pn   | H          | P0             | P1 | P2 | ... | Pn-1 | Pn | L               | P0  | P1 | P2 | ... | Pn-1 | Pn |
|                       |             |                         |    |    |     |      |      |            | X              | X  | X  | ... | X    | X  | H               | L   | L  | L  | ... | L    | L  |

- L = Low Logic Level
- H = High Logic Level
- X = Don't Care
- P = Present State (Shift Register)
- R = Previous State (Latched)



**Computing Power Dissipation**

Use the following equation to estimate the upper-limit power dissipation (PD) for the MAX16807:

$$PD = DUTY \times \left[ (V_{+} \times I_{+}) + \sum_{i=0}^{i=7} V_{OUTi} \times I_{OUTi} \right] + (V_{CC} \times I_{CC})$$

where:

V+ = Supply voltage

I+ = Operating supply current

DUTY = PWM duty cycle applied to  $\overline{OE}$

V<sub>OUTi</sub> = MAX16807 port output voltage when driving load LED(s)

I<sub>OUTi</sub> = LED drive current programmed by R<sub>SET</sub>

PD = Power dissipation

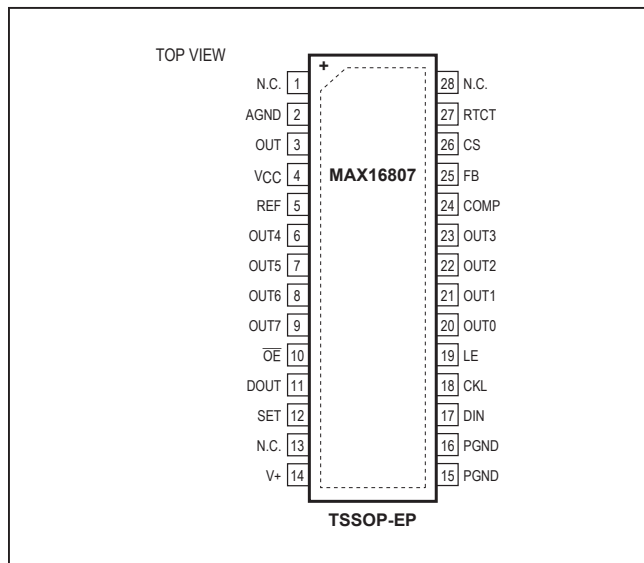
**PCB Layout Guidelines**

Careful PCB layout is critical to achieve low switching losses and clean, stable operation. Use a multilayer board whenever possible for better noise immunity. Protect sensitive analog grounds by using a star ground configuration. Minimize ground noise by connecting AGND, PGND, the input bypass-capacitor ground lead, and the output-filter ground lead to a single point (star ground configuration). Also, minimize trace lengths to reduce stray capacitance, trace resistance, and radiated noise. The trace between the output voltage-divider and the FB pin must be kept short, as well as the trace between AGND and PGND.

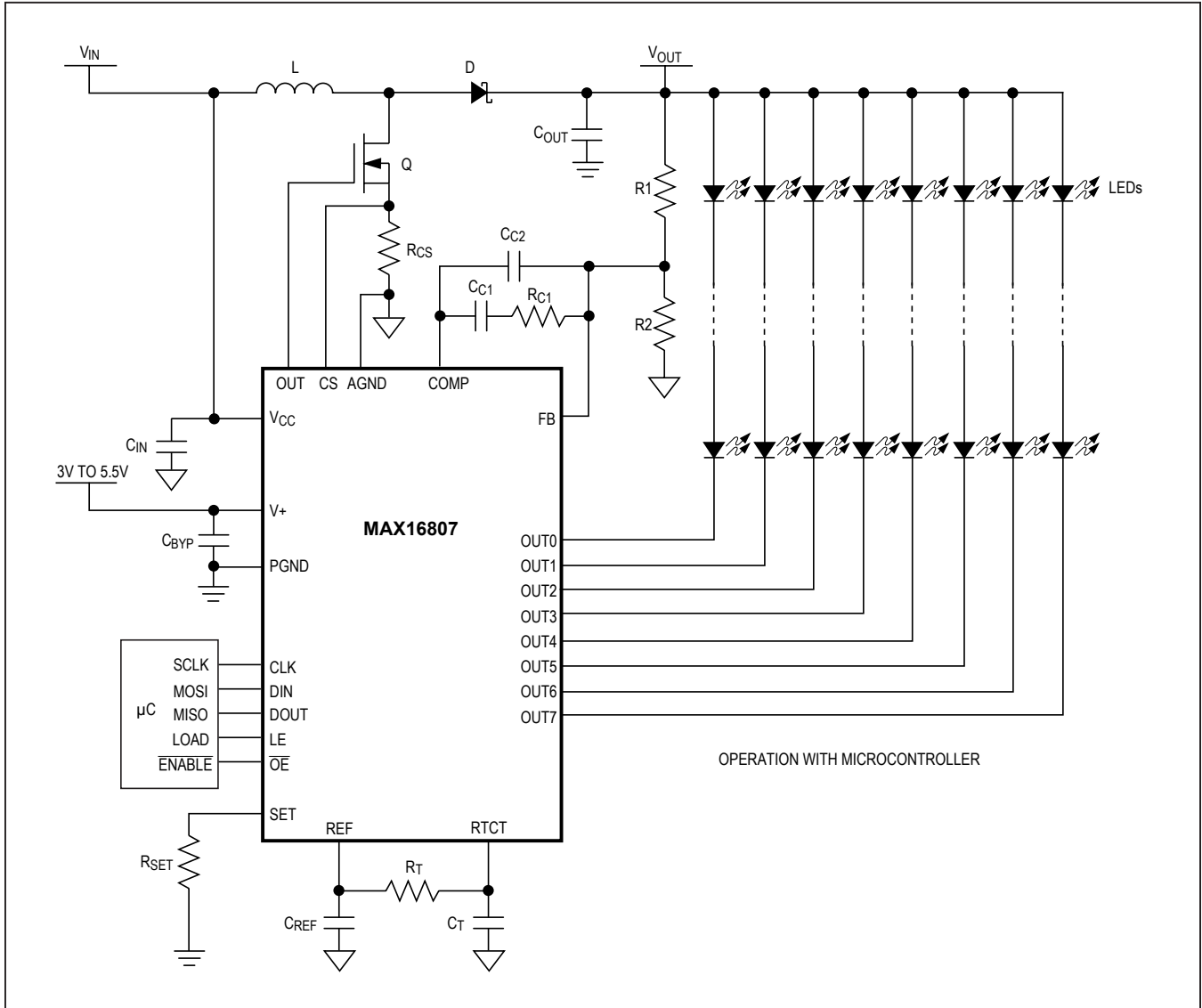
**Chip Information**

PROCESS: BiCMOS

**Pin Configuration**



Typical Operating Circuits (continued)



Package Information

For the latest package outline information and land patterns (footprints), go to [www.maximintegrated.com/packages](http://www.maximintegrated.com/packages). Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

| PACKAGE TYPE | PACKAGE CODE | DOCUMENT NO.            |
|--------------|--------------|-------------------------|
| 28 TSSOP     | U28ME+1      | <a href="#">21-0108</a> |

## Revision History

| REVISION NUMBER | REVISION DATE | DESCRIPTION  | PAGES CHANGED |
|-----------------|---------------|--|---------------|
| 0               | 10/06         | Initial release  | —             |
| 1               | 4/07          | Release of the MAX16808  | 1             |
| 2               | 8/09          | Removal of the MAX16808 from the data sheet.   | 1–21          |
| 3               | 11/14         | No <i>I</i> V OPN in <i>Ordering Information</i> , removed automotive reference in <i>Applications</i> section | 1             |

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim Integrated's website at [www.maximintegrated.com](http://www.maximintegrated.com).

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