



**THE DATASHEET OF
MC33389CDH**



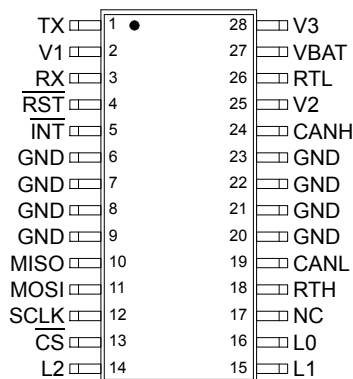


Table 2. 33389 Pin Definitions: SOICW 28-Lead

A functional description of each pin can be found in the Functional Pin Description section beginning on [page 17](#).

Pin Number	Pin Name	Formal Name	Definition
1	TX	Transmitter Data	Transmitter input of the LS CAN interface
2	V1	Voltage Regulator One	This 5.0 V pin is a 3% low drop voltage regulator dedicated to the microcontroller supply.
3	RX	Receiver Data	Receiver output of the LS CAN interface
4	$\overline{\text{RST}}$	Reset	This is an Input/Output pin.
5	$\overline{\text{INT}}$	Interrupt	This output is asserted LOW when an enabled interrupt condition occurs.
6 -9 20 - 23	GND	Ground	These device ground pins are internally connected to the package lead frame to provide a 33389-to-PCB thermal path.
10	MISO	Master In/Slave Out	This pin is the tri-state output from the shift register.
11	MOSI	Master Out/Slave In	This pin is for the input of serial instruction data.
12	SCLK	System Clock	This pin clocks the internal shift registers.
13	$\overline{\text{CS}}$	Chip Select	This pin communicates with the system MCU and enables SPI communication.
14, 15, 16	L0: L2	Wake-up Input (L0: L2)	Input interfaces to external circuitry. Levels at these pins can be read by SPI and input can be used as programmable wake-up input in Sleep or Stop mode.
17	NC	No Connect	This pin does not connect.
18	RTH	Thermal Resistance High	Pin for the connection of the bus termination to CANH
19	CANL	CAN Low	CAN low input/output
24	CANH	CAN High	CAN high input/output
25	V2	Voltage Regulator Two	This 5.0 V pin is a low drop voltage regulator dedicated to the peripherals supply.
26	RTL	Thermal Resistance Low	Pin for the connection of the bus termination to CANL
27	VBAT	Voltage Battery	This pin is voltage supply from the battery.
28	V3	Voltage Regulator Three	This pin is a 10 Ω switch to V_{BAT} , used to supply external contacts or relays.

Table 3. Maximum Ratings (continued)

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Ratings	Symbol	Value	Unit
THERMAL RESISTANCE			
RTH, RTL Termination Resistance	R_{RTHRTL}	500 to 16 k	Ω
Junction to Heatsink Thermal Resistance for HSOP-20 33% Power on V1, 66% on V2 (including CAN) ⁽²⁾	R_{AJC}	3.1	$^{\circ}\text{C/W}$
Junction to Pin Thermal Resistance for SO-28WD ⁽³⁾	$R_{AS/P}$	17	$^{\circ}\text{C/W}$
Thermal Shutdown Temperature	T_{SD}	165	$^{\circ}\text{C}$
Peak Package Reflow Temperature During Reflow ^{(4), (5)}	T_{PPRT}	Note 5	$^{\circ}\text{C}$

Notes

- Refer to thermal management in device description section.
- Refer to thermal management in device section. Ground pins 6, 7, 8, 9, 20, 21, 22, and 23 of SO28WB package.
- Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
- Freescale's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), Go to www.freescale.com, search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts. (i.e. MC33xxxD enter 33xxx), and review parametrics.

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Table 4. Static Electrical Characteristics (continued)

Characteristics noted under conditions V_{BAT} , $-40^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$ unless otherwise noted. Typical values noted reflect the approximate parameter means at $T_A = 25^{\circ}\text{C}$ under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER OUTPUT (CONTINUED)					
V1 Output Current Limitation $V1_{NOM} - 100\text{ mV}$	I1MAX	130	170	200	mA
V1 Overtemperature Shut OFF Threshold Junction Temperature	TV1H	160	—	190	$^{\circ}\text{C}$
V1 Pre-Warning Temperature Threshold Junction Temperature	TV1L	130	—	160	$^{\circ}\text{C}$
V1 Temperature Threshold Difference	TV1H-TV1L	20	—	40	$^{\circ}\text{C}$
V1 Reset Threshold on V1 $5.5\text{ V} < V_{BAT} < 27\text{ V}$	VR1	4.1 V2 - 0.4	4.3 V1 - 0.28	4.8 V1 - 0.1	V
		(C Version)			
		(D Version)			
V1 Reset Active V1 Range	V1R	1.0	VR1	—	V
V1 Reverse Current from V1 to V_{BAT} and GND $V1 = 4.9\text{ V}$, $0 < V_{BAT} < 4.9\text{ V}$	IREV	—	—	1.0	mA
V2 Output Voltage $0\text{ mA} < I_{OUT} < 200\text{ mA}$, $5.5\text{ V} < V_{BAT} < 40\text{ V}$	V2NOM	4.75	5.0	5.25	V
V2 Drop Voltage $I_{OUT} = 200\text{ mA}$ ⁽⁷⁾	V2DROP	—	0.2	0.5	V
V2 Drop Voltage $I_{OUT} = 20\text{ mA}$ ⁽⁷⁾	V2DROP	—	0.05	0.15	V
V2 Output Current Limitation $V2_{NOM} - 100\text{ mV}$	I1MAX	220	280	350	mA
V2 Threshold on V2 to Report V2 OFF V2 Nominal	VR2	4.1	4.55	4.75	V
VR2 Delay Time	VR2	20	—	70	μs
V2 Overtemperature Pre-Warning Threshold V2 Junction Temperature	TV2L	130	—	160	$^{\circ}\text{C}$
V2 Overtemperature Switch-OFF Threshold V2 Junction Temperature	TV2H	155	—	185	$^{\circ}\text{C}$
V2 Line Regulation $9.0\text{ V} < V_{BAT} < 16.5$	V2LR1	-15	—	+15	mV
V2 Load Regulation $4.0\text{ mA} < I_{LOAD} < 200\text{ mA}$	V2LR2	-75	—	+75	mV
V2 Line Ripple Rejection 100 Hz , 1.0 V_{PP} on V_{BAT} ⁽⁸⁾	V2LRR	30	55	—	dB

Notes

7. Measured when V1 has dropped 100mV below its nominal value
8. Guaranteed by design; however, it is not production tested

Table 4. Static Electrical Characteristics (continued)

Characteristics noted under conditions V_{BAT} , $-40^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$ unless otherwise noted. Typical values noted reflect the approximate parameter means at $T_A = 25^{\circ}\text{C}$ under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER OUTPUT (CONTINUED)					
V2 Percentage Difference V2-V1 $V_{BAT} > 9.0$, $I_{V1} = 20$ mA, $I_{V2} = 40$ mA	$V2_{V2-V1}$	-3.0	—	3.0	%
V3 High Level Voltage Drop $I_{V3} = -50$ mA, $9.0 \text{ V} < V_{BAT} < 40 \text{ V}$	$V3_{DROP}$	—	0.4	1.0	V
V3 High Level Voltage Drop $I_{V3} = -50$ mA, $6.0 \text{ V} < V_{BAT} < 9.0 \text{ V}$	$V3_{DROP}$	—	—	1.5	V
V3 Leakage Output Limitation $5.5 \text{ V} < V_{BAT} < 27 \text{ V}$	$I3_{LIM}$	100	150	250	mA
V3 Leakage Current $V3 = 0$ (V3 OFF)	$I3_{LEAK}$	—	—	15	μA
V3 Overtemperature Detection Junction Temperature	T_{V3}	155	—	185	$^{\circ}\text{C}$
V3 Voltage with -30 mA (negative current for Relay Switch OFF) No Functional Error Allowed for $t \leq 100$ ms	V_{V3}	0.3	—	0.5	V
CAN Transceiver V2 for Forced Bus Stand-by Mode (Fail Safe)	VRC2	3.0	3.9	4.7	V
CANH/L Differential Receiver, Threshold Voltage	V_{CANTH}	-3.2	—	-2.5	V
CANH/L Differential Receiver, Dominant to Recessive Threshold (Bus Failures 1, 2, and 5)	$V_{CANDRTH}$	-3.2	—	-2.5	V
CANH Recessive Output Voltage TX = High, $R(RTH) < 4.0$ k	V_{CANH}	—	—	0.2	V
CANL Recessive Output Voltage TX = High, $R(RTH) < 4.0$ k	V_{CANL}	V2-0.2	—	—	V
CANH Output Voltage, Dominant TX = 0 V, Bus Normal Mode, $I_{CANH} = -40$ mA	V_{CANH}	V2-1.4	—	—	V
CANL Output Voltage, Dominant TX = 0 V, Bus Normal Mode, $I_{CANL} = -40$ mA	V_{CANL}	—	—	1.4	V
CANH Output Current Limit ($V_{CANH} = 0.0$ V, TX = 0)	I_{CANH}	50	75	100	mA
CANL Output Current Limit ($V_{CANL} = 14$ V, TX = 0)	I_{CANL}	50	95	130	mA
Detection Threshold for Short Circuit to Battery Voltage Bus Normal Mode	$V_{CANH}-V_{CANL}$	7.3	7.9	8.9	V
Detection Threshold for Short Circuit to Battery Voltage Bus Stand-by Mode	V_{CANH}	$V_{BAT}/2+3$	—	$V_{BAT}/2+5$	V
CANH Output Current, Failure 3 Bus Stand-by Mode $V_{CANH} = 12$ V	I_{CANHF3}	—	5.0	10	μA
CANL Output Current, Failure 4 Bus Stand-by Mode, $V_{CANL} = 0.0$ V, $V_{BAT} = 12$ V	I_{CANLF4}	—	0.0	2.0	μA

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Table 4. Static Electrical Characteristics (continued)

Characteristics noted under conditions V_{BAT} , $-40^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$ unless otherwise noted. Typical values noted reflect the approximate parameter means at $T_A = 25^{\circ}\text{C}$ under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER OUTPUT (CONTINUED)					
CANL Wake-Up Voltage Threshold Bus Stand-by Mode	V_{WAKEL}	2.5	3.3	3.9	V
CANH Wake-Up Voltage Threshold Bus Stand-by Mode	V_{WAKEH}	1.2	2.0	2.7	V
Wake-Up Threshold Difference	$V_{WAKEL} - V_{WAKEH}$	0.2	—	—	V
CANH Single Ended Receiver Threshold Failures 4, 6, and 7	V_{CANH}	1.5	1.85	2.15	V
CANL Single Ended Receiver Threshold Failures 3 and 8	V_{CANL}	2.8	3.05	3.4	V
CANL Pull-Up Current Bus Normal Mode	I_{CANLPU}	45	75	90	μA
CANH Pull Down Current Bus Normal Mode	I_{CANLPD}	45	75	90	μA
Receiver Differential Input Impedance CANH/CANL	R_{DIFF}	100	—	180	$\text{k}\Omega$
Differential Receiver Common Mode Voltage Range	V_{COM}	-8.0	—	8.0	V
RTL to V2 Switch on Resistance $I_{OUT} < -10 \text{ mA}$, Bus Normal Operating Mode	R_{RTL}	10	25	70	Ω
RTL to Battery Switch Series Resistance Bus Stand-by Mode	R_{RTL}	8.0	12.5	20	$\text{k}\Omega$
RTH to Ground Switch on Resistance $I_{OUT} < 10 \text{ mA}$, All Modes	R_{RTH}	—	25	70	Ω
CONTROL INTERFACE					
High Level Input Voltage	V_{IH}	0.7 V1	—	$V1 + 0.3 \text{ V}$	V
$\overline{\text{CS}}$ Threshold for SPI Wake-Up SBC in Sleep Mode, $V1 < 1.5 \text{ V}$	V_{CSTH}	—	2.2	—	V
$\overline{\text{CS}}$ Filter Time for SPI Wake-Up SBC in Sleep Mode, $V1 < 1.0 \text{ V}$	t_{CSFT}	—	—	3.0	μs
Low Level Input Voltage	V_{IL}	-0.3	—	0.3 V1	V
High Level Input Current on $\overline{\text{CS}}$ $V_I = 4.0 \text{ V}$	I_{CSH}	-100	—	-20	μA
Low Level Input Current on $\overline{\text{CS}}$ $V_I = 1.0 \text{ V}$	I_{CSL}	-100	—	-20	μA
TX High Level Input Current $V_I = 4.0 \text{ V}$	I_{TXH}	-200	-80	-25	μA
TX Low Level Input Current $V_I = 1.0 \text{ V}$	I_{TXL}	-800	-320	-100	μA
SI, SCLK Input Current $0 < V_{IN} < V1$	I_{SISLK}	-10	—	+10	μA

DYNAMIC ELECTRICAL CHARACTERISTICS

Table 5. Dynamic Electrical Characteristics

Characteristics noted under conditions $7.0\text{ V} \leq V_{\text{SUP}} \leq 18\text{ V}$, $-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$, $GND = 0\text{ V}$ unless otherwise noted. Typical values noted reflect the approximate parameter means at $T_A = 25^\circ\text{C}$ under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
MICROCONTROLLER INTERFACE					
AC CANL/CANH Slew Rates, Rising or Falling Edges, TX from Recessive to Dominant State $C_{\text{LOAD}} - 10\text{ nF}$, $133\ \Omega$ Termination Resistors	t_{CANRD}	3.5	5.0	10	V/ μs
AC CANL/CANH Slew Rates, Rising or Falling Edges, TX from Dominant to Recessive State $C_{\text{LOAD}} - 10\text{ nF}$, $133\ \Omega$ Termination Resistors	t_{CANDR}	2.0	3.5	10	V/ μs
AC Propagation Delay TX to RX Low $C_{\text{LOAD}} - 10\text{ nF}$, $133\ \Omega$ Termination Resistors	t_{DH}	—	1.2	2.0	μs
AC Propagation Delay TX to RX High $C_{\text{LOAD}} - 10\text{ nF}$, $133\ \Omega$ Termination Resistors	t_{DL}	—	2.0	3.0	μs
Wake-Up Filter Time	t_{WUFT}	8.0	20	38	μs
RST Duration after V1 High	t_{RES}	—	1.0	—	ms
SCLK Clock Period	t_{PSCLK}	500	—	—	ns
SCLK Clock High Time	t_{WSCLKH}	175	—	—	ns
SCLK Clock Low Time	t_{WSCLKL}	175	—	—	ns
Falling Edge of $\overline{\text{CS}}$ to Rising Edge of SCLK	t_{LEAD}	250	50	—	ns
Falling Edge of SCLK to Rising Edge of $\overline{\text{CS}}$	t_{LEAD}	250	50	—	ns
SI to Falling Edge of SCLK	t_{SISU}	125	25	—	ns
Falling Edge of SCLK to SI	$t_{\text{SI(HOLD)}}$	125	25	—	ns
SO Rise Time ($C_L = 200\text{ pF}$)	t_{RSO}	—	25	75	ns
SO Fall Time ($C_L = 200\text{ pF}$)	t_{FSO}	—	25	75	ns
SI, $\overline{\text{CS}}$, SCLK Incoming Signal Rise Time	t_{RSI}	—	—	200	ns
SI, $\overline{\text{CS}}$, SCLK Incoming Signal Fall Time	t_{FSI}	—	—	200	—
Time from Falling Edge of CS to SO Low Impedance High Impedance	$t_{\text{SO(EN)}}$ $t_{\text{SO(DIS)}}$	—	—	200 200	ns
Time from Rising Edge of SCLK to SO Data Valid $0.2\text{ V}_1\text{ or }V_2 \leq \text{SO} \leq 0.8\text{ V}_1\text{ or }V_2$, $C_L = 200\text{ pF}$	t_{VALID}	—	50	125	—
Running Mode Oscillator Tolerance (Normal Request, Normal and Stand-by Modes ⁽⁹⁾)	RMOT	-12	—	+12	%
Software Watchdog Timing 1 ⁽⁹⁾	t_{SW1}	4.4	5.0	5.6	ms
Software Watchdog Timing 2 ⁽⁹⁾	t_{SW2}	8.8	10	11.2	ms
Software Watchdog Timing 3 ⁽⁹⁾	t_{SW3}	17.6	20	22.4	ms
Software Watchdog Timing 4 ⁽⁹⁾	t_{SW4}	28	32	36	ms

Notes

9. Software watchdog timing accuracy is based on the running mode oscillator tolerance

Table 5. Dynamic Electrical Characteristics (continued)

Characteristics noted under conditions $7.0\text{ V} \leq V_{\text{SUP}} \leq 18\text{ V}$, $-40^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$, $\text{GND} = 0\text{ V}$ unless otherwise noted. Typical values noted reflect the approximate parameter means at $T_A = 25^{\circ}\text{C}$ under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
BUS TRANSMITTER (CONTINUED)					
AC Failure 4, 7, and 8 Recovery Time Bus Normal Mode	t_{AC478R}	10	—	60	μs
AC Failure 3, 4, and 7 Detection Time Bus Stand-by Mode, $V_{\text{BAT}} = 12\text{ V}$	t_{AC347D}	0.8	—	8.0	ms
AC Failure 3, 4 and 7 Recovery Time Bus Stand-by Mode, $V_{\text{BAT}} = 12\text{ V}$	t_{AC347R}	—	2.5	—	ms
AC Edge Count Difference Between CANH/CANL for Failures 1, 2, 5 Detection Bus Normal Mode	$\text{CAN}_{125\text{D}}$	—	3.0	—	—
AC Edge Count Difference Between CANH/CANL for Failures 1, 2, 5 Recovery Bus Normal Mode	$\text{CAN}_{125\text{R}}$	—	3.0	—	—
TX Permanent Dominant Timer Disable Time Bus Normal and Failure Modes	t_{TXD}	0.75	—	4.0	ms
POWER INPUT TIMING					
V1 Reset Delay Time	t_{D}	2.0	—	20	μs
V1 Line Regulation $9.0\text{ V} < V_{\text{BAT}} < 16.5$, $I_{\text{LOAD}} = 10\text{ mA}$	t_{D}	-15	2.0	+15	mV
V1 Line Regulation $5.5\text{ V} < V_{\text{BAT}} < 27\text{ V}$ $I_{\text{LOAD}} = 10\text{ mA}$	t_{D}	-50	10	+50	mV
V1 Load Regulation $1.0\text{ mA} < I_{\text{LOAD}} < 100\text{ mA}$	t_{D}	-50	—	+50	mV
V1 Line Ripple Rejection 100 Hz, 1.0 V_{PP} on $V_{\text{BAT}} = 12\text{ V}$, $I_{\text{LOAD}} = 100\text{ mA}$ (12)	t_{D}	30	55	—	dB
V1 Line Transient Response V_{BAT} from 12 V to 40 V in $1.0\text{ }\mu\text{s}$, ($10\text{ }\mu\text{F}$, $\text{ESR} = 3\text{ }\Omega$)	t_{D}	—	27	—	mV
V1 Load Transient Response I_{LOAD} from $10\text{ }\mu\text{A}$ to 100 mA in $1.0\text{ }\mu\text{s}$ ($\text{CLOAD} = 10\text{ }\mu\text{F}$, $\text{ESR} = 3\text{ }\Omega$) (13)	t_{D}	—	400	—	mV
V1 Load Transient Response I_{LOAD} from $10\text{ }\mu\text{A}$ to 100 mA in $1.0\text{ }\mu\text{s}$ ($\text{CLOAD} = 10\text{ }\mu\text{F}$, $\text{ESR} = 0.1\text{ }\Omega$)	t_{D}	—	16	—	mV

Notes

- 12. Guaranteed by design. Not production tested.
- 13. This condition does not produce a reset

TIMING DIAGRAMS

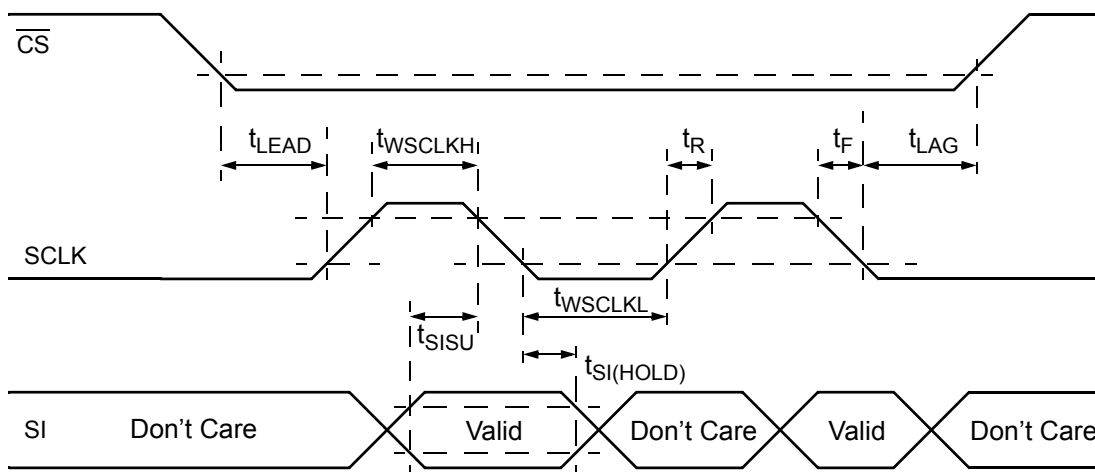


Figure 4. Input Timing Switch Characteristics

FUNCTIONAL DESCRIPTION

INTRODUCTION

The System Basis Chip (SBC) is an integrated circuit dedicated to car body applications. It includes three main blocks:

1. A dual voltage regulator
2. Reset, watchdog, wake-up inputs, cyclic wake-up

3. CAN low speed fault tolerant physical interface

Supplies

Two low drop regulators and one switch to V_{BAT} are provided to supply the ECU microcontroller or peripherals, with independent control and monitoring through SPI.

FUNCTIONAL PIN DESCRIPTION

TRANSMIT AND RECEIVE DATA (TX AND RX)

The RX and TX pins (receive data and transmit data pins, respectively) are connected to a microcontroller's CAN protocol handler. TX is an input and controls the CANH and CANL line state (dominant when TX is LOW, recessive when TX is HIGH). RX is an output and reports the bus state.

VOLTAGE REGULATOR ONE AND TWO (V1 AND V2)

The V1 pin is a 3% low drop voltage regulator dedicated to the microcontroller supply (nominal 5V supply).

The V2 pin is a low drop voltage regulator dedicated to the peripherals supply (nominal 5V supply).

RESET (\overline{RST})

The \overline{RST} (reset) pin is an input/output pin. The typical reset duration from SBC to microcontroller is 1ms. If longer times are required, an external capacitor can be used. SBC provides two \overline{RST} output pull-up currents. A typical 30 μ A pull up when V_{reset} is below 2.5V and a 300 μ A pull up when reset voltage is higher than 2.5V. \overline{RST} is also an input for the SBC. It means the MC33389 is forced to Normal Request mode after \overline{RST} is released by the microcontroller.

INTERRUPT (\overline{INT})

The Interrupt pin \overline{INT} is an output that is set LOW when an interrupt occurs. \overline{INT} is enabled using the Interrupt Register (INTR). When an interrupt occurs, \overline{INT} stays LOW until the interrupt source is cleared.

\overline{INT} output also reports a wake-up event.

GROUND (GND)

This pin is the ground of the integrated circuit.

MASTER IN/ SLAVE OUT (MISO)

MISO is the Master In Slave Out pin of the serial peripheral interface. Data is sent from the SBC to the microcontroller through the MISO pin.

MASTER OUT/ SLAVE IN (MOSI)

MOSI is the Master Out Slave In pin of the serial peripheral interface. Control data from a microcontroller is received through this pin.

SYSTEM CLOCK (SCLK)

This pin clocks the internal shift registers for SPI communication.

CHIP SELECT (\overline{CS})

\overline{CS} is the Chip Select pin of the serial peripheral interface (SPI). When this pin is LOW, the SPI port of the device is selected.

LEVEL 0-2 INPUTS (L0: L2)

The L0: L2 pins can be connected to contact switches or the output of other ICs for external inputs. The input states can be read by the SPI. These inputs can be used as wake-up events for the SBC.

NO CONNECT (NC)

No pin connection.

TERMINATION RESISTANCE (HIGH AND LOW?) (RTH AND RTL)

External CAN bus high and low termination resistance pins are connected to these pins.

CAN HIGH AND CAN LOW OUTPUTS (CANH AND CANL)

The CAN High and CAN Low pins are the interfaces to the CAN bus lines. They are controlled by TX input level, and the state of CANH and CANL is reported through RX output.

VOLTAGE BATTERY (VBAT)

This pin is the voltage supply from the battery.

VOLTAGE REGULATOR THREE (V3)

This pin is a 10 Ω switch to VBAT, which is used to supply external contacts or relays.

Table 8. V3 Control

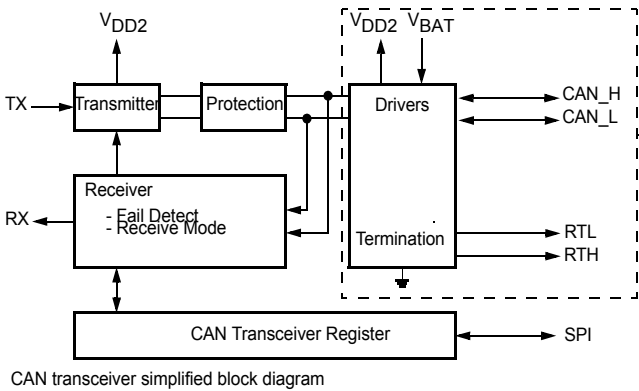
—	In Sleep Mode, During Disable Time of Cyclic Sense if Configured
—	Over Temp Threshold Reached
—	V1 Disabled (for any reason)
—	V2 Over Temperature Shutdown

Supply and V_{BAT} Block

- **V_{BAT} Monitoring**—V_{BAT} is the main power supply coming from the battery voltage after an external protection diode (for reverse battery). V_{BAT} is monitored for under voltage and over voltage.
- **V_{BAT} Under Voltage**—V_{BAT} is monitored for under voltage if it is below 4.0 V the BatFail flag is set in the VSSR register and a maskable interrupt is sent to the microcontroller.
- **V_{BAT} Over Voltage**— When V_{BAT} is > 20 V, the BatHigh flag is set in the VSSR register. A maskable interrupt is sent to the microcontroller. No specific action is taken to reduce current consumption (to limit power dissipation). This is to allow the entire flexibility to the microcontroller for a decision.

CAN Transceiver

The device incorporates a low speed 125 kBaud CAN physical interface. Its electrical parameters for the CANL,



CANH, RTL, RTH, RX, and TX pins are identical to the 33388, stand alone CAN physical interface.

The mode control for the CAN transceiver (Normal, V_{BAT} Stand-by, Sleep, etc.) are selectable through the 33389 SPI interface.

- Baud Rate up to 125 kBit/s
- Supports unshielded bus wires
- Short-circuit proof to battery and ground in 12 V powered systems
- Supports single-wire transmission modes with ground offset voltages up to 1.5 V
- Automatic switching to single wire mode in case of bus failures
- Automatic reset to differential mode if bus failure is removed
- Low Electromagnetic Interference (EMI) due to built-in slope control and signal symmetry
- Fully integrated receiver filters
- Thermally protected
- Bus lines protected against automotive transients
- Low current Bus Stand-by mode with wake-up capability via the bus
- An unpowered node does not disturb the bus lines

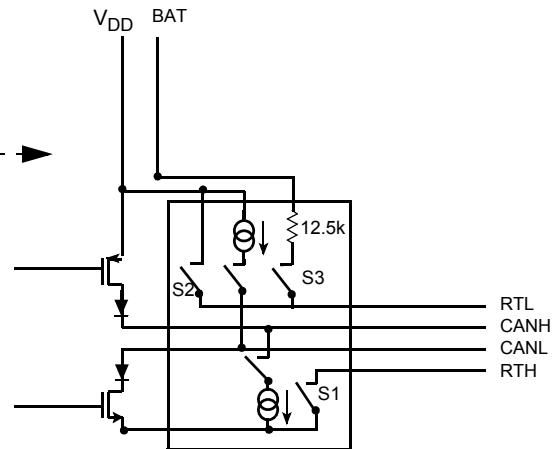


Figure 5. CAN Simplified Block Diagram

CONSEQUENCE OF FAILURE DETECTIONS

- S1 is the switch from RTH to Ground
- S2 is the switch from RTL to V2 and
- S3 is the switch from RTL to V_{BAT}

Each failure type provides data concerning which switch is open and which driver is disabled.

- Failure 1: Nothing done
- Failure 2: Nothing done
- Failure3: S1 open. Driver CANH is disabled

- Failure4: S2 and S3 open. Driver CANL is disabled
- Failure5: Nothing done
- Failure6: S2 and S3 open. Driver CANL disabled
- Failure7: S2 and S3 open. Driver CANL disabled

Failure8: S1 Open. CANH driver disable

CAN Transceiver Description

The CAN transceiver is an interface between CAN protocol controller and the physical bus. It is intended for low

speed applications up to 125 kBit/s in passenger cars. It provides differential transmission capability, but will switch in error condition to single wire transmitter and/or receiver.

The rise and fall slopes are limited to reduce radio frequency interference (RFI). This provides use of an unshielded twisted pair or a parallel pair of wires for the bus. It supports transmission capability on either bus wire if one of the bus wire is corrupted. The logic failure detection automatically selects a suitable transmission mode.

In a normal operation (no wiring failures), the differential bus state is the output to RX. The differential receiver inputs are connected to CANH and CANL through integrated filters. The filtered inputs signals are also used for the single wire receivers. The CANH and CANL receivers have threshold voltages, assuring maximum noise margin in single wire modes. In the RX Only mode, the transmitter is disabled; however, the receive part of the transceiver remains active. In this mode, RX reports bus and TX activity (RX = TX or Bus dominant). Failure detection and management is the same as the Bus Normal mode.

Failure Detector

The failure detector is active in RXTX and RX Only operation modes. The detector recognizes the following single bus failures and switches to an appropriate mode.

1. CANH wire interrupted
2. CANL wire interrupted or shorted to 5.0 V
3. CANH short-circuit to battery
4. CANL short-circuit to ground
5. CANH short-circuit to ground
6. CANL short-circuit to battery
7. CANL mutually shorted to CANH
8. CANH to V2 (5.0 V)

Note: Shorts-circuit failures are detected for 0 to 50 Ω shorts.

The differential receiver (CANH-CANL) threshold is set at -2.8 V, this assures a proper reception in the normal operating modes. In case of failures 1, 2, and 5 the on-going message is not destroyed due to noise margin.

Failures 3 and 6 are detected by comparators respectively connected to CANH and CANL. If the comparator threshold is exceeded for a certain time (T_{AC3D} , T_{AC6D}), the reception is switched to single wire mode. This time is required to avoid false triggering by external RF fields. Recovery from these failures is detected automatically after a certain (T_{AC3R} , T_{AC6R}) time-out (filtering).

Failures 4 and 7 initially result in a permanent dominant level at RX. After a time-out, the CANL driver and the RTL pins are switched OFF. Only a weak pull-up at CANL remains. Reception continues by switching to Single Wire

mode through CANH. When Failures 4 or 7 are removed, the recessive bus levels are restored. If the differential voltage remains below the recessive threshold for a certain (T_{AC478R}) time, reception and transmission switch back to the Differential mode.

If any of the eight wiring failure occurs, a flag is set in the TESRH and TESRL Status registers. Eight different types of errors are distinguished out of these eight errors. They are separately stored in these register. Please refer to the [Tables 35](#) and [36](#). A maskable interrupt is sent to the microcontroller. On error recovery, the corresponding flag is reset after read-out operation.

During all single wire transmissions, the EMC performance (both immunity and emission) is worse than in the Differential mode. Integrated receiver filters suppress any high frequency noise induced into the bus wires. The cut-off frequency of these filters is a compromise between propagation delay and high frequency suppression. In the Single Wire mode, low frequency noise can not be distinguished from the expected signal.

In the event of a permanent dominant TX state (for more than 2.0 ms) the output drivers are disabled. That assures the operation of the complete system in case of a permanent dominant TX state of one control unit. The CAN interface of a defective ECU, which has TX permanently low, will automatically be set to the receive only mode and therefore will not lock the complete CAN bus.

Protection

A current limiting circuit protects the transmitter output stages against short-circuit to positive and negative battery voltage. If the junction temperature exceeds a maximum value, the transmitter output stages are disabled. Because the transmitter is responsible for a part of the power dissipation, this results in a reduced power dissipation resulting in a lower chip temperature. All other parts of the transceiver will remain operating. The CANH and CANL inputs are protected against electrical transients, and may occur in an automotive environment.

Thermal Management

The 33389 is proposed in two different packages:

1. HSOP-20 for high power applications
2. SO28WB with eight pins to the lead frame for medium power applications

HSOP20 Package

For such a package, the heat flow is mainly vertical and each heat source (dissipating element) can be seen as an independent thermal resistance to the Heatsink. The thermal network can be roughly depicted in [Figure 6](#).

Table 9. Normal Request: V1 Active and V2/V3 Passive

Entering Normal Request	Leaving Normal Request
SBC Reset Just Released	When First Receiving the SW Timing Word, SBC goes to Normal
—	If Time-out Without Receiving SPI Commands (75ms), SBC goes to Sleep

SBC Normal Mode

In this mode, V1 and V2 are active, V3 can be set active or passive via the SPI. Therefore, the whole ECU can be operated. Normal mode is entered by a SWCR configuration in the Normal Request mode.

Table 10. SBC Normal Mode: V1/V2 Active While V3 is Active or Passive

Entering Normal Mode	Leaving Normal Mode
By SPI command	By SPI command, going to any other mode
After SWCR register configuration in Normal Request mode	Watchdog time-out, going to Normal Request after activating Reset
—	V1 undervoltage detection, going to Normal Request mode after activating Reset

SBC Stand-by Mode

In this mode V1 is active and V2 is passive. V3 can be either permanently active or permanently passive. This is a low power mode with V1 active in order to have a fast reaction time in case of any wake-up.

For Stand-by mode, the S Bus Circuit (SBC) monitors the software. It means the microcontroller runs, is monitored, and must serve as a watchdog trigger.

Table 11. Stand-by: V1 Active, V2 Passive, V3 Active or Passive, Watchdog is Active

Entering Stand-by	Leaving Stand-by
—	If SW Timeout Going to Normal Request After Microcontroller Reset
By SPI Command	By SPI Command Going to any Other Mode

Table 11. Stand-by: V1 Active, V2 Passive, V3 Active or Passive, Watchdog is Active

Entering Stand-by	Leaving Stand-by
—	V1 Under Voltage Detection, Going to Normal Request Mode After Activating Reset
—	External Activation of the $\overline{\text{RST}}$ Pin

S Bus Circuit Sleep Mode

This is a low power consumption mode. V1 and V2 are disabled. V3 can be permanently disabled or cyclically active.

Table 12. SBC Sleep Mode: V1/V2 are Passive, V3 is Passive or Cyclic

Entering Sleep Mode	Leaving Sleep Mode
If SW Timing Not Configured 75 ms After Entering Normal Request Mode	CAN Wake-Up, Going to Normal Request
By SPI Command	If a Wake-Up is Detected with Cyclic Sense
For 33389ADW Only: If V1 is Below V1 Reset for More Than 100 ms	If a Wake-Up is Detected with Wake-Up Not Connected to V3 (permanent sense)
—	Forced Wake-Up (See Forced Wake-Up Section)
—	SPI Wake-Up (See Wake-Up by SPI Section)

Emergency Mode

In case the microcontroller detects the ECU or the system is no longer under control, it may decide to switch the SBC to the Emergency mode. V1, V2, and V3 become passive and wake-ups are not detected. The only way to leave this mode is to disconnect the ECU from the battery voltage (BatFail detection).

Table 13. SBC Emergency Mode: V1:V3 are Passive

Entering Emergency Mode	Leaving Emergency Mode
By SPI Command	SBC BatFail Detection (Disconnection of the Battery Voltage)

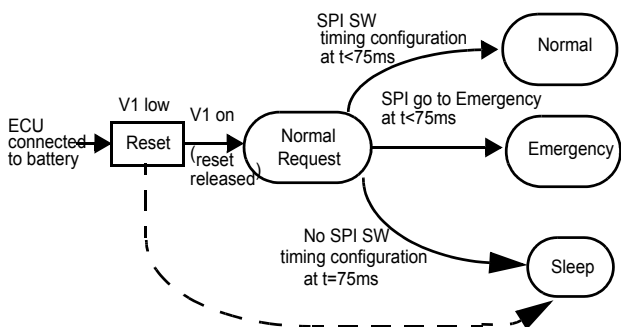


Figure 8. Typical Behavior at Power-On

Note: In the Normal Request mode, if a SPI command is received before the software timing configuration (SWCR register), it will not be taken into account by the SBC (except for the go-to Emergency mode).

Correspondence Between SBC and CAN Transceiver Modes

Table 14 provides different possible CAN transceiver modes versus SBC modes.

Table 14. CAN Modes vs. SBC Modes

When SBC Is In The Following Mode	CAN Transceiver Can Be In
Reset Condition	Bus Stand-by Mode
Normal Request	Bus Stand-by Mode
Normal	RXTX or RXOnly or BusStand-by
Stand-by	Bus Stand-by
Sleep	Bus Stand-by
Emergency	Bus Stand-by
Normal and V2 OFF (over load) In case V2 is turned OFF either by SPI command (Stand-by mode) or by the SBC itself due to V2 over load condition (V2 short to ground or V2 over temperature) the CAN is automatically set into the Bus Stand-by mode and does not return to TXRX mode automatically when V2 is back to 5.0 V. The CAN must be re configured to TXRX or RX Only mode after a V2 turn OFF	Bus Stand-by

Watchdog

The software window watchdog function monitors the microcontroller operation in the Normal and Stand-by modes.

The window watchdog timing is derived from the SBC clock. The desired watchdog timing must be first transmitted during the SBC configuration, in the Normal Request mode, via SPI to SWCR. It can also be changed later on. Selectable watchdog timings are 5.0 ms, 10 ms, 20 ms, 33 ms, 50 ms, 75 ms, 100 ms and 200 ms. These timings correspond to the full disable window plus full enable window.

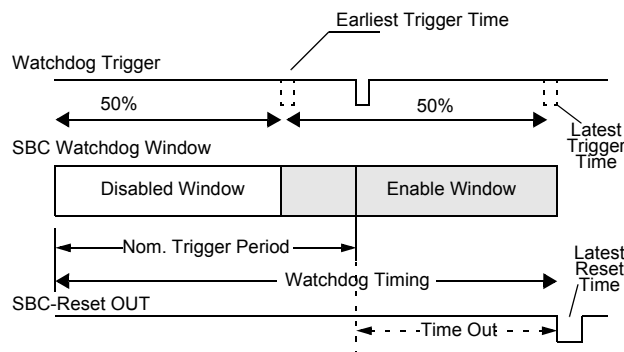


Figure 9. Window Watchdog Timing

As soon as the watchdog trigger is received in the Enable Window, the internal counter is reset and begins a new disable window. The SBC triggers the watchdog word at CS low-to-high transition. Any watchdog trigger outside the Enable Window leads to an SBC reset.

- Normal and Stand-by Modes— The SBC get the watchdog word from the microcontroller via SPI in the Normal mode. In case of a trigger time failure (no trigger or trigger outside the Enable Window) the SBC reset is switched to active.
- Normal Request, Sleep, and Emergency Mode— Watchdog is not active in these modes.

WAKE-UP CAPABILITIES

Several wake-up capabilities are available.

Forced Wake-Up

The forced wake-up is enabled and disabled by SPI in the V3 register. It is used to automatically wake-up the system by supplying V1 with proper reset in the Sleep mode. This corresponds to jump into the Normal Request mode. If the SBC is not properly configured within 75 ms, it switches back to the Sleep mode until the next wake-up. If both Cyclic Sense and Forced Wake-Up are enabled by the SPI while in the Sleep mode, only Cyclic Sense is active.

The period of Forced Wake-Up are 32 ms, 64 ms, 128 ms, 256 ms, 512 ms, 1024 ms, 2048 ms, and 8192 ms chosen by SPI in the Cyclic Timing Control Register (CYTCR).

Wake-Up Inputs (Local Wake-Up)/Cyclic Sense

SBC provides three wake-up inputs to monitor external events such as closing/opening of switches. The wake-up feature is available in Normal, Stand-by, and Sleep modes.

ARCHIVED

ARCHIVE INFORMATION

Mode	V1 & V2 Regulators, V3 Switch	Wake-Up Capabilities (if enabled)	Reset Pin (RST)	Interrupt Pin INT	Software Watchdog	CAN Cell
Normal	V1: ON V2: ON V3: ON/OFF	—	High (Active Low -go to Reset State if W/D or V1 Under Voltage Occurs)	If Enabled, Signal Failure Condition or L0, L1, L2 Inputs State Change	Running	Tx/Rx, or Rx Only, or Term V _{BAT}
Stand-by	V1: ON V2: OFF V3: ON/OFF	—	Same as Normal Mode	Same as Normal Mode	Running	Term V _{BAT}
Sleep	V1: OFF V2: OFF V3: OFF/Cyclic	<ul style="list-style-type: none"> • CAN • SPI • L0,L1,L2 • Cyclic Sense • Forced Wake-Up 	Low	Not Active	Not Running	Term V _{BAT} + Wake-Up Capability
Emergency	V1: OFF V2: OFF V3: OFF	None	Low	Not Active	Not Running	Term V _{BAT}

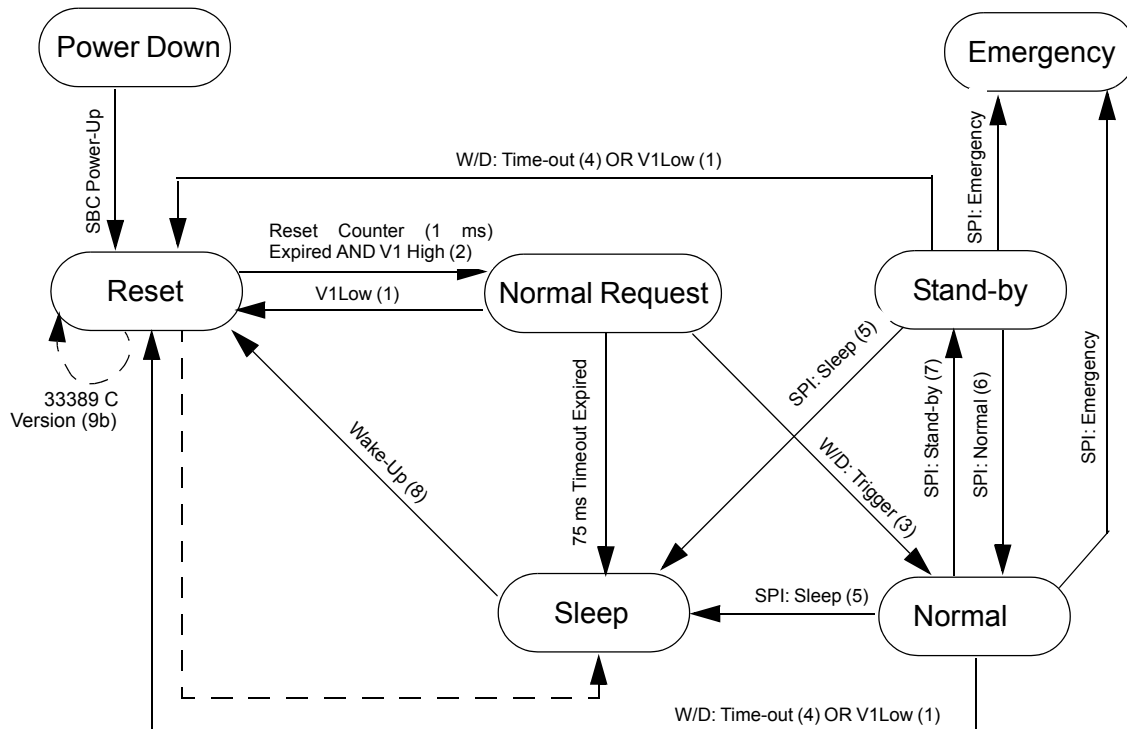


Figure 13. State Machine

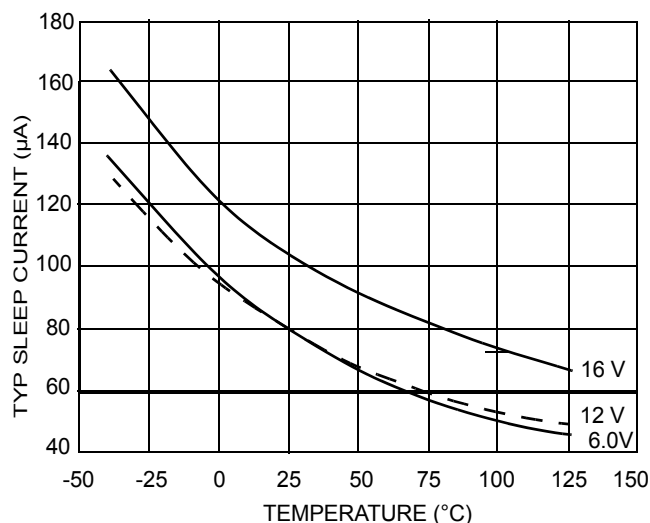


Figure 15. Current vs Temp and Batt Voltage

LOGIC COMMANDS AND REGISTERS

SPI Introduction

This SPI system is flexible enough to communicate directly with numerous standard peripherals and MCUs available from Motorola and other semiconductor manufacturers. SPI reduces the number of pins necessary for input/output on the 33389. The SPI system of communication consists of the MCU transmitting, and in return, receiving one data bit of information per clock cycle. Data bits of information are simultaneously transmitted by one pin, Microcontroller Out Serial In (MOSI), and received by another pin, Microcontroller In Serial Out (MISO), of the MCU. Figure 16 illustrates the basic SPI configuration between an MCU and one 33389. The SPI serial operation is guaranteed to 2.0 MHz.

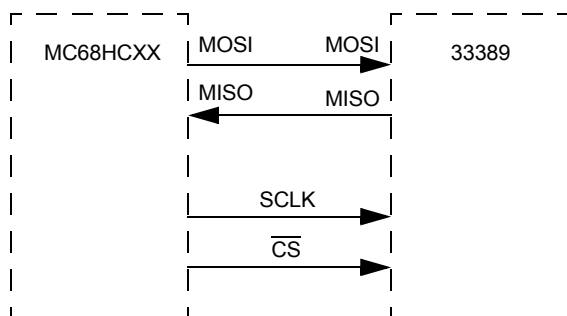


Figure 16. SPI Interface with Microcontroller

CS PIN

The system MCU selects the MC33389 to be communicated with, through the use of the CS pin. Whenever the pin is in logic low state, data can be transferred from the

MCU to the MC33389 and vice versa. Clocked-in data from the MCU is transferred from the MC33389 shift register and latched into the addressed registers on the rising edge of the CS signal if the read/write bit is set and the parity check was successful.

The CS pin controls the output driver of the serial output pin. Whenever the CS pin goes to a logic low state, the MISO pin output driver is enabled allowing information to be transferred from the MC33389 to the MCU. To avoid any spurious data, it is essential that the high-to-low transition of the CS signal occur only when SCLK is in a logic low state.

SCLK PIN

The system clock pin (SCLK) clocks the internal shift registers of the MC33389. The serial input pin (MOSI) accepts data into the input shift register on the falling edge of the SCLK signal while the serial output pin (MISO) shifts data information out of the shift register on the rising edge of the SCLK signal. False clocking of the shift register must be avoided to guarantee validity of data. It is essential that the SCLK pin be in a logic low state whenever chip select bar pin (CS) makes any transition. For this reason, it is recommended though not necessary, that the SCLK pin be kept in a low logic state as long as the device is not accessed (CS in logic high state). When CS is in a logic high state, any signal at the SCLK and MOSI pin is ignored and MISO is tristated (high impedance).

MOSI PIN

This pin is for the input of serial instruction data. MOSI information is read in on the falling edge of SCLK. To program the MC33389 by setting appropriate programming registers, a sixteen bit serial stream of data is required to be

Table 18. Mode Control Validating Register (MCVR)

Address		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MCVR \$003	R						MSVR2	MSVR1	MSVR0
	W						MCR2	MCR1	MCR0
RESET		—	—	—	—	—	0	0	0

Table 19. MCR and MCVR Bit Definition

MC(V)R2	MC(V)R1	MC(V)R0	—	MSR2	MSR1	MSR0
Automatically Entered After Reset			Normal Request	0	0	0
0	0	1	Normal	0	0	1
0	1	0	Stand-by	0	1	0
1	0	0	Sleep	1	0	0
1	1	1	Emergency	1	1	1

This register configures the state of V3 high-side switch in Normal and Stand-by modes, and the V3 operation and the Forced wake-up or the cyclic sense option for the sleep mode operation.

Table 20. V3 Control Register (V3R)

Address		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
V3R \$005	R					WI2V3	FWU	CYS	V3R0
	W								
RESET		—	—	—	—	1	0	0	0

Table 21. V3R Bit Definition

WI2V3	FWU	CYS	V3R0	—	Comments
x	0	0	0	V3 OFF	Only in Normal and Stand-by Mode Available
x	0	0	1	V3 ON	
x	x	1	x	Cyclic Sense ON	—
x	1	0	x	Forced Wake-Up ON	Only in Sleep Mode Available
1	x	x	x	Wake-Up Inputs Linked to V3	

In low power modes, cyclic sense has priority. A reset of the register occurs when $\overline{\text{RST}} = \text{low}$.

Table 22. Cyclic Timing Control Register (CYTCR)

Address		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CYTCR \$006	R						CYTCR2	CYTCR1	CYTCR0
	W								
RESET		—	—	—	—	—	0	0	0

This register is used to select the cyclic sense or force wake-up timing.

Table 23. CYTCR Bit Definition

CYTCR2	CYTCR1	CYTCR0	Comments	t(ms) Typical
0	0	0	Timer ON, t1 (Default)	32
0	0	1	Timer ON, t2	64
0	1	0	Timer ON, t3	128
0	1	1	Timer ON, t4	256
1	0	0	Timer ON, t5	512
1	0	1	Timer ON, t6	1024
1	1	0	Timer ON, t7	2048
1	1	1	Timer ON, t8	8192

Note: A reset of the register occurs when $\overline{\text{RST}} = \text{Low}$.

Table 24. Software Watchdog Control Register (SWCR)

Address		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SWCR \$009	R						SWCR2	SWCR1	SWCR0
	W								
RESET		—	—	—	—	—	0	0	0

This register is used to select the window watchdog time period. Open window of the selected period is only the second half of the selected period.

Table 25. SWCR Bit Definition

SWCR2	SWCR1	SWCR0	Comments	t(ms) Typical
0	0	0	Timer ON, t1 (Default)	5
0	0	1	Timer ON, t2	10
0	1	0	Timer ON, t3	20
0	1	1	Timer ON, t4	33
1	0	0	Timer ON, t5	50
1	0	1	Timer ON, t6	75
1	1	0	Timer ON, t7	100
1	1	1	Timer ON, t8	200

Note: The software watchdog is only running in Normal and Stand-by modes. A reset of this register occurs when $\overline{\text{RST}} = \text{Low}$.

Table 26. Ground Shift Level Register (GSLR)

Address		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
GSLR \$00A	R					TXDOM	SHIFT	GSLR1	GSLR0
	W								
RESET		—	—	—	—	—	0	0	0

This register is used to monitor the ground shift of the vehicle network.

Table 27. GSLR Bit Definition

GSLR1	GSLR0	Typical Ground Shift Level
0	0	0.7 V
0	1	-1.2 V
1	0	-1.7 V
1	1	-2.2 V

SHIFT

1 = Ground shift above the threshold selected by GSLR1 and GSLR2

0 = No ground shift

The SHIFT information is latched until a read operation of the GSLR register occurs. The GSLR register is set to 0 after power-ON reset. A reset of GSLR1 and GSLR0 occurs when \overline{RST} = Low.

TXDOM

0 = No failure on TX

1 = TX permanent dominant

Table 28. Wake-Up Input Control Register (WUICR)

Address		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WUICR \$00C	R					SPIWU	BUSWU	WUCR1	WUICR0
	W								
RESET		—	—	—	—	0	0	0	0

This register configures the wake-up level for the L0, L1, and L2 inputs. It reports the CAN wake-up and SPI (CS) wake-up events during the Read operation.

Table 29. WUICR Bit Definition

WUICR1	WUICR0	Description
0	0	Wake-Up Inputs Disabled
0	1	Positive Edge Sensitive
1	0	Negative Edge Sensitive
1	1	Positive and Negative Sensitive

Table 30. WUICR Bit Definition

SPIWU	BUSWU	Description
0	0	No Wake-Up Events
0	1	Wake-Up Event on CAN Bus
1	0	Wake-Up Event on SPI Bus

The information is SPIWU and BUSWU is latched. Bits SPIWU and BUSWU will be reset by a read operation of the WUICR register and are set to 0 after a power-ON reset. A reset of WUICR1 and WUICR0 occurs when \overline{RST} = Low.

Table 31. Wake-Up Input Status Register (WUISR)

Address		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WUISR \$00F	R						WUISR2	WUISR1	WUISR0
	W								
RESET		—	—	—	—	—	0	0	0

This register reads back the wake input (L0, L1, L2) causing the SBC to wake-up.

Table 32. WUISR Bit Definition

WUISR2	WUISR1	WUISR0	Description
0	0	0	No Event on Wake-Up Inputs
x	x	1	Event on L0
x	1	x	Event on L1
1	x	x	Event on L2

In case of a wake-up event, the appropriate bit is set to 1. The bits will be reset by a Read operation of the register. After power-ON reset, all bits are set to 0.

Table 33. Wake-Up Input Real Time Information (WUIRTI)

Address		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WUIRTI \$011	R						WUIRTI2	WUIRTI1	WUIRTI0
	W								
RESET		—	—	—	—	—	0	0	0

This register reports the real time information on the state; (High or Low) of the L0, L1, and L2 inputs. The bits WUIRT1 2:0 contain the real time logic value coming from the wake-up inputs (0 means input below threshold, 1 means input above threshold. Typical threshold is 3.5 V).

Table 34. Over Temperature Status Register (OTSR)

Address		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OTSR \$012	R					OPWV2	OPWV1	OTV2	OTV1
	W							OTV2C	
RESET		—	—	—	—	0	0	0	0

This register reads back the over temperature status for the V1 and V2 regulators. It is used to turn V2 ON after a V2 over temperature shutdown occurred in the Write mode.

- OTV1: 1 = V1 over temperature shutdown, 0 = V1 no over temperature
- OTV2: 1 = V2 over temperature shutdown, 0 = V2 no over temperature
- OPWM1: 1 = V2 over temperature pre-warning, 0 = V2 normal temperature
- OPWV2: 1 = V2 over temperature pre-warning, 0 = V2 normal temperature

In case of V1 or V2 over temperature, the appropriate voltage regulators are switched OFF automatically, and the over temperature flags are set (latched). The flags can be reset by a Read operation of the register OTSR. Once V2 is switched OFF because of over temperature (OTV2 = 1) it can only be switched ON again by forcing OTV2C = 0 by a Write operation.

The V1 and V2 pre-warning flags are set as long as the first over temperature exists. The flags disappear, when the temperature is below the threshold. An over temperature of the V2 power supply will also switch OFF V3. After a power-ON reset, all bits of the register are set to 0.

Table 35. Transceiver Error Status Register for CANH (TESRH)

Address		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TESRH \$014	R					TESRH3	TESRH2	TESRH1	TESRH0
	W								
RESET		—	—	—	—	0	0	0	0

This register reports the CANH failure status.

Table 36. TESRH Bit Definition

TESRH3	TESRH2	TESRH1	TESRH0	Description
0	0	0	0	No Failure on CANH
0	x	0	1	CANH Wire Interruption
x	x	1	x	CANH Short Circuit to V _{BAT}
0	1	0	x	CANH Short Circuit to Ground
1	x	0	x	CANH Short Circuit to V _{CC}

In case of CANH line failures, the appropriate bit(s) are set according to [Table 36](#). This information is latched. The register can be reset by a Read operation. After power-ON is reset, all bits are set to 0.

Table 37. Transceiver Error Status Register for CANL and Tx (TESRL)

Address		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TESRL \$017	R					TESRL3	TESRL2	TESRL1	TESRL0
	W								
RESET		—	—	—	—	0	0	0	0

This register reports the CANL and Tx permanent failure status

Table 38. TESRL Bit Definition

TESRL3	TESRL2	TESRL1	TESRL0	Description
0	0	0	0	No Failure
0	x	0	1	CANL Wire Interruption
0	1	0	x	CANL Short Circuit to Ground/CANH mutually shorted to CANL
x	x	1	x	CANL Short Circuit to V _{BAT}
1	x	0	x	CANL Short Circuit to V _{DD}

In case of CANL line failures, the appropriate bit(s) are set according to [Table 38](#). This information is latched. The register can be reset by a Read operation. After power-ON is reset, all bits are set to 0.

Table 39. Reset Source Register (RSR)

Address		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RSR \$018	R						RSR2	RSR1	RSR0
	W								
RESET		—	—	—	—	—	1	0	1

This register reports the source of a reset already occurred.

RSR0: 1 = > V_{DD1} under voltage occurred (RSR2 = 1 in this case), 0 = > no over voltage on V occurred

RSR1: 1 = > Software watchdog reset occurred (RSR 2 = 1 in this case), 0 = > no SW watchdog reset occurred

RSR2: 1 = > External reset occurred (RSR0 = RSR1= 0 in this case), 0 = > no external reset occurred

Events related to the bits in register RSR are latched. All bits can be reset by a Read operation of the register. After a power-ON reset, RSR2 and RSR0 are set to 1. Therefore, the first read out of the register after power-ON delivers RSR[2:0] = [101].

Table 40. Voltage Supply Status Register (VSSR)

Address		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
VSSR \$01B	R					V3SR	V2SR	VBSR1	VBSR0
	W								
RESET		—	—	—	—	0	0	—	—
POR		—	—	—	—	0	0	0	1

This register monitors the status of the V2, V3, and V_{BAT} voltage level.

Table 41. VBSR1 VBSR0

VBSR1	VBSR0	Description
0	0	No Failure on VBAT
x	1	Under Voltage (BATFail)
1	x	Over Voltage (BATHigh)

V2SR: 1 = V2 ON, 0 = V2 OFF

V3SR: 1 = V3 over temperature, 0 = V3 no over temperature

VBSR1 is real time information. It cannot be reset. Bits V3SR, V2SR, and VBSR0 are latched and can be reset by a Read operation of the register.

The next two registers (IMR1 and IMR2) mask the interrupt function.

Table 42. Interrupt Mask Control Register 1 (IMR1)

Address		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IMR1 \$01D	R					HV	HTPW	MTPW	BATU
	W								
RESET		—	—	—	—	0	0	0	0

Table 43. Interrupt Mask Control Register 2 (IMR2)

Address		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IMR2 \$01E	R						BUSF	SPIE	WU
	W								
RESET		—	—	—	—	—	0	0	0

To enable the appropriate interrupt, the mask bit has to be set to 1. To disable the interrupt the bit, it must be cleared to 0. After a power-ON reset or RST = Low, the bits are cleared to 0. All interrupts are disabled. Explanation for the abbreviations:

HV = V_{BAT} High voltage

HT = High temperature on V1 or V2

MTPW = Medium temperature pre-warning on V1 or V2

BATU = Battery under voltage (BATFail)

BUSF = CAN bus failure

SPIE = SPI error

WU = Wake-up

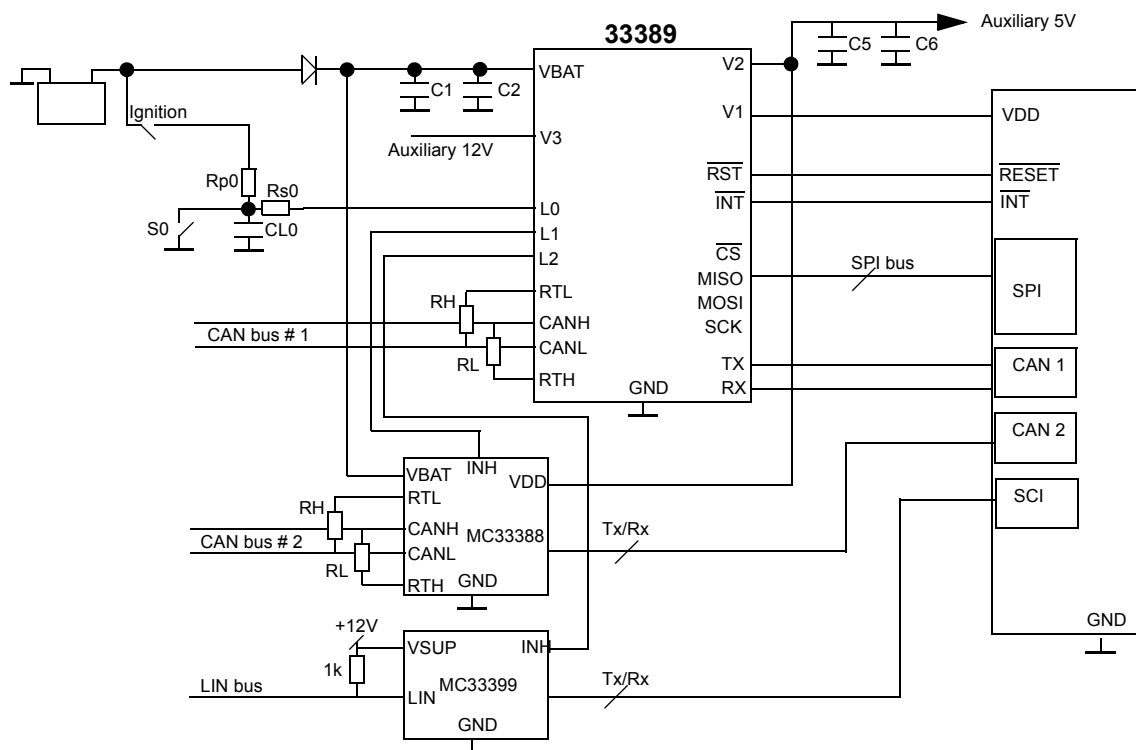
The next two registers (ISR1 and ISR2) read the interrupt source. All bits in registers ISR1 and ISR2 are copies of the appropriate bits in different SPI registers. For a faster read-out, these bits are merged in ISR1 and ISR2. A reset cannot be completed for registers ISR1 and ISR2.

Table 44. Interrupt Source Register 1 (ISR1)

Address		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ISR \$021	R					HV	HTPW	MTPW	BATU
	W								
RESET		—	—	—	—	0	0	0	0

Table 45. Interrupt Source Register 2 (ISR2)

Address		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ISR \$022	R						BUSF	SPIE	WU
	W								
RESET		—	—	—	—	—	0	0	0



(Wake-up input linked to peripheral circuits: (ex: low speed CAN or LIN transceivers).

Figure 25. Typical Application Schematic 2

The SBC offers several capabilities to help users debug their application.

- External bias of V1 and reset pin
- Turn OFF software watchdog in the Stand-by mode
- Special debug samples with software watchdog disable at power-up (contact local Motorola representative)

DEBUG AND PROGRAM DOWNLOAD INTO FLASH MEMORY

While the SBC is powered, it enters Normal Request mode and expects during the 75 ms time period in the NR mode, an SPI trigger word (to enter Normal mode and select the watchdog time period). If this does not occur, the SBC enters the Sleep mode and turns off V1.

When the software is debugged, and when using development tools, it is not always easy to make sure these events happen properly. It is thus possible to externally power the V1 line with an external 5.0 V supply, and to force the Reset pin to V1 or to an external 5.0 V. These can be

done at nominal voltage and temperature. By doing this, 5.0 V is provided to the MCU V_{DD} and reset lines.

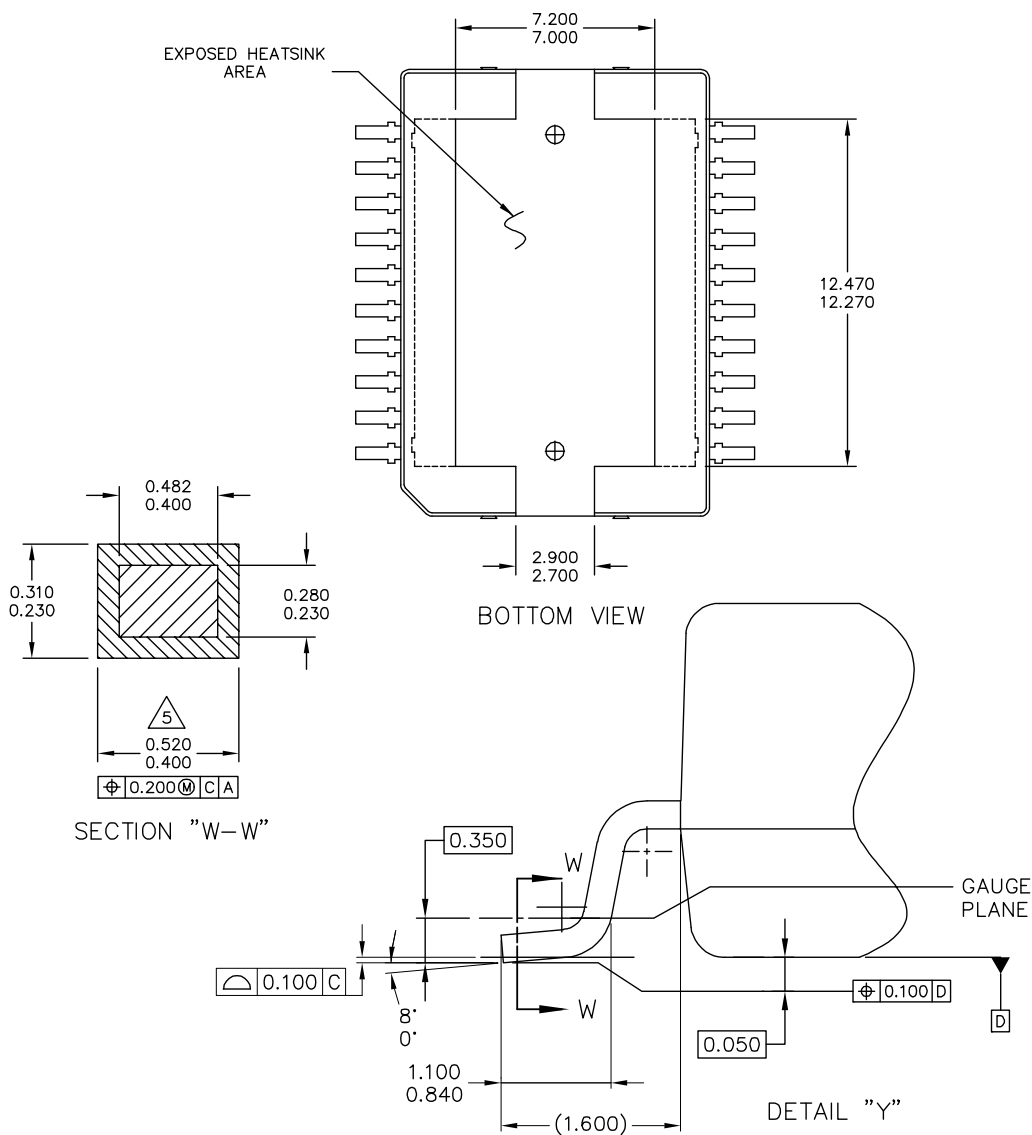
Under this condition the SBC is not operational. However, the reset pin is pulled low and is sinking 5 mA to ground. This means, the external circuitry driving reset must have a current capability higher than 5 mA in order to drive the reset in the high-state.

DISABLE OF SOFTWARE WATCHDOG IN STAND-BY MODE

The software watchdog can be disabled in Stand-by mode only. In order to disable it the following operation must be done:

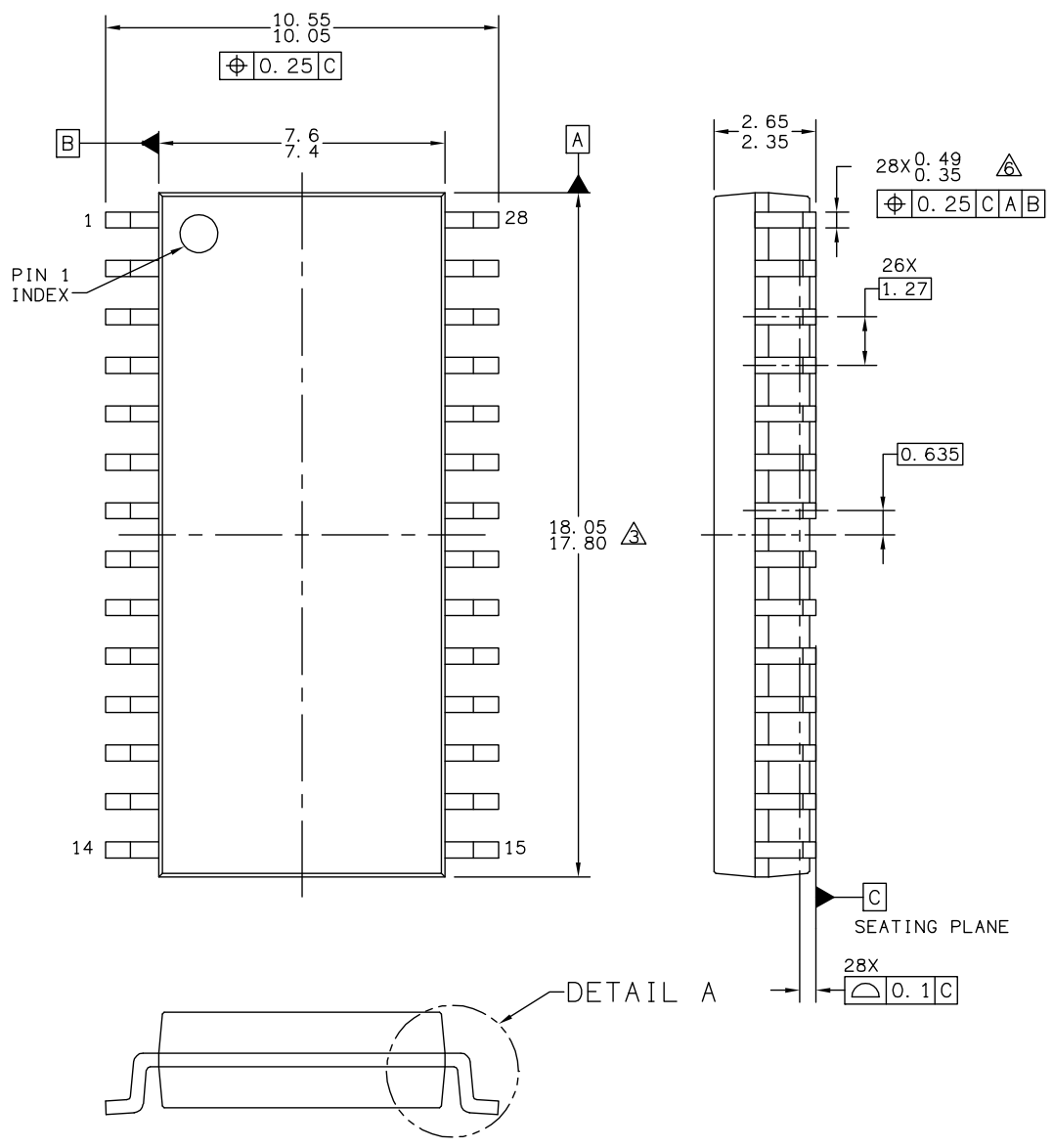
- Write to MCR register—data 011 (bit 2, bit 1, bit 0)
- Write to MCVR register—data 011 (bit 2, bit 1, bit 0)

Then the SBC enters the Stand-by mode without software watchdog. However the V2 can not be turned on, and the CAN cell can not be used.



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	CASE NUMBER: 979-04	19 MAY 2005
	STANDARD: NON-JEDEC	

DH SUFFIX
VW SUFFIX (Pb-FREE)
20 PIN
PLASTIC PACKAGE
98ASH70273A
ISSUE E



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		CASE NUMBER: 751F-05		10 MAR 2005
		STANDARD: MS-013AE		

DW SUFFIX
 EG SUFFIX (Pb-FREE)
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