THE DATASHEET OF

MC74HCT4094ADR2G

www.win-source.net 0086-755-83957316

MC74HCT4094A

8-Bit Shift and Store Register with LSTTL Compatible Inputs

High−Performance Silicon−Gate CMOS

The MC74HCT4094A is a high speed CMOS 8−bit serial shift and storage register. This device consists of an 8−bit shift register and latch with 3−state output buffers. Data is shifted on positive clock (CP) transitions. The data in the shift register is transferred to the storage register when the Strobe (STR) input is high. The output buffers are enabled when the Output Enable (OE) input is set high. Two serial outputs (QS_1, QS_2) are available for cascading multiple devices.

The MC74HCT4094A can be used to interface TTL or CMOS outputs to high speed CMOS inputs.

Features

- Wide Operating Voltage Range: 4.5 to 5.5 V
- Low Power Dissipation: I_{CC} = < 10 μA
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- These are Pb−Free Devices

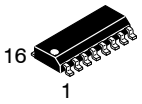
Typical Applications

- Serial−to−Parallel Conversion
- Remote Control Storage Register

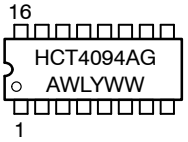
ON Semiconductor®

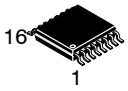
http://onsemi.com

MARKING DIAGRAMS

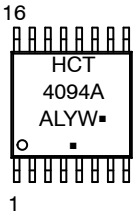


SOIC−16
D SUFFIX
CASE 751B





TSSOP−16
DT SUFFIX
CASE 948F



A	=	Assembly Location
WL, L	=	Wafer Lot
YY, Y	=	Year
WW, W	=	Work Week
G, ▪	=	Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 9 of this data sheet.

© Semiconductor Components Industries, LLC, 2011

March, 2011 − Rev. 0

Publication Order Number:
MC74HCT4094A/D

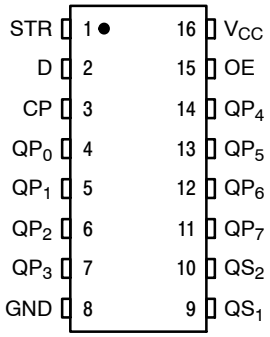


Figure 1. Pin Assignment

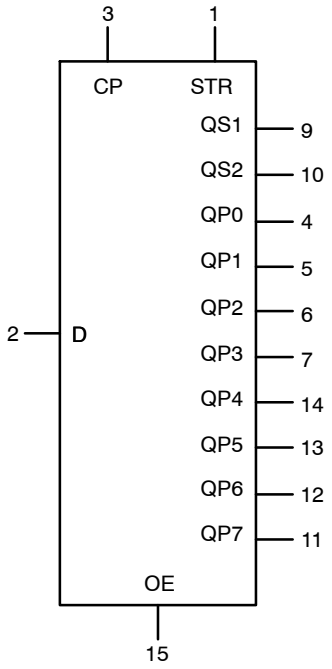


Figure 2. Logic Symbol

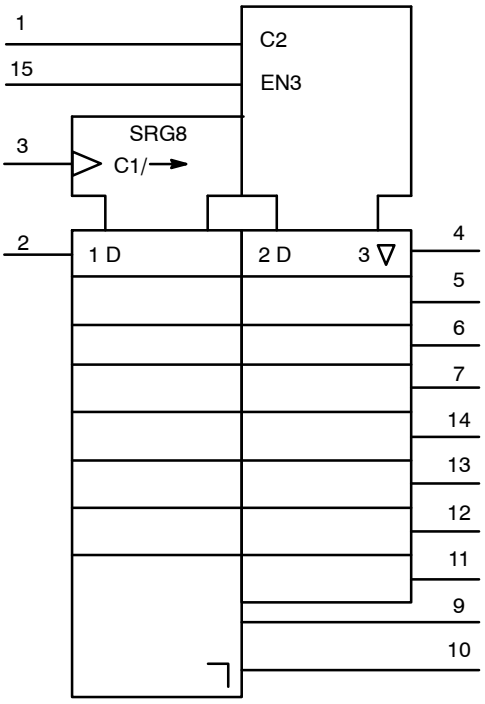


Figure 3. IEC Logic Symbol

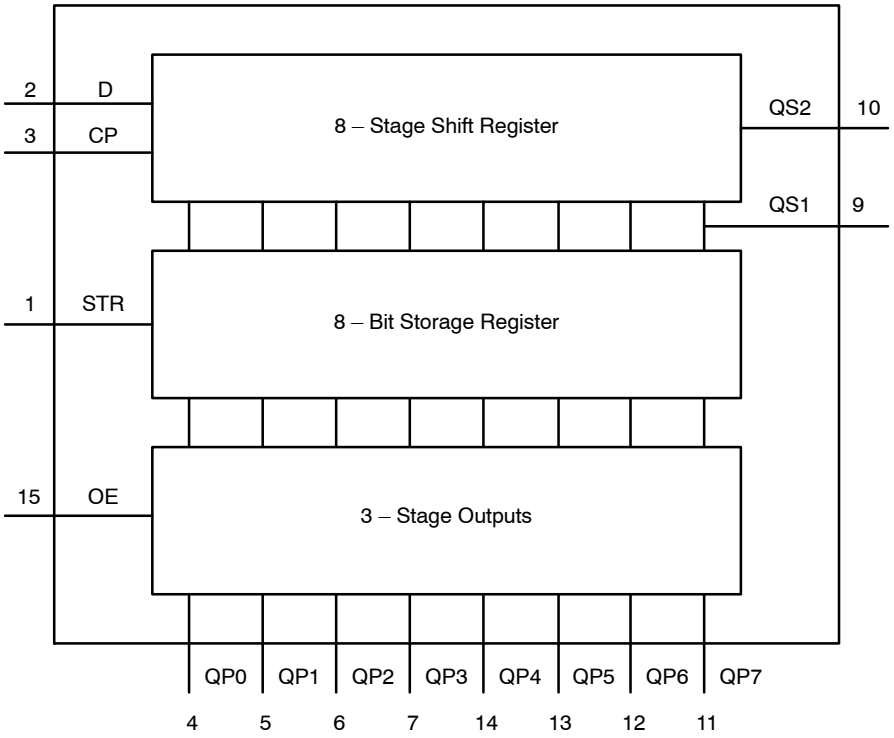


Figure 4. Functional Diagram

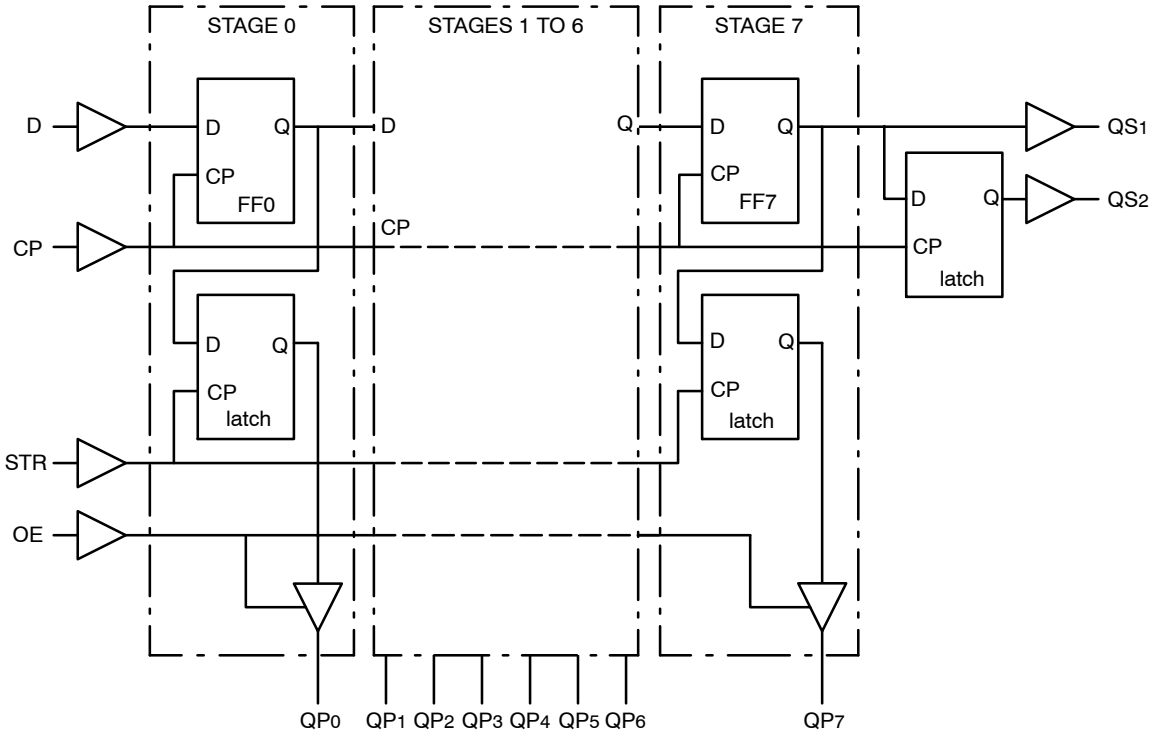


Figure 5. Logic Diagram

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
V_{out}	DC Output Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 35	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 75	mA
P_D	Power Dissipation in Still Air, SOIC Package† TSSOP Package†	500 450	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

†Derating – SOIC Package: – 7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	4.5	5.5	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	–55	+125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	0	500	ns

FUNCTIONAL TABLE

INPUTS				PARALLEL OUTPUTS		SERIAL OUTPUTS	
CP	OE	STR	D	QP0	QPn	QS1	QS2
↑	L	X	X	Z	Z	Q'6	NC
↓	L	X	X	Z	Z	NC	QP7
↑	H	L	X	NC	NC	Q'6	NC
↑	H	H	L	L	QPn−1	Q'6	NC
↑	H	H	H	H	QPn−1	Q'6	NC
↓	H	H	H	NC	NC	NC	QP7

Notes

1. H = HIGH voltage level
   L = LOW voltage level
   X = don't care
   Z = high impedance OFF−state
   NC = no change
   ↑ = LOW−to−HIGH CP transition
   ↓ = HIGH−to−LOW CP transition
   Q'6 = the information in the seventh register stage is transferred to the 8th register stage and QSn output at the positive clock edge

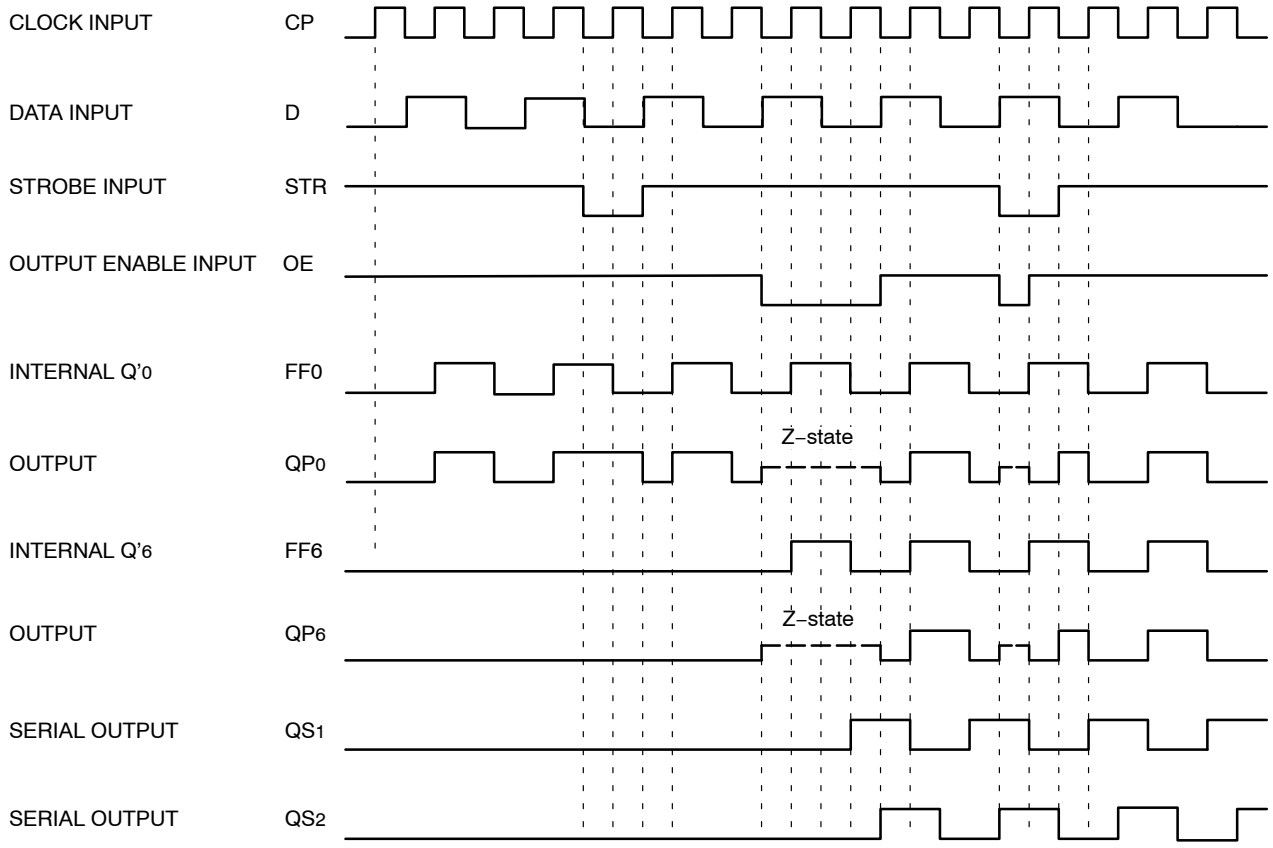


Figure 6. Timing Diagram

DC CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} (V)	Guaranteed Limits			Unit
				−55°C to 25°C	≤ 85°C	≤ 125°C	
V_{IH}	Minimum High−Level Input Voltage	V_{OUT} = 0.1 V or V_{CC} − 0.1 V $\lvert I_{OUT} \rvert \leq$ 20 μA	4.5	2.0	2.0	2.0	V
			5.5	2.0	2.0	2.0	
V_{IL}	Maximum Low−Level Input Voltage	V_{OUT} = 0.1 V or V_{CC} − 0.1 V $\lvert I_{OUT} \rvert \leq$ 20 μA	4.5	0.8	0.8	0.8	V
			5.5	0.8	0.8	0.8	
V_{OH}	Minimum High−Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL} $\lvert I_{OUT} \rvert \leq$ 20 μA	4.5	4.4	4.4	4.4	V
			5.5	5.4	5.4	5.4	
		$V_{IN} = V_{IH}$ or V_{IL}, $\lvert I_{OUT} \rvert$ = 6 mA	4.5	4.25	4.2	4.1	
V_{OL}	Maximum Low−Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL}, $\lvert I_{OUT} \rvert \leq$ 20 μA	4.5	0.1	0.1	0.1	V
			5.5	0.1	0.1	0.1	
		$V_{IN} = V_{IH}$ or V_{IL}, $\lvert I_{OUT} \rvert$ = 6 mA	4.5	0.25	0.3	0.4	
I_{IN}	Maximum Input Leakage Current	$V_{IN} = V_{CC}$ or GND	5.5	±0.1	±1	±1	μA
I_{OZ}	Maximum Tri−State Output Leakage Current	$V_{IN} = V_{CC}$ or GND $V_{OUT} = V_{CC}$ or GND	5.5	±0.5	±5	±10	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND	5.5	4.0	40	80	μA

ΔI_{CC}	Additional Quiescent Supply Current	V_{in} = 2.4V, Any One Input $V_{in} = V_{CC}$ or GND, Other Inputs I_{out} = 0μA		≥ −55°C	25 to 125°C	
			5.5	2.9	2.4	mA

AC CHARACTERISTICS ($t_f = t_r = 6$ ns, $C_L = 50$ pF)

Symbol	Parameter	Test Conditions	V_{CC} (V)	Guaranteed Limits			Unit
				−55°C to 25°C	≤ 85°C	≤ 125°C	
t_{PHL}, t_{PLH}	Maximum Propagation Delay CP to QS_1	Figure 7	4.5	30	38	45	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay CP to QS_2	Figure 7	4.5	27	34	41	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay CP to QP_n	Figure 7	4.5	39	49	59	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay STR to QP_n	Figure 8	4.5	36	45	54	ns
t_{PZH}, t_{PZL}	Maximum 3−State Output Enable Time OE to QP_n	Figure 9	4.5	35	44	53	ns
t_{PHZ}, t_{PLZ}	Maximum 3−State Output Enable Time OE to QP_n	Figure 9	4.5	25	31	38	ns
t_{THL}, t_{TLH}	Maximum Output Transition Time	Figure 7	4.5	18	22	25	ns
t_W	Minimum Clock Pulse Width High or Low	Figure 7	4.5	16	20	24	ns
t_W	Minimum Strobe Pulse Width High	Figure 8	4.5	16	20	24	ns
t_{SU}	Minimum Set−up Time D to CP	Figure 10	4.5	10	13	15	ns
t_{SU}	Minimum Set−up Time CP to STR	Figure 8	4.5	20	25	30	ns
t_h	Minimum Hold Time D to CP	Figure 10	4.5	3	3	3	ns
t_h	Minimum Hold Time CP to STR	Figure 8	4.5	0	0	0	ns
f_{MAX}	Minimum Clock Pulse Frequency	Figure 7	4.5	30	24	20	MHz
C_{in}	Maximum Input Capacitance		–	10	10	10	pF
C_{out}	Maximum Output Capacitance		–	15	15	15	pF
C_{PD}	Power Dissipation Capacitance (Note 2)		–	140	140	140	pF

2. C_{PD} is defined as the value of the IC's equivalent capacitance from which the operating current can be calculated from: $I_{CC}(\text{operating}) \approx C_{PD} \times V_{CC} \times f_{IN} \times N_{SW}$ where N_{SW} = total number of outputs switching and f_{IN} = switching frequency.

AC WAVEFORMS

(V_M = 1.3 V)

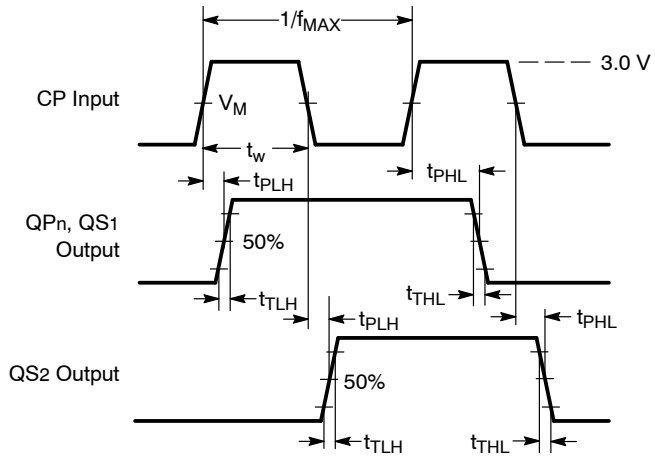


Figure 7. Waveforms showing the clock (CP) to output (QPn, QS1, QS2) propagation delays, the clock pulse width and the maximum clock frequency.

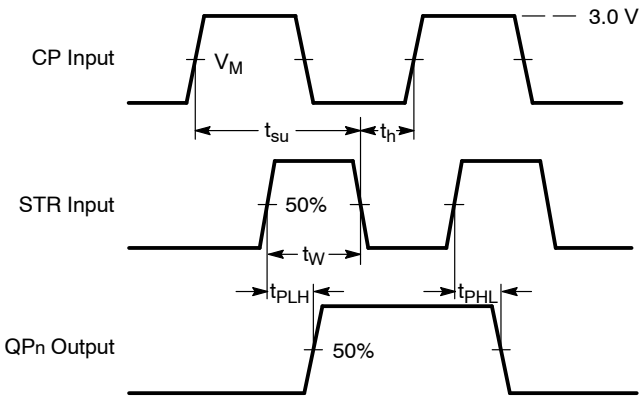


Figure 8. Waveforms showing the strobe (STR) to output (QPn) propagation delays, the strobe pulse width, the clock set−up and hold times for the strobe input.

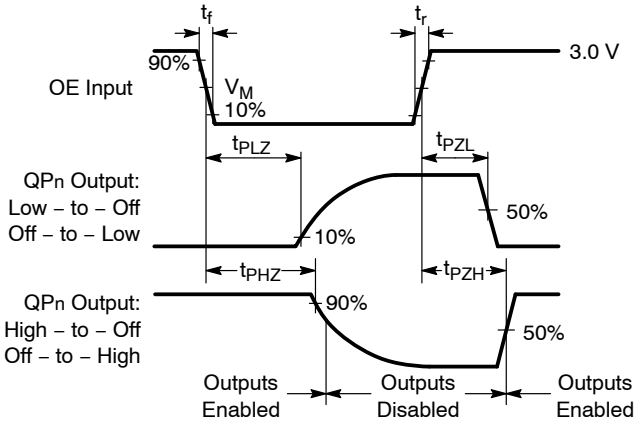


Figure 9. Waveforms showing the 3−state enable and disable times for input OE.

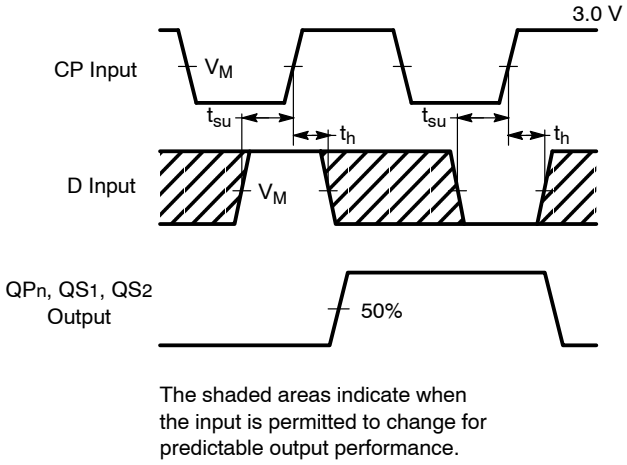
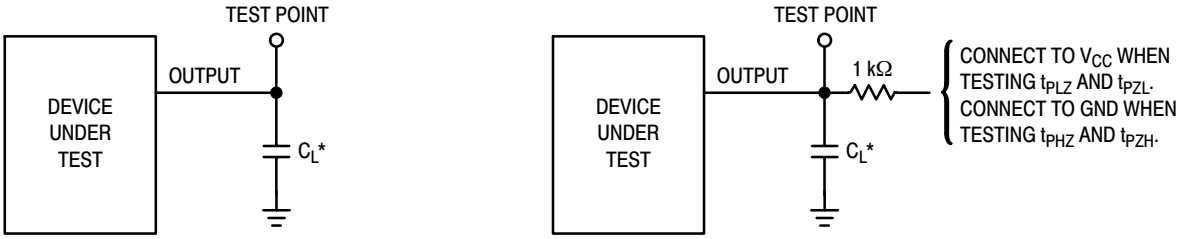


Figure 10. Waveforms showing the data set−up and hold times for the data input.

TEST CIRCUITS



*Includes all probe and jig capacitance

*Includes all probe and jig capacitance

Figure 11. AC Characteristics Load Circuits

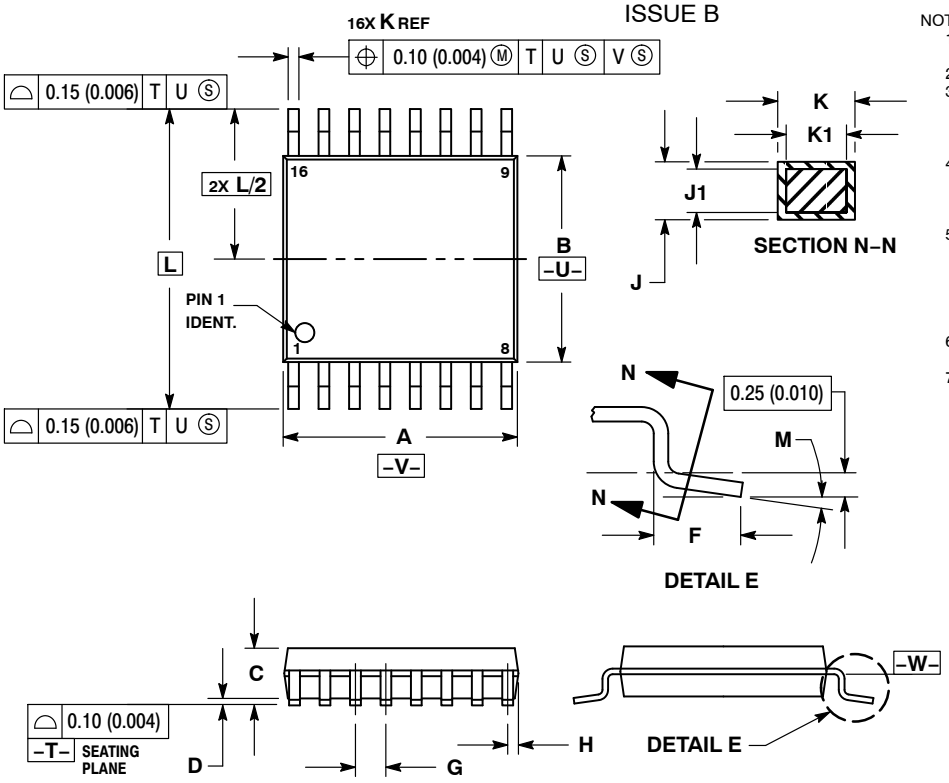
ORDERING INFORMATION

Device	Package	Shipping†
MC74HCT4094ADG	SOIC−16 (Pb−Free)	48 Units / Rail
MC74HCT4094ADR2G	SOIC−16 (Pb−Free)	2500 Tape & Reel
MC74HCT4094ADT	TSSOP−16*	96 Units / Rail
MC74HCT4094ADTR2G	TSSOP−16*	2500 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*This package is inherently Pb−Free.

PACKAGE DIMENSIONS

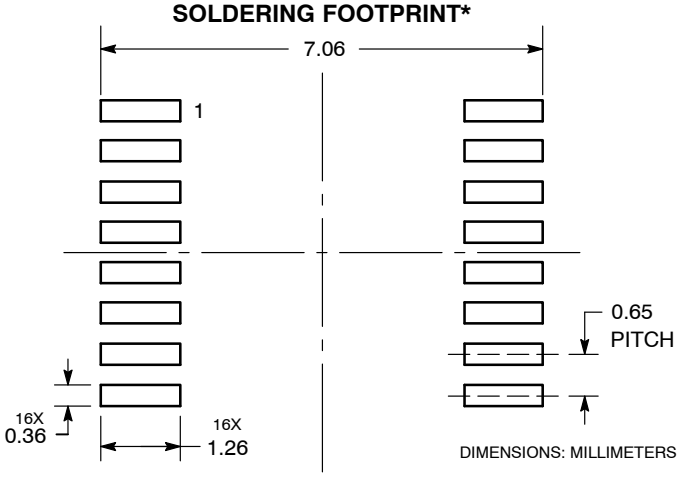
TSSOP−16
DT SUFFIX
CASE 948F−01
ISSUE B



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	−−−	1.20	−−−	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

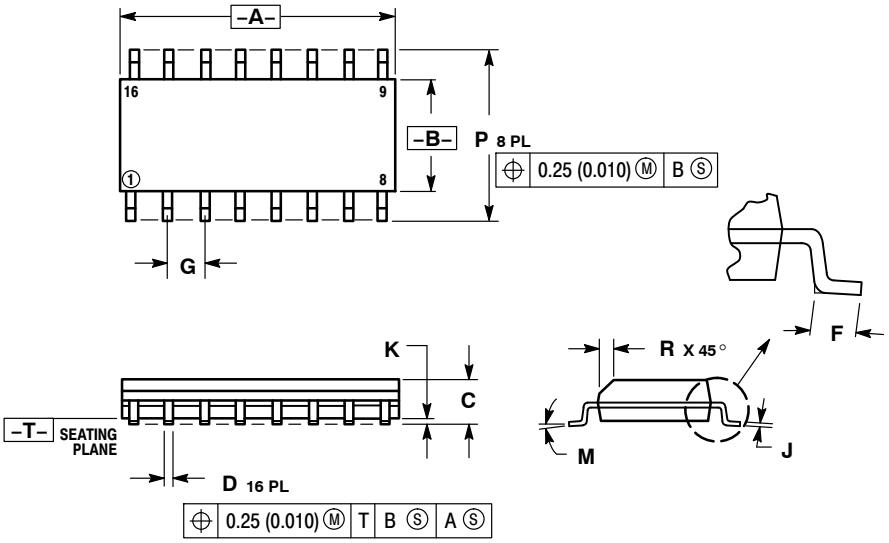
SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

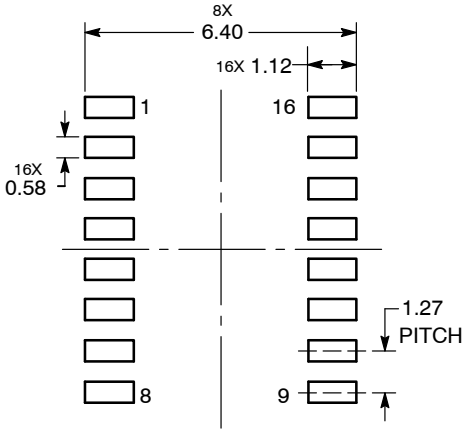
SOIC−16
CASE 751B−05
ISSUE K



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor and ON are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. “Typical” parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including “Typicals” must be validated for each customer application by customer’s technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81−3−5773−3850

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

- View MC74HCT4094ADR2G on WIN SOURCE
- ON Semiconductor Information

Optimize Your Supply Chain with WIN SOURCE Solutions

- Global Sourcing Solution
- Obsolete Management
- Cost Control Management
- Shortage Management
- Alternative Solution
- Excess Inventory Management