



**THE DATASHEET OF  
FDMC86184**





# FDMC86184

## N-Channel Shielded Gate PowerTrench® MOSFET

100 V, 57 A, 8.5 mΩ

### Features

- Shielded Gate MOSFET Technology
- Max  $r_{DS(on)}$  = 8.5 mΩ at  $V_{GS} = 10$  V,  $I_D = 21$  A
- Max  $r_{DS(on)}$  = 24.8 mΩ at  $V_{GS} = 6$  V,  $I_D = 10$  A
- 50% Lower Qrr than Other MOSFET Suppliers
- Lowers Switching Noise/EMI
- MSL1 Robust Package Design
- 100% UIL Tested
- RoHS Compliant

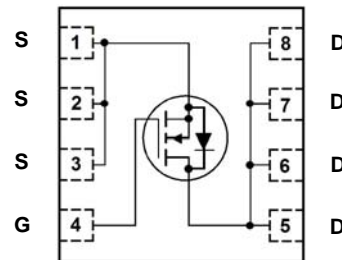
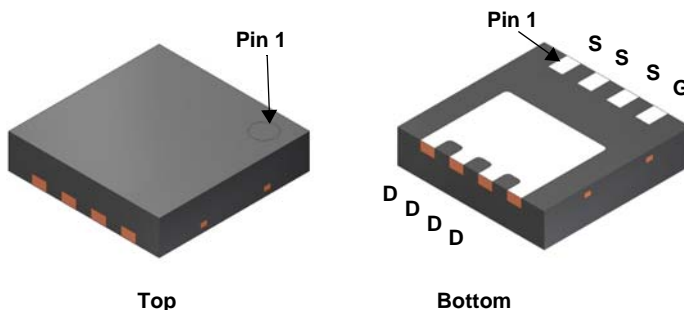


### General Description

This N-Channel MV MOSFET is produced using ON Semiconductor's advanced PowerTrench® process that incorporates Shielded Gate technology. This process has been optimized to minimize on-state resistance and yet maintain superior switching performance with best in class soft body diode.

### Applications

- Primary DC-DC MOSFET
- Synchronous Rectifier in DC-DC and AC-DC
- Motor Drive
- Solar



### MOSFET Maximum Ratings $T_A = 25$ °C unless otherwise noted.

Symbol	Parameter	Rated	Units
$V_{DS}$	Drain to Source Voltage	100	V
$V_{GS}$	Gate to Source Voltage	±20	V
$I_D$	Drain Current -Continuous	$T_C = 25$ °C (Note 5)	57
	-Continuous	$T_C = 100$ °C (Note 5)	36
	-Continuous	$T_A = 25$ °C (Note 1a)	12
	-Pulsed	(Note 4)	266
$E_{AS}$	Single Pulse Avalanche Energy	(Note 3)	121
$P_D$	Power Dissipation	$T_C = 25$ °C	54
	Power Dissipation	$T_A = 25$ °C (Note 1a)	2.3
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	°C

### Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	2.3	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	53	

### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMC86184	FDMC86184	Power 33	13 "	12 mm	3000 units

## Electrical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
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### Off Characteristics

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250\text{ }\mu\text{A}$ , $V_{GS} = 0\text{ V}$	100			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$		59		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 80\text{ V}$ , $V_{GS} = 0\text{ V}$			1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{ V}$ , $V_{DS} = 0\text{ V}$			100	nA

### On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$ , $I_D = 110\text{ }\mu\text{A}$	2.0	3.1	4.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 110\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$		-9		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{ V}$ , $I_D = 21\text{ A}$		6.4	8.5	m $\Omega$
		$V_{GS} = 6\text{ V}$ , $I_D = 10\text{ A}$		11	24.8	
		$V_{GS} = 10\text{ V}$ , $I_D = 21\text{ A}$ , $T_J = 125\text{ }^\circ\text{C}$		11	18	
$g_{FS}$	Forward Transconductance	$V_{DS} = 5\text{ V}$ , $I_D = 21\text{ A}$		49		S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 50\text{ V}$ , $V_{GS} = 0\text{ V}$ , $f = 1\text{ MHz}$		1490	2090	pF
$C_{oss}$	Output Capacitance			906	1270	pF
$C_{rss}$	Reverse Transfer Capacitance			13	25	pF
$R_g$	Gate Resistance		0.1	0.4	1.2	$\Omega$

### Switching Characteristics

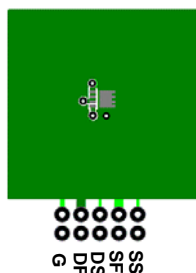
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 50\text{ V}$ , $I_D = 21\text{ A}$ , $V_{GS} = 10\text{ V}$ , $R_{GEN} = 6\text{ }\Omega$		12	22	ns	
$t_r$	Rise Time			4	10	ns	
$t_{d(off)}$	Turn-Off Delay Time			17	31	ns	
$t_f$	Fall Time			4	10	ns	
$Q_g$	Total Gate Charge		$V_{GS} = 0\text{ V to }10\text{ V}$		21	30	nC
$Q_g$	Total Gate Charge		$V_{GS} = 0\text{ V to }6\text{ V}$		14	20	nC
$Q_{gs}$	Gate to Source Charge	$V_{DD} = 50\text{ V}$ , $I_D = 21\text{ A}$		6.5		nC	
$Q_{gd}$	Gate to Drain "Miller" Charge			4.6		nC	
$Q_{oss}$	Output Charge		$V_{DD} = 50\text{ V}$ , $V_{GS} = 0\text{ V}$		61		nC

### Drain-Source Diode Characteristics

$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}$ , $I_S = 2.1\text{ A}$ (Note 2)		0.7	1.2	V
		$V_{GS} = 0\text{ V}$ , $I_S = 21\text{ A}$ (Note 2)		0.8	1.3	
$t_{rr}$	Reverse Recovery Time	$I_F = 10\text{ A}$ , $di/dt = 300\text{ A}/\mu\text{s}$		27	44	ns
$Q_{rr}$	Reverse Recovery Charge			46	74	nC
$t_{rr}$	Reverse Recovery Time	$I_F = 10\text{ A}$ , $di/dt = 1000\text{ A}/\mu\text{s}$		21	34	ns
$Q_{rr}$	Reverse Recovery Charge			96	154	nC

Notes:

1.  $R_{\theta JA}$  is determined with the device mounted on a  $1\text{ in}^2$  pad 2 oz copper pad on a  $1.5 \times 1.5\text{ in.}$  board of FR-4 material.  $R_{\theta CA}$  is determined by the user's board design.



a.  $53\text{ }^\circ\text{C/W}$  when mounted on a  $1\text{ in}^2$  pad of 2 oz copper



b.  $125\text{ }^\circ\text{C/W}$  when mounted on a minimum pad of 2 oz copper

2. Pulse Test: Pulse Width <  $300\text{ }\mu\text{s}$ , Duty cycle < 2.0%.

3.  $E_{AS}$  of 121 mJ is based on starting  $T_J = 25\text{ }^\circ\text{C}$ ; N-ch:  $L = 3\text{ mH}$ ,  $I_{AS} = 9\text{ A}$ ,  $V_{DD} = 100\text{ V}$ ,  $V_{GS} = 10\text{ V}$ . 100% test at  $L = 0.3\text{ mH}$ ,  $I_{AS} = 21\text{ A}$ .

4. Pulsed  $I_D$  please refer to Fig 11 SOA graph for more details.

5. Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.

**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted.

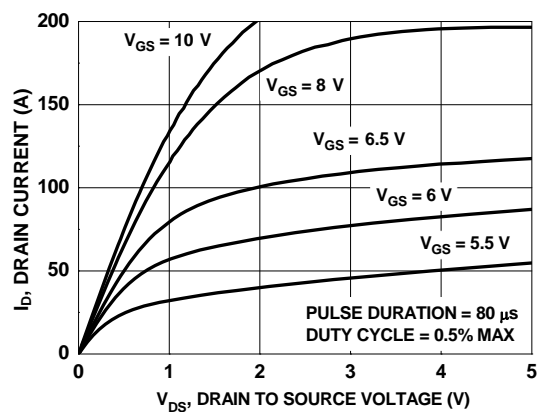


Figure 1. On-Region Characteristics

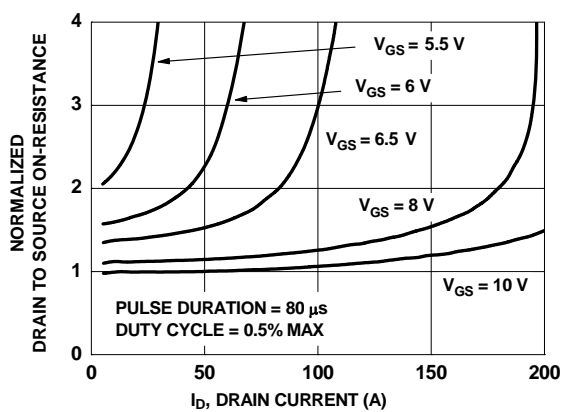


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

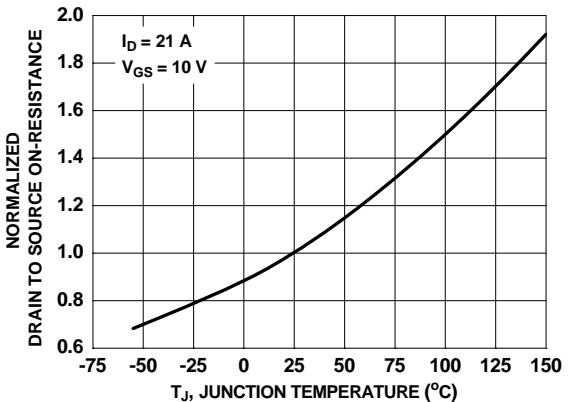


Figure 3. Normalized On-Resistance vs. Junction Temperature

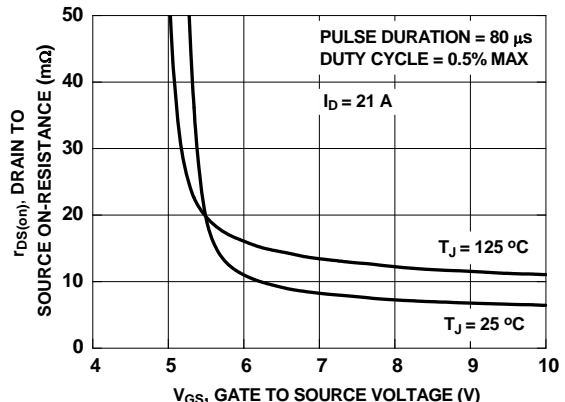


Figure 4. On-Resistance vs. Gate to Source Voltage

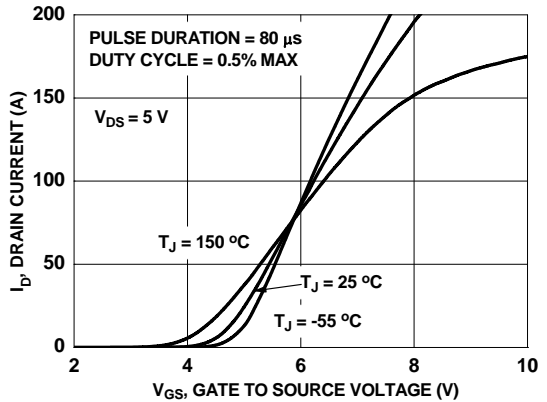


Figure 5. Transfer Characteristics

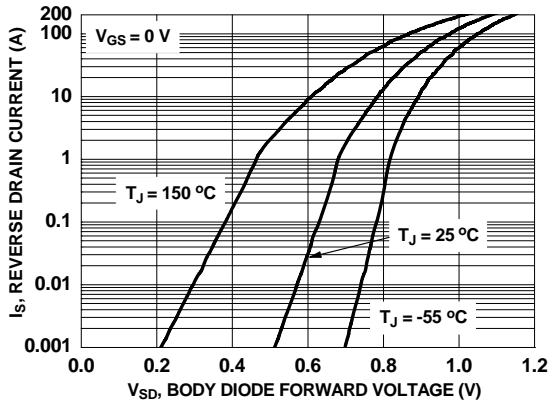
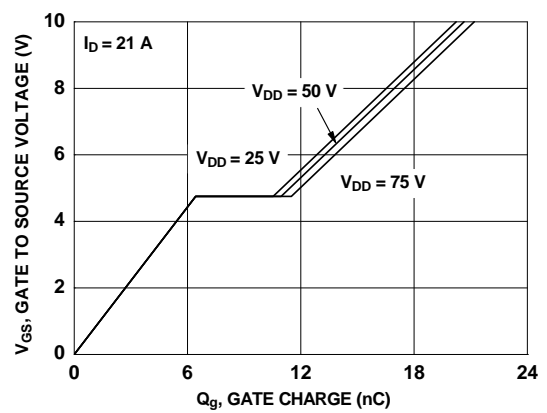
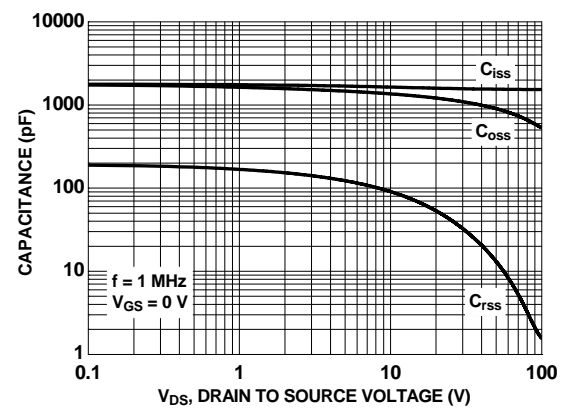


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

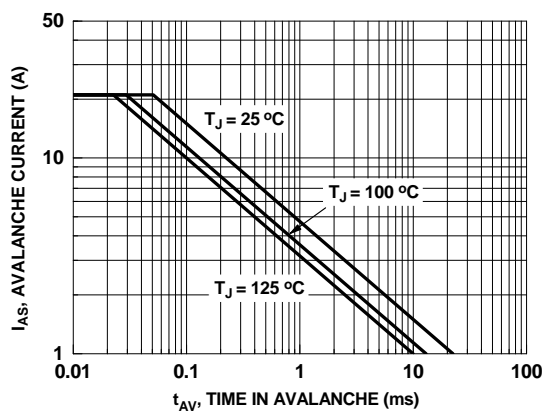
**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted.



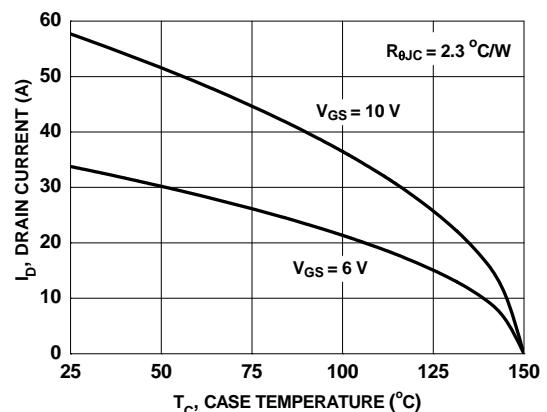
**Figure 7. Gate Charge Characteristics**



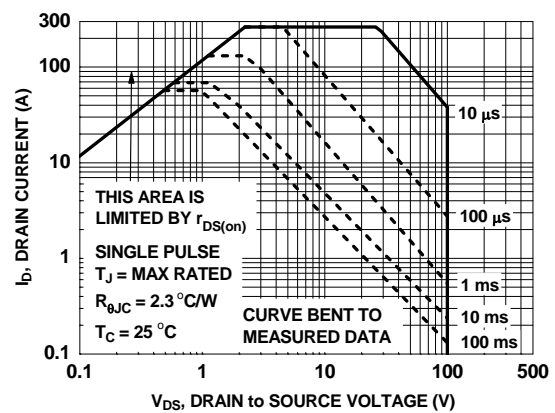
**Figure 8. Capacitance vs. Drain to Source Voltage**



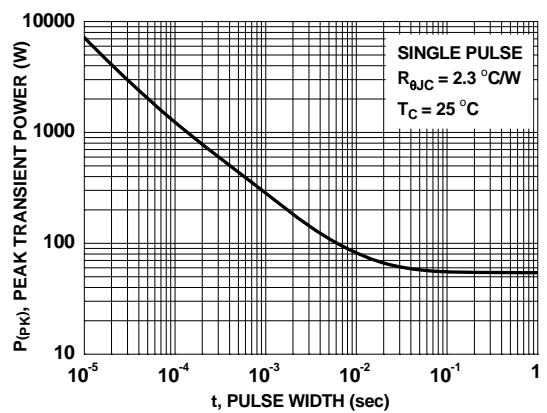
**Figure 9. Unclamped Inductive Switching Capability**



**Figure 10. Maximum Continuous Drain Current vs. Case Temperature**

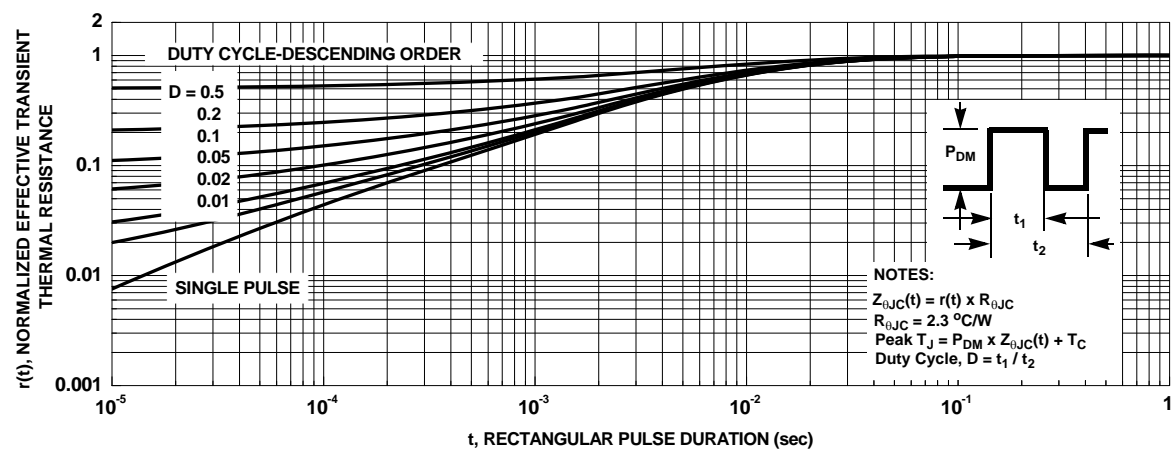


**Figure 11. Forward Bias Safe Operating Area**

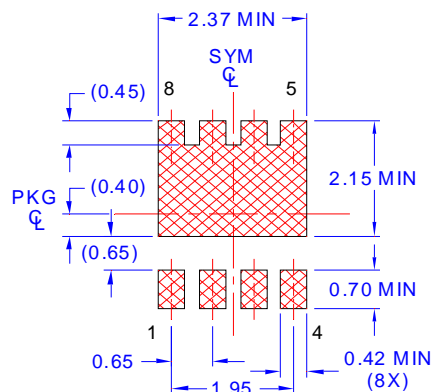
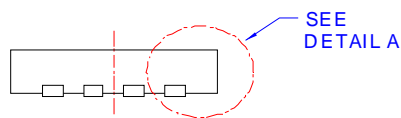
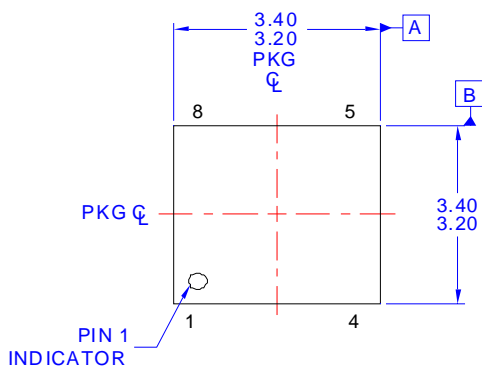


**Figure 12. Single Pulse Maximum Power Dissipation**

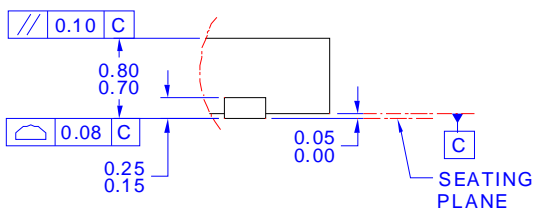
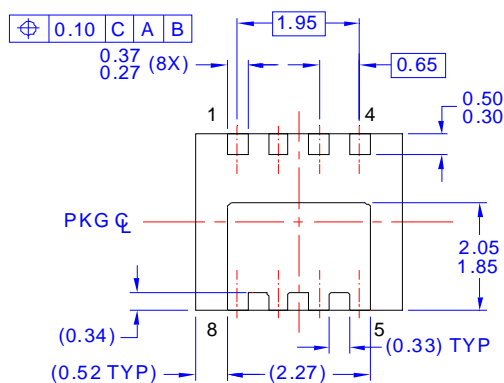
**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted.



## Dimensional Outline and Pad Layout



LAND PATTERN RECOMMENDATION



DETAIL A  
SCALE: 2X

### NOTES: UNLESS OTHERWISE SPECIFIED

- A) PACKAGE STANDARD REFERENCE: JEDEC MO-240, ISSUE A, VAR. BA, DATED OCTOBER 2002.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
- D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
- E) DRAWING FILE NAME: PQFN08HREV1

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