



**THE DATASHEET OF
MRF19030LR5**



RF Power Field Effect Transistors

N-Channel Enhancement-Mode Lateral MOSFETs

Designed for class AB PCN and PCS base station applications with frequencies from 1800 to 2000 MHz. Suitable for FM, TDMA, CDMA and multicarrier amplifier applications.

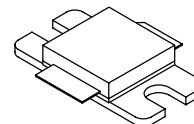
- CDMA Performance @ 1990 MHz, 26 Volts
IS-95 CDMA Pilot, Sync, Paging, Traffic Codes 8 Thru 13
885 kHz — -47 dBc in 30 kHz BW
1.25 MHz — -55 dBc in 12.5 kHz BW
2.25 MHz — -55 dBc in 1 MHz BW
Output Power — 4.5 Watts Avg.
Power Gain — 13.5 dB
Efficiency — 17%
- Capable of Handling 10:1 VSWR, @ 26 Vdc, 1960 MHz, 30 Watts CW Output Power

Features

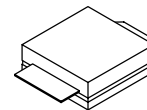
- Internally Matched for Ease of Use
- High Gain, High Efficiency and High Linearity
- Integrated ESD Protection
- Designed for Maximum Gain and Insertion Phase Flatness
- Excellent Thermal Stability
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- Low Gold Plating Thickness on Leads, 40μ" Nominal.
- RoHS Compliant
- In Tape and Reel. R3 Suffix = 250 Units per 32 mm, 13 Inch Reel.

MRF19030LR3
MRF19030LSR3

1930-1990 MHz, 30 W, 26 V
LATERAL N-CHANNEL
RF POWER MOSFETs



CASE 465E-04, STYLE 1
NI-400
MRF19030LR3



CASE 465F-04, STYLE 1
NI-400S
MRF19030LSR3

ARCHIVE INFORMATION

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Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	-0.5, +65	Vdc
Gate-Source Voltage	V_{GS}	-0.5, +15	Vdc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	83.3 0.48	W W/°C
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature	T_C	150	°C
Operating Junction Temperature	T_J	200	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.1	°C/W

Table 3. ESD Protection Characteristics

Test Conditions	Class
Human Body Model	2 (Minimum)
Machine Model	M3 (Minimum)

Table 4. Electrical Characteristics ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Off Characteristics					
Drain-Source Breakdown Voltage ($V_{GS} = 0 \text{ Vdc}$, $I_D = 20 \mu\text{A}$)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current ($V_{DS} = 28 \text{ Vdc}$, $V_{GS} = 0 \text{ Vdc}$)	I_{DSS}	—	—	1	μAdc
Gate-Source Leakage Current ($V_{GS} = 5 \text{ Vdc}$, $V_{DS} = 0 \text{ Vdc}$)	I_{GSS}	—	—	1	μAdc
On Characteristics					
Gate Threshold Voltage ($V_{DS} = 10 \text{ Vdc}$, $I_D = 100 \mu\text{Adc}$)	$V_{GS(th)}$	2	3	4	Vdc
Gate Quiescent Voltage ($V_{DS} = 28 \text{ Vdc}$, $I_D = 300 \text{ mA}$)	$V_{GS(Q)}$	2	3.3	4.5	Vdc
Drain-Source On-Voltage ($V_{GS} = 10 \text{ Vdc}$, $I_D = 1 \text{ Adc}$)	$V_{DS(on)}$	—	0.29	0.4	Vdc
Forward Transconductance ($V_{DS} = 10 \text{ Vdc}$, $I_D = 1 \text{ Adc}$)	g_{fs}	—	2	—	S
Dynamic Characteristics					
Input Capacitance (Including Input Matching Capacitor in Package) ⁽¹⁾ ($V_{DS} = 26 \text{ Vdc}$, $V_{GS} = 0$, $f = 1 \text{ MHz}$)	C_{iss}	—	98.5	—	pF
Output Capacitance ⁽¹⁾ ($V_{DS} = 26 \text{ Vdc}$, $V_{GS} = 0$, $f = 1 \text{ MHz}$)	C_{oss}	—	37	—	pF
Reverse Transfer Capacitance ($V_{DS} = 26 \text{ Vdc}$, $V_{GS} = 0$, $f = 1 \text{ MHz}$)	C_{rss}	—	1.3	—	pF
Functional Tests (In Freescale Test Fixture, 50 ohm system)					
Two-Tone Common-Source Amplifier Power Gain ($V_{DD} = 26 \text{ Vdc}$, $P_{out} = 30 \text{ W PEP}$, $I_{DQ} = 300 \text{ mA}$, $f_1 = 1960.0 \text{ MHz}$, $f_2 = 1960.1 \text{ MHz}$)	G_{ps}	—	13	—	dB
Two-Tone Drain Efficiency ($V_{DD} = 26 \text{ Vdc}$, $P_{out} = 30 \text{ W PEP}$, $I_{DQ} = 300 \text{ mA}$, $f_1 = 1960.0 \text{ MHz}$, $f_2 = 1960.1 \text{ MHz}$)	η	—	36	—	%
3rd Order Intermodulation Distortion ($V_{DD} = 26 \text{ Vdc}$, $P_{out} = 30 \text{ W PEP}$, $I_{DQ} = 300 \text{ mA}$, $f_1 = 1960.0 \text{ MHz}$, $f_2 = 1960.1 \text{ MHz}$)	IMD	—	-31	—	dBc
Input Return Loss ($V_{DD} = 26 \text{ Vdc}$, $P_{out} = 30 \text{ W PEP}$, $I_{DQ} = 300 \text{ mA}$, $f_1 = 1960.0 \text{ MHz}$, $f_2 = 1960.1 \text{ MHz}$)	IRL	—	-13	—	dB
Two-Tone Common-Source Amplifier Power Gain ($V_{DD} = 26 \text{ Vdc}$, $P_{out} = 30 \text{ W PEP}$, $I_{DQ} = 300 \text{ mA}$, $f_1 = 1930.0 \text{ MHz}$, $f_2 = 1930.1 \text{ MHz}$ and $f_1 = 1990.0 \text{ MHz}$, $f_2 = 1990.1 \text{ MHz}$)	G_{ps}	12	13	—	dB
Two-Tone Drain Efficiency ($V_{DD} = 26 \text{ Vdc}$, $P_{out} = 30 \text{ W PEP}$, $I_{DQ} = 300 \text{ mA}$, $f_1 = 1930.0 \text{ MHz}$, $f_2 = 1930.1 \text{ MHz}$ and $f_1 = 1990.0 \text{ MHz}$, $f_2 = 1990.1 \text{ MHz}$)	η	33	36	—	%
3rd Order Intermodulation Distortion ($V_{DD} = 26 \text{ Vdc}$, $P_{out} = 30 \text{ W PEP}$, $I_{DQ} = 300 \text{ mA}$, $f_1 = 1930.0 \text{ MHz}$, $f_2 = 1930.1 \text{ MHz}$ and $f_1 = 1990.0 \text{ MHz}$, $f_2 = 1990.1 \text{ MHz}$)	IMD	—	-31	-28	dBc
Input Return Loss ($V_{DD} = 26 \text{ Vdc}$, $P_{out} = 30 \text{ W PEP}$, $I_{DQ} = 300 \text{ mA}$, $f_1 = 1930.0 \text{ MHz}$, $f_2 = 1930.1 \text{ MHz}$ and $f_1 = 1990.0 \text{ MHz}$, $f_2 = 1990.1 \text{ MHz}$)	IRL	—	-13	-9	dB

1. Part is internally matched both on input and output.

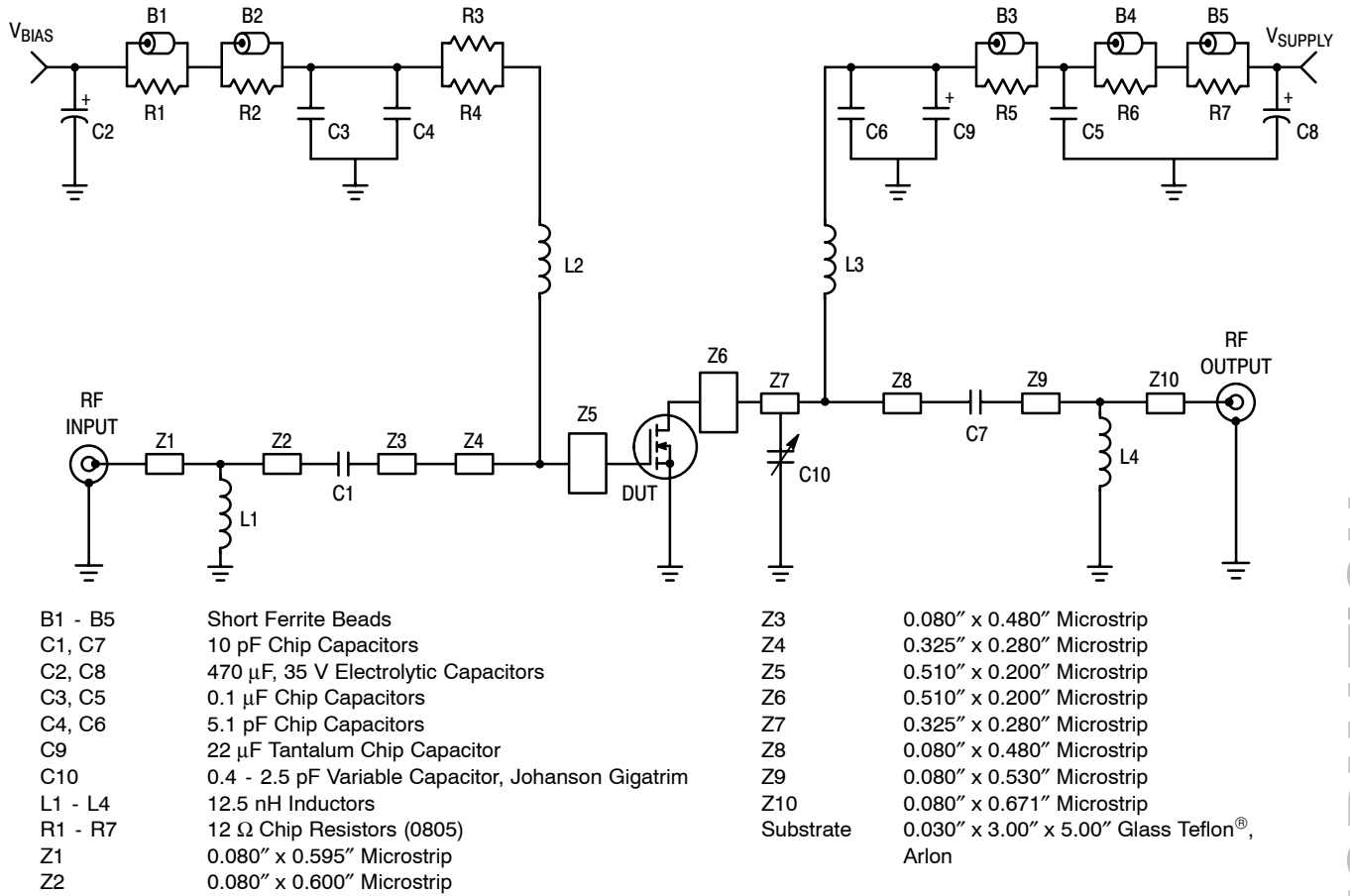
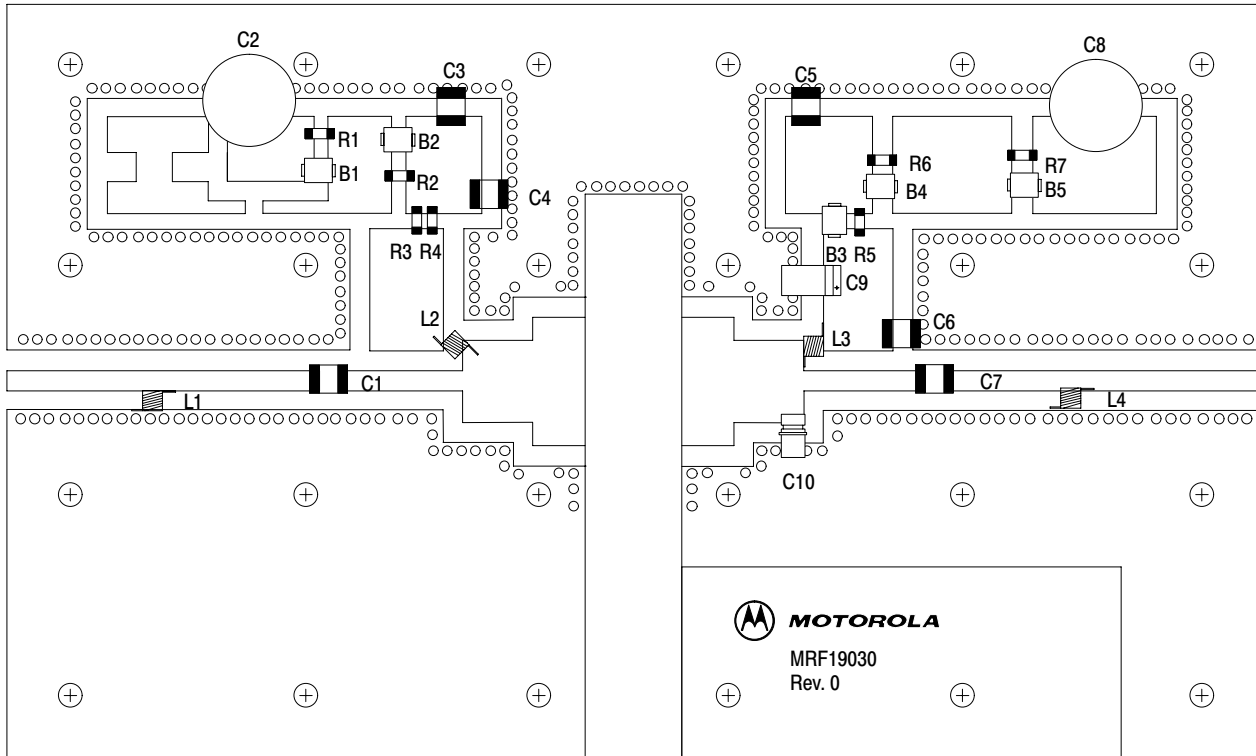


Figure 1. MRF19030LR3(SR3) Test Circuit Schematic



Freescale has begun the transition of marking Printed Circuit Boards (PCBs) with the Freescale Semiconductor signature/logo. PCBs may have either Motorola or Freescale markings during the transition period. These changes will have no impact on form, fit or function of the current product.

Figure 2. MRF19030LR3(SR3) Test Circuit Component Layout

TYPICAL CHARACTERISTICS

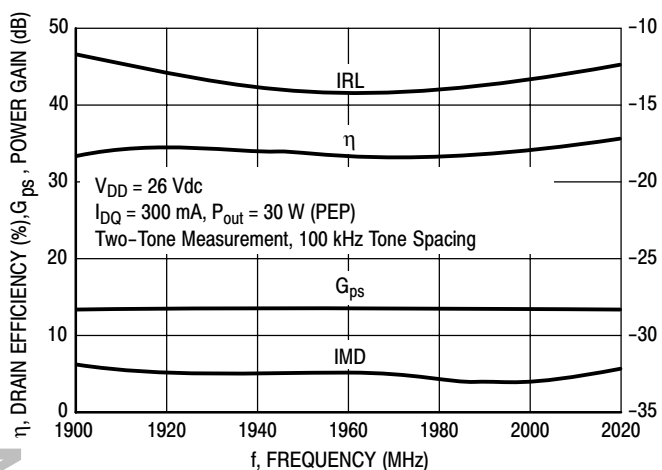


Figure 3. Class AB Broadband Circuit Performance

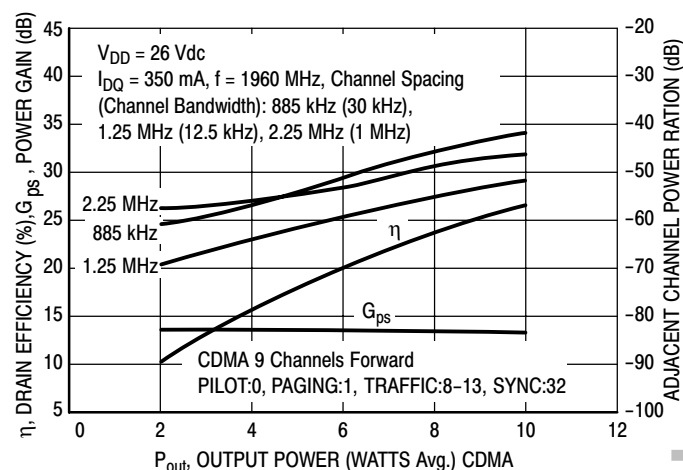


Figure 4. CDMA ACPR, Power Gain and Drain Efficiency versus Output Power

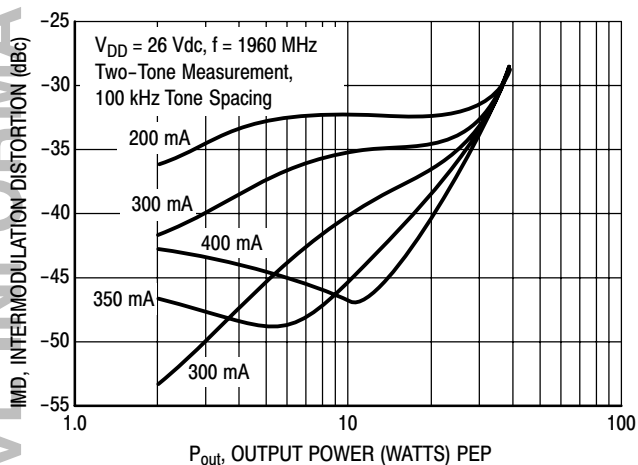


Figure 5. Intermodulation Distortion versus Output Power

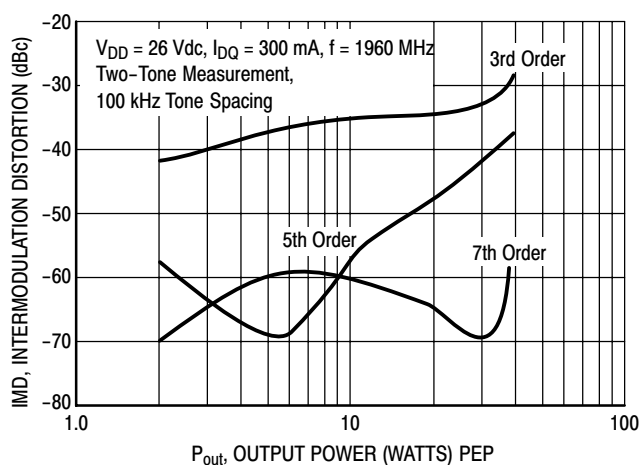


Figure 6. Intermodulation Distortion Products versus Output Power

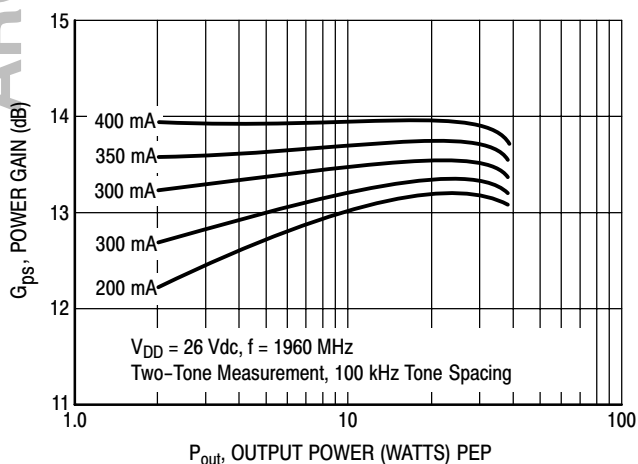


Figure 7. Power Gain versus Output Power

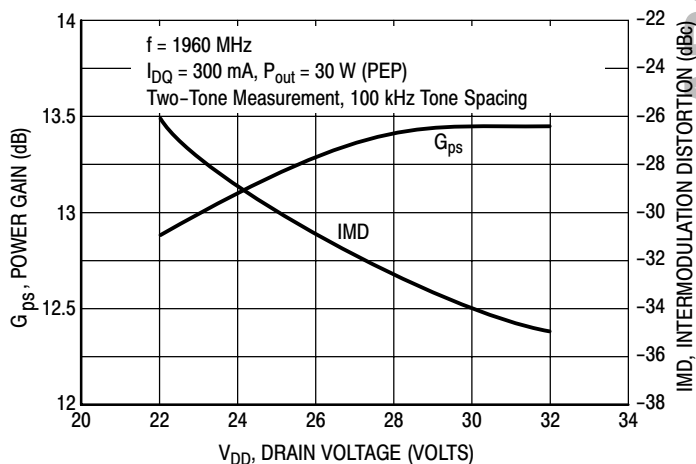
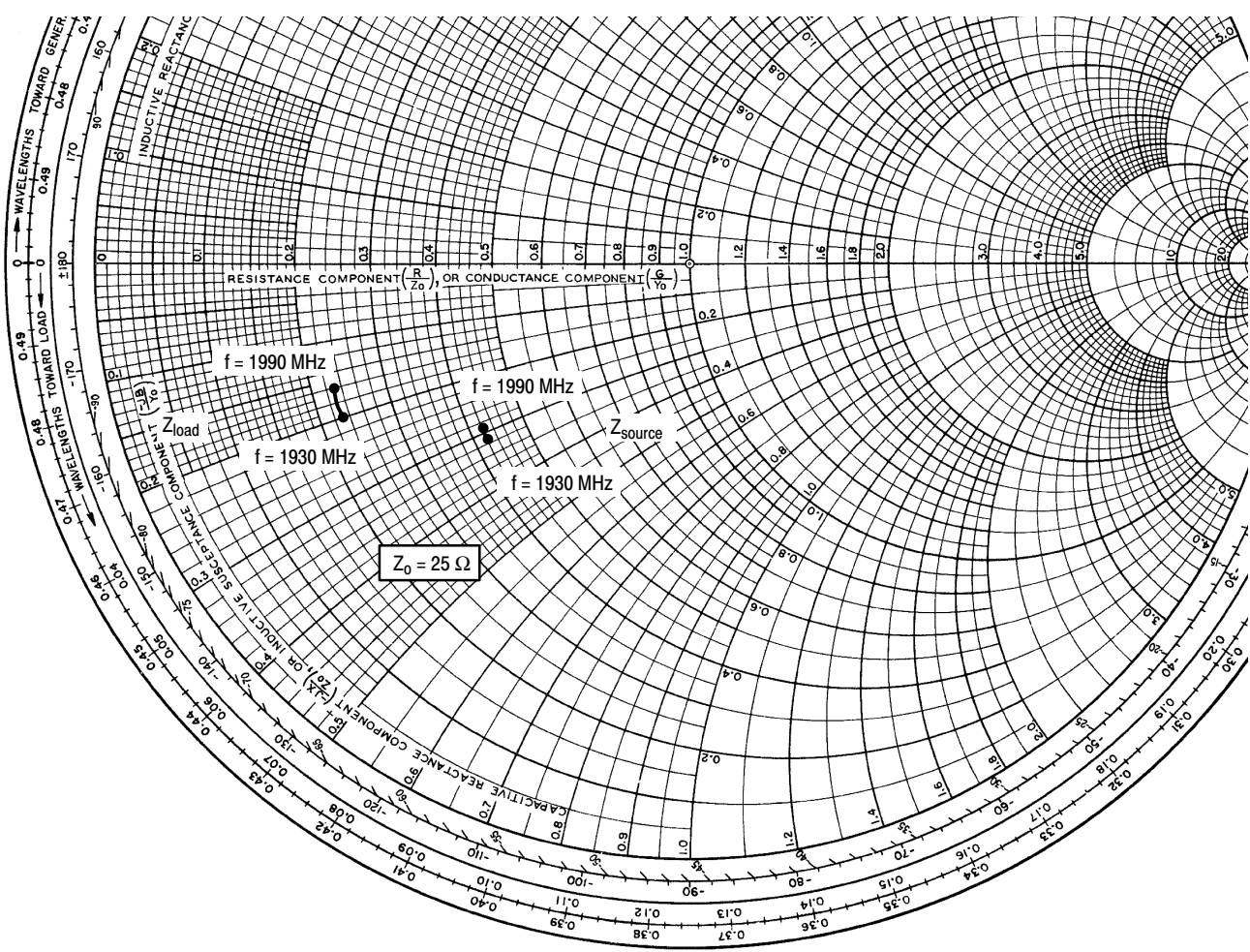


Figure 8. Power Gain and Intermodulation Distortion versus Supply Voltage



$V_{DD} = 26\text{ V}$, $I_{DQ} = 300\text{ mA}$, $P_{out} = 30\text{ W PEP}$

f MHz	Z_{source} Ω	Z_{load} Ω
1930	$10.57 - j7.69$	$5.81 - j5.01$
1960	$10.54 - j7.43$	$5.84 - j4.67$
1990	$10.47 - j7.21$	$5.84 - j4.35$

Z_{source} = Test circuit impedance as measured from gate to ground.
 Z_{load} = Test circuit impedance as measured from drain to ground.

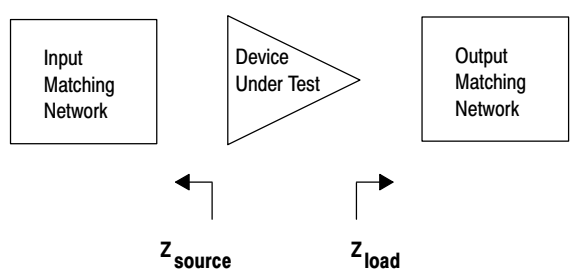
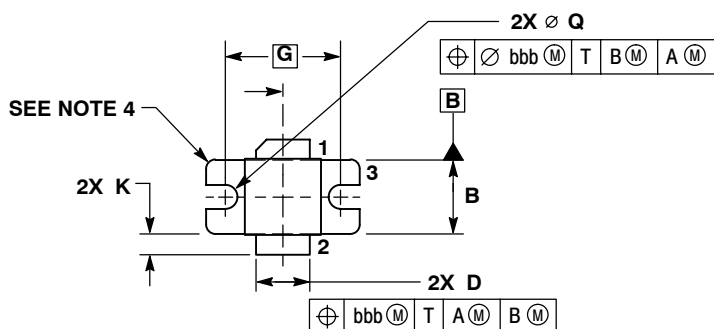


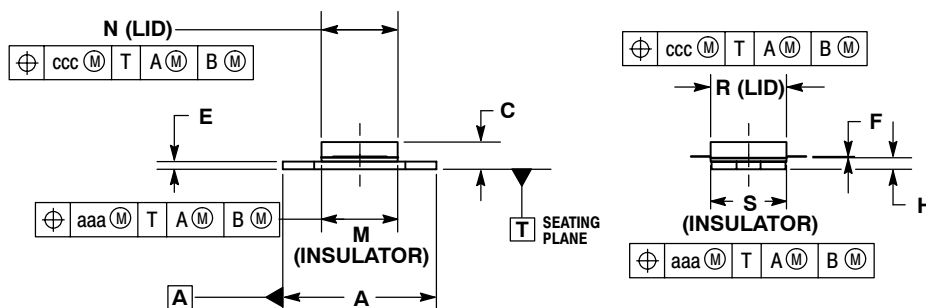
Figure 9. Series Equivalent Source and Load Impedance

PACKAGE DIMENSIONS



- NOTES:
1. CONTROLLING DIMENSION: INCH.
 2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
 3. DIMENSION H IS MEASURED 0.030 (0.762) AWAY FROM PACKAGE BODY.
 4. INFORMATION ONLY: CORNER BREAK (4X) TO BE .060±.005 (1.52±0.13) RADIUS OR .06±.005 (1.52±0.13) x 45° CHAMFER.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.795	.805	20.19	20.44
B	.380	.390	9.65	9.9
C	.125	.163	3.17	4.14
D	.275	.285	6.98	7.24
E	.035	.045	0.89	1.14
F	.004	.006	0.10	0.15
G	.600 BSC		15.24 BSC	
H	.057	.067	1.45	1.7
K	.092	.122	2.33	3.1
M	.395	.405	10	10.3
N	.395	.405	10	10.3
Q	∅ .120	∅ .130	∅ 3.05	∅ 3.3
R	.395	.405	10	10.3
S	.395	.405	10	10.3
aaa	.005 BSC		0.127 BSC	
bbb	.010 BSC		0.254 BSC	
ccc	.015 BSC		0.381 BSC	

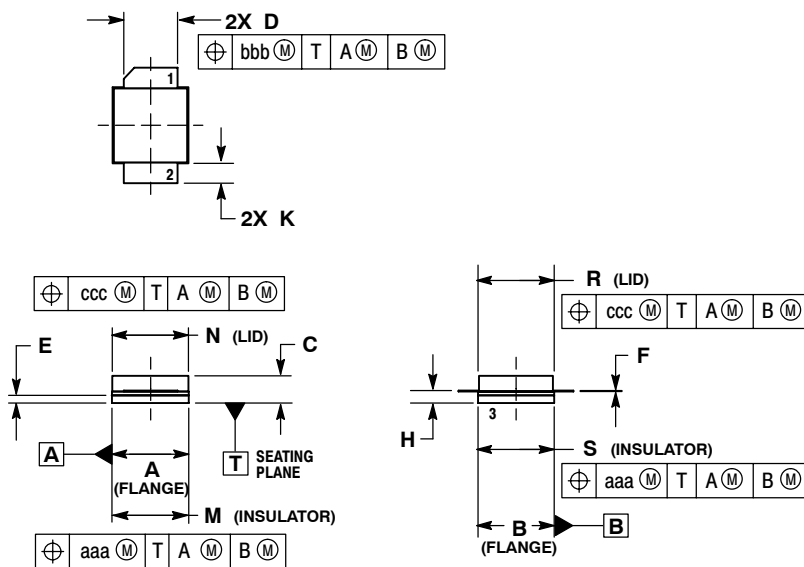


- STYLE 1:
1. PIN 1. DRAIN
 2. GATE
 3. SOURCE

**CASE 465E-04
ISSUE F
NI-400
MRF19030LR3**

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- NOTES:
1. CONTROLLING DIMENSION: INCH.
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 3. DIMENSION H IS MEASURED 0.030 (0.762) AWAY FROM PACKAGE BODY.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.395	.405	10.03	10.29
B	.395	.405	10.03	10.29
C	.125	.163	3.18	4.14
D	.275	.285	6.98	7.24
E	.035	.045	0.89	1.14
F	.004	.006	0.10	0.15
H	.057	.067	1.45	1.70
K	.092	.122	2.34	3.10
M	.395	.405	10.03	10.29
N	.395	.405	10.03	10.29
R	.395	.405	10.03	10.29
S	.395	.405	10.03	10.29
aaa	.005 REF		0.127 REF	
bbb	.010 REF		0.254 REF	
ccc	.015 REF		0.38 REF	

- STYLE 1:
1. PIN 1. DRAIN
 2. GATE
 3. SOURCE

**CASE 465F-04
ISSUE E
NI-400S
MRF19030LSR3**

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