THE DATASHEET OF

NB669GQ-Z

NB669

24V, High Current Synchronous Buck Converter With LDO

DESCRIPTION

The NB669 is a fully integrated high frequency synchronous rectified step-down switch mode converter with 5V fixed output voltage. It offers very compact solution to achieve 6A continuous output current and 9A peak output current over a wide input supply range with excellent load and line regulation. The NB669 operates at high efficiency over a wide output current load range.

Constant-On-Time (COT) control mode provides fast transient response and eases loop stabilization.

Under voltage lockout is internally set as 4.15 V. An open drain power good signal indicates the output is within its nominal voltage range.

NB669 also provides a 5V LDO, which can be used to power the external peripheries, such as the keyboard controller in the laptop computer. A 300kHz CLK is also available; its output can be used to drive an external charge pump, generating gate drive voltage for the load switches without reducing the main converter's efficiency.

Full protection features include OCP, OVP, UVP and thermal shut down.

The converter requires minimum number of external components and is available in QFN16 (3mmx3mm) package.

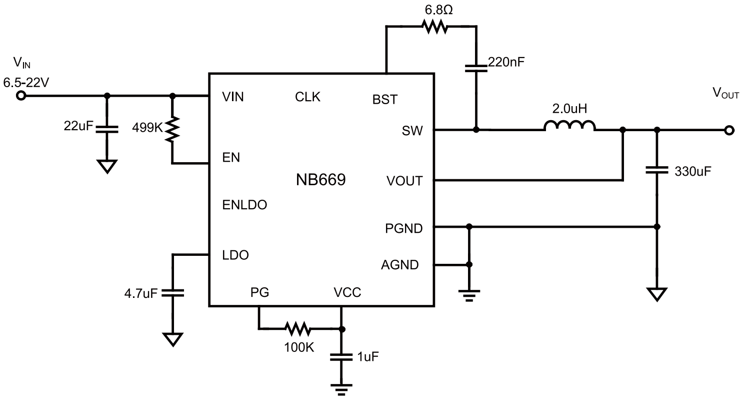
FEATURES

- Wide 6.5V to 24V Operating Input Range
- 5V Fixed Output Voltage
- Built-in 5V, 100mA LDO with Switches
- 6A Continuous Output Current
- 9A Peak Output Current
- 300kHZ CLK for External Charge Pump
- Low R_{DS}(ON) Internal Power MOSFETs
- Proprietary Switching Loss Reduction Technique
- Internal Soft Start
- Output Discharge
- 500kHZ Switching Frequency
- OCP, OVP, UVP Protection and Thermal Shutdown
- Latch off Reset via EN or Power Cycle.

APPLICATIONS

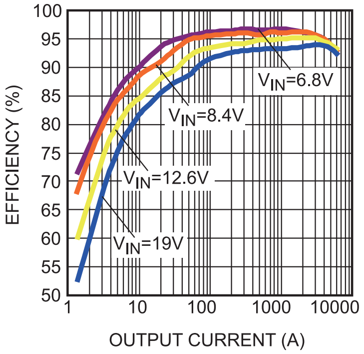
- Laptop Computer
- Tablet PC
- Networking Systems
- Personal Video Recorders
- Flat Panel Television and Monitors
- Distributed Power Systems

TYPICAL APPLICATION



Efficiency vs. Load Current

V_{OUT}=5V, f_{SW}=500kHz,
L=2μH, DCR=7.3mΩ

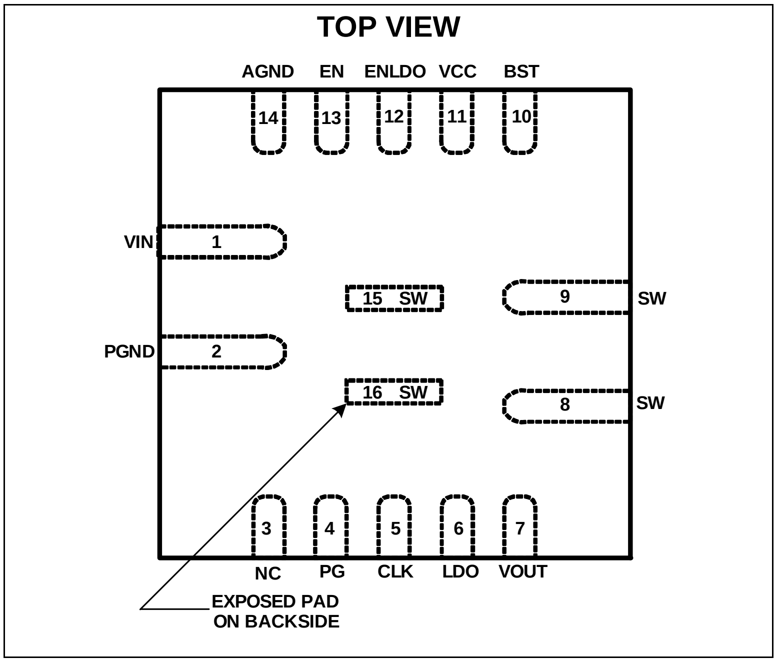


ORDERING INFORMATION

Part Number*	Package	Top Marking
NB669GQ	QFN16 (3mmx3mm)	AEV

***** For Tape & Reel, add suffix –Z (e.g. NB669GQ–Z)

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS (1)

Supply Voltage V_{IN}	24V
V_{SW}	-0.3V to V_{IN} + 0.3V
V_{SW} (30ns)	-3V to V_{IN} + 4V
V_{SW} (5ns)	-6V to V_{IN}+4V
V_{BST}	V_{SW} + 5.5V
V_{EN}	12V
Enable Current I_{EN}(2)	2.5mA
All Other Pins	-0.3V to +5.5V
Continuous Power Dissipation (T_A=+25°C) (3)	
QFN16	1.8W
Junction Temperature	150°C
Lead Temperature	260°C
Storage Temperature	-65°C to +150°C

Recommended Operating Conditions (4)

Supply Voltage V_{IN}	6.5V to 22V
Output Voltage V_{OUT}	5V
Enable Current I_{EN}	1mA
Operating Junction Temp. (T_J)	-40°C to +125°C

Thermal Resistance (5)

	θ_{JA}	θ_{JC}	
QFN16 (3mmx3mm)	70	15	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) Refer to Page 11 of Configuring the EN Control.
3) The maximum allowable power dissipation is a function of the maximum junction temperature T_J(MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by $P_D(MAX)=(T_J(MAX)-T_A)/\theta_{JA}$. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) The device is not guaranteed to function outside of its operating conditions.
5) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_J = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Supply Current						
Supply Current (Shutdown)	$I_{IN\ Shtdn}$	V_{EN} = 0V		1	2	μA
Supply Current (Quiescent)	I_{IN}	V_{EN} = 2V, V_{ENLDO} = 2V , V_{OUT} = 5.2V	140	220	300	μA
Supply Current (No Load)	I_{IN}	V_{EN} = 2V, V_{ENLDO} = 2V , V_{OUT} = 5.05V, Io=0A		240		μA
Supply Current (Standby)	I_{IN_Stby}	V_{EN} = 0V, V_{ENLDO} = 2V , I_{LDO} = 0A	40	80	120	μA
MOSFET						
High-side Switch On Resistance	HS_{RDS-ON}			30		mΩ
Low-side Switch On Resistance	LS_{RDS-ON}			15		mΩ
Switch Leakage	SW_{LKG}	V_{EN} = 0V, V_{SW} = 0V		0	1	μA
Current Limit						
Low-side Valley Current Limit	I_{LIMIT}		8	8.5	9.5	A
Switching frequency and minimum off timer						
Switching Frequency	F_{SW}		400	500	600	kHz
Minimum Off Time(6)	T_{OFF}			350		ns
Over-voltage and Under-voltage Protection						
OVP Threshold	V_{OVP}		125	130	135	% $V_{OUT\ Ref}$
OVP Delay(6)	T_{OVPDEL}			2.5		μs
UVP Threshold	V_{UVP}		55	60	65	% $V_{OUT\ Ref}$
UVP Delay(6)	T_{UVPDEL}			8		μs
V_{OUT}_Ref And Soft Start						
V_{OUT} Ref Voltage	V_{OUT}_Ref		4.95	5.05	5.15	V
Soft Start Time	T_{SS}		1.5	1.8	1.95	ms
Enable And UVLO						
Enable Input Low Voltage	VIL_{EN}		1.15	1.25	1.35	V
Enable Hysteresis	V_{EN-HYS}			100		mV
Enable Input Current	I_{EN}	V_{EN} = 2V		5		μA
		V_{EN} = 0V		0		
Enable LDO Input Low Voltage	V_{ENLDO}		1.15	1.25	1.35	V
Enable LDO Hysteresis	$V_{ENLDO-HYS}$			100		mV

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_J = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
VCC Under Voltage Lockout Threshold Rising	VCC_{Vth}			4.65	4.85	V
VCC Under Voltage Lockout Threshold Hysteresis	VCC_{HYS}			500		mV
CLK Output						
CLK Output High Level Voltage	V_{CLKH}	I_{Vclk}= -5mA	4.75	4.95	5.15	V
CLK Output Low Level Voltage	V_{CLKL}	I_{Vclk}= 5mA	0	0.05	0.1	V
CLK Frequency	F_{CLK}	T_J = 25°C		300		kHz
LDO Regulator						
LDO Regulator	V_{LDO}		4.95	5.1	5.25	V
LDO Load Regulation		I_{LDO} =50mA		5		%
LDO Load capability		Before switch-over	70	90	120	mA
		After switch-over	100			mA
Switch Rdson	R_{Switch}	I_{LDO} =50mA		1.3	2	Ω
VCC Regulator						
VCC Regulator	V_{CC}		5	5.2	5.4	V
VCC Load Regulation		Icc=5mA		5		%
Power Good						
PG Rising (Good)	$PG_{Vth\text{-}Hi}$			95		% V_{OUT_Ref}
PG Falling (Fault)	$PG_{Vth\text{-}Lo}$			85		
PG Rising (Fault)	$PG_{Vth\text{-}Hi}$			115		
PG Falling (Good)	$PG_{Vth\text{-}Lo}$			105		
Power Good Lower to High Delay	PG_{Td}			0.5		ms
Power Good Sink Current Capability	V_{PG}	Sink 4mA			0.4	V
Power Good Leakage Current	I_{PG_LEAK}	V_{PG} = 3.3V			100	nA
Thermal Protection						
Thermal Shutdown (6)	T_{SD}			150		°C
Thermal Shutdown Hysteresis				25		°C

Note:

6) Guaranteed by design.

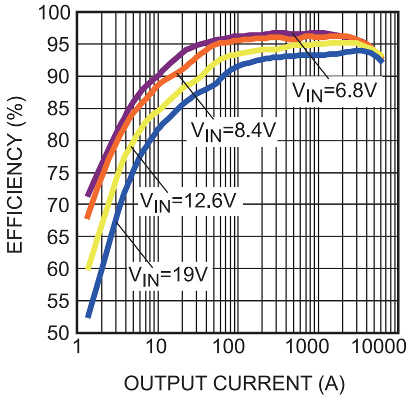
PIN FUNCTIONS

PIN #	Name	Description
1	VIN	Supply Voltage. The VIN pin supplies power for internal MOSFET and regulator. The NB669 operates from a +6.5V to +24V input rail. An input capacitor is needed to decouple the input rail. Use wide PCB traces and multiple vias to make the connection.
2	PGND	Power Ground. Use wide PCB traces and multiple vias to make the connection.
3	NC	Not connected.
4	PG	Power good output. The output of this pin is an open drain signal and is high if the output voltage is higher than 95% of the nominal voltage. There is a delay from Vout ≥ 95% to PGOOD goes high.
5	CLK	300kHZ CLK output to drive the external charge pump
6	LDO	Internal 5V LDO output. Decouple with a minimum 4.7µF ceramic capacitor as close to the pin as possible. X7R or X5R grade dielectric ceramic capacitors are recommended for their stable temperature characteristics. Once the output voltage of the Buck regulator is ready, it will switch over the LDO output to save the power loss.
7	VOUT	Output voltage sense. For the NB669, the output of the Buck regulator is fixed to 5V. VOUT pin is used to sense the output voltage of the Buck regulator, connect this pin to the output capacitor of the regulator directly. This pin also acts as the input of the 5V LDO switch over power input. Keep the VOUT sensing trace far away from the SW node. Vias should also be avoided on the VOUT sensing trace.
8, 9 Exposed Pad 15, 16	SW	Switch Output. Connect this pin to the inductor and bootstrap capacitor. This pin is driven up to the VIN voltage by the high-side switch during the on-time of the PWM duty cycle. The inductor current drives the SW pin negative during the off-time. The on-resistance of the low-side switch and the internal diode fixes the negative voltage. Use wide and short PCB traces to make the connection. Try to minimize the area of the SW pattern.
10	BST	Bootstrap. A capacitor connected between SW and BST pins is required to form a floating supply across the high-side switch driver.
11	VCC	Internal 5V LDO output. The driver and control circuits are powered from this voltage. Decouple with a minimum 1µF ceramic capacitor as close to the pin as possible. X7R or X5R grade dielectric ceramic capacitors are recommended for their stable temperature characteristics.
12	ENLDO	100mA LDO and VCC enable pin. ENLDO is internally pulled up to high. Leave this pin open to enable the LDO. Drive it low to turn off all the regulators.
13	EN	Buck regulator and charge pump clock enable pin. EN is a digital input that turns the Buck regulator and CLK on or off. When the power supply of the control circuit is ready, drive EN high to turn on the Buck regulator and charge pump clock, drive it low to turn them off.
14	AGND	Analog ground. The internal reference is referred to AGND.

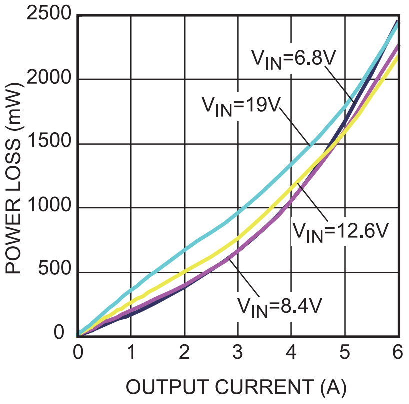
TYPICAL PERFORMANCE CHARACTERISTICS

Performance waveforms are tested on the evaluation board of the Design Example section.
V_{IN}=12V, V_{OUT} =5V, L=2µH, T_J=+25°C, unless otherwise noted.

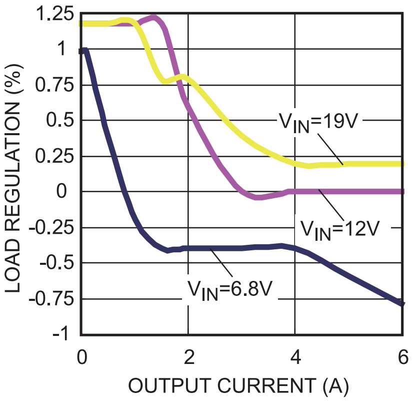
Efficiency vs. Load Current
V_{OUT}=5V, f_{SW}=500kHz,
L=2µH, DCR=7.3mΩ



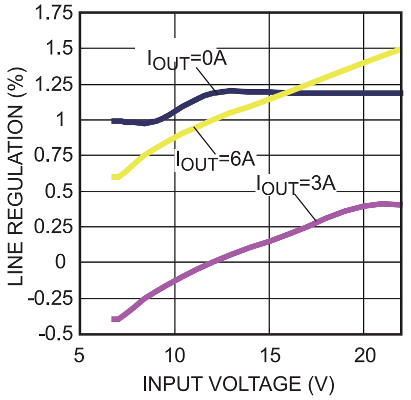
Power Loss
V_{OUT}=5V, f_{SW}=500kHz,
L=2µH, DCR=7.3mΩ



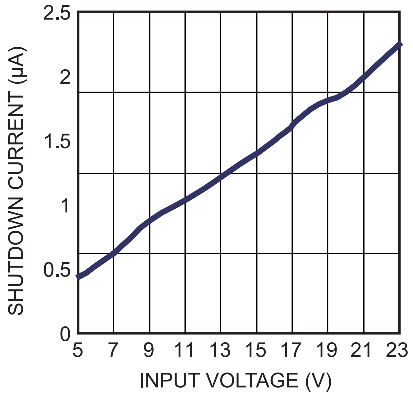
Load Regulation



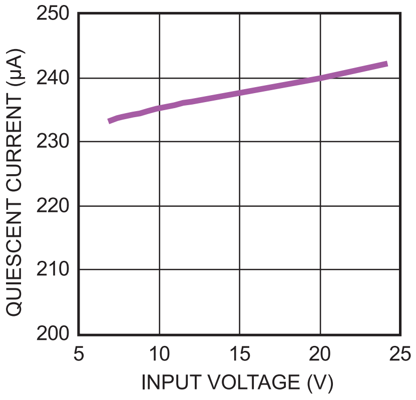
Line Regulation



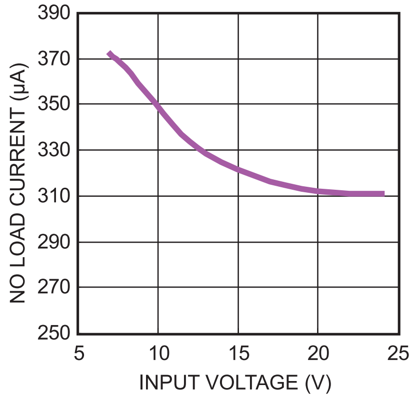
Supply Current (Shutdown) vs. Input Voltage



Supply Current (Quiescent) vs. Input Voltage



Supply Current(No Load) vs. Input Voltage

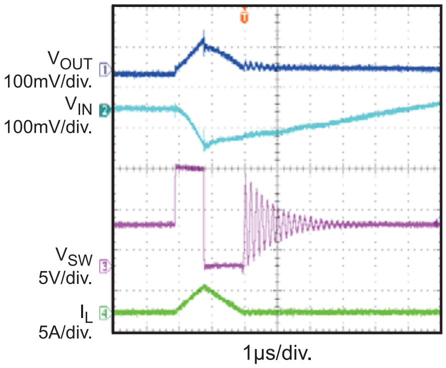


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board of the Design Example section. V_{IN}=12V, V_{OUT} =5V, L=2µH, T_J=+25°C, unless otherwise noted.

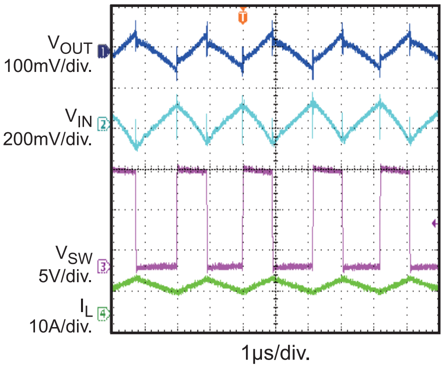
Input/Output Voltage Ripple

I_{OUT} = 0A



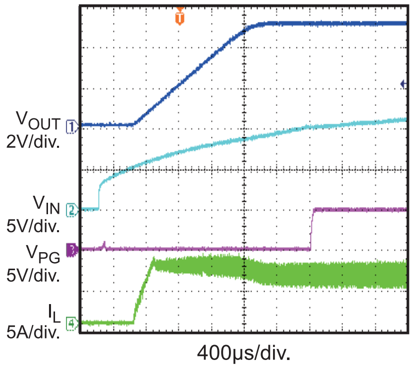
Input/Output Voltage Ripple

I_{OUT} = 6A



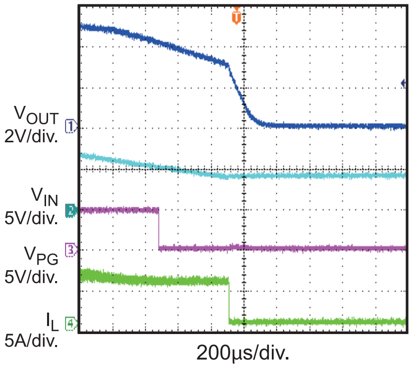
Power Good Through V_{IN} Start-Up

I_{OUT} = 6A



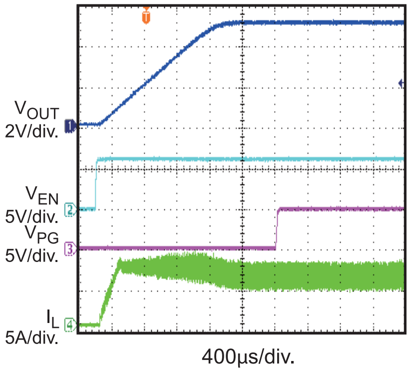
Power Good Through V_{IN} Shutdown

I_{OUT} = 6A



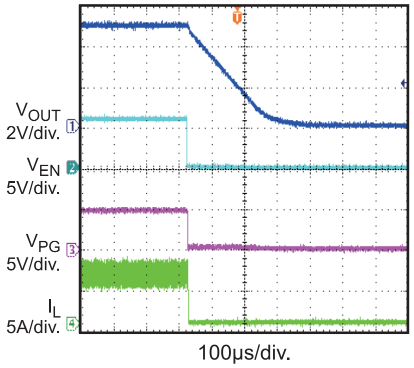
Power Good Through EN Start-Up

I_{OUT} = 6A



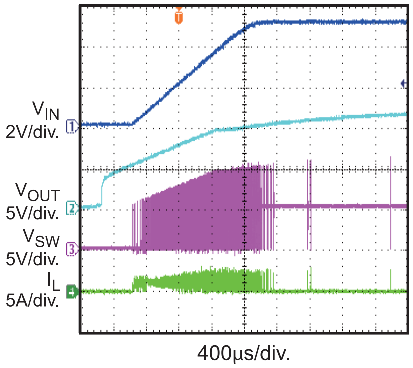
Power Good Through EN Shutdown

I_{OUT} = 6A



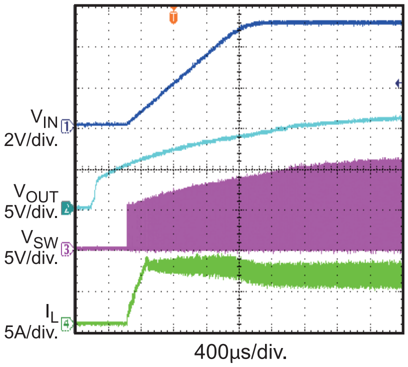
Start-Up Through V_{IN}

I_{OUT} = 0A



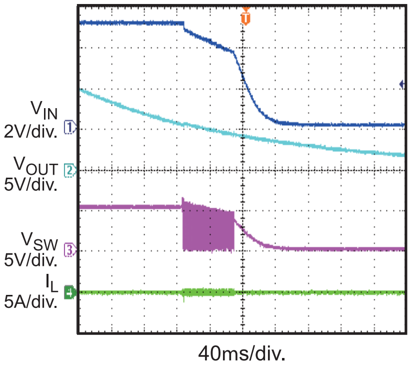
Start-Up Through V_{IN}

I_{OUT} = 6A



Shutdown Through V_{IN}

I_{OUT} = 0A

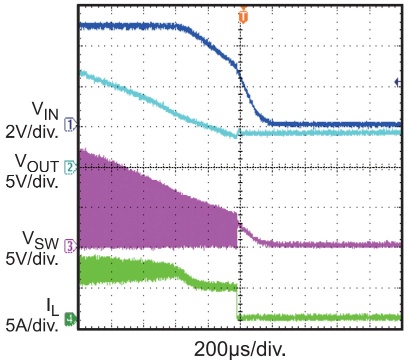


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board of the Design Example section.
V_{IN}=12V, V_{OUT} =5V, L=2µH, T_J=+25°C, unless noted.

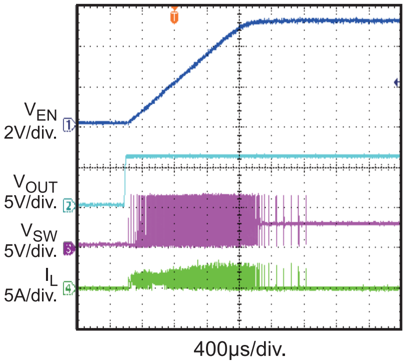
Shutdown Through V_{IN}

I_{OUT} = 6A



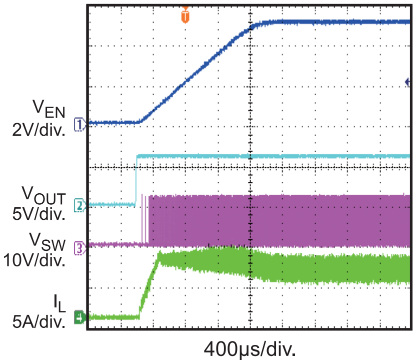
Start-Up Through EN

I_{OUT} = 0A



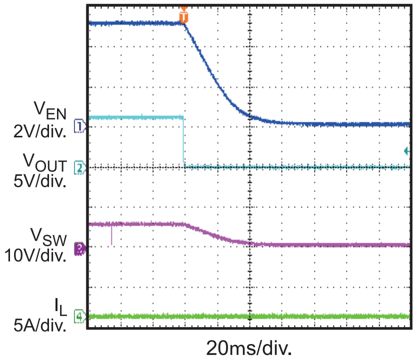
Start-Up Through EN

I_{OUT} = 6A



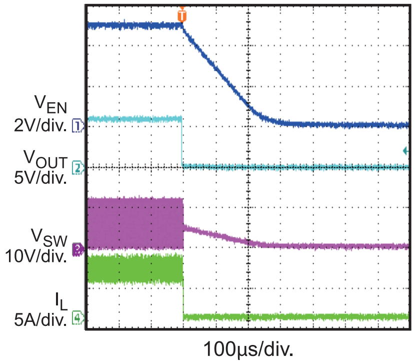
Shutdown Through EN

I_{OUT} = 0A



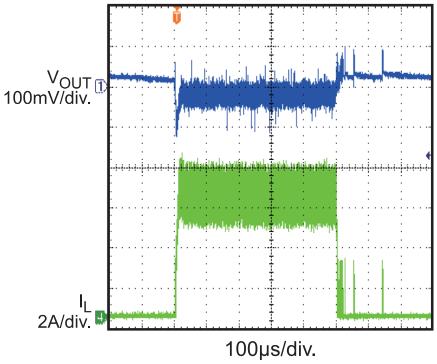
Shutdown Through EN

I_{OUT} = 6A

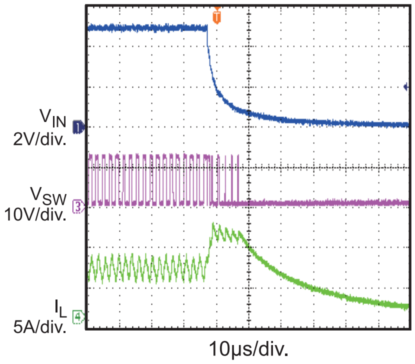


Transient

I_{OUT} = 0A-6A@2.5A/µs
f_{SW} = 500kHz, C_{OUT} = 330µF

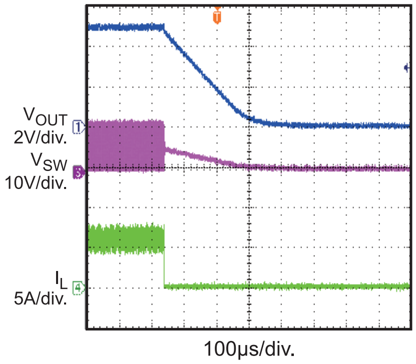


Short Circuit Protection



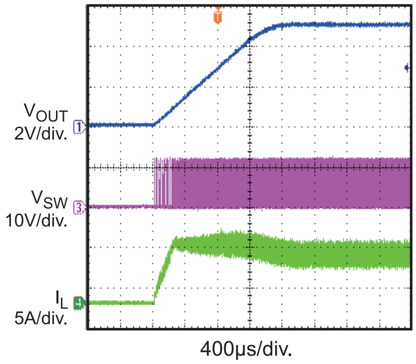
Thermal Shutdown

I_{OUT} =6A



Thermal Recovery

I_{OUT} =6A



BLOCK DIAGRAM

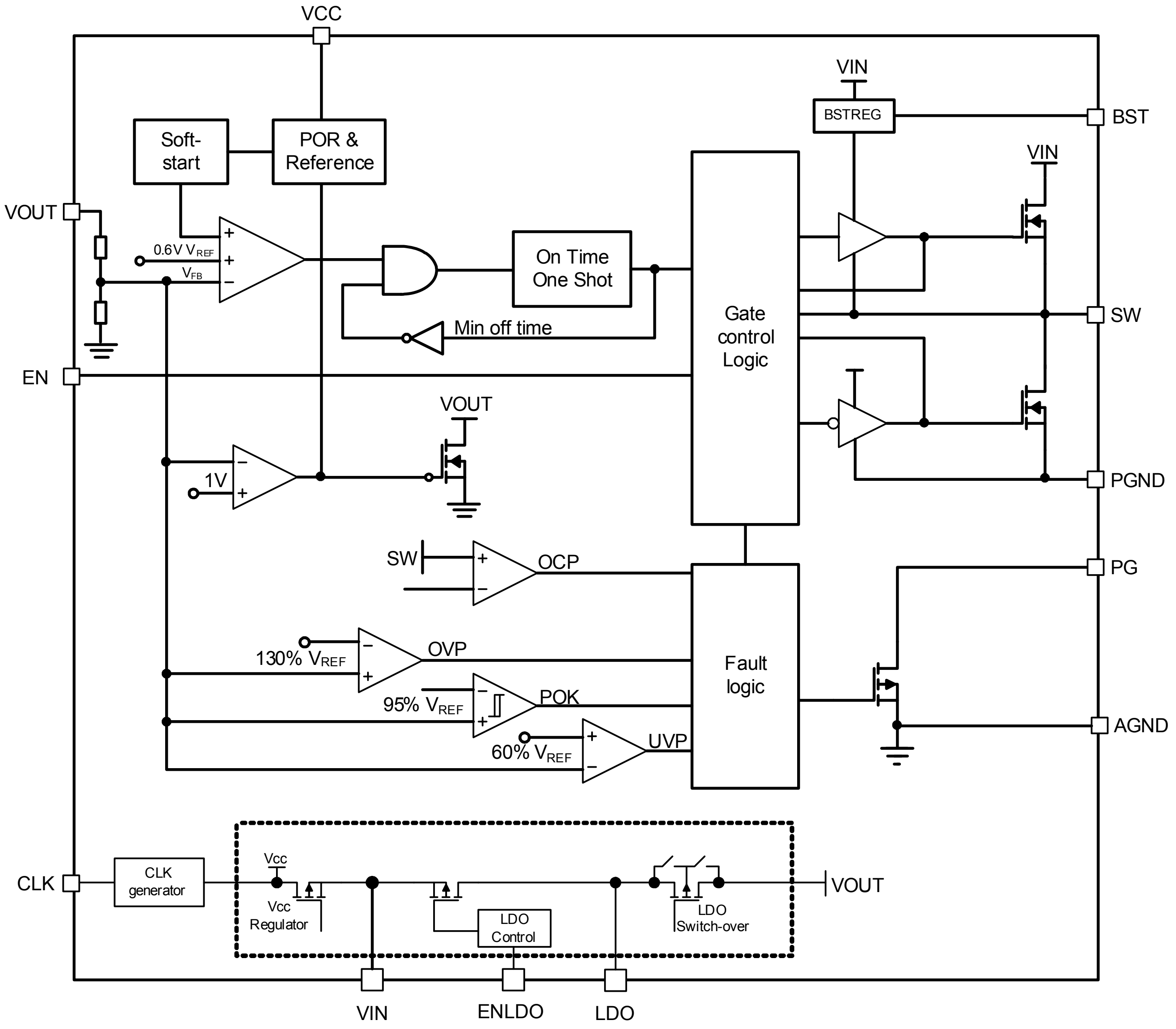


Figure 1—Functional Block Diagram

OPERATION

PWM Operation

The NB669 is fully integrated synchronous rectified step-down switch mode converter. Constant-on-time (COT) control is employed to provide fast transient response and easy loop stabilization. At the beginning of each cycle, the high-side MOSFET (HS-FET) is turned ON when the feedback voltage (V_{FB}) is below the reference voltage (V_{REF}), which indicates insufficient output voltage. The ON period is determined by the output voltage and input voltage to make the switching frequency fairy constant over input voltage range.

After the ON period elapses, the HS-FET is turned off, or becomes OFF state. It is turned ON again when V_{FB} drops below V_{REF}. By repeating operation this way, the converter regulates the output voltage. The integrated low-side MOSFET (LS-FET) is turned on when the HS-FET is in its OFF state to minimize the conduction loss. There will be a dead short between input and GND if both HS-FET and LS-FET are turned on at the same time. It's called shoot-through. In order to avoid shoot-through, a dead-time (DT) is internally generated between HS-FET off and LS-FET on, or LS-FET off and HS-FET on.

An internal compensation is applied for COT control to make a more stable operation even when ceramic capacitors are used as output capacitors, this internal compensation will then improve the jitter performance without affect the line or load regulation.

Heavy-Load Operation

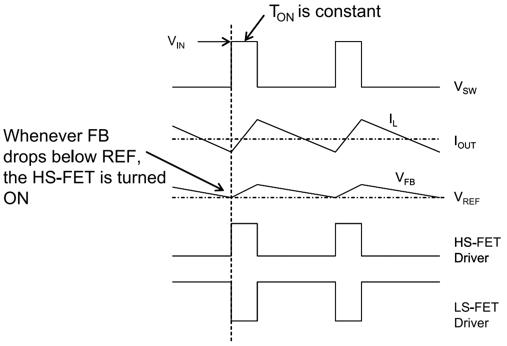


Figure 2—Heavy Load Operation

When the output current is high and the inductor current is always above zero amps, it is called continuous-conduction-mode (CCM). The CCM mode operation is shown in Figure 2 shown. When V_{FB} is below V_{REF}, HS-FET is turned on for a fixed interval. When the HS-FET is turned off, the LS-FET is turned on until next period.

In CCM mode operation, the switching frequency is fairly constant and it is called PWM mode.

Light-Load Operation

With the load decrease, the inductor current decrease too. Once the inductor current touch zero, the operation is transition from continuous-conduction-mode (CCM) to discontinuous-conduction-mode (DCM).

The light load operation is shown in Figure 3. When V_{FB} is below V_{REF}, HS-FET is turned on for a fixed interval which is determined by one- shot on-timer as equation 1 shown. When the HS-FET is turned off, the LS-FET is turned on until the inductor current reaches zero. In DCM operation, the V_{FB} does not reach V_{REF} when the inductor current is approaching zero. The LS-FET driver turns into tri-state (high Z) whenever the inductor current reaches zero. A current modulator takes over the control of LS-FET and limits the inductor current to less than -1mA. Hence, the output capacitors discharge slowly to GND through LS-FET. As a result, the efficiency at light load condition is greatly improved. At light load condition, the HS-FET is not turned ON as frequently as at heavy load condition. This is called skip mode.

At light load or no load condition, the output drops very slowly and the NB669 reduces the switching frequency naturally and then high efficiency is achieved at light load.

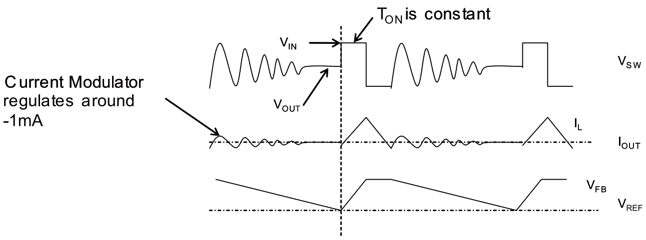


Figure 3—Light Load Operation

As the output current increases from the light load condition, the time period within which the current modulator regulates becomes shorter. The HS-FET is turned ON more frequently. Hence, the switching frequency increases correspondingly. The output current reaches the critical level when the current modulator time is zero. The critical level of the output current is determined as follows:

$$I_{OUT} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times L \times F_{SW} \times V_{IN}} \quad (1)$$

It turns into PWM mode once the output current exceeds the critical level. After that, the switching frequency stays fairly constant over the output current range.

Jitter and FB Ramp Slope

Jitter occurs in both PWM and skip modes when noise in the V_{FB} ripple propagates a delay to the HS-FET driver, as shown in Figures 4 and 5. Jitter can affect system stability, with noise immunity proportional to the steepness of V_{FB}'s downward slope. However, V_{FB} ripple does not directly affect noise immunity.

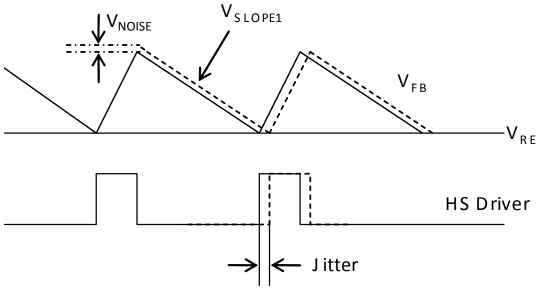


Figure 4—Jitter in PWM Mode

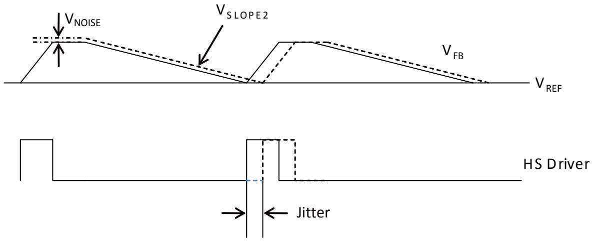


Figure 5—Jitter in Skip Mode

Selecting the Output Capacitors

The traditional constant-on-time control scheme is intrinsically unstable if output capacitor's ESR is not large enough as an effective current-sense resistor. Ceramic capacitors usually can not be used as output capacitor.

Figure 6 shows an equivalent circuit in PWM mode with the HS-FET off. To realize the stability, the ESR value should be chosen as follow:

$$R_{ESR} \geq \frac{\frac{T_{SW}}{0.7 \times \pi} + \frac{T_{ON}}{2}}{C_{OUT}} \quad (2)$$

T_{SW} is the switching period.

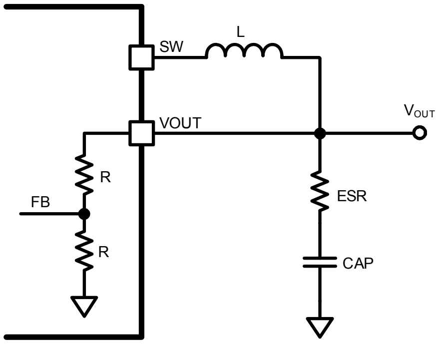


Figure 6—Simplified Circuit in PWM Mode

The NB669 has built in internal ramp compensation to make sure the system is stable even without the help of output capacitor's ESR; and thus the pure ceramic capacitor solution can be applicant. The pure ceramic capacitor solution can significantly reduce the output ripple, total BOM cost and the board area.

Configuring the EN Control

The NB669 has two enable pins to control the on/off of the internal regulators.

ENLDO is used to enable or disable the whole chip. Once ENLDO is off, all the regulators include Vcc will be off. ENLDO is internally pulled high so it can be floated in the normal operation. When ENLDO is pulled high, Pull En high to turn on the Buck regulator also the charge pump clk, and pull EN low to turn them off. Do not float the EN pin.

See Table1 for the logics to control the regulators

Table 1—ENLDO/EN Control

State	ENLDO	EN	VCC	VOUT/CLK	LDO
S0	1	1	ON	ON	ON
S3	1	0	ON	OFF	ON
S4/S5	0	0	OFF	OFF	OFF
Others	0	1	OFF	OFF	OFF

For automatic start-up the EN pin can be pulled up to input voltage through a resistive voltage divider. Choose the values of the pull-up resistor (R_{UP} from Vin pin to EN pin) and the pull-down resistor (R_{DOWN} from EN pin to GND) to determine the automatic start-up voltage:

$$V_{IN-START} = 1.25 \times \frac{R_{UP} + R_{DOWN}}{R_{DOWN}}(V) \tag{3}$$

For example, for R_{UP}=150kΩ and R_{DOWN}=51kΩ, the $V_{IN-START}$ is set at 4.92V.

To avoid noise, a 10nF ceramic capacitor from EN to GND is recommended.

There is an internal Zener diode on the EN pin, which clamps the EN pin voltage to prevent it from running away. The maximum pull up current assuming a worst case 12V internal Zener clamp should be less than 1mA.

Therefore, when EN is driven by an external logic signal, the EN voltage should be lower than 12V; when EN is connected with VIN through a pull-up resistor or a resistive voltage divider, the resistance selection should ensure the maximum pull up current less than 1mA.

If using a resistive voltage divider and VIN higher than 12V, the allowed minimum pull-up resistor R_{UP} should meet the following equation:

$$\frac{V_{IN}(V)-12}{R_{UP}(k\Omega)} - \frac{12}{R_{DOWN}(k\Omega)} < 1(mA) \tag{4}$$

Especially, just using the pull-up resistor R_{UP} (the pull-down resistor is not connected), the $V_{IN-START}$ is determined by input UVLO, and the minimum resistor value is:

$$R_{UP}(k\Omega) > \frac{V_{IN}(V)-12}{1(mA)} \tag{5}$$

A typical pull-up resistor is 499kΩ.

Soft Start

The NB669 employs soft start (SS) mechanism to ensure smooth output during power-up. When the EN pin becomes high, the internal reference voltage ramps up gradually; hence, the output voltage ramps up smoothly, as well. Once the reference voltage reaches the target value, the soft start finishes and it enters into steady state operation.

If the output is pre-biased to a certain voltage during startup, the IC will disable the switching of both high-side and low-side switches until the voltage on the internal reference exceeds the sensed output voltage at the internal FB node.

5V Linear Regulator

There is a built-in 100-mA standby linear regulator which outputs 5V.The 5V LDO is intended mainly for auxiliary 5V supply for the notebook system during standby mode.

Add a ceramic capacitor with a value between 4.7µF and 22µF placed close to the LDO pins to stabilize LDOs.

5V LDO Switch Over

When the output voltage becomes higher than 4.77V and the power good flag is generated, internal 5V LDO regulator is shut off and the LDO output is connected to Vout pin by the internal switch over MOSFET. The 20-us power good deglitch time helps a switch over without glitch.

CLK for Charge Pump

The 300kHz CLK signal can be used to drive an external charge pump circuit to generate approximately 12-15V DC voltage. The CLK voltage becomes available once the VIN is higher than UVLO threshold. Example of charge pump control circuit is shown in Figure 7.

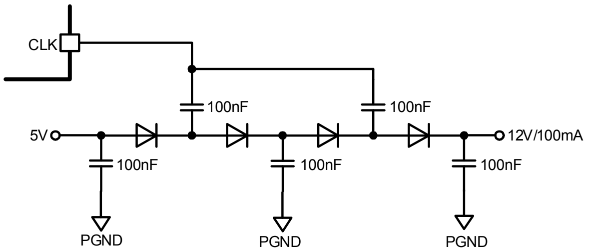


Figure 7—Charge Pump Circuit

Power Good (PG)

The NB669 has power-good (PG) output used to indicate whether the output voltage of the Buck regulator is ready or not. The PG pin is the open drain of a MOSFET. It should be connected to V_{CC} or other voltage source through a resistor (e.g. 100k). After the input voltage is applied, the MOSFET is turned on so that the PG pin is pulled to GND before SS is ready. After FB voltage reaches 95% of REF voltage, the PG pin is pulled high after a delay. The PG delay time is 0.5ms.

When the FB voltage drops to 85% of REF voltage, the PG pin will be pulled low.

Over Current Protection

NB669 has cycle-by-cycle over current limiting control. The current-limit circuit employs a "valley" current-sensing algorithm. The part uses the Rds(on) of the low side MOSFET as a current-sensing element. If the magnitude of the current-sense signal is above the current-limit threshold, the PWM is not allowed to initiate a new cycle.

The trip level is fixed internally. The inductor current is monitored by the voltage between GND pin and SW pin. GND is used as the positive current sensing node so that GND should be connected to the source terminal of the bottom MOSFET.

Since the comparison is done during the high side MOSFET OFF and low side MOSFET ON state, the OC trip level sets the valley level of the inductor current. Thus, the load current at over-current threshold, I_{OC}, can be calculated as follows:

$$I_{OC} = I\_limit + \frac{\Delta I_{inductor}}{2} \qquad (6)$$

In an over-current condition, the current to the load exceeds the current to the output capacitor; thus the output voltage tends to fall off. Eventually, it will end up with crossing the under voltage protection threshold and shutdown. And fault latching can be reset by EN going low or Power-cycling of VIN.

Over/Under-Voltage Protection (OVP/UVP)

NB669 monitors output voltage to detect over and under voltage. When the feedback voltage becomes higher than 115% of the target voltage, the controller will enter Dynamic Regulation Period. During this period, the LS will off when the LS current goes to -1A, this will then discharge the output and try to keep it within the normal range. If the dynamic regulation can not limit the increasing of the Vo, once the feedback voltage becomes higher than 130% of the feedback voltage, the OVP comparator output goes high and the circuit latches as the high-side MOSFET driver OFF and the low-side MOSFET driver turn on acting as an -1A current source.

When the feedback voltage becomes lower than 60% of the target voltage, the UVP comparator output goes high if the UV still occurs after 26us delay; then the fault latch will be triggered---latches HS off and LS on; the LS FET keeps on until the inductor current goes zero. Also fault latching can be reset by EN going low or Power-cycling of VIN.

UVLO Protection

The NB669 has under-voltage lock-out protection (UVLO). When the VCC voltage is higher than the UVLO rising threshold voltage, the part will be powered up. It shuts off when the VIN voltage is lower than the UVLO falling threshold voltage. This is non-latch protection. The part is disabled when the VCC voltage falls below 4.65V. If an application requires a higher under-voltage lockout (UVLO), use the EN pin as shown in Figure 8 to adjust the input voltage UVLO by using two external resistors. It is recommended to use the enable resistors to set the UVLO falling threshold (VSTOP) above 4.65V. The rising threshold (VSTART) should be set to provide enough hysteresis to allow for any input supply variations. Besides fault latching can be reset by EN going low or Power-cycling of VIN.

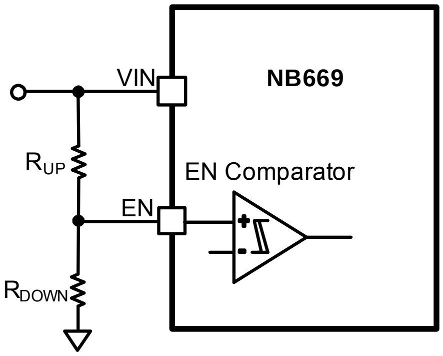


Figure 8—Adjustable UVLO

Thermal Shutdown

Thermal shutdown is employed in the NB669. The junction temperature of the IC is internally monitored. If the junction temperature exceeds the threshold value (typical 150ºC), the converter shuts off. This is a non-latch protection. There is about 25ºC hysteresis. Once the junction temperature drops to about 125ºC, it initiates a SS.

Output Discharge

NB669 discharges the output when EN is low, or the controller is turned off by the protection functions (UVP & OCP, OCP, OVP, UVLO, and thermal shutdown). The part discharges outputs using an internal 6Ω MOSFET.

APPLICATION INFORMATION

Input Capacitor

The input current to the step-down converter is discontinuous and therefore requires a capacitor to supply the AC current to the step-down converter while maintaining the DC input voltage. Ceramic capacitors are recommended for best performance and should be placed as close to the VIN pin as possible. Capacitors with X5R and X7R ceramic dielectrics are recommended because they are fairly stable with temperature fluctuations.

The capacitors must also have a ripple current rating greater than the maximum input ripple current of the converter. The input ripple current can be estimated as follows:

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \qquad (7)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, where:

$$I_{CIN} = \frac{I_{OUT}}{2} \qquad (8)$$

For simplification, choose the input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitance value determines the input voltage ripple of the converter. If there is an input voltage ripple requirement in the system, choose the input capacitor that meets the specification.

The input voltage ripple can be estimated as follows::

$$\Delta V_{IN} = \frac{I_{OUT}}{F_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \qquad (9)$$

Under worst-case conditions where $V_{IN} = 2V_{OUT}$:

$$\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{F_{SW} \times C_{IN}} \qquad (10)$$

Output Capacitor

The output capacitor is required to maintain the DC output voltage. Ceramic or POSCAP capacitors are recommended. The output voltage ripple can be estimated as:

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 \times F_{SW} \times C_{OUT}}) \qquad (11)$$

In the case of ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is mainly caused by the capacitance. For simplification, the output voltage ripple can be estimated as:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times F_{SW}{}^{2} \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \qquad (12)$$

In the case of POSCAP capacitors, the ESR dominates the impedance at the switching frequency. The ramp voltage generated from the ESR is high enough to stabilize the system. Therefore, an external ramp is not needed. A minimum ESR value around 12mΩ is required to ensure stable operation of the converter. For simplification, the output ripple can be approximated as:

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \qquad (13)$$

Maximum output capacitor limitation should be also considered in design application. NB669 has an around 1.8ms soft-start time period. If the output capacitor value is too high, the output voltage can't reach the design value during the soft-start time, and then it will fail to regulate. The maximum output capacitor value C_{O_MAX} can be limited approximately by:

$$C_{O\_MAX} = (I_{LIM\_AVG} - I_{OUT}) \times T_{ss} / V_{OUT} \qquad (14)$$

Where, I_{LIM_AVG} is the average start-up current during soft-start period. T_{ss} is the soft-start time.

Inductor

The inductor is necessary to supply constant current to the output load while being driven by the switched input voltage. A larger-value inductor will result in less ripple current that will result in lower output ripple voltage. However, a larger-value inductor will have a larger physical footprint, higher series resistance, and/or lower saturation current. A good rule for determining the inductance value is to design the peak-to-peak ripple current in the inductor to be in the range of 30% to 40% of the maximum output current, and that the peak inductor current is below the maximum switch current limit. The inductance value can be calculated by:

$$L = \frac{V_{OUT}}{F_{SW} \times \Delta I_L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (15)$$

Where ΔI_L is the peak-to-peak inductor ripple current.

The inductor should not saturate under the maximum inductor peak current, where the peak inductor current can be calculated by:

$$I_{LP} = I_{OUT} + \frac{V_{OUT}}{2F_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (16)$$

PCB Layout Guide

The following guidelines should be followed when designing the PC board for the NB669:

1. The high current paths (GND, IN, and SW) should be placed very close to the device with short, direct and wide traces.
2. Put the input capacitors as close to the IN and GND pins as possible.
3. Put the decoupling capacitor as close to the VCC and AGND pins as possible. Place the Cap close to AGND if the distance is long. And place >3 Vias if via is required to reduce the leakage inductance.
4. Keep the VOUT sensing trace far away from the SW node.Vias should also be avoided on the VOUT sensing trace.
5. Keep the BST voltage path (BST, C3, and SW) as short as possible.
6. Keep the IN and GND pads connected with large copper and use at least two layers for IN and GND trace to achieve better thermal performance. Also, add several Vias with 10mil_drill/18mil_copper_width close to the IN and GND pads to help on thermal dissipation.
7. AGND connects PGND with KELVIN Connecting.
8. Four-layer layout is strongly recommended to achieve better thermal performance.

Note:

Please refer to the PCB Layout Application Note for more details.

AGND KELVIN
CONNECT TO PGND

DO NOT CONNECT
TO AGND HERE

Figure 9—Recommend Layout

Recommend Design Example

A typical application schematic is shown in Figure 10 when large ESR caps are used, and Figure 11 shows the schematic when low ESR caps are applied. The typical performance and circuit waveforms have been shown in the Typical Performance Characteristics section. For more possible applications of this device, please refer to related Evaluation Board Datasheets.

TYPICAL APPLICATION

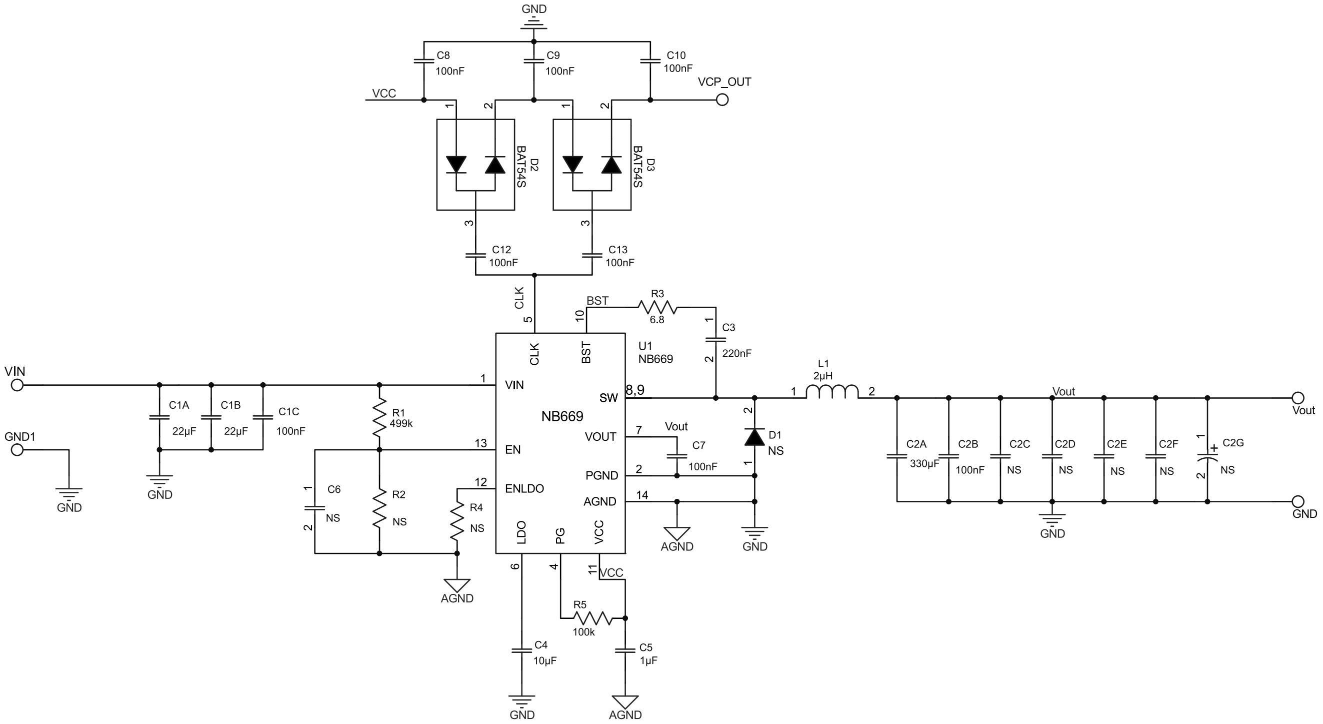


Figure 10---Typical Application Circuit with Poscap

NB669 V_{IN}=6.5-22V, V_{OUT}=5V, I_{OUT}=6A, F_{SW}=500kHz

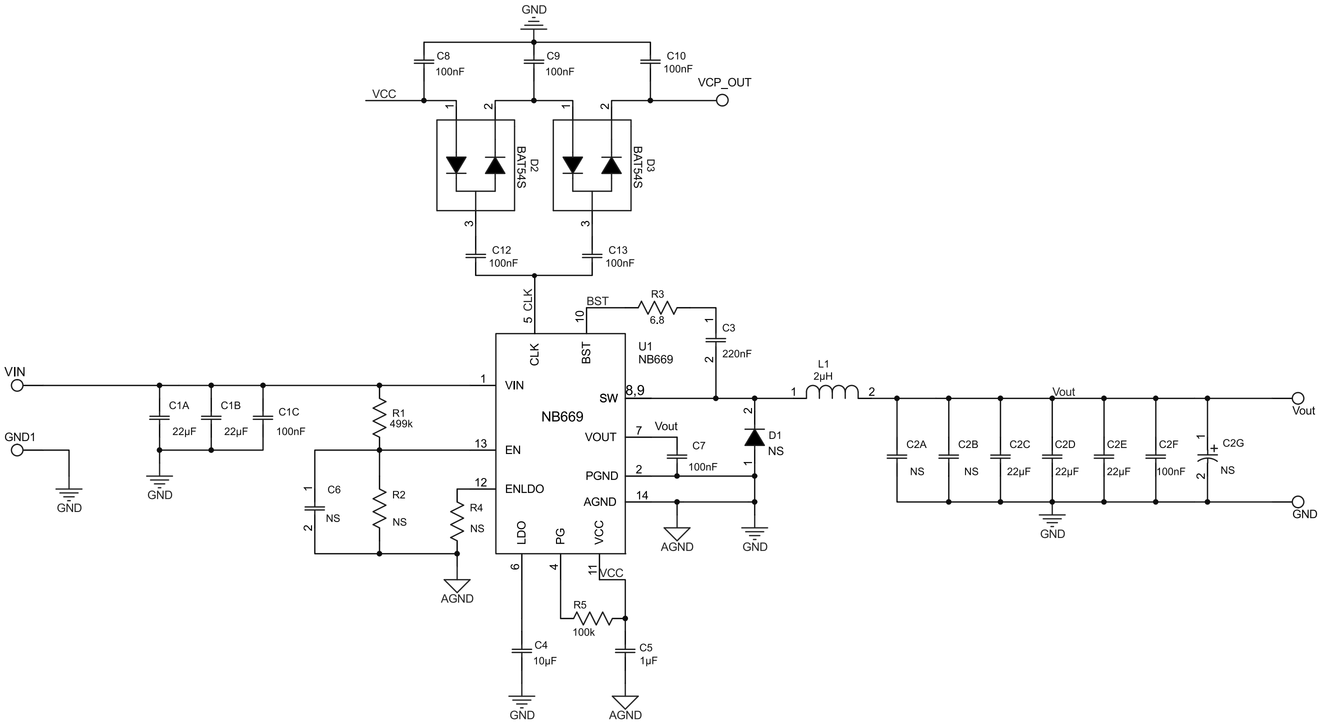
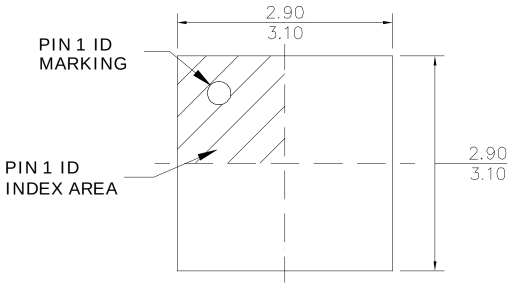


Figure 11---Typical Application Circuit with Low ESR Ceramic Capacitor

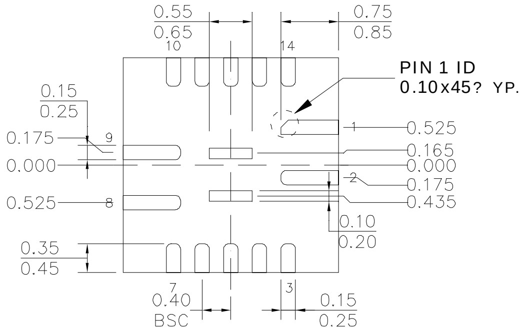
NB669 V_{IN}=6.5-22V, V_{OUT}=5V, I_{OUT}=6A, F_{SW}=500kHz

PACKAGE INFORMATION

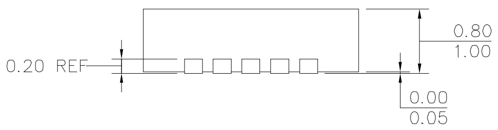
QFN16 (3X3mm)



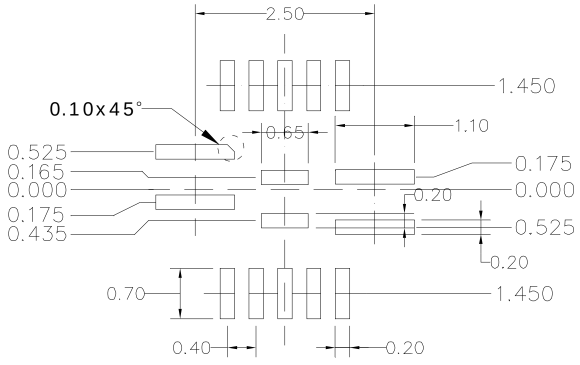
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.