



THE DATASHEET OF OPA656TDB2



WIDEBAND, UNITY-GAIN STABLE, FET-INPUT OPERATIONAL AMPLIFIER

 Check for Samples: [OPA656-DIE](#)

FEATURES

- Unity-Gain Bandwidth
- Low Input Bias Current
- Low Offset and Drift
- Low DL
- High Output Current
- Low Input Voltage Noise

APPLICATIONS

- Wideband Photodiode Amplifiers
- Sample-and-Hold Buffers
- CCD Output Buffers
- ADC Input Buffers
- Wideband Precision Amplifiers
- Test and Measurement Front Ends

DESCRIPTION

The OPA656 combines a very wideband, unity-gain stable, voltage-feedback op amp with a FET-input stage to offer an ultra high dynamic-range amplifier for ADC (analog-to-digital converter) buffering and transimpedance applications. Extremely low DC errors give good precision in optical applications.

The high unity-gain stable bandwidth and JFET input allows exceptional performance in high-speed, low-noise integrators.

ORDERING INFORMATION⁽¹⁾

PRODUCT	PACKAGE DESIGNATOR	PACKAGE ⁽²⁾	ORDERABLE PART NUMBER	PACKAGE QUANTITY
OPA656	TD	Bare die in waffle pack	OPA656TDB1	400
			OPA656TDB2	10

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
- (2) Processing is per the Texas Instruments commercial production baseline and is in compliance with the Texas Instruments Quality Control System in effect at the time of manufacture. Electrical screening consists of DC parametric and functional testing at room temperature only. Unless otherwise specified by Texas Instruments AC performance and performance over temperature is not warranted. Visual Inspection is performed in accordance with MIL-STD-883 Test Method 2010 Condition B at 75X minimum.



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

BARE DIE INFORMATION

DIE THICKNESS	BACKSIDE FINISH	BACKSIDE POTENTIAL	BOND PAD METALLIZATION COMPOSITION	BOND PAD THICKNESS
15 mils.	Silicon with backgrind	V _{S-}	TiW/AlCu (0.5%)	1100 nm

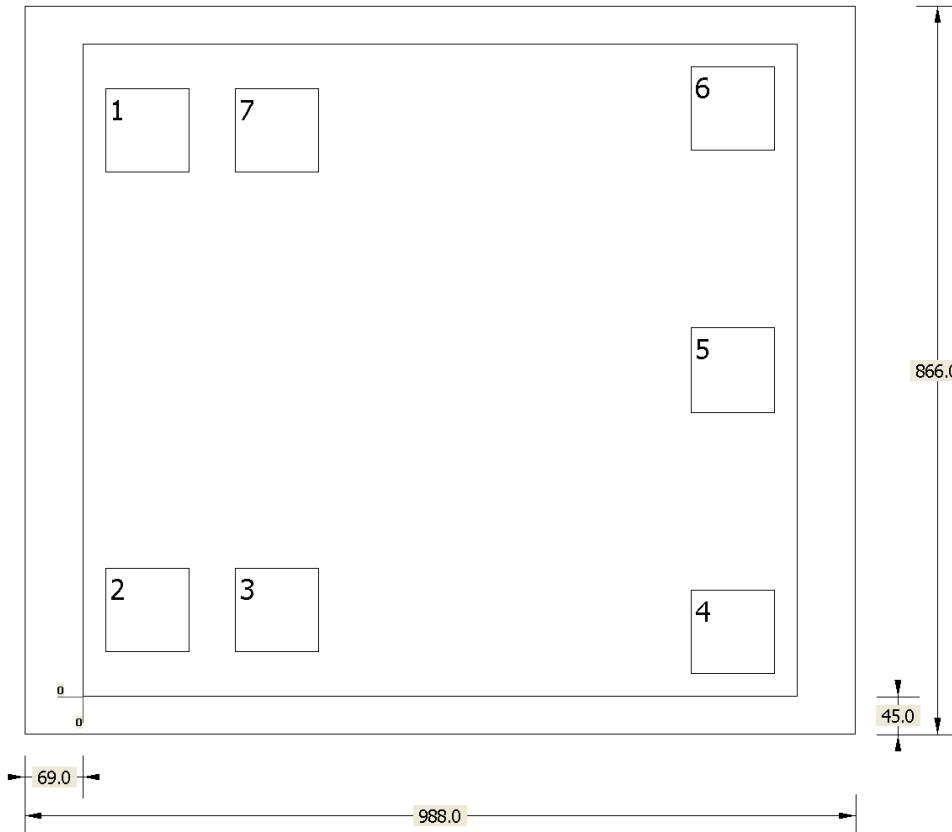


Table 1. Bond Pad Coordinates in Microns⁽¹⁾

DESCRIPTION	PAD NUMBER	X MIN	Y MIN	X MAX	Y MAX
Inverting Input	1	27	623	127	723
NonInverting Input	2	27	53	127	153
N/C	3	181	53	281	153
Output	4	723	27	823	127
V _{S-}	5	723	337	823	439
V _{S+}	6	723	649	823	749
N/C	7	181	623	281	723

(1) Substrate is V_{S-}.

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
OPA656TDB1	ACTIVE			0	400	TBD	Call TI	N / A for Pkg Type	
OPA656TDB2	ACTIVE			0	10	TBD	Call TI	N / A for Pkg Type	

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

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⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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