



THE DATASHEET OF PH9030L,115



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Kind regards,

Team Nexperia

1. Product profile

1.1 General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product is designed and qualified for use in computing, communications, consumer and industrial applications only.

1.2 Features and benefits

- High efficiency due to low switching and conduction losses
- Suitable for logic level gate drive sources

1.3 Applications

- DC-to-DC convertors
- Notebook computers
- Portable equipment
- Switched-mode power supplies

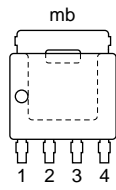
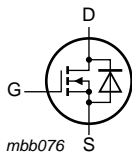
1.4 Quick reference data

Table 1. Quick reference

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 150\text{ °C}$	-	-	30	V
I_D	drain current	$T_{mb} = 25\text{ °C}$; $V_{GS} = 10\text{ V}$; see Figure 1 ; see Figure 3	-	-	63	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; see Figure 2	-	-	62.5	W
Dynamic characteristics						
Q_{GD}	gate-drain charge	$V_{GS} = 4.5\text{ V}$; $I_D = 10\text{ A}$; $V_{DS} = 12\text{ V}$; see Figure 10 ; see Figure 11	-	3.2	-	nC
Static characteristics						
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10\text{ V}$; $I_D = 25\text{ A}$; $T_j = 25\text{ °C}$; see Figure 8 ; see Figure 9	-	7	9	mΩ

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1,2,3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

**SOT669
(LFAK)**

3. Ordering information

Table 3. Ordering information

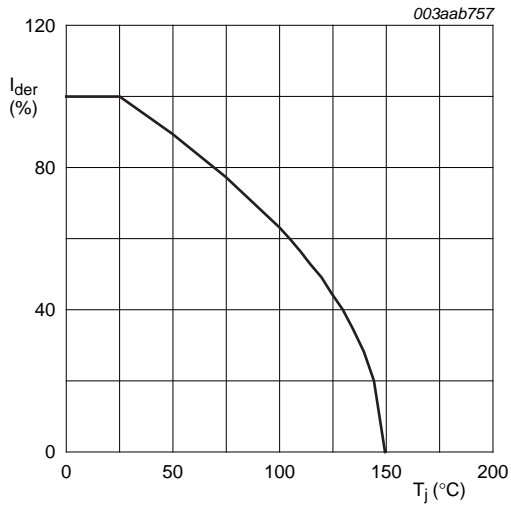
Type number	Package		Description	Version
	Name			
PH9030L	LFAK		Plastic single-ended surface-mounted package (LFAK); 4 leads	SOT669

4. Limiting values

Table 4. Limiting values

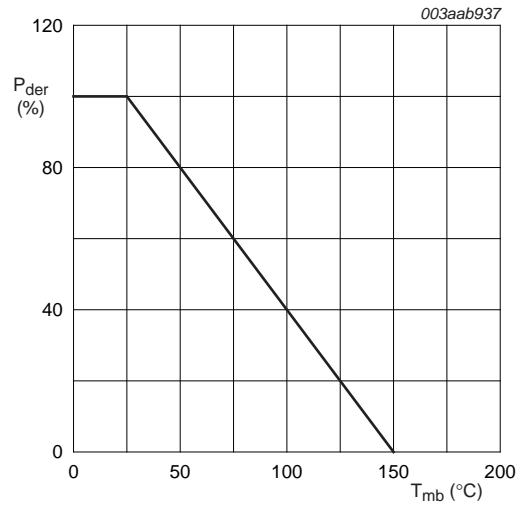
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 150\text{ °C}$	-	30	V
V_{DGR}	drain-gate voltage	$25\text{ °C} \leq T_j \leq 150\text{ °C}$; $R_{GS} = 20\text{ k}\Omega$	-	30	V
V_{GS}	gate-source voltage		-20	20	V
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_j = 100\text{ °C}$; see Figure 1	-	39	A
		$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; see Figure 1 ; see Figure 3	-	63	A
I_{DM}	peak drain current	$t_p \leq 10\text{ }\mu\text{s}$; pulsed; $T_{mb} = 25\text{ °C}$; see Figure 3	-	214	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; see Figure 2	-	62.5	W
T_{stg}	storage temperature		-55	150	°C
T_j	junction temperature		-55	150	°C
Source-drain diode					
I_S	source current	$T_{mb} = 25\text{ °C}$	-	52	A
I_{SM}	peak source current	$t_p \leq 10\text{ }\mu\text{s}$; pulsed; $T_{mb} = 25\text{ °C}$	-	208	A
Avalanche Ruggedness					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10\text{ V}$; $T_{j(\text{init})} = 25\text{ °C}$; $I_D = 33\text{ A}$; $V_{sup} \leq 30\text{ V}$; unclamped; $t_p = 0.08\text{ ms}$; $R_{GS} = 50\text{ }\Omega$	-	53	mJ



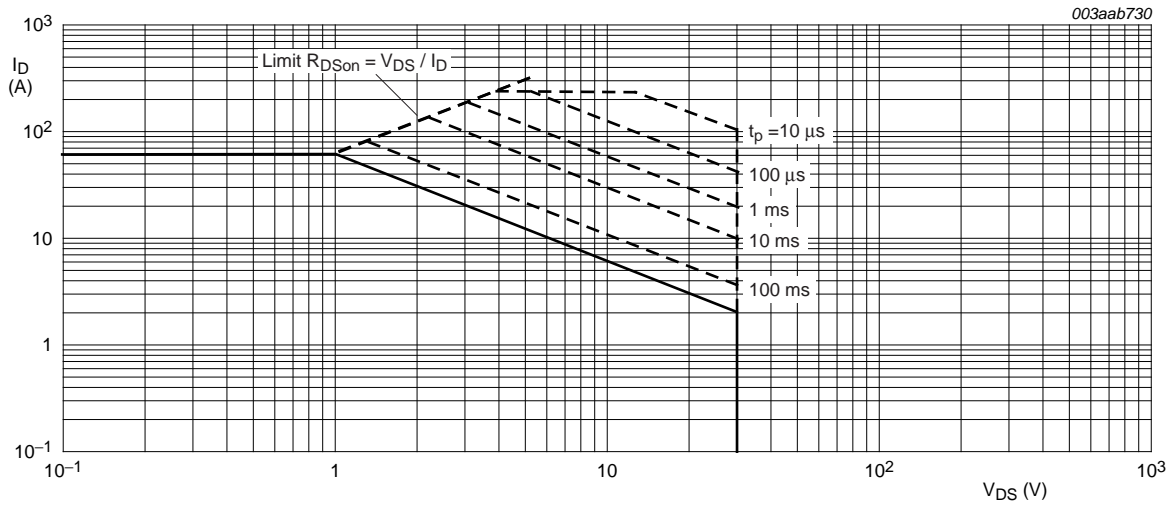
$$I_{der} = \frac{I_D}{I_{D(25^\circ\text{C})}} \times 100\%$$

Fig 1. Normalized continuous drain current as a function of solder point temperature



$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ\text{C})}} \times 100\%$$

Fig 2. Normalized total power dissipation as a function of solder point temperature



$T_{mb} = 25^\circ\text{C}; I_{DM}$ is single pulse

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 4	-	-	2	K/W



Fig 4. Transient thermal impedance from junction to solder point as a function of pulse duration

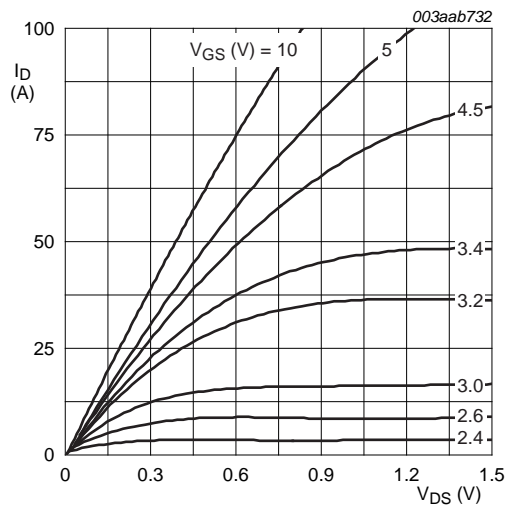
6. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A$; $V_{GS} = 0 V$; $T_j = 25 \text{ }^\circ C$	30	-	-	V
		$I_D = 250 \mu A$; $V_{GS} = 0 V$; $T_j = -55 \text{ }^\circ C$	27	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}$; $V_{DS} = V_{GS}$; $T_j = 25 \text{ }^\circ C$; see Figure 6 ; see Figure 7	1.3	1.7	2	V
V_{GSth}	gate-source threshold voltage	$I_D = 1 \text{ mA}$; $V_{DS} = V_{GS}$; $T_j = -55 \text{ }^\circ C$; see Figure 7 ; see Figure 6	-	-	2.6	V
		$I_D = 1 \text{ mA}$; $V_{DS} = V_{GS}$; $T_j = 150 \text{ }^\circ C$; see Figure 7 ; see Figure 6	0.8	-	-	V
I_{DSS}	drain leakage current	$V_{DS} = 30 V$; $V_{GS} = 0 V$; $T_j = 25 \text{ }^\circ C$	-	-	1	μA
I_{GSS}	gate leakage current	$V_{GS} = 16 V$; $V_{DS} = 0 V$; $T_j = 25 \text{ }^\circ C$	-	-	100	nA
		$V_{GS} = -16 V$; $V_{DS} = 0 V$; $T_j = 25 \text{ }^\circ C$	-	-	100	nA
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10 V$; $I_D = 25 A$; $T_j = 150 \text{ }^\circ C$; see Figure 8 ; see Figure 9	-	11.9	15.8	m Ω
		$V_{GS} = 4.5 V$; $I_D = 25 A$; $T_j = 25 \text{ }^\circ C$; see Figure 8 ; see Figure 9	-	10	12.5	m Ω
		$V_{GS} = 10 V$; $I_D = 25 A$; $T_j = 25 \text{ }^\circ C$; see Figure 8 ; see Figure 9	-	7	9	m Ω
I_{DSS}	drain leakage current	$V_{DS} = 30 V$; $V_{GS} = 0 V$; $T_j = 150 \text{ }^\circ C$	-	-	100	μA
R_G	internal gate resistance (AC)	$f = 1 \text{ MHz}$	-	0.56	-	Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 10 A$; $V_{DS} = 12 V$; $V_{GS} = 4.5 V$; see Figure 10 ; see Figure 11	-	13.3	-	nC
Q_{GS}	gate-source charge		-	4.8	-	nC
Q_{GD}	gate-drain charge		-	3.2	-	nC
$Q_{GS(th)}$	pre-threshold gate-source charge		-	1.8	-	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge		-	3	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = 10 A$; $V_{DS} = 12 V$; see Figure 10 ; see Figure 11	-	2.72	-	V
C_{iss}	input capacitance	$V_{DS} = 12 V$; $V_{GS} = 0 V$; $f = 1 \text{ MHz}$; $T_j = 25 \text{ }^\circ C$; see Figure 12	-	1565	-	pF
		$V_{DS} = 0 V$; $V_{GS} = 0 V$; $f = 1 \text{ MHz}$; $T_j = 25 \text{ }^\circ C$	-	1839	-	pF
C_{oss}	output capacitance	$V_{DS} = 12 V$; $V_{GS} = 0 V$; $f = 1 \text{ MHz}$; $T_j = 25 \text{ }^\circ C$; see Figure 12	-	355	-	pF
C_{rss}	reverse transfer capacitance		-	186	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 12 V$; $R_L = 0.5 \Omega$; $V_{GS} = 4.5 V$; $R_{G(ext)} = 5.6 \Omega$	-	20	-	ns
t_r	rise time		-	41	-	ns
$t_{d(off)}$	turn-off delay time		-	15	-	ns

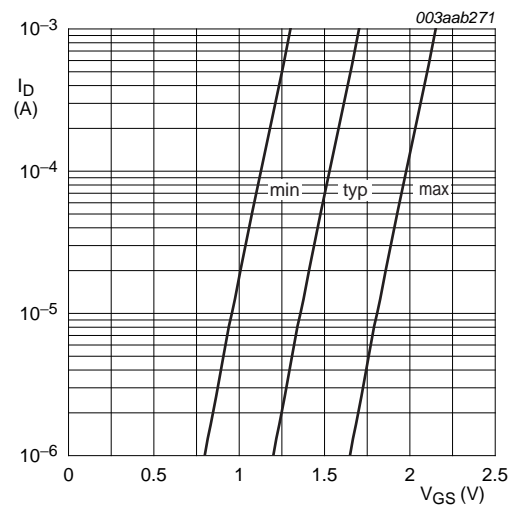
Table 6. Characteristics ...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_f	fall time	$V_{DS} = 12\text{ V}$; $R_L = 0.5\ \Omega$; $R_L = 0.5\ \Omega$; $V_{GS} = 4.5\text{ V}$; $R_{G(ext)} = 5.6\ \Omega$	-	25	-	ns
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 25\text{ A}$; $V_{GS} = 0\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$; see Figure 14	-	0.89	1.16	V
t_{rr}	reverse recovery time	$I_S = 20\text{ A}$; $di_S/dt = -100\text{ A/s}$; $V_{GS} = 0\text{ V}$;	-	43	-	ns
Q_r	recovered charge	$V_{DS} = 30\text{ V}$	-	15	-	nC



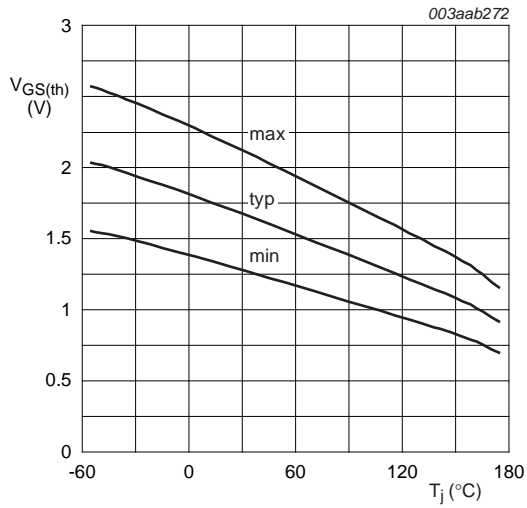
$T_j = 25\text{ }^\circ\text{C}$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values



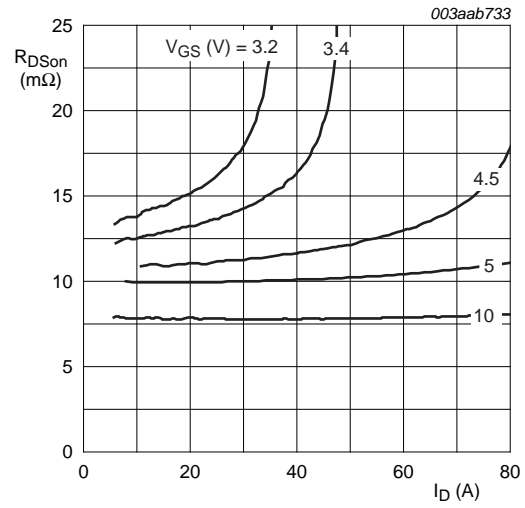
$T_j = 25\text{ }^\circ\text{C}$; $V_{DS} = 5\text{ V}$

Fig 6. Sub-threshold drain current as a function of gate-source voltage



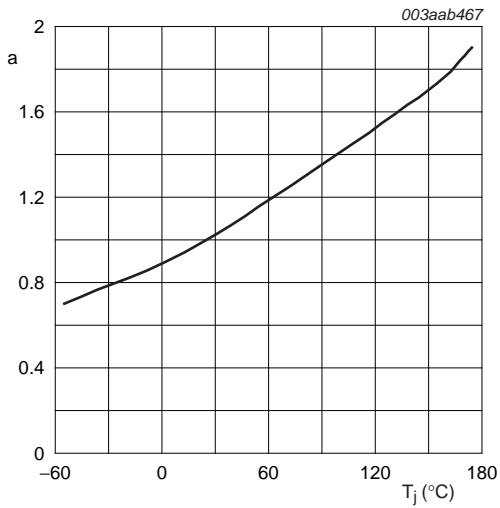
$$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$$

Fig 7. Gate-source threshold voltage as a function of junction temperature



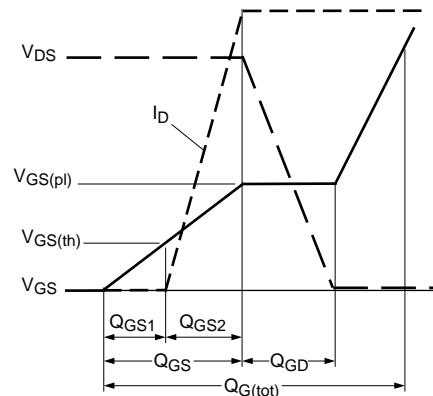
$$T_j = 25 \text{ °C}$$

Fig 8. Drain-source on-state resistance as a function of drain current; typical values



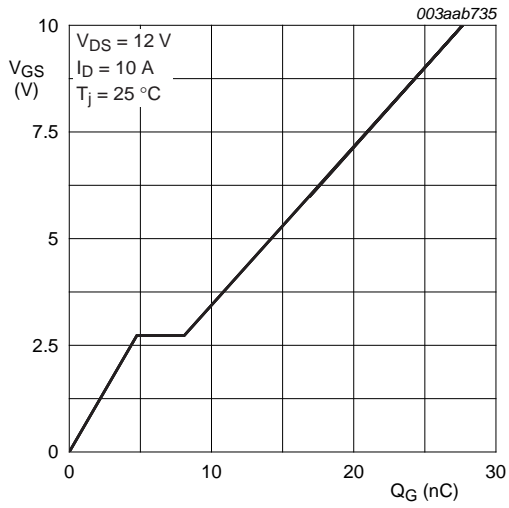
$$a = \frac{R_{DSon}}{R_{DSon(25\text{°C})}}$$

Fig 9. Normalized drain-source on-state resistance factor as a function of junction temperature



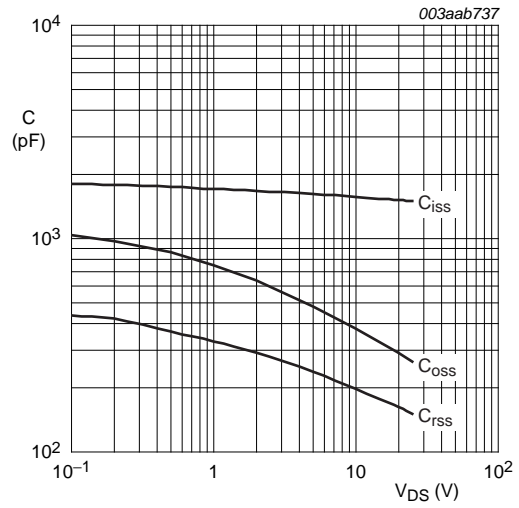
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Fig 10. Gate charge waveform definitions



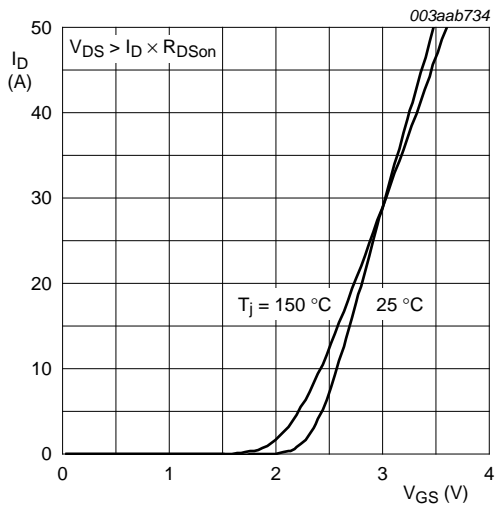
$I_D = 10\text{ A}; V_{DS} = 12\text{ V}$

Fig 11. Gate-source voltage as a function of gate charge; typical values



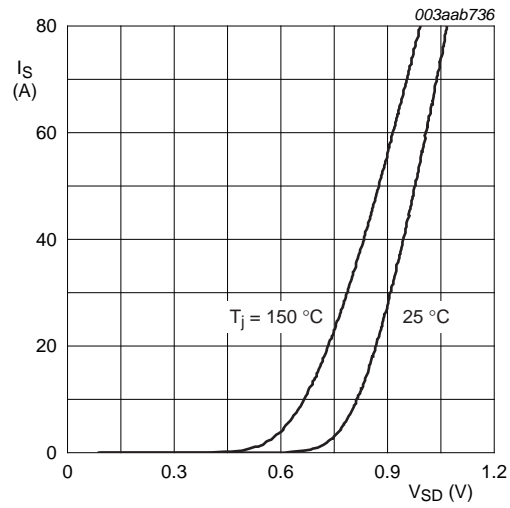
$V_{GS} = 0\text{ V}; f = 1\text{ MHz}$

Fig 12. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$T_j = 25\text{ °C and } 150\text{ °C}; V_{DS} > I_D \times R_{DSon}$

Fig 13. Transfer characteristics: drain current as a function of gate-source voltage; typical values



$T_j = 25\text{ °C and } 150\text{ °C}; V_{GS} = 0\text{ V}$

Fig 14. Source current as a function of source-drain voltage; typical values

7. Package outline

Plastic single-ended surface-mounted package (LFAK); 4 leads

SOT669

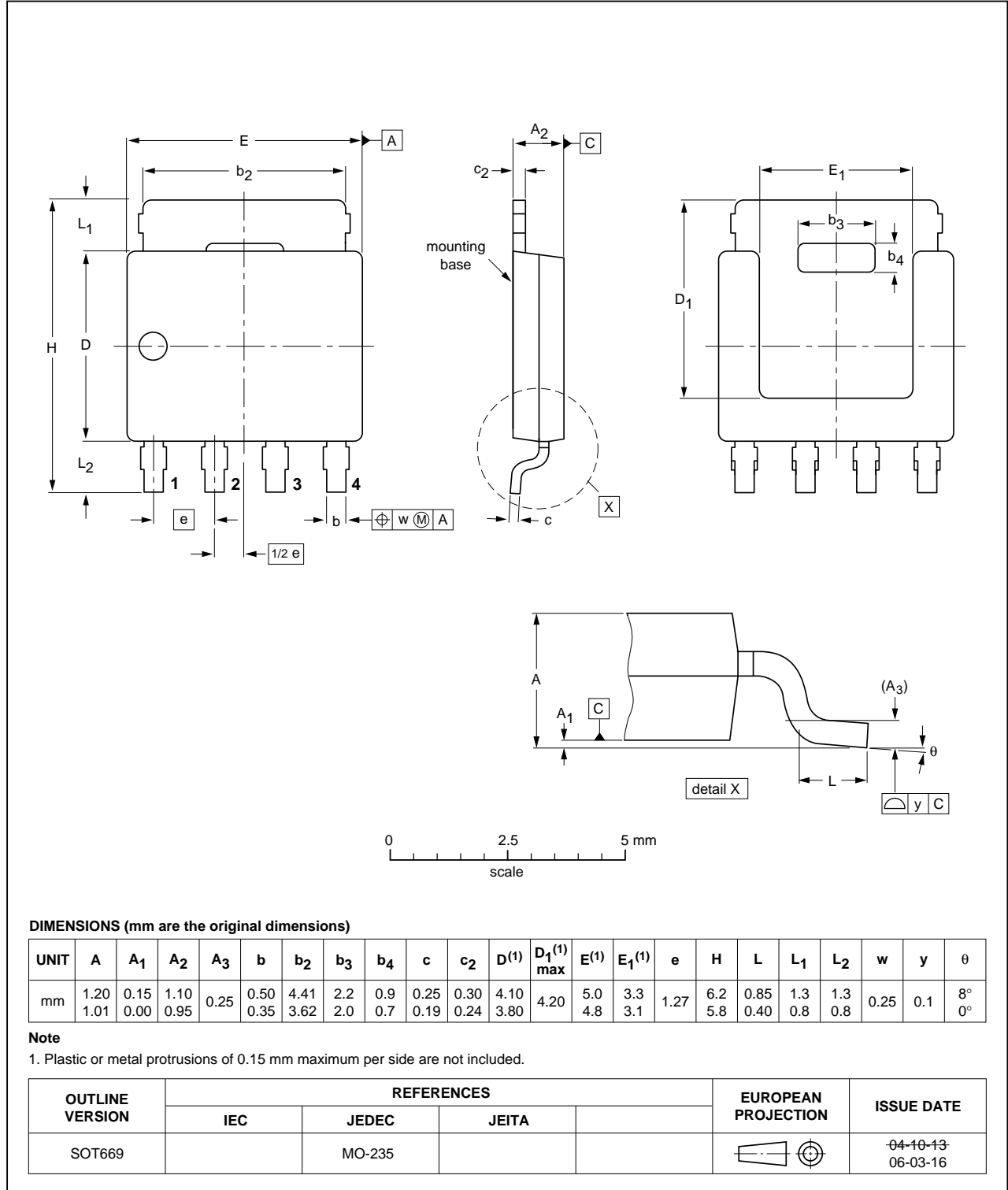


Fig 15. Package outline SOT669 (LFAK)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PH9030L_1	20080729	Product data sheet	-	-

9. Legal information

9.1 Data sheet status

Document status [1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

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