

# PHB/PHD66NQ03LT

N-channel TrenchMOS™ logic level FET

Rev. 06 — 2 August 2004

Product data sheet

## 1. Product profile

### 1.1 General description

Logic level N-channel enhancement mode field effect transistor in a plastic package using TrenchMOS™ technology.

### 1.2 Features

- Logic level threshold
- Low on-state resistance.

### 1.3 Applications

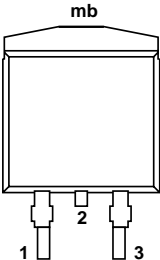
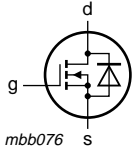
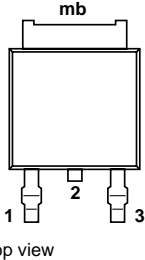
- DC-to-DC converters
- General purpose switching.

### 1.4 Quick reference data

- $V_{DS} \leq 25$  V
- $I_D \leq 66$  A
- $R_{DS(on)} \leq 10.5$  m $\Omega$
- $Q_{gd} = 3.6$  nC (typ).

## 2. Pinning information

Table 1: Discrete pinning

Pin	Description	Simplified outline	Symbol
1	gate (g)		
2	drain (d) <sup>[1]</sup>		
3	source (s)		
mb	mounting base; connected to drain (d)		
			
		Top view	
		SOT404 (D <sup>2</sup> -PAK)	SOT428 (D-PAK)

[1] It is not possible to make a connection to pin 2 of the SOT404 and SOT428 packages.

### 3. Ordering information

**Table 2: Ordering information**

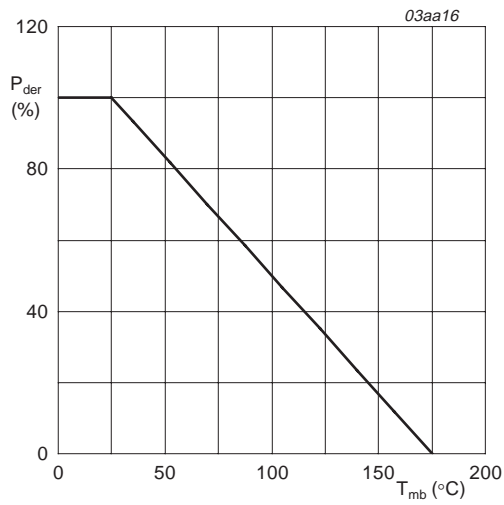
Type number	Package		Version
	Name	Description	
PHB66NQ03LT	D <sup>2</sup> -PAK	Plastic single-ended surface mounted package (Philips version of D <sup>2</sup> -PAK); 3 leads (one lead cropped)	SOT404
PHD66NQ03LT	D-PAK	Plastic single-ended surface mounted package (Philips version of D-PAK); 3 leads (one lead cropped)	SOT428

### 4. Limiting values

**Table 3: Limiting values**

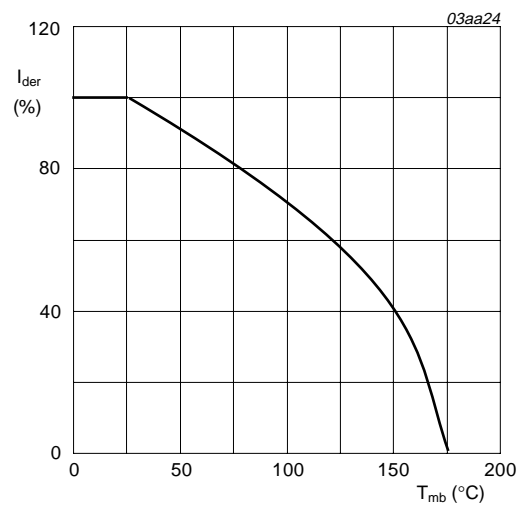
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>DS</sub>	drain-source voltage (DC)	25 °C ≤ T <sub>j</sub> ≤ 175 °C	-	25	V
V <sub>DGR</sub>	drain-gate voltage (DC)	25 °C ≤ T <sub>j</sub> ≤ 175 °C; R <sub>GS</sub> = 20 kΩ	-	25	V
V <sub>GS</sub>	gate-source voltage (DC)		-	±20	V
I <sub>D</sub>	drain current (DC)	T <sub>mb</sub> = 25 °C; V <sub>GS</sub> = 5 V; <a href="#">Figure 2</a> and <a href="#">3</a>	-	57	A
		T <sub>mb</sub> = 100 °C; V <sub>GS</sub> = 5 V; <a href="#">Figure 2</a>	-	40	A
		T <sub>mb</sub> = 25 °C; V <sub>GS</sub> = 10 V	-	66	A
		T <sub>mb</sub> = 100 °C; V <sub>GS</sub> = 10 V	-	45	A
I <sub>DM</sub>	peak drain current	T <sub>mb</sub> = 25 °C; pulsed; t <sub>p</sub> ≤ 10 μs; <a href="#">Figure 3</a>	-	228	A
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; <a href="#">Figure 1</a>	-	93	W
T <sub>stg</sub>	storage temperature		-55	+175	°C
T <sub>j</sub>	junction temperature		-55	+175	°C
<b>Source-drain diode</b>					
I <sub>S</sub>	source (diode forward) current (DC)	T <sub>mb</sub> = 25 °C	-	57	A
I <sub>SM</sub>	peak source (diode forward) current	T <sub>mb</sub> = 25 °C; pulsed; t <sub>p</sub> ≤ 10 μs	-	228	A
<b>Avalanche ruggedness</b>					
E <sub>DS(AL)S</sub>	non-repetitive drain-source avalanche energy	unclamped inductive load; I <sub>D</sub> = 43 A; t <sub>p</sub> = 0.15 ms; V <sub>DD</sub> ≤ 25 V; R <sub>GS</sub> = 50 Ω; V <sub>GS</sub> = 10 V; starting at T <sub>j</sub> = 25 °C	-	90	mJ



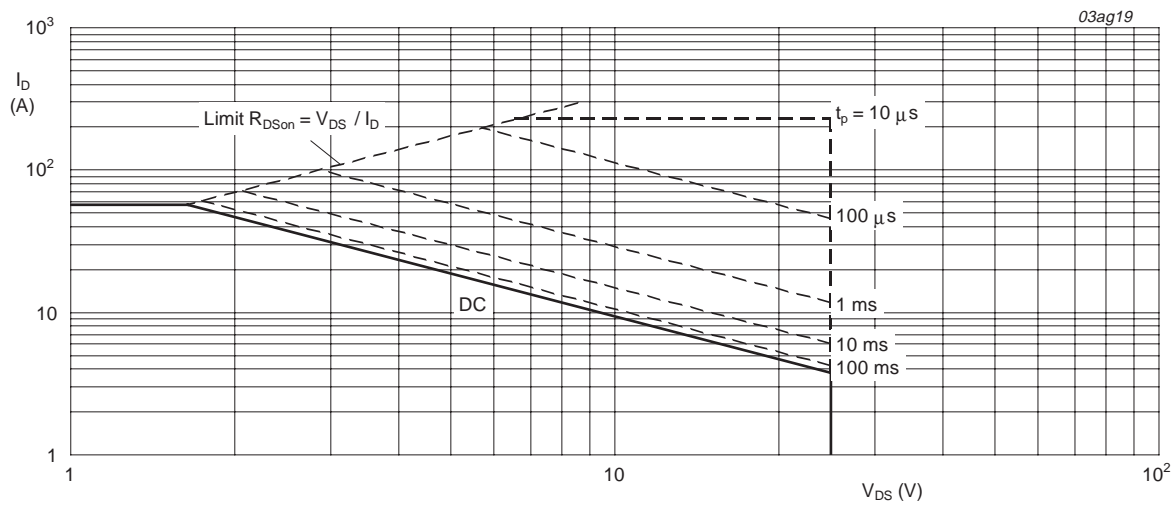
$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

Fig 1. Normalized total power dissipation as a function of mounting base temperature.



$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of mounting base temperature.



$T_{mb} = 25^{\circ}C$ ;  $I_{DM}$  is single pulse;  $V_{GS} = 5 V$

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.

## 5. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	<a href="#">Figure 4</a>	-	-	1.6	K/W	
$R_{th(j-a)}$	thermal resistance from junction to ambient	SOT404	mounted on a printed-circuit board; minimum footprint; vertical in still air	-	50	-	K/W
		SOT428	mounted on a printed-circuit board; minimum footprint; vertical in still air	-	75	-	K/W
			mounted on a printed-circuit board; SOT404 minimum footprint; vertical in still air	-	50	-	K/W

### 5.1 Transient thermal impedance

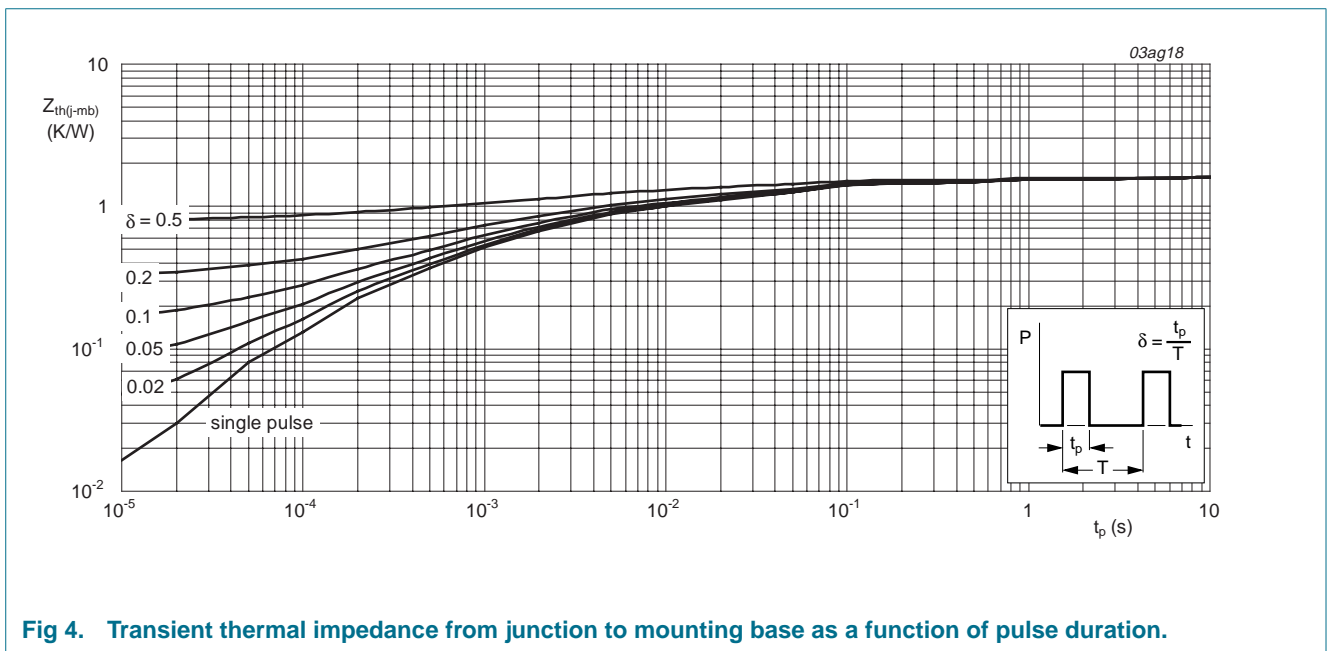
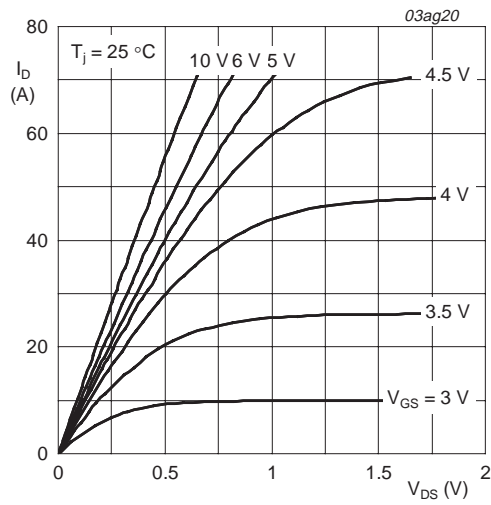


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration.

## 6. Characteristics

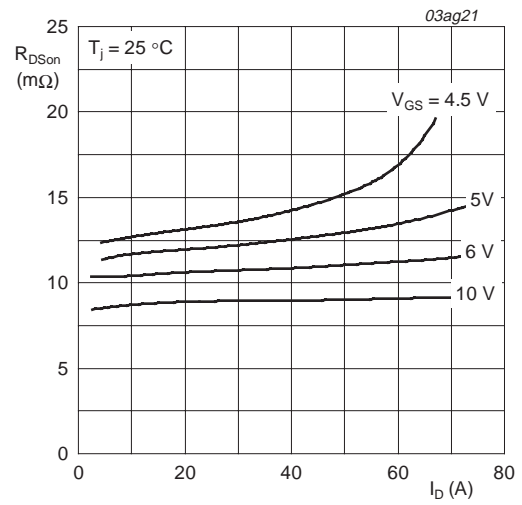
**Table 5: Characteristics**
*T<sub>j</sub> = 25 °C unless otherwise specified.*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
V <sub>(BR)DSS</sub>	drain-source breakdown voltage	I <sub>D</sub> = 250 μA; V <sub>GS</sub> = 0 V T <sub>j</sub> = 25 °C T <sub>j</sub> = -55 °C	25 22	- -	- -	V V
V <sub>GS(th)</sub>	gate-source threshold voltage	I <sub>D</sub> = 1 mA; V <sub>DS</sub> = V <sub>GS</sub> ; <a href="#">Figure 9</a> and <a href="#">10</a> T <sub>j</sub> = 25 °C T <sub>j</sub> = 175 °C T <sub>j</sub> = -55 °C	1 0.5 -	1.5 - -	2 - 2.2	V V V
I <sub>DSS</sub>	drain-source leakage current	V <sub>DS</sub> = 25 V; V <sub>GS</sub> = 0 V T <sub>j</sub> = 25 °C T <sub>j</sub> = 175 °C	- - -	- - -	10 500	μA μA
I <sub>GSS</sub>	gate-source leakage current	V <sub>GS</sub> = ±15 V; V <sub>DS</sub> = 0 V	-	10	100	nA
R <sub>DS(on)</sub>	drain-source on-state resistance	V <sub>GS</sub> = 10 V; I <sub>D</sub> = 25 A; <a href="#">Figure 6</a> and <a href="#">8</a> T <sub>j</sub> = 25 °C T <sub>j</sub> = 175 °C V <sub>GS</sub> = 5 V; I <sub>D</sub> = 25 A; <a href="#">Figure 6</a> and <a href="#">8</a>	- - -	9.1 16.4 11.2	10.5 18.9 13.6	mΩ mΩ mΩ
<b>Dynamic characteristics</b>						
Q <sub>g(tot)</sub>	total gate charge	I <sub>D</sub> = 50 A; V <sub>DS</sub> = 15 V; V <sub>GS</sub> = 5 V; <a href="#">Figure 11</a>	-	12	-	nC
Q <sub>gs</sub>	gate-source charge		-	4.5	-	nC
Q <sub>gd</sub>	gate-drain (Miller) charge		-	3.6	-	nC
C <sub>iss</sub>	input capacitance	V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 25 V; f = 1 MHz; <a href="#">Figure 13</a>	-	860	-	pF
C <sub>oss</sub>	output capacitance		-	330	-	pF
C <sub>rss</sub>	reverse transfer capacitance		-	145	-	pF
t <sub>d(on)</sub>	turn-on delay time	V <sub>DS</sub> = 15 V; R <sub>L</sub> = 0.6 Ω; V <sub>GS</sub> = 5 V; R <sub>G</sub> = 5.6 Ω	-	15	25	ns
t <sub>r</sub>	rise time		-	90	135	ns
t <sub>d(off)</sub>	turn-off delay time		-	25	40	ns
t <sub>f</sub>	fall time		-	25	40	ns
<b>Source-drain diode</b>						
V <sub>SD</sub>	source-drain (diode forward) voltage	I <sub>S</sub> = 25 A; V <sub>GS</sub> = 0 V; <a href="#">Figure 12</a>	-	0.95	1.2	V
t <sub>rr</sub>	reverse recovery time	I <sub>S</sub> = 10 A; dI <sub>S</sub> /dt = -100 A/μs;	-	32	-	ns
Q <sub>r</sub>	recovered charge	V <sub>GS</sub> = 0 V; V <sub>R</sub> = 25 V	-	20	-	nC



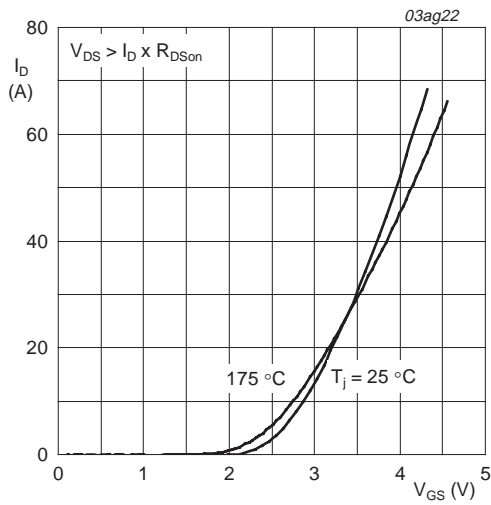
$T_j = 25\text{ }^\circ\text{C}$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.



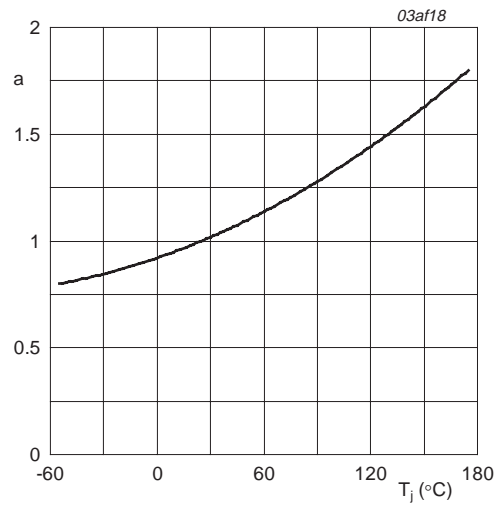
$T_j = 25\text{ }^\circ\text{C}$

Fig 6. Drain-source on-state resistance as a function of drain current; typical values.



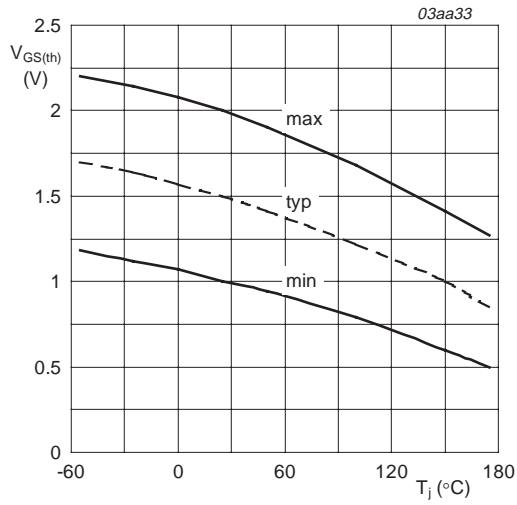
$T_j = 25\text{ }^\circ\text{C}$  and  $175\text{ }^\circ\text{C}$ ;  $V_{DS} > I_D \times R_{DS(on)}$

Fig 7. Transfer characteristics: drain current as a function of gate-source voltage; typical values.



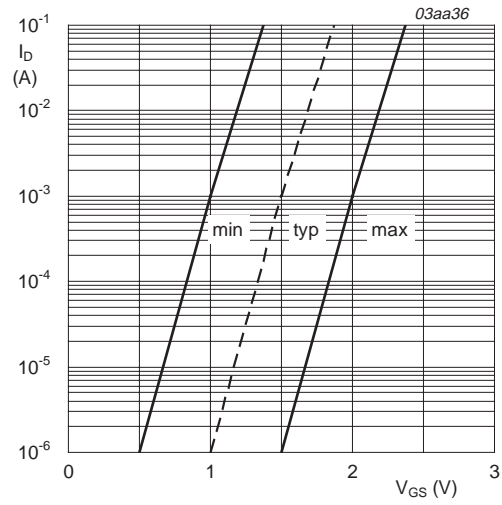
$$a = \frac{R_{DS(on)}}{R_{DS(on)(25^\circ\text{C})}}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature.



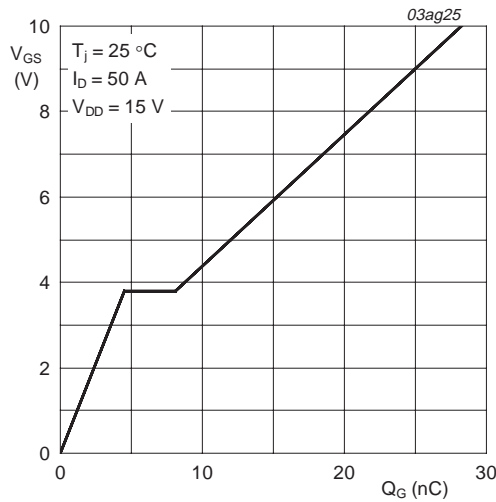
$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature.



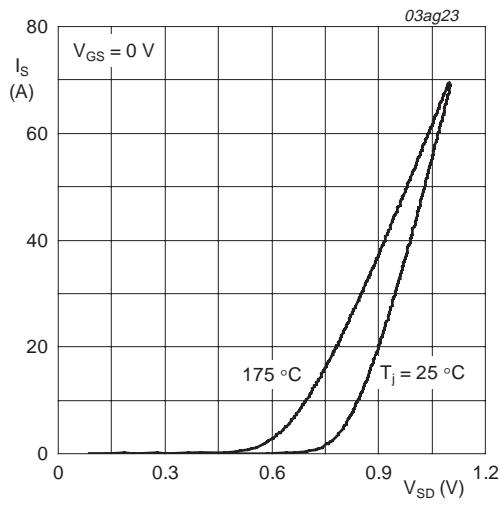
$T_j = 25 \text{ °C}; V_{DS} = 5 \text{ V}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage.



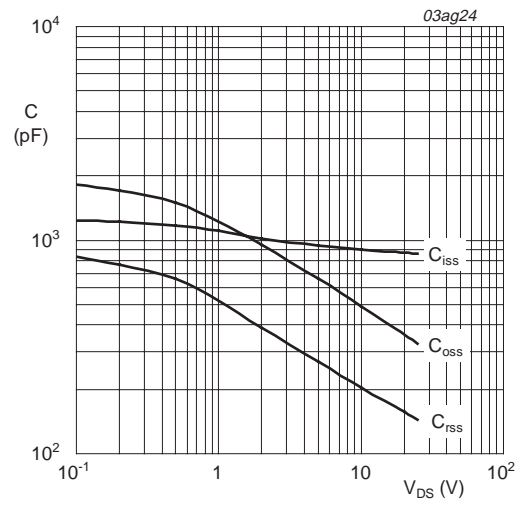
$I_D = 50 \text{ A}; V_{DS} = 15 \text{ V}$

Fig 11. Gate-source voltage as a function of gate charge; typical values.



$T_J = 25\text{ °C}$  and  $175\text{ °C}$ ;  $V_{GS} = 0\text{ V}$

**Fig 12. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values.**



$V_{GS} = 0\text{ V}$ ;  $f = 1\text{ MHz}$

**Fig 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.**

7. Package outline

Plastic single-ended surface mounted package (Philips version of D<sup>2</sup>-PAK); 3 leads (one lead cropped)

SOT404

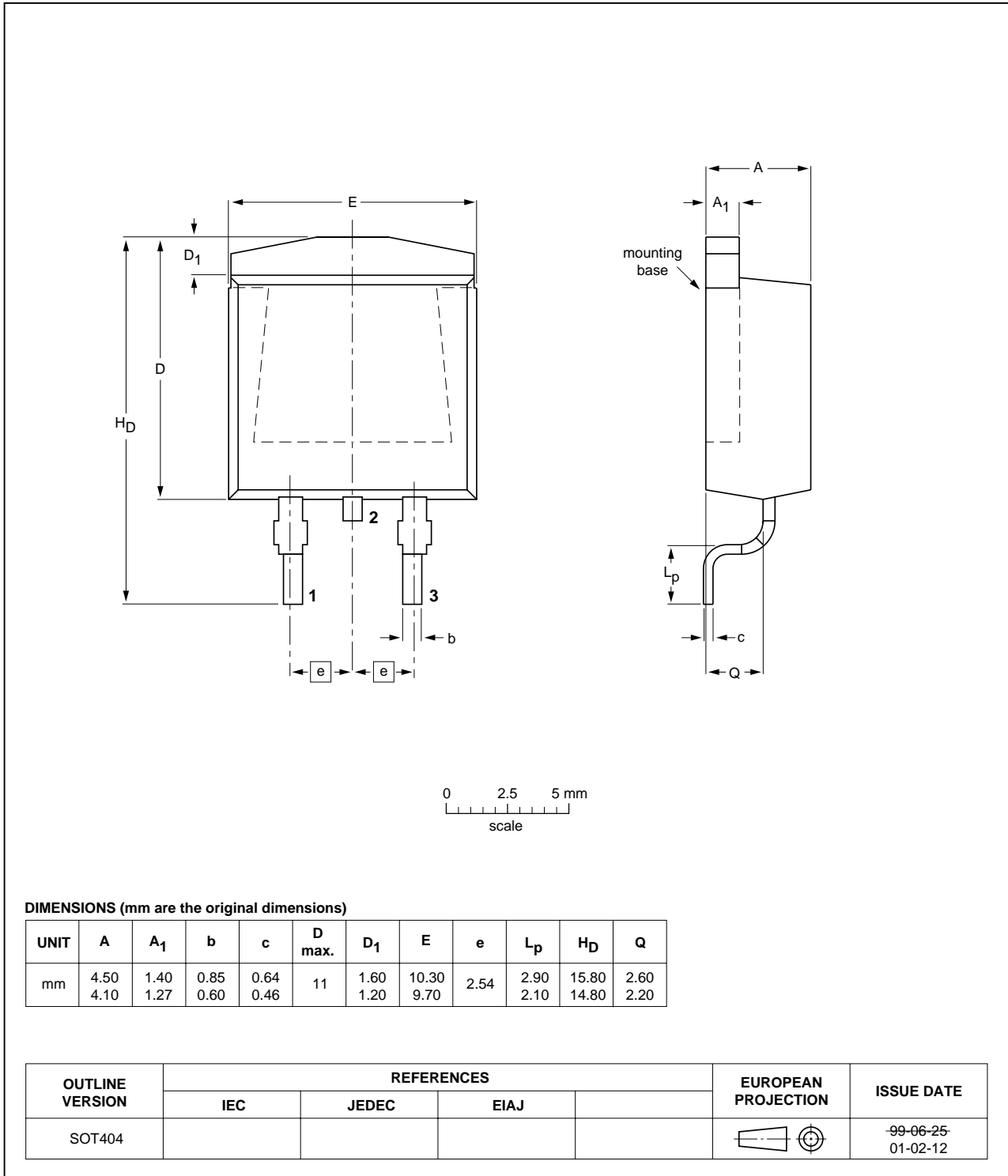


Fig 14. SOT404 (D<sup>2</sup>-PAK) package outline.

Plastic single-ended surface mounted package (Philips version of D-PAK); 3 leads (one lead cropped)

SOT428

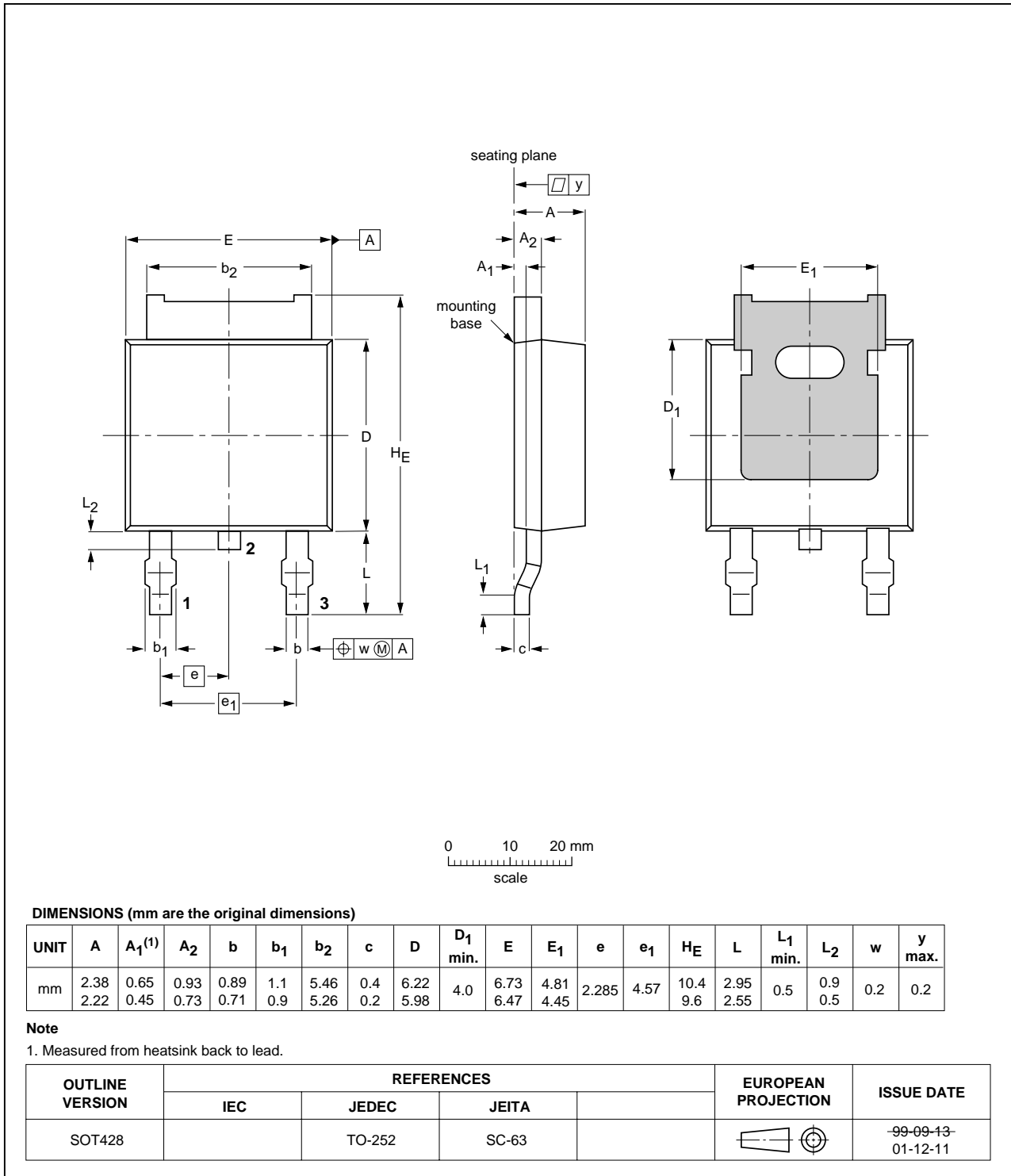


Fig 15. SOT428 (D-PAK) package outline.

## 8. Revision history

**Table 6: Revision history**

Document ID	Release date	Data sheet status	Change notice	Document number	Supersedes
PHB_PHD66NQ03LT_6	20040802	Product data sheet	-	9397 750 13429	PHP_PHB_PHD66NQ03LT_5
Modifications:		<ul style="list-style-type: none"> <li>• Removal of PHP66NQ03LT (now in separate data sheet)</li> <li>• Data sheet updated to latest standard.</li> </ul>			
PHP_PHB_PHD66NQ03LT_5	20040415	Product data sheet	-	9397 750 13107	PHP_PHB_PHD66NQ03LT_4
PHP_PHB_PHD66NQ03LT_4	20020909	Product data sheet	-	9397 750 10158	PHP_PHB_PHD66NQ03LT_3
PHP_PHB_PHD66NQ03LT_3	20020312	Product data sheet	-	9397 750 09284	PHP_PHB_PHD66NQ03LT_2
PHP_PHB_PHD66NQ03LT_2	20011210	Product data sheet	-	9397 750 09119	PHP_PHB_PHD66NQ03LT_1
PHP_PHB_PHD66NQ03LT_1	20011012	Product data sheet	-	9397 750 08725	-

## 9. Data sheet status

Level	Data sheet status <sup>[1]</sup>	Product status <sup>[2]</sup> <sup>[3]</sup>	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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