



**THE DATASHEET OF
PHK12NQ03LT,518**



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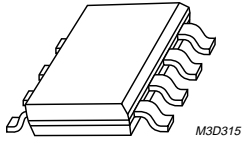
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Kind regards,

Team Nexperia



PHK12NQ03LT

N-channel TrenchMOS™ logic level FET

Rev. 02 — 02 March 2004

Product data

1. Product profile

1.1 Description

N-channel enhancement mode field-effect transistor in a plastic package using TrenchMOS™ technology.

1.2 Features

- Low on-state resistance
- Fast switching.

1.3 Applications

- DC-to-DC converters
- Portable equipment applications.

1.4 Quick reference data

- $V_{DS} \leq 30\text{ V}$
- $I_D \leq 11.8\text{ A}$
- $P_{tot} \leq 2.5\text{ W}$
- $R_{DS(on)} \leq 14\text{ m}\Omega$

2. Pinning information

Table 1: Pinning - SOT96-1 (SO8), simplified outline and symbol

Pin	Description	Simplified outline	Symbol
1,2,3	source (s)	<p>Top view MBK187</p> <p>SOT96-1 (SO8)</p>	<p>MBB076</p>
4	gate (g)		
5,6,7,8	drain (d)		

3. Ordering information

Table 2: Ordering information

Type number	Package		Version
	Name	Description	
PHK12NQ03LT	SO8	Plastic small outline package; 8 leads	SOT96



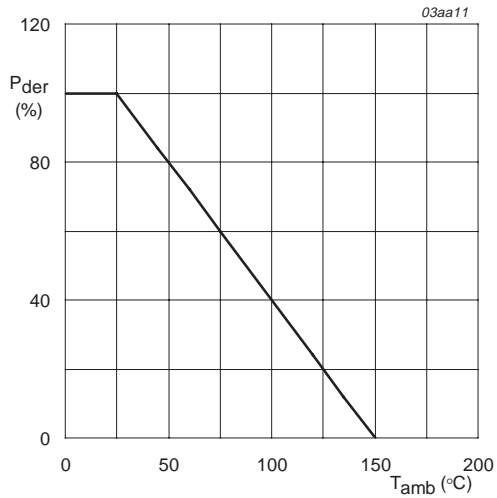
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4. Limiting values

Table 3: Limiting values

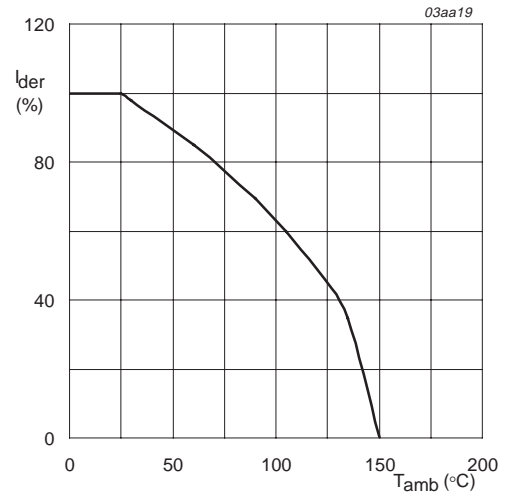
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage (DC)	$25\text{ °C} \leq T_j \leq 150\text{ °C}$	-	30	V
V_{GS}	gate-source voltage		-	± 20	V
I_D	drain current	$T_{amb} = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ s}$; Figure 2 and 3	-	11.8	A
I_{DM}	peak drain current	$T_{amb} = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$; Figure 3	-	35.3	A
P_{tot}	total power dissipation	$T_{amb} = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ s}$; Figure 1	-	2.5	W
T_{stg}	storage temperature		-55	+150	°C
T_j	junction temperature		-55	+150	°C
Source-drain diode					
I_S	source (diode forward) current	$T_{amb} = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ s}$	-	11.8	A
Avalanche ruggedness					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	unclamped inductive load; $I_D = 7.7\text{ A}$; $t_p = 2.35\text{ ms}$; $V_{DD} \leq 30\text{ V}$; $V_{GS} = 10\text{ V}$; starting $T_j = 25\text{ °C}$	-	440	mJ



$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

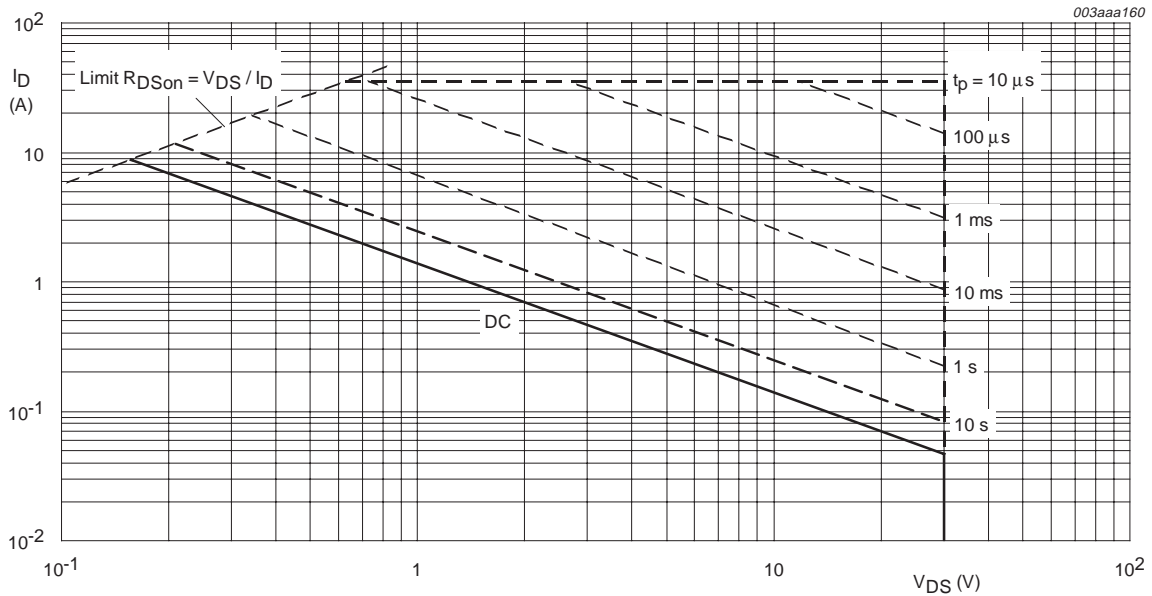
Fig 1. Normalized total power dissipation as a function of ambient temperature.



V_{GS} ≥ 5 V

$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of ambient temperature.



T_{amb} = 25 °C; I_{DM} is single pulse

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.

5. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	mounted on a printed-circuit board; minimum footprint; $t_p \leq 10$ s; Figure 4	-	-	50	K/W

5.1 Transient thermal impedance

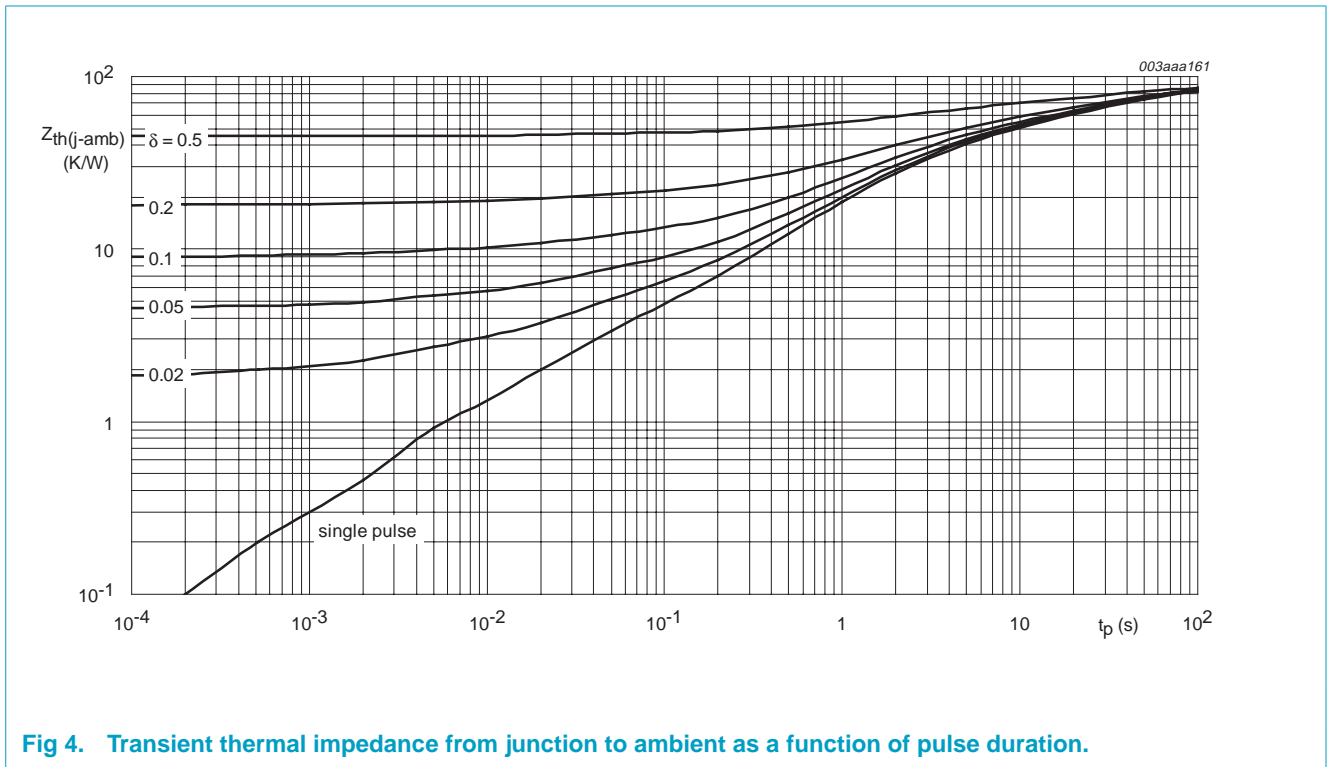


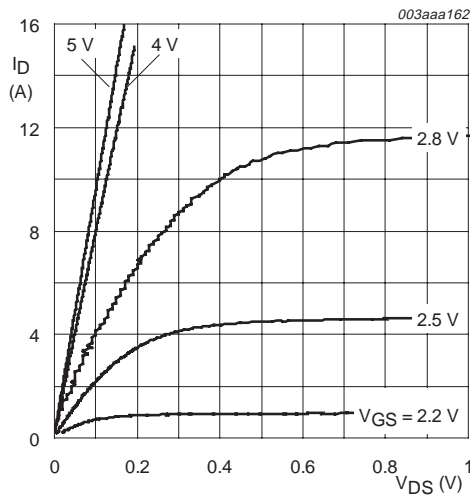
Fig 4. Transient thermal impedance from junction to ambient as a function of pulse duration.

6. Characteristics

Table 5: Characteristics

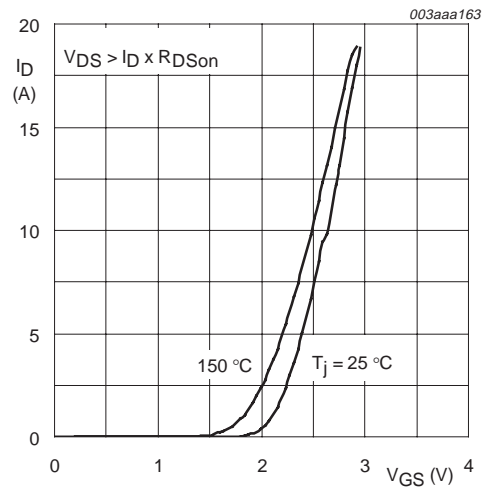
$T_j = 25\text{ °C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250\ \mu\text{A}; V_{GS} = 0\ \text{V}$	30	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 250\ \mu\text{A}; V_{DS} = V_{GS}; T_j = 25\text{ °C};$ Figure 9	1	-	2	V
I_{DSS}	drain-source leakage current	$V_{DS} = 24\ \text{V}; V_{GS} = 0\ \text{V}$				
		$T_j = 25\text{ °C}$	-	-	1	μA
		$T_j = 100\text{ °C}$	-	-	5	μA
I_{GSS}	gate-source leakage current	$V_{GS} = \pm 20\ \text{V}; V_{DS} = 0\ \text{V}$	-		100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 4.5\ \text{V}; I_D = 10\ \text{A};$ Figure 8	-	11	14	$\text{m}\Omega$
		$V_{GS} = 10\ \text{V}; I_D = 12\ \text{A};$ Figure 8	-	8.9	10.5	$\text{m}\Omega$
Dynamic characteristics						
g_{fs}	forward transconductance	$V_{DS} = 15\ \text{V}; I_D = 10\ \text{A};$	-	34	-	S
$Q_{g(tot)}$	total gate charge	$I_D = 15\ \text{A}; V_{DD} = 16\ \text{V}; V_{GS} = 5\ \text{V};$ Figure 13	-	17.6	-	nC
Q_{gs}	gate-source charge		-	4	-	nC
Q_{gd}	gate-drain (Miller) charge		-	4.4	-	nC
C_{iss}	input capacitance	$V_{GS} = 0\ \text{V}; V_{DS} = 16\ \text{V}; f = 1\ \text{MHz};$ Figure 11	-	1335	-	pF
C_{oss}	output capacitance		-	391	-	pF
C_{rss}	reverse transfer capacitance		-	190	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DD} = 16\ \text{V}; R_D = 10\ \Omega; V_{GS} = 10\ \text{V}$	-	10.6	-	ns
t_r	rise time		-	11.7	-	ns
$t_{d(off)}$	turn-off delay time		-	37	-	ns
t_f	fall time		-	19	-	ns
Source-drain (reverse) diode						
V_{SD}	source-drain (diode forward) voltage	$I_S = 1\ \text{A}; V_{GS} = 0\ \text{V};$ Figure 12	-	0.7	1.0	V
t_{rr}	reverse recovery time	$I_S = 2.3\ \text{A}; di_S/dt = -100\ \text{A}/\mu\text{s}; V_{GS} = 0\ \text{V}$	-	70	-	ns



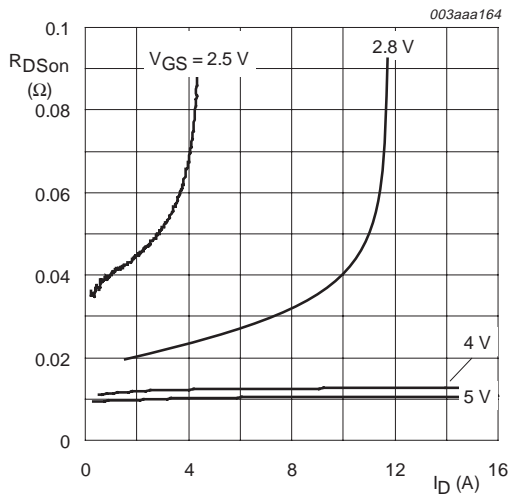
$T_j = 25^\circ\text{C}$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.



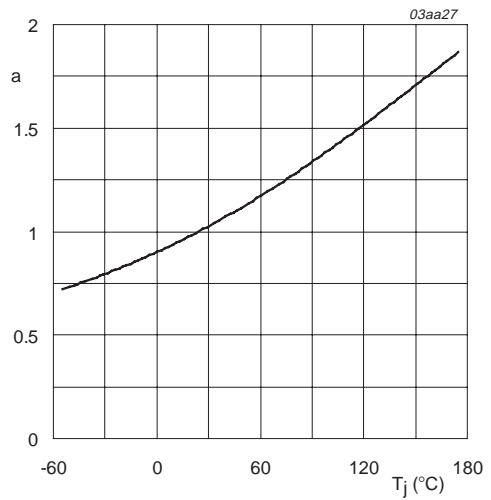
$T_j = 25^\circ\text{C}$ and 150°C ; $V_{DS} > I_D \times R_{DSon}$

Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values.



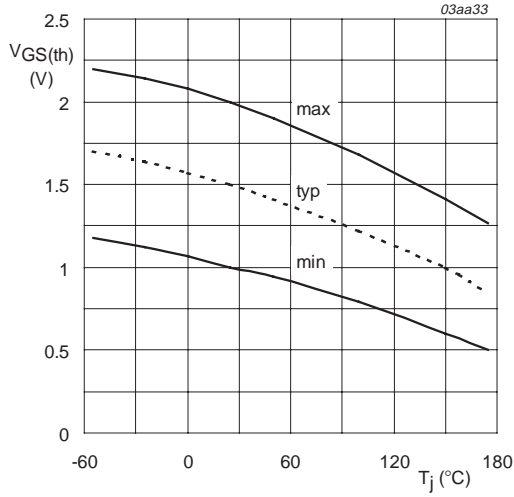
$T_j = 25^\circ\text{C}$

Fig 7. Drain-source on-state resistance as a function of drain current; typical values.



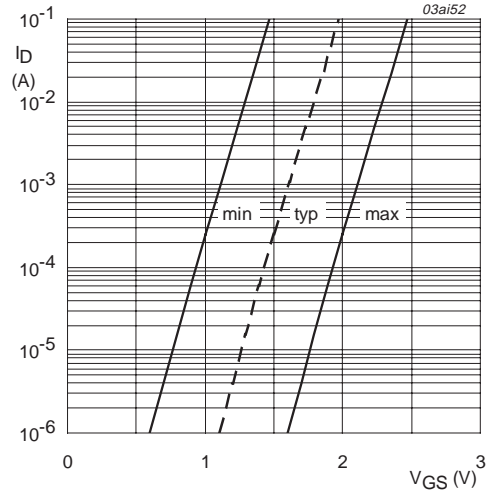
$$a = \frac{R_{DSon}}{R_{DSon(25^\circ\text{C})}}$$

Fig 8. Normalized drain source on-state resistance factor as a function of junction temperature.



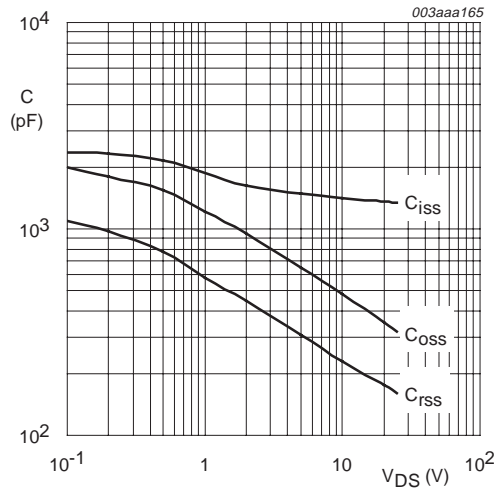
$I_D = 250 \mu A; V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature.



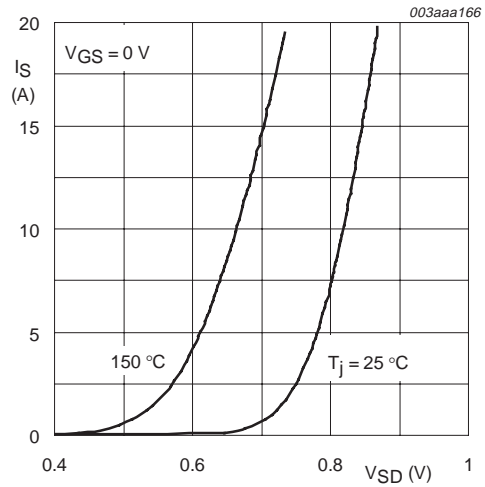
$T_j = 25 \text{ }^{\circ}C; V_{DS} = 5 \text{ V}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage.



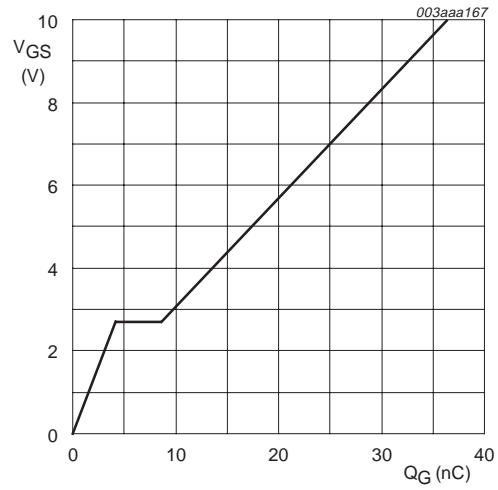
$V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$

Fig 11. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.



$T_j = 25 \text{ }^{\circ}C \text{ and } 150 \text{ }^{\circ}C; V_{GS} = 0 \text{ V}$

Fig 12. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values.



$I_D = 15\text{ A}; V_{DD} = 16\text{ V}$

Fig 13. Gate-source voltage as a function of gate charge; typical values.

7. Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm

SOT96-1

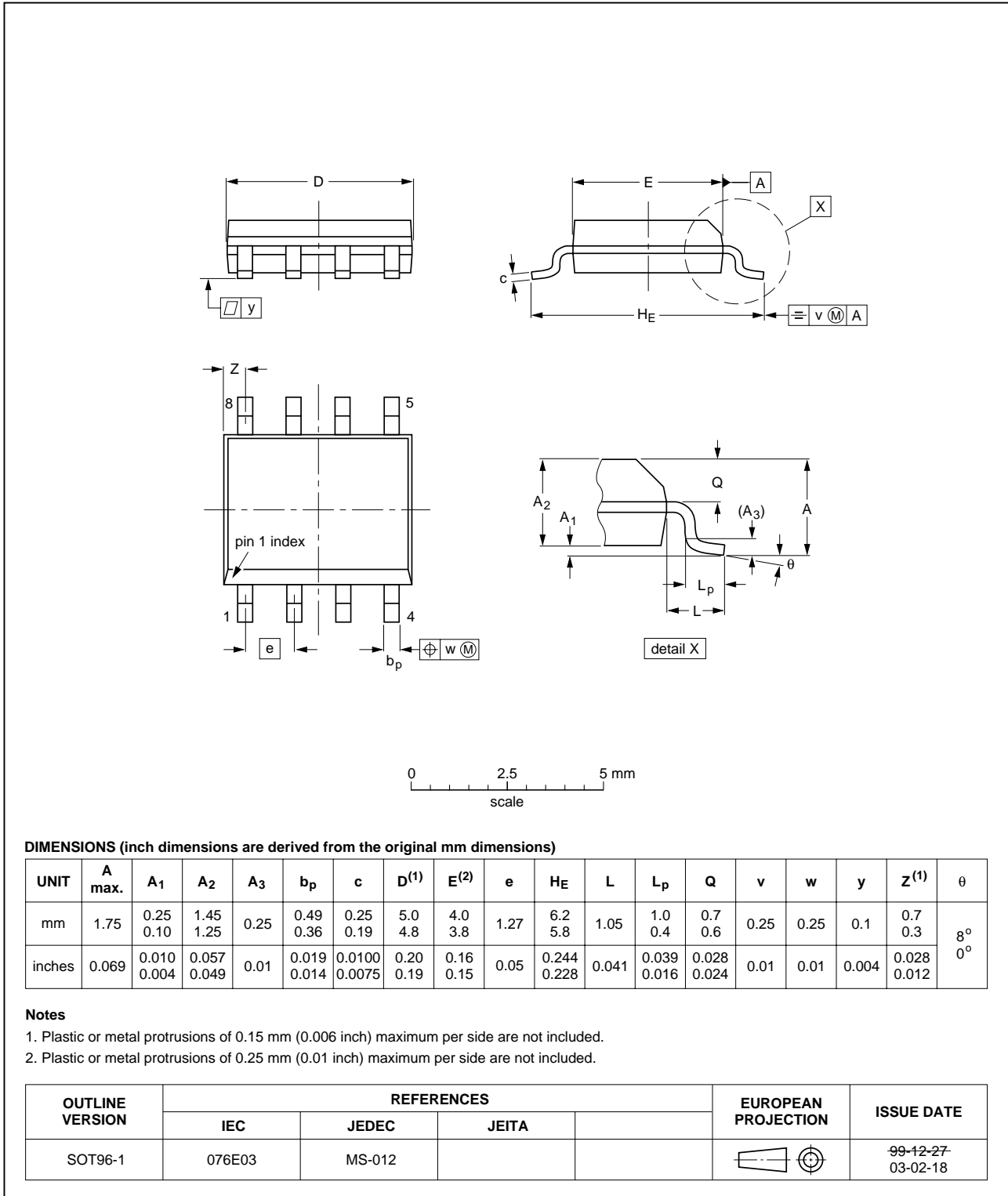


Fig 14. SOT96-1 (SO8).

8. Revision history

Table 6: Revision history

Rev	Date	CPCN	Description
02	20040302	-	Product data (9397 750 12955) Modifications <ul style="list-style-type: none">• Data sheet updated to latest presentation standards.• Section 1.4 “Quick reference data” correction to I_D value.• Section 4 “Limiting values” I_D, I_{DM}, P_{tot} and I_S conditions and values corrected.• Section 4 “Limiting values” Figure 1, 2 and 3 corrected.• Section 4 “Limiting values” $E_{DS(AL)S}$ added.• Section 5 “Thermal characteristics” typ and max values corrected.• Section 5 “Thermal characteristics” Figure 4 corrected.• Section 6 “Characteristics” Figure 13 corrected.
01	20020322	-	Product data (9397 750 09405)

9. Data sheet status

Level	Data sheet status ^[1]	Product status ^{[2][3]}	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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Contact information

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