



**THE DATASHEET OF  
SN74CBT3257PWG4**



# SN74CBT3257

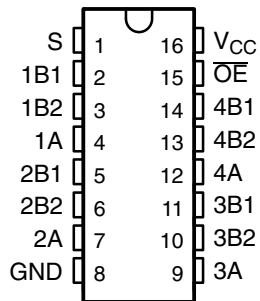
## 4-BIT 1-OF-2 FET MULTIPLEXER/DEMULTIPLEXER

SCDS017M – MAY 1995 – REVISED JANUARY 2004

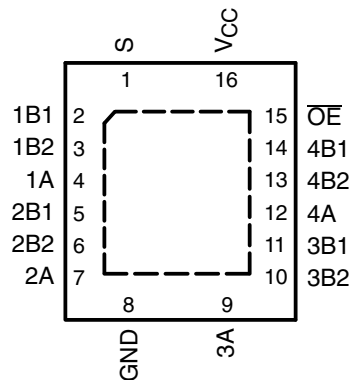
- 5-Ω Switch Connection Between Two Ports

- TTL-Compatible Input Levels

**D, DB, DBQ, OR PW PACKAGE  
(TOP VIEW)**



**RGY PACKAGE  
(TOP VIEW)**



### description/ordering information

The SN74CBT3257 is a 4-bit 1-of-2 high-speed TTL-compatible FET multiplexer/demultiplexer. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

Output-enable ( $\overline{OE}$ ) and select-control (S) inputs select the appropriate B1 and B2 outputs for the A-input data.

### ORDERING INFORMATION

| $T_A$         | PACKAGE†          |                | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---------------|-------------------|----------------|-----------------------|------------------|
| -40°C to 85°C | QFN – RGY         | Tape and reel  | SN74CBT3257RGYR       | CU257            |
|               | SOIC – D          | Tube           | SN74CBT3257D          | CBT3257          |
|               |                   | Tape and reel  | SN74CBT3257DR         |                  |
|               | SSOP – DB         | Tape and reel  | SN74CBT3257DBR        | CU257            |
|               | SSOP (QSOP) – DBQ | Tape and reel  | SN74CBT3257DBQR       | CU257            |
|               | TSSOP – PW        | Tube           | SN74CBT3257PW         | CU257            |
| Tape and reel |                   | SN74CBT3257PWR |                       |                  |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

### FUNCTION TABLE

| INPUTS          |   | FUNCTION         |
|-----------------|---|------------------|
| $\overline{OE}$ | S |                  |
| L               | L | A port = B1 port |
| L               | H | A port = B2 port |
| H               | X | Disconnect       |



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**TEXAS  
INSTRUMENTS**

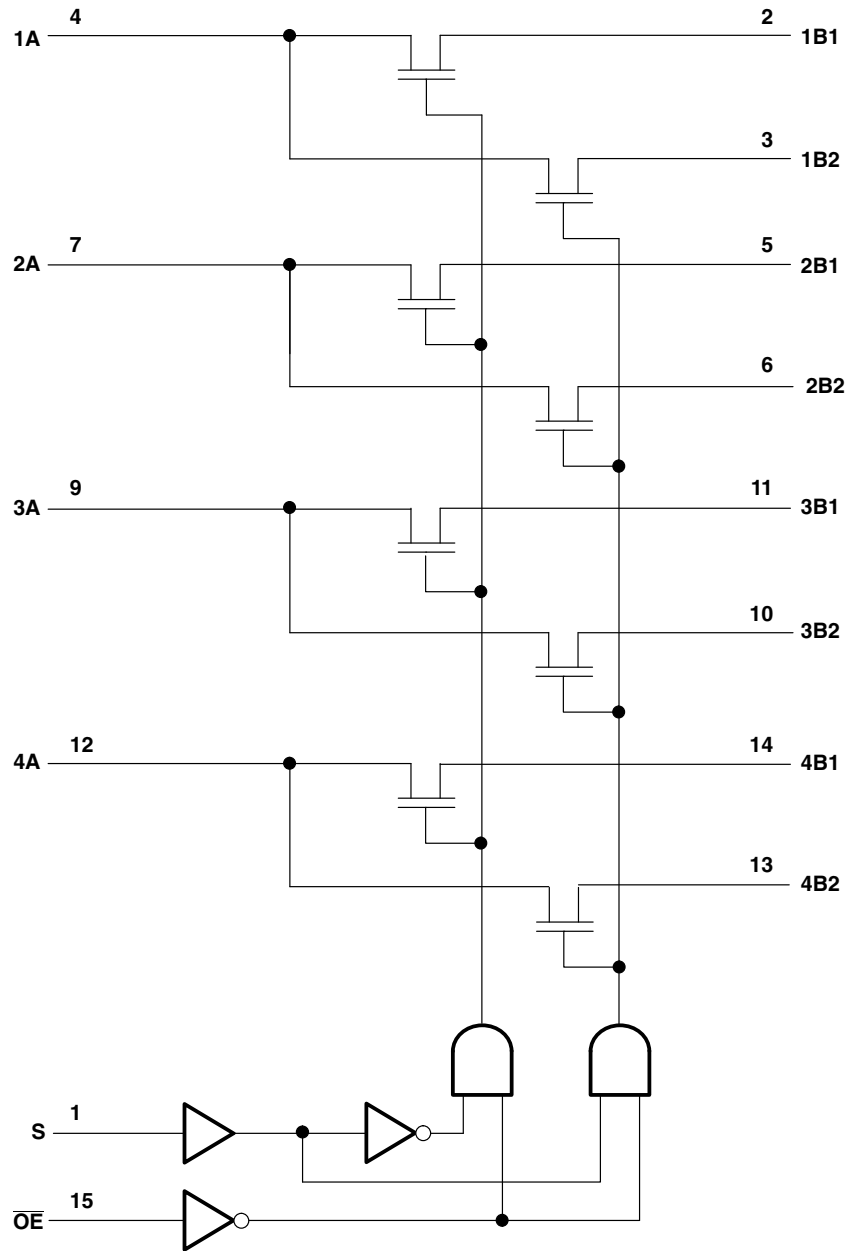
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# SN74CBT3257 4-BIT 1-OF-2 FET MULTIPLEXER/DEMULTIPLEXER

SCDS017M – MAY 1995 – REVISED JANUARY 2004

## logic diagram (positive logic)



# SN74CBT3257

## 4-BIT 1-OF-2 FET MULTIPLEXER/DEMULTIPLEXER

SCDS017M – MAY 1995 – REVISED JANUARY 2004

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

|  |                |
|--|----------------|
| Supply voltage range, $V_{CC}$                                   | –0.5 V to 7 V  |
| Input voltage range, $V_I$ (see Note 1)                          | –0.5 V to 7 V  |
| Continuous channel current                                       | 128 mA         |
| Input clamp current, $I_K$ ( $V_{I/O} < 0$ )                     | –50 mA         |
| Package thermal impedance, $\theta_{JA}$ (see Note 2): D package | 73°C/W         |
| (see Note 2): DB package   | 82°C/W         |
| (see Note 2): DBQ package  | 90°C/W         |
| (see Note 2): PW package   | 108°C/W        |
| (see Note 3): RGY package  | 39°C/W         |
| Storage temperature range, $T_{stg}$                             | –65°C to 150°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
 2. The package thermal impedance is calculated in accordance with JESD 51-7.  
 3. The package thermal impedance is calculated in accordance with JESD 51-5.

### recommended operating conditions (see Note 4)

|   | MIN | MAX | UNIT |
|---|-----|-----|------|
| $V_{CC}$ Supply voltage                   | 4   | 5.5 | V    |
| $V_{IH}$ High-level control input voltage | 2   |     | V    |
| $V_{IL}$ Low-level control input voltage  |     | 0.8 | V    |
| $T_A$ Operating free-air temperature      | –40 | 85  | °C   |

NOTE 4: All unused control inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER         |  | TEST CONDITIONS   |   | MIN | TYP‡ | MAX  | UNIT |   |
|-------------------|--|-------------------|---|-----|------|------|------|---|
| $V_{IK}$          |  | $V_{CC} = 4.5$ V, | $I_I = -18$ mA                                      |     |      | –1.2 | V    |   |
| $I_I$             |  | $V_{CC} = 5.5$ V, | $V_I = 5.5$ V or GND                                |     |      | ±1   | µA   |   |
| $I_{CC}$          |  | $V_{CC} = 5.5$ V, | $I_O = 0$ , $V_I = V_{CC}$ or GND                   |     |      | 3    | µA   |   |
| $\Delta I_{CC}$ § | Control inputs                           | $V_{CC} = 5.5$ V, | One input at 3.4 V, Other inputs at $V_{CC}$ or GND |     |      | 2.5  | mA   |   |
| $C_i$             | Control inputs                           | $V_I = 3$ V or 0  |   |     |      | 3.5  | pF   |   |
| $C_{io(OFF)}$     | A port                                   | $V_O = 3$ V or 0, | $\overline{OE} = V_{CC}$                            |     |      | 6.5  | pF   |   |
|                   | B port                                   |                   |   |     |      | 4    |      |   |
| $r_{on}$ ¶        | $V_{CC} = 4$ V,<br>TYP at $V_{CC} = 4$ V | $V_I = 2.4$ V,    | $I_I = 15$ mA                                       |     |      | 14   | Ω    |   |
|                   |  |                   |   |     |      | 5    |      | 7 |
|                   | $V_{CC} = 4.5$ V                         | $V_I = 0$         | $I_I = 64$ mA                                       |     |      | 5    |      | 7 |
|                   |  |                   |   |     |      | 5    |      | 7 |
|                   |  | $V_I = 2.4$ V,    | $I_I = 15$ mA                                       |     |      | 10   | 15   |   |

‡ All typical values are at  $V_{CC} = 5$  V (unless otherwise noted),  $T_A = 25^\circ\text{C}$ .

§ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than  $V_{CC}$  or GND.

¶ Measured by the voltage drop between the A and the B terminals at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (A or B) terminals.



# SN74CBT3257

## 4-BIT 1-OF-2 FET MULTIPLEXER/DEMULTIPLEXER

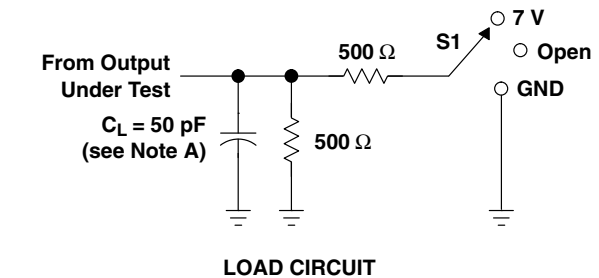
SCDS017M – MAY 1995 – REVISED JANUARY 2004

switching characteristics over recommended operating free-air temperature range,  $C_L = 50$  pF (unless otherwise noted) (see Figure 1)

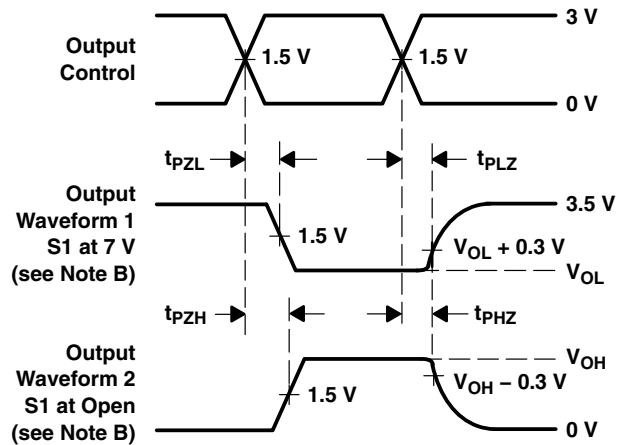
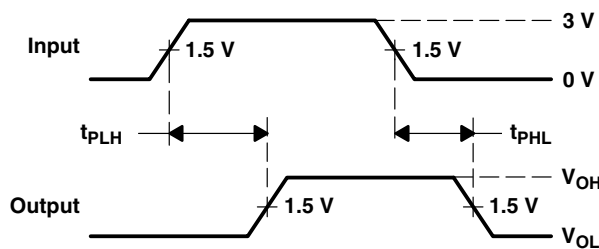
| PARAMETER        | FROM (INPUT)    | TO (OUTPUT) | $V_{CC} = 4$ V |     | $V_{CC} = 5$ V<br>$\pm 0.5$ V |     | UNIT |
|------------------|-----------------|-------------|----------------|-----|-------------------------------|-----|------|
|                  |                 |             | MIN            | MAX | MIN                           | MAX |      |
| $t_{pd}^\dagger$ | A or B          | B or A      | 0.35           |     | 0.25                          |     | ns   |
| $t_{pd}$         | S               | A           | 5.5            |     | 1.6                           | 5   | ns   |
| $t_{en}$         | S               | B           | 5.7            |     | 1.6                           | 5.2 | ns   |
|                  | $\overline{OE}$ | A or B      | 5.6            |     | 1.8                           | 5.1 |      |
| $t_{dis}$        | S               | B           | 5.2            |     | 1                             | 5   | ns   |
|                  | $\overline{OE}$ | A or B      | 5.5            |     | 2.2                           | 5.5 |      |

$^\dagger$  The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

### PARAMETER MEASUREMENT INFORMATION



| TEST              | S1   |
|-------------------|------|
| $t_{pd}$          | Open |
| $t_{PLZ}/t_{PZL}$ | 7 V  |
| $t_{PHZ}/t_{PZH}$ | Open |



- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5$  ns,  $t_f \leq 2.5$  ns.
  - The outputs are measured one at a time with one transition per measurement.
  - $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
  - All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2) | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|---------|
| SN74CBT3257D     | LIFEBUY       | SOIC         | D               | 16   | 40          | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | CBT3257                 |         |
| SN74CBT3257DBQR  | LIFEBUY       | SSOP         | DBQ             | 16   | 2500        | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 85    | CU257                   |         |
| SN74CBT3257DBR   | LIFEBUY       | SSOP         | DB              | 16   | 2000        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | CU257                   |         |
| SN74CBT3257DG4   | LIFEBUY       | SOIC         | D               | 16   | 40          | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | CBT3257                 |         |
| SN74CBT3257DR    | LIFEBUY       | SOIC         | D               | 16   | 2500        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | CBT3257                 |         |
| SN74CBT3257PW    | LIFEBUY       | TSSOP        | PW              | 16   | 90          | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | CU257                   |         |
| SN74CBT3257PWR   | LIFEBUY       | TSSOP        | PW              | 16   | 2000        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | CU257                   |         |
| SN74CBT3257RGYR  | LIFEBUY       | VQFN         | RGY             | 16   | 3000        | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 85    | CU257                   |         |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

| Device          | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74CBT3257DBQR | SSOP         | DBQ             | 16   | 2500 | 330.0              | 12.5               | 6.4     | 5.2     | 2.1     | 8.0     | 12.0   | Q1            |
| SN74CBT3257DBR  | SSOP         | DB              | 16   | 2000 | 330.0              | 16.4               | 8.35    | 6.6     | 2.4     | 12.0    | 16.0   | Q1            |
| SN74CBT3257DR   | SOIC         | D               | 16   | 2500 | 330.0              | 16.4               | 6.5     | 10.3    | 2.1     | 8.0     | 16.0   | Q1            |
| SN74CBT3257PWR  | TSSOP        | PW              | 16   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |
| SN74CBT3257RGYR | VQFN         | RGY             | 16   | 3000 | 330.0              | 12.4               | 3.8     | 4.3     | 1.5     | 8.0     | 12.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device          | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74CBT3257DBQR | SSOP         | DBQ             | 16   | 2500 | 340.5       | 338.1      | 20.6        |
| SN74CBT3257DBR  | SSOP         | DB              | 16   | 2000 | 356.0       | 356.0      | 35.0        |
| SN74CBT3257DR   | SOIC         | D               | 16   | 2500 | 340.5       | 336.1      | 32.0        |
| SN74CBT3257PWR  | TSSOP        | PW              | 16   | 2000 | 367.0       | 367.0      | 35.0        |
| SN74CBT3257RGYR | VQFN         | RGY             | 16   | 3000 | 367.0       | 367.0      | 35.0        |

**TUBE**


\*All dimensions are nominal

| Device         | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|----------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| SN74CBT3257D   | D            | SOIC         | 16   | 40  | 507    | 8      | 3940   | 4.32   |
| SN74CBT3257DG4 | D            | SOIC         | 16   | 40  | 507    | 8      | 3940   | 4.32   |
| SN74CBT3257PW  | PW           | TSSOP        | 16   | 90  | 530    | 10.2   | 3600   | 3.5    |

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4211283-4/E 08/12

- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



4220204/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

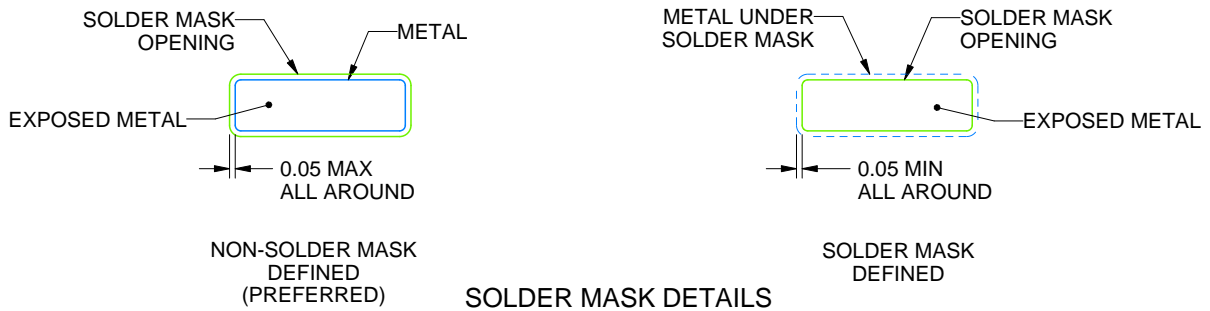
PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220204/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

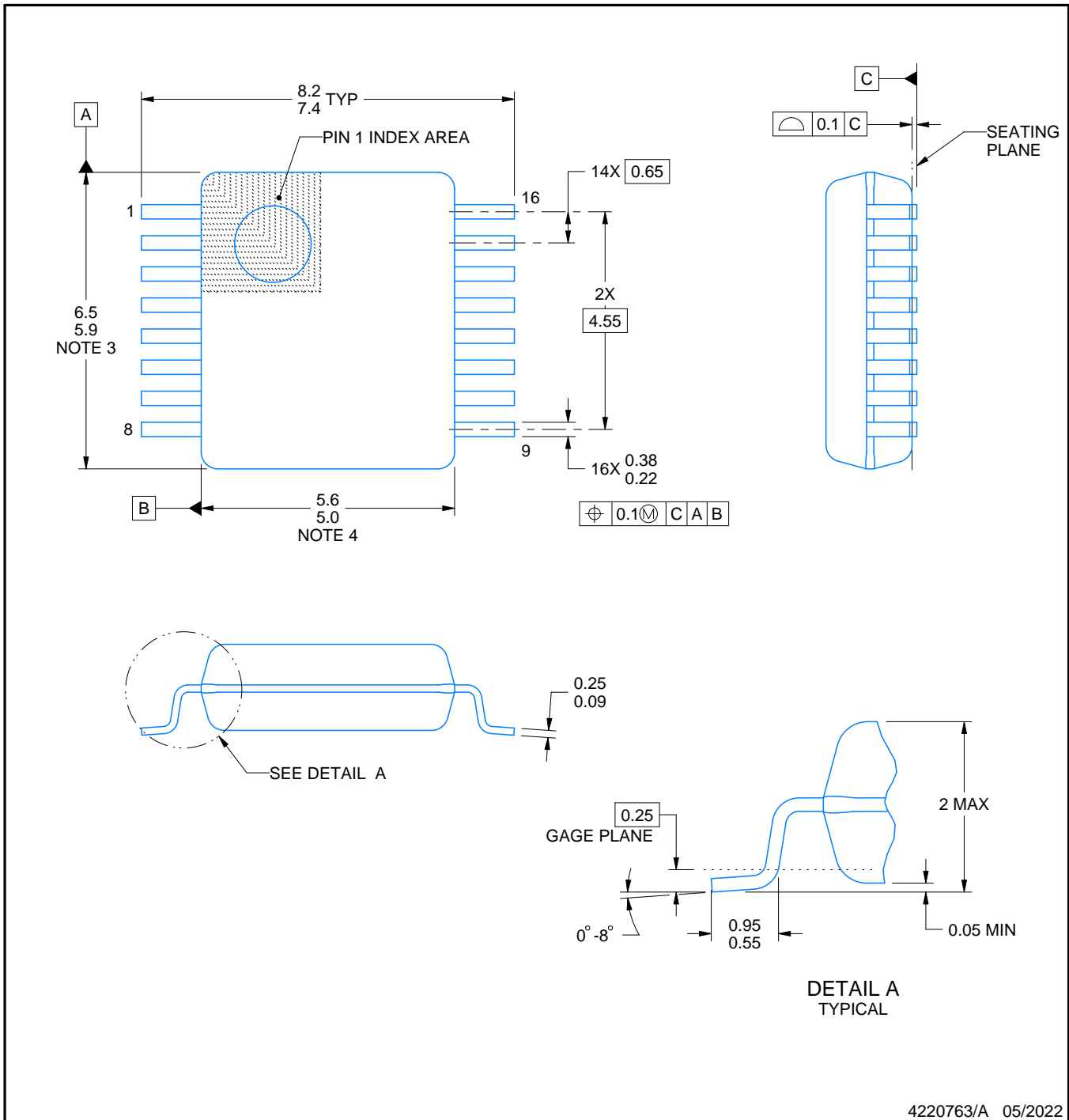
# DB0016A



# PACKAGE OUTLINE

## SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



### NOTES:

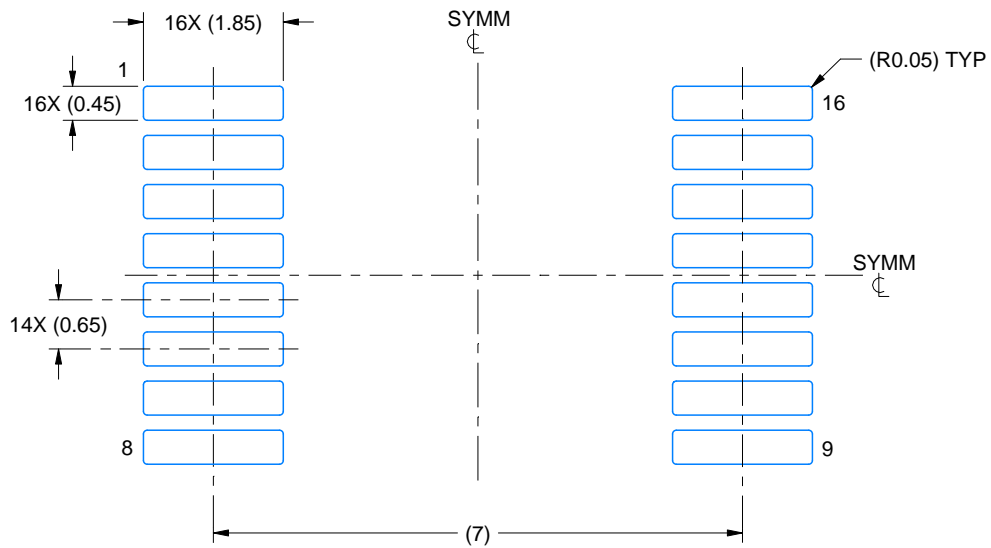
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.

# EXAMPLE BOARD LAYOUT

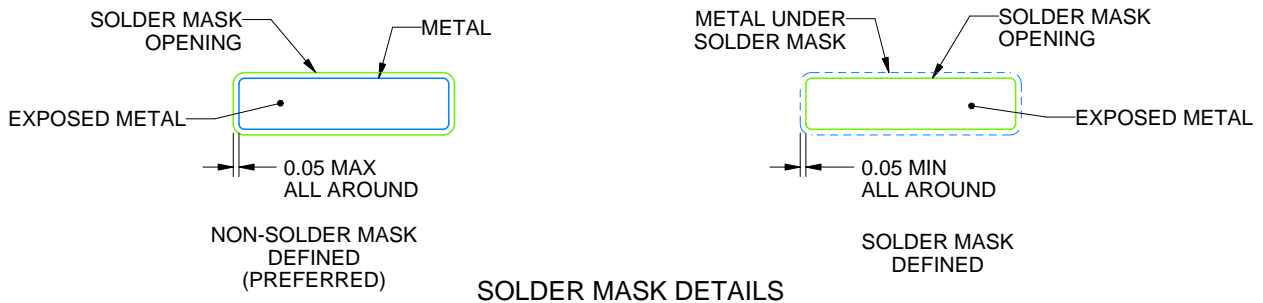
DB0016A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220763/A 05/2022

NOTES: (continued)

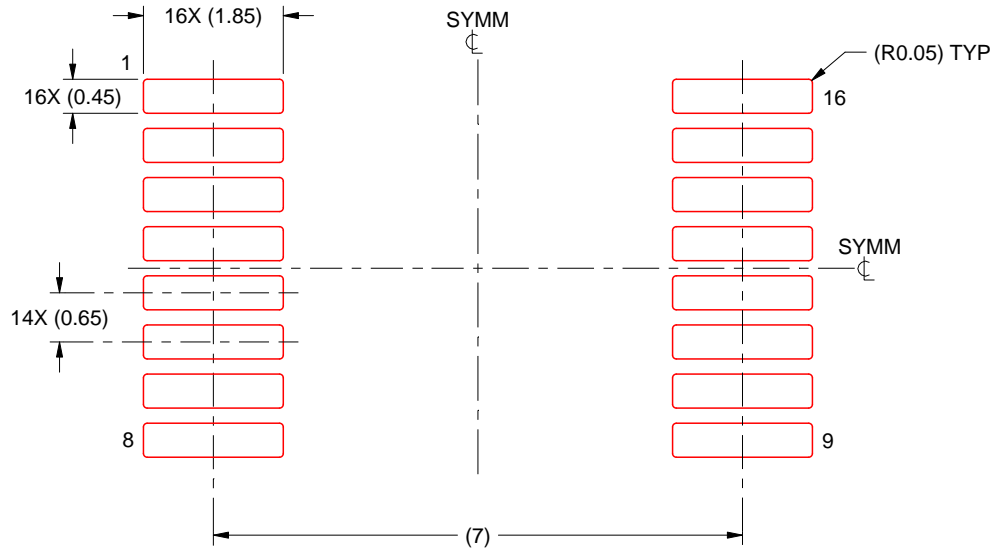
- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DB0016A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220763/A 05/2022

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

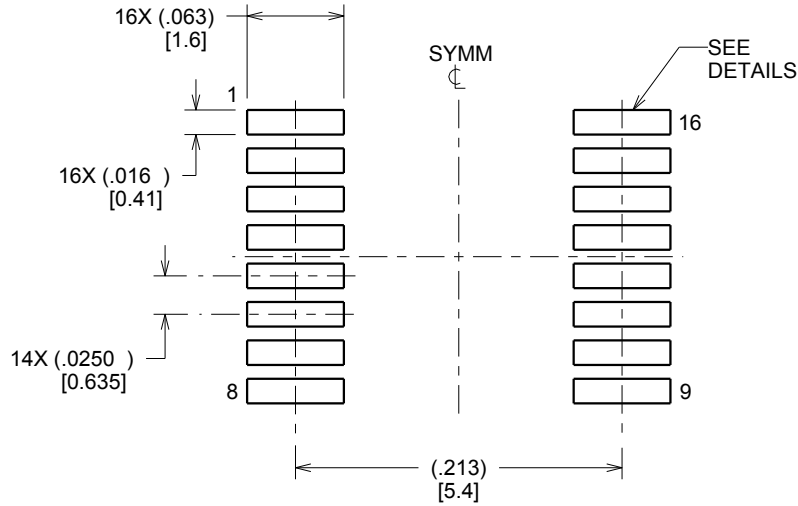


# EXAMPLE BOARD LAYOUT

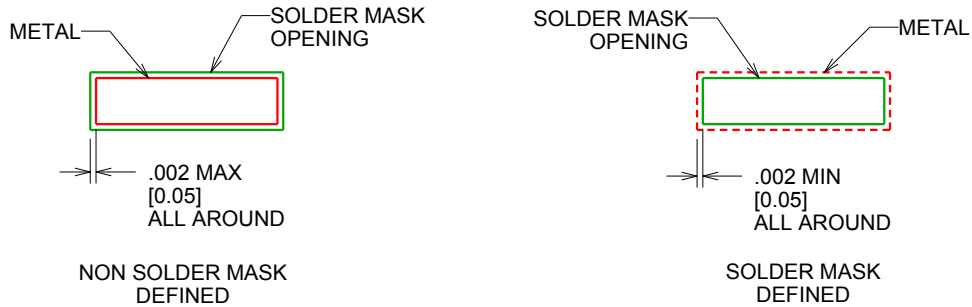
DBQ0016A

SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:8X



SOLDER MASK DETAILS

4214846/A 03/2014

NOTES: (continued)

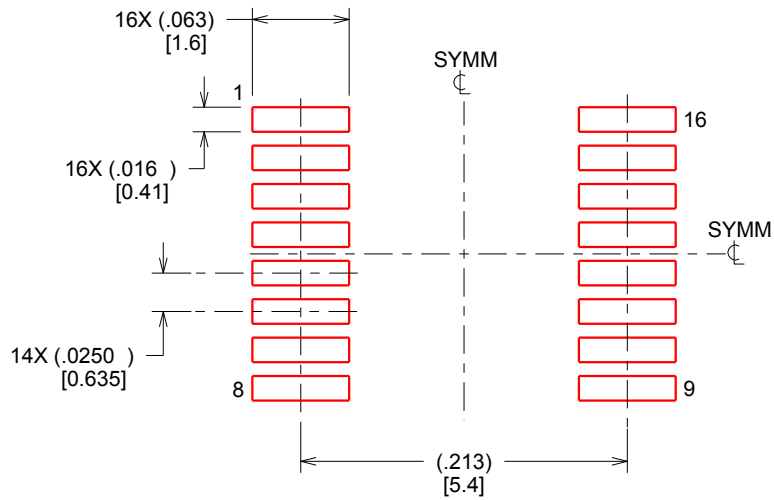
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DBQ0016A

SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.127 MM] THICK STENCIL  
SCALE:8X

4214846/A 03/2014

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

RGY (R-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



4203539-3/1 06/2011

- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - This drawing is subject to change without notice.
  - QFN (Quad Flatpack No-Lead) package configuration.
  - The package thermal pad must be soldered to the board for thermal and mechanical performance.
  - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
  - Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
  - Package complies to JEDEC MO-241 variation BA.

RGY (R-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD

**THERMAL INFORMATION**

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4206353-3/P 03/14

NOTE: All linear dimensions are in millimeters

RGY (R-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



4208122-3/P 03/14

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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