

RD1-4020

DisplayPort to DVI output

User Guide

Rev. B

**MegaChips**

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## 1. Purpose and scope

This document provides description and setup instructions for the DisplayPort® Receiver STDP4020 reference design board [RD1-4020\_400-530] targeted for DP to DVI conversion applications.

## 2. Description

The STDP4020 is an integrated circuit featuring a four lane DisplayPort receiver, quad LVDS & LVTTTL transmitter with I2S and SPDIF audio outputs for digital audio-video conversion application. This device also includes SPI interface, I2C Slave (Host Interface), I2C Master Interface, UART (GProbe) interface, and general-purpose IO pins. The RD1-4020 is a low cost compact four layer board that includes necessary interfaces and features to fully demonstrate the STDP4020 receiver functionalities. The RD1-4020 board includes discrete TMDS transmitter chips, converting LVTTTL output from STDP4020 into DVI. This board is capable of handling both single link and dual link DVI output supporting video resolution from 640 x 480 up to 2560 x 1600. The RD1-4020 also features digital audio outputs SPDIF and I2S up to 8 Ch.

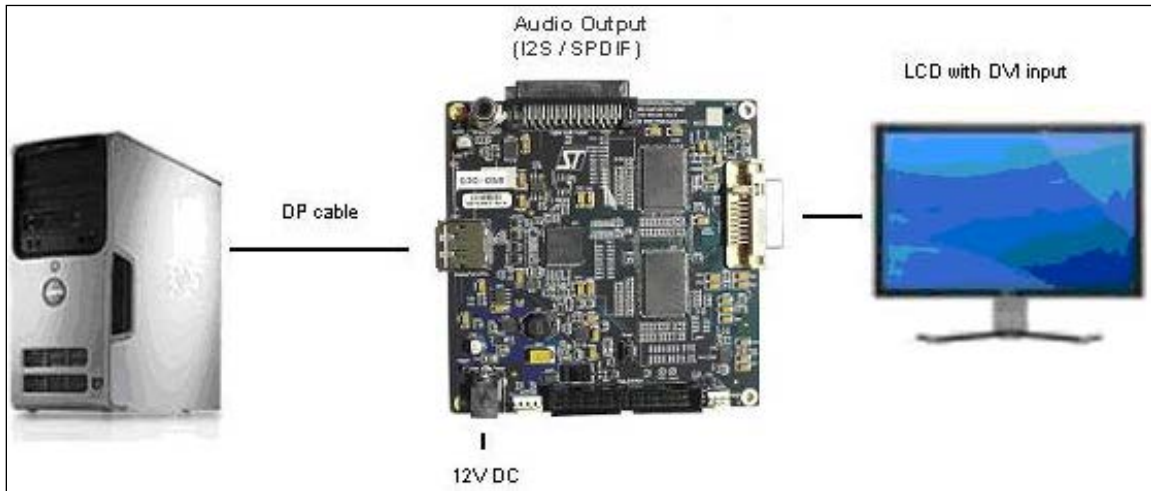
This reference design meets the following objectives:

1. Stand-alone operation: Includes the necessary firmware (either IROM or external SPI) to work independently; this means the intended functionalities are performed without depending on external (Host) controllers.
2. Slave configuration: Provision to configure the device by an external Host controller through the Host Interface to I2C (most likely when no SPI Flash is used).

## 3. Set up instructions

The picture below [Figure 1] is a connection diagram showing the RD1-4020 board used for transferring a PC DisplayPort signal into a dual link DVI output. Software utility: GProbe tool (ver 5.7.X.X), WinI2C tool

Figure 1. Connection diagram: PC DP signal to dual link DVI output



This board uses the standard DisplayPort connector recommended in the DP specification to connect the DisplayPort output from the PC to the input of the RD1-4020 board, and a dual link DVI connector to interface with a commercial DVI monitor.

1. Connect the DisplayPort output from a PC source to the RD1-4020 reference board using a DP cable.
2. Connect the output to a DVI monitor using a DVI cable. Connect the 12 V (4A) DC power brick supplied for powering the board. A DisplayPort source that supports DP-Audio transmission is recommended for testing digital audio output of the RD1-4020 board.
3. Once the connection is established, power ON the PC, DVI display, and the RD1-4020 (DP receiver) board. An image should pop up on the screen within 5-6 seconds.

### 3.1. I2C host port

Host connector (CN401) allows configuration of the STDP4020 IC from an external host (microcontroller) through conventional I2C interface. User can plug two wires into pin 5 and pin 6 of this connector to access the I2C port of the chip. STDP4020 default device ID is 0xE6/0xE7, but can be changed through bootstrap settings. Refer to the STDP4020 datasheet for further details.

### 3.2. In-System Programming (ISP)

RD1-4020 uses SPI Flash to store the firmware. In case of a new firmware upgrade, one of the following methods can be used.

1. ISP through DisplayPort connector: Allows programming the SPI Flash through DisplayPort input connector. Requires DP ISP board and GProbe software tool (contact MegaChips).
2. ISP through UART connector: Allows programming the SPI Flash through UART (RS232) connector. Requires GProbe board (RS232 converter circuit) and GProbe software tool (contact MegaChips).

## 4. Diagnosis

If the image does not come up, follow the steps below for diagnosis.

*Note: The diagnosis requires the MegaChips GProbe software and hardware tool. Contact MegaChips for the GProbe software and board.*

1. Install the GProbe diagnostic tool on a computer and set the baud rate to 115,200.
2. Connect MegaChips GProbe board (not supplied) to the serial port (or USB port if using USB version) of the computer.
3. Connect the other end of the GProbe board to connector (CN403) on the RD1-4020 board using 4-wire cable (part of the GProbe board).

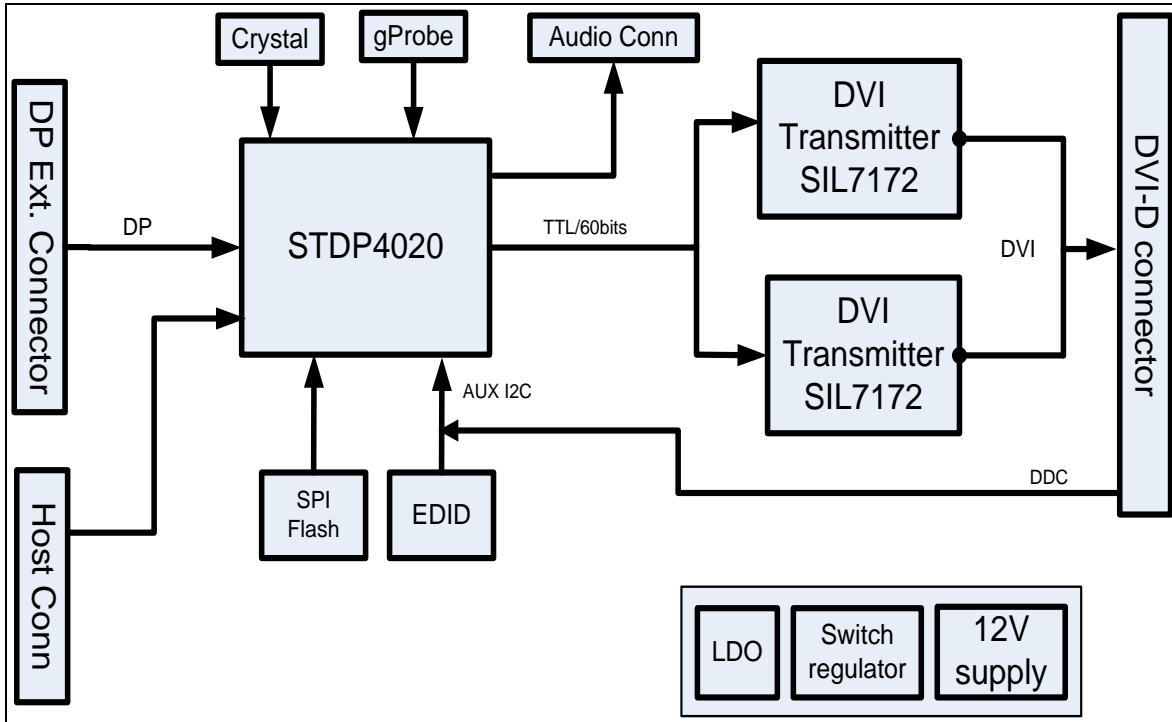
*Note: CHECK POLARITY while connecting the cable; Pin 1 is marked on the board. The 4-wire cable connection from CN403 to GProbe board is 1 to 1.*

4. Hit the Reset button on the board (RESET SW402). You will see the firmware version and date of firmware in the GProbe window. This indicates the DP receiver IC is functional. If the message does not appear, reprogram the Flash using the ISP method described in the GProbe user guide.
5. Using an oscilloscope, check the video input and output from the STDP4020.

*Note: Refer to the STDP4020 datasheet for pin out descriptions.*

4.1. Board description

Figure 2. Block diagram





## 4.2. Principal components and functions

Below is a summary of all necessary connectors, switches, and other components. Please refer to the latest board schematics for further details.

**Table 1. Principal components and functions**

| Label                | Description  | RefDes     |
|----------------------|--|------------|
| Power Input (+12 V)  | Input 12 V, down conversion to 5 V, 3.3 V, and 1.2 V. This board uses a switch regulator for 5 V and an LDO [ <b>low-dropout</b> ] for 3.3 V and 1.2 V. Note the analog and digital supplies (3.3A and 3.3D or 1.2A and 1.2D) are isolated using ferrite beads.  | CN301      |
| STDP4020             | MegaChips DisplayPort Receiver [STDP4020] is capable of receiving and converting DisplayPort signals into 60-bit LVTTTL output ports that can be mapped to transfer video data either in two pixels per clock or single pixel per clock up to 300 MHz pixel rate. The STDP4020 supports RGB and YCC video color formats with color depth of 12 (YCC 4:2:2 only), 10, and 8 bits.         | U601       |
| DP Input             | DisplayPort input connector  | CN501      |
| Flash                | The board includes an SPI Flash of 2 MB to hold the firmware. The SPI Flash can be programmed (ISP) through DP AUX Channel or through UART interface.  | U702       |
| DVI Out              | DVI output connector   | CN1101     |
| Sil7172              | Dual-Link DVI transmitters Sil7172   | U901,U1001 |
| Digital Audio Output | Digital Audio Output [S/PDIF & I2S in 3.3V logic]: This board supports both compressed and uncompressed audio formats. The extracted audio signal is transferred on a digital audio output bus. This device comprises four I2S audio output ports supporting up to eight channel LPCM audio and a single wire S/PDIF output for encoded audio  | CN402      |
| S/PDIF Output        | Standard S/PDIF output signal.   | CN404      |
| Host Interface       | Host Interface (I2C): This board includes a provision to access the STDP4020 device from an external host controller through the Host Interface (I2C port) connection.   | CN401      |
| GProbe               | GProbe Interface (+3.3 V logic): The board also includes a GProbe connector that connects to the STDP4020 UART port for communication with external PC sources for debug purposes. The MegaChips GProbe tool (software) and PC serial port interface board together create a debug environment for device debug and firmware update. The GProbe interface is also used for ISP purposes. | CN403      |
| Reset                | Reset Button, when pressed, triggers a system master reset through the internal reset circuitry. The reset button is used for system reset and debug purposes and is not required for production board design as the STDP4020 produces an internal reset during power ON.  | SW402      |
| IR Input             | An IR connector for interfacing ST's IR receiver.  | CN701      |
| LED                  | Single LED for indicating the power on status.   | D301       |
| Crystal              | An external crystal of 27 MHz. The design makes use of internal oscillator circuitry.  | X701       |

| Label             | Description  | RefDes                               |
|-------------------|--|--------------------------------------|
| ESD Diodes        | ESD protection diodes for DisplayPort signal (main lanes, AUX and HPD line). The board implements low cost ESD diodes.             | ESD501<br>ESD503<br>ESD504<br>ESD505 |
| EDID              | EDID Option: Currently not populated to allow pass through.  | U701                                 |
| SW401             | Switches UART between Host Interface & GProbe Interface (see mark on PCB).   | SW401                                |
| Bootstrap Options | The bootstrap options can be configured for:<br>– Single/Dual TTL<br>– IROM/ SPI Flash<br>Refer to the datasheet for more details. | R606<br>R607<br>R608<br>R609         |

### 4.3. Connector descriptions

The RD1-4020 has the following connectors. The locations of these connectors are shown in the board picture in Figure 3.

**CN301** – +12 V DC 4A Power Input Jack

**CN403** – GProbe Interface (4x1 pin keyed header) connects to the UART port of the STDP4020. Use the MegaChips GProbe board and interface cable for connecting the board to an external PC that has GProbe software running.

|              |           |
|--------------|-----------|
| <b>Pin 1</b> | +5V       |
| <b>Pin 2</b> | GPROBE_TX |
| <b>Pin 3</b> | GPROBE_RX |
| <b>Pin 4</b> | GND       |

**CN401** – I2C Host Interface (header 17X2) connector for connecting external host. This is used only when an external host controller accesses the DisplayPort receiver; not used for normal operation. In normal operation, internal MCU controls the overall functioning of the DisplayPort receiver (refer to the schematics for complete pin description for the Host Interface).

|                      |                 |
|----------------------|-----------------|
| <b>Pin 1 &amp; 2</b> | +5V             |
| <b>Pin 3 &amp; 4</b> | GND             |
| <b>Pin 5</b>         | I2C_SCL         |
| <b>Pin 6</b>         | I2C_SDA         |
| <b>Pin 7</b>         | HOST_TX         |
| <b>Pin 8</b>         | HOST_RX         |
| <b>Pin 9</b>         | RESET from Host |

|             |             |
|-------------|-------------|
| Pin 10      | NC          |
| Pin 11 & 12 | GND         |
| Pin 13      | AUX_UART_TX |
| Pin 14      | AUX_UART_RX |
| Pin 15      | AUX_I2C_SCL |
| Pin 16      | AUX_I2C_SDA |
| Pin 17 & 18 | NC          |
| Pin 19 & 20 | GND         |
| Pin 21 & 22 | NC          |
| Pin 23      | IRQ         |
| Pin 24      | IR_IN       |
| Pin 25      | I2C_MST_SCL |
| Pin 26      | I2C_MST_SDA |
| Pin 27 & 28 | GND         |
| Pin 29 & 30 | NC          |
| Pin 31      | TP401       |
| Pin 32      | NC          |
| Pin 33      | TP402       |
| Pin 34      | NC          |

**CN404** – SPDIF output connector.

|       |       |
|-------|-------|
| Pin 1 | GND   |
| Pin 2 | I2S_0 |
| Pin 3 | GND   |

**CN402** – I2S Digital Audio Output (52 pin) connector. Pinout details are shown below.

|                   |                   |
|-------------------|-------------------|
| Pin A1            | NC                |
| Pin A2 & A3       | GND               |
| Pin A4 through A6 | NC                |
| Pin A7            | GND               |
| Pin A8 & A9       | NC                |
| Pin A10           | I2S_3             |
| Pin A11           | I2S_2             |
| Pin A12           | I2S_1             |
| Pin A13           | NC                |
| Pin A14           | I2S_0             |
| Pin A15           | R412 / OR / I2S_0 |
| Pin A16 & A17     | GND               |

|                     |          |
|---------------------|----------|
| Pin A18             | I2S_MCLK |
| Pin A19 through A21 | NC       |
| Pin A22             | I2S_BCLK |
| Pin A23             | +5V      |
| Pin A24             | I2S_WCLK |
| Pin A25 & A26       | +5V      |
| Pin B1              | GND      |
| Pin B2 & B3         | NC       |
| Pin B4 & B5         | GND      |
| Pin B6 & B7         | NC       |
| Pin B8 & B9         | GND      |
| Pin B10 through B13 | NC       |
| Pin B14 & B15       | GND      |
| Pin B16 through B18 | NC       |
| Pin B19 & B20       | GND      |
| Pin B21             | +12V     |
| Pin B22             | NC       |
| Pin B23             | +12V     |
| Pin B24             | NC       |
| Pin B25             | +12V     |
| Pin B26             | GND      |

**CN1101** – Dual-Link DVI-D connector.

|        |             |
|--------|-------------|
| Pin 1  | DVI_TX2-    |
| Pin 2  | DVI_TX2+    |
| Pin 3  | GND         |
| Pin 4  | DVI_TX4-    |
| Pin 5  | DVI_TX4+    |
| Pin 6  | AUX_I2C_SCL |
| Pin 7  | AUX_I2C_SDA |
| Pin 8  | NC          |
| Pin 9  | DVI_TX1-    |
| Pin 10 | DVI_TX1+    |
| Pin 11 | GND         |
| Pin 12 | DVI_TX3-    |
| Pin 13 | DVI_TX3+    |
| Pin 14 | +5V         |
| Pin 15 | GND         |
| Pin 16 | DVI_HPD_DET |
| Pin 17 | DVI_TX0-    |

|                          |          |
|--------------------------|----------|
| <b>Pin 18</b>            | DVI_TX0+ |
| <b>Pin 19</b>            | GND      |
| <b>Pin 20</b>            | DVI_TX5- |
| <b>Pin 21</b>            | DVI_TX5+ |
| <b>Pin 22</b>            | GND      |
| <b>Pin 23</b>            | DVI_CLK+ |
| <b>Pin 24</b>            | DVI_CLK- |
| <b>Pin C1 through C4</b> | NC       |
| <b>Pin C5 &amp; C6</b>   | GND      |

**CN701** – IR input

|              |       |
|--------------|-------|
| <b>Pin 1</b> | GND   |
| <b>Pin 2</b> | +5V   |
| <b>Pin 3</b> | IR_IN |

**CN501** – DisplayPort connector

|               |                 |
|---------------|-----------------|
| <b>Pin 1</b>  | ML_L3N          |
| <b>Pin 2</b>  | GND             |
| <b>Pin 3</b>  | ML_L3P          |
| <b>Pin 4</b>  | ML_L2N          |
| <b>Pin 5</b>  | GND             |
| <b>Pin 6</b>  | ML_L2P          |
| <b>Pin 7</b>  | ML_L1N          |
| <b>Pin 8</b>  | GND             |
| <b>Pin 9</b>  | ML_L1P          |
| <b>Pin 10</b> | ML_L0N          |
| <b>Pin 11</b> | GND             |
| <b>Pin 12</b> | ML_L0P          |
| <b>Pin 13</b> | GND             |
| <b>Pin 14</b> | GND             |
| <b>Pin 15</b> | +3V3_AVDD/AUX_P |
| <b>Pin 16</b> | GND             |
| <b>Pin 17</b> | GND / AUX_N     |
| <b>Pin 18</b> | HPD_OUT         |
| <b>Pin 19</b> | GND             |
| <b>Pin 20</b> | +3V3_DVDD       |

## 4.4. Switches

Host Interface Switch: (SW401): This switch selects the use of GProbe connector or Host Interface connector.

|              |           |
|--------------|-----------|
| <b>Pin 1</b> | HOST_TX   |
| <b>Pin 2</b> | UART_TX   |
| <b>Pin 3</b> | GPROBE_TX |
| <b>Pin 4</b> | HOST_RX   |
| <b>Pin 5</b> | UART_RX   |
| <b>Pin 6</b> | GPROBE_RX |

## 4.5. Stuffing options

### 4.5.1. Single/dual TTL

**Single TTL configuration:** stuff R609, unstuff R608

**Dual TTL configuration:** stuff R608, unstuff R609

### 4.5.2. IROM/SPI-Flash

**OCM boot from IROM code:** stuff R607, unstuff R606

**OCM boot from external ROM code:** stuff R606, unstuff R607

## 5. Revision history

**Table 2. Document revision history**

| Date        | Revision | Changes  |
|-------------|----------|--|
| 27-Aug-2010 | A        | Initial version.   |
| 02-Jun-2014 | B        | Updated to comply with MegaChips documentation style/formatting. |

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