THE DATASHEET OF

TDA21301

Version 1.03 , Aug 2004

Datasheet

DS-CoreControl-TDA21301

TDA21301

Authors: Edward Chang

Published by Infineon Technologies AG
http://www.infineon.com/DCDC

Discrete & Power Management

Never stop thinking.

Contents:

Multi-Phase PWM Controller for CPU Core Power Supply

P-TSSOP-28

Features :

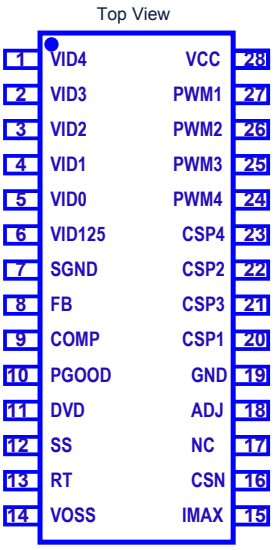
- Multi-Phase PWM Conversion with Automatically Phase Selection
- VRD10.X Compliant
- Active Droop Compensation For Fast Load Response
- Smooth V_{CORE} Voltage Transition during the Dynamic VIDs
- Inductive DCR Current Sense Technique
- Hiccup Mode Over Current Protection
- Programmable Switching Frequency (50kHz ~ 400kHz per Phase), Under Voltage Lockout, and Soft-Start
- High Output Ripple Frequency times numbers of working Channels

Application :

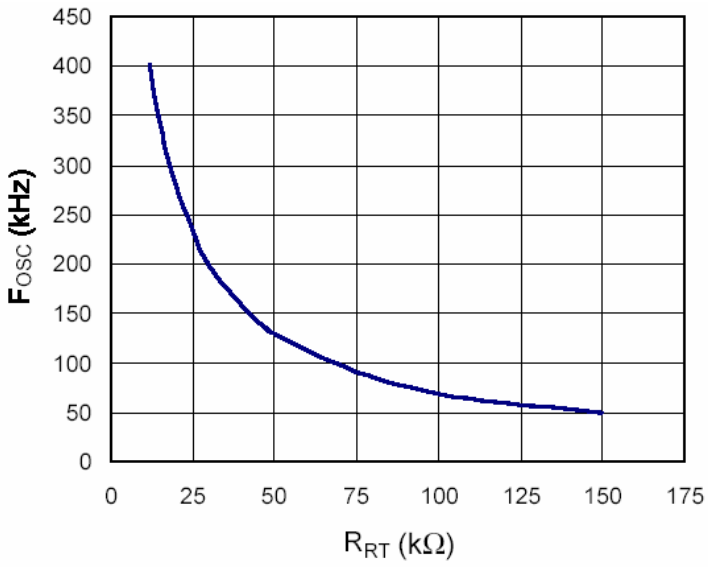
- Intel Processor Voltage Regulator : VRM10.X
- Low Output Voltage High Output Current DC-DC Converters
- Voltage Regulator Modules

Type	Package	Marking	Ordering Code
TDA21301	P-TSSOP-28	21301	Q67042-S4228

Pinout Drawing:



Frequency VS R_{RT}



Pinout Description:

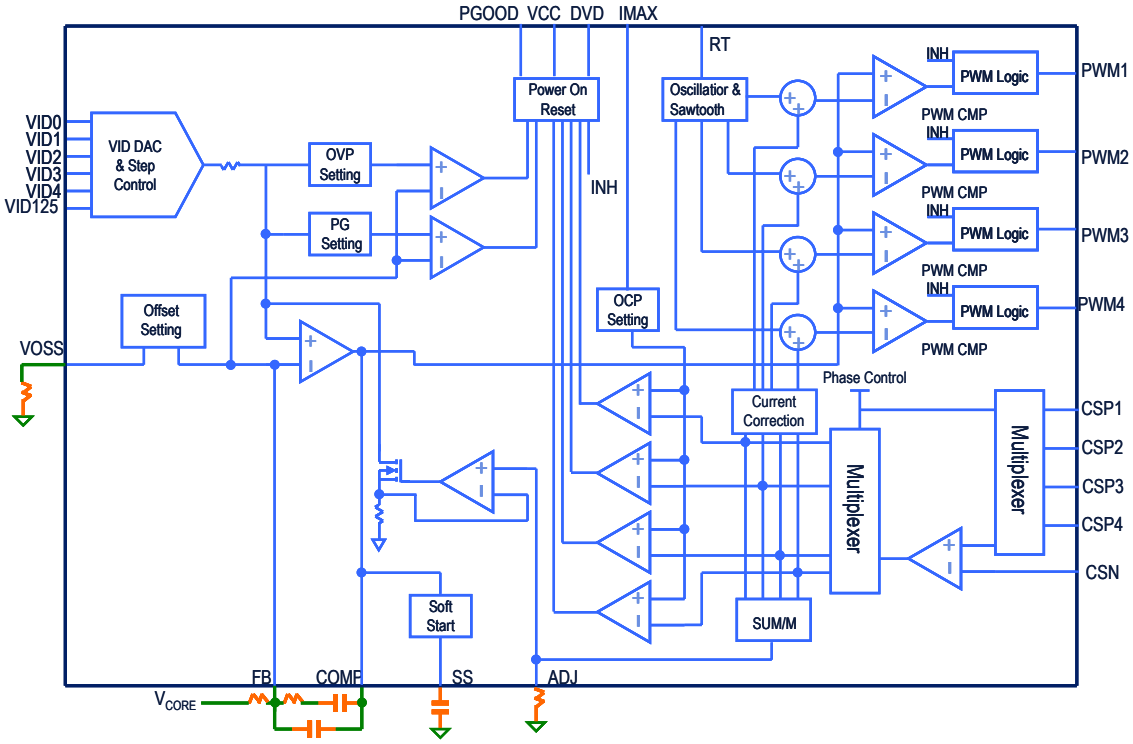
Number	Name	Description
1	VID4	Voltage Identification DAC Input. Internally pull up to 1.2V.
2	VID3	Voltage Identification DAC Input. Internally pull up to 1.2V.
3	VID2	Voltage Identification DAC Input. Internally pull up to 1.2V.
4	VID1	Voltage Identification DAC Input. Internally pull up to 1.2V.
5	VID0	Voltage Identification DAC Input. Internally pull up to 1.2V.
6	VID125	Voltage Identification DAC Input. Internally pull up to 1.2V.
7	SGND	The negative input pin of the differential converter output voltage sense amplifier
8	FB	Internal error amplifier inverting input pin
9	COMP	Output of the error amplifier and input of the PWM comparators
10	PGOOD	Open drain power good signal output pin
11	DVD	Connect the external voltage divider to program the controller under voltage lockout based on the input voltage of the power stage.
12	SS	Soft-Start. Connect with a capacitor to GND to set the Soft-Start Interval. Pulling down this pin below 1V shall shut the converter down.
13	RT	Connect a resistor to GND to set the channel switching frequency
14	VOSS	Connect a resistor to GND to set the initial offset voltage.
15	IMAX	Connect a resistor to GND to set the over current level.
16	CSN	The negative input pin of the differential current sense amplifier connects to output voltage
17	NC	No connect
18	ADJ	Connect a resistor to GND to set the Droop Voltage.
19	GND	Ground pin of the IC
20	CSP1	Differential current sense positive input pin connects to switching node.
21	CSP3	Differential current sense positive input pin connects to switching node.
22	CSP2	Differential current sense positive input pin connects to switching node.
23	CSP4	Differential current sense positive input pin connects to switching node.
24	PWM4	Channel 4 PWM output pin
25	PWM3	Channel 3 PWM output pin
26	PWM2	Channel 2 PWM output pin
27	PWM1	Channel 1 PWM output pin
28	VCC	IC power supply pin connects to 5V

General Description

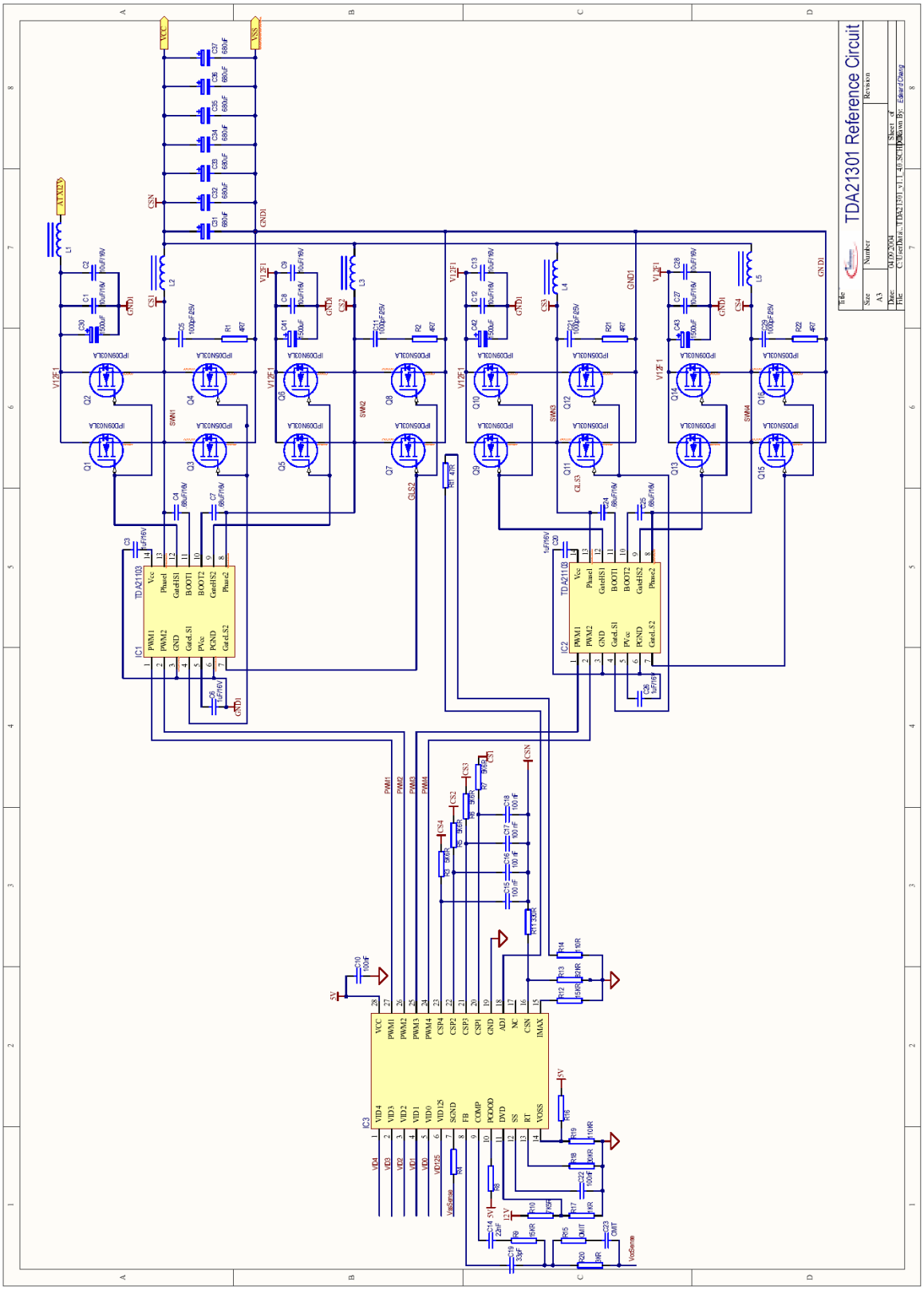
TDA21301 is a multi-phase DC-DC buck converter controller integrated all control functions for the next generation GHz CPU voltage regulator. TDA21301 automatically controls 2 to 4 interleaved buck switching power stage operation. The multi-phase architecture is able to provide high output current with lower power dissipation on the switching devices and minimizing the input ripple current and output ripple voltage. The equivalent high operation frequency optimizes the voltage regulator design for better transient response and thermal performance.

TDA21301 utilizes the DCR of the output inductors in every channel as the current sense element. The differential current sense in every channel results precious channel current information to the controller for good droop adjustment, channel current balance, channel switching devices thermal balance and over current protection. The offset error caused by individual differential current sense amplifier can be eliminated due to that the multiplexer is use to select the different channel current sense signals with single differential current sense amplifier.

Block Diagram



Reference Circuit



Absolute Maximum Ratings

At Tj = 25 °C, unless otherwise specified

Parameter	Symbol	Value		Unit
		Min.	Max.	
Voltage supplied to 'VCC' pin; DC	V_{CC}	-0.3	7	V
Input, Output or I/O Pin		-0.3	Vcc+0.3	
Junction temperature	T_J	0	125	°C
Storage temperature	T_S	-65	150	
ESD Rating; Human Body Model		2		kV
ESD Rating; Machine Model		200		V
IEC climatic category; DIN EN 60068-1		55/150/56		-

Thermal Characteristic

Parameter	Symbol	Values			Unit
		Min.	Typ.	Max.	
Thermal resistance, junction-soldering point					K/W
Thermal resistance, junction-ambient				50	

Electrical Characteristic

At Vcc=5V, Tj = 25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Values			Unit
			Min.	Typ.	Max.	
Supply Characteristic						
Bias supply current	I_{CC}	PWM1,2,3,4 Open		12	16	mA
Power On Reset Characteristic						
POR Threshold	V_{CCRTH}	V_{CC} rising threshold	4.0	4.2	4.5	V
Hysteresis	V_{CCHYS}		0.2	0.5		
V_{DVD} Threshold	V_{DVDTP}	Low to High Enable	1.1	1.2	1.3	
V_{DVD} Hysteresis	V_{DVDHYS}	V_{VCC} falling threshold		0.05		
Oscillator						

Oscillator Frequency Accuracy	f_{OSC}	R_{RT} = 32 kΩ	170	200	230	kHz
Oscillator Frequency Adjustable Range	f_{OSC_ADJ}		50		400	
Ramp Amplitude	ΔV_{OSC}	R_{RT} = 32 kΩ		1.9		V
Ramp Valley	V_{RV}		0.7	1.0		V
Maximum Duty Cycle		Every Phase	62	66	75	%
RT Pin Voltage	V_{RT}	R_{RT} = 32 kΩ	1.55	1.6	1.65	V
Reference and DAC						
DACOUT Voltage Accuracy	ΔV_{DAC}	$V_{DAC} \geq 1V$	-1		+1	%
		$V_{DAC} < 1V$	-10		+10	mV
DAC (VID0~VID125) Input Low		R_{RT} = 32 kΩ			0.4	V
DAC (VID0~VID125) Input High	V_{RV}		0.8			V
DAC (VID0~VID125) Bias Current	I_{BIAS_DAC}		25	50	75	uA
VOSS Pin Voltage	V_{VOSS}	R_{VOSS} = 100 kΩ	1.55	1.6	1.65	V
Error Amplifier						
Open Loop Gain				85		dB
Gain Bandwidth	GBW			10		MHz
Slew Rate	SR	COMP = 10 pF		3		V/uS
Maximum Voltage						V
Differential Sense Amplifier						
Input Impedance	Z_{IMP}			16		kΩ
Gain Bandwidth	GBW			10		MHz
Slew Rate	SR	COMP = 10 pF		3		V/uS
Differential Current Sense GM Amplifier						
ISP1, 2, 3, 4 Full Scale Source Current	I_{ISPFSS}		60			uA
ISP1, 2, 3, 4 Current for OCP	I_{ISPOCP}		90			uA

At Vcc=5V, Tj = 25 °C, unless otherwise specified

Protection						
SS Current	Iss	Vss = 1V	8	13	18	uA
Over Voltage Trip (V_{SENSE} / DACOUT)	ΔV_{OVT}		130	140	150	%
IMAX Voltage	V_{IMAX}	R_{IMAX} = 32 kΩ	1.55	1.6	1.65	V
Power Good						
Power Good Rising Threshold (V_{SENSE} / DACOUT)	V_{PG}	V_{SENSE} Rising		92		%
Power Good Low Voltage	V_{PGL}	I_{PG} = 4mA			0.2	V

Operating Conditions

At Tj = 25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Values			Unit
			Min.	Typ.	Max.	
Voltage supplied to 'VCC' pins	V_{VCC}		4.5	5.0	5.5	V
Ambient temperature	T_A		0		70	°C
Junction temperature	T_J		0		125	°C

VRD10.X VID Table

Pin Names								Pin Names						
VID125	VID4	VID3	VID2	VID1	VID0	Vcore		VID125	VID4	VID3	VID2	VID1	VID0	Vcore
0	0	1	0	1	0	0.8375		0	1	1	0	1	0	1.2125
1	0	1	0	0	1	0.8500		1	1	1	0	0	1	1.2250
0	0	1	0	0	1	0.8625		0	1	1	0	0	1	1.2375
1	0	1	0	0	0	0.8750		1	1	1	0	0	0	1.2500
0	0	1	0	0	0	0.8875		0	1	1	0	0	0	1.2625
1	0	0	1	1	1	0.9000		1	1	0	1	1	1	1.2750
0	0	0	1	1	1	0.9125		0	1	0	1	1	1	1.2875
1	0	0	1	1	0	0.9250		1	1	0	1	1	0	1.3000
0	0	0	1	1	0	0.9375		0	1	0	1	1	0	1.3125
1	0	0	1	0	1	0.9500		1	1	0	1	0	1	1.3250
0	0	0	1	0	1	0.9625		0	1	0	1	0	1	1.3375
1	0	0	1	0	0	0.9750		1	1	0	1	0	0	1,3500
0	0	0	1	0	0	0.9875		0	1	0	1	0	0	1.3625
1	0	0	0	1	1	1.0000		1	1	0	0	1	1	1.3750
0	0	0	0	1	1	1.0125		0	1	0	0	1	1	1.3875
1	0	0	0	1	0	1.0250		1	1	0	0	1	0	1.4000
0	0	0	0	1	0	1.0375		0	1	0	0	1	0	1.4125
1	0	0	0	0	1	1.0500		1	1	0	0	0	1	1.4250
0	0	0	0	0	1	1.0625		0	1	0	0	0	1	1.4375
1	0	0	0	0	0	1.0750		1	1	0	0	0	0	1.4500
0	0	0	0	0	0	1.0875		0	1	0	0	0	0	1.4625
1	1	1	1	1	1	OFF		1	0	1	1	1	1	1.4750
0	1	1	1	1	1	OFF		0	0	1	1	1	1	1.4875
1	1	1	1	1	0	1.1000		1	0	1	1	1	0	1.5000
0	1	1	1	1	0	1.1125		0	0	1	1	1	0	1.5125
1	1	1	1	0	1	1.1250		1	0	1	1	0	1	1.5250
0	1	1	1	0	1	1.1375		0	0	1	1	0	1	1.5375
1	1	1	1	0	0	1.1500		1	0	1	1	0	0	1.5500
0	1	1	1	0	0	1.1625		0	0	1	1	0	0	1.5625
1	1	1	0	1	1	1.1750		1	0	1	0	1	1	1.5750
0	1	1	0	1	1	1.1875		0	0	1	0	1	1	1.5875
1	1	1	0	1	0	1.2000		1	0	1	0	1	0	1.6000

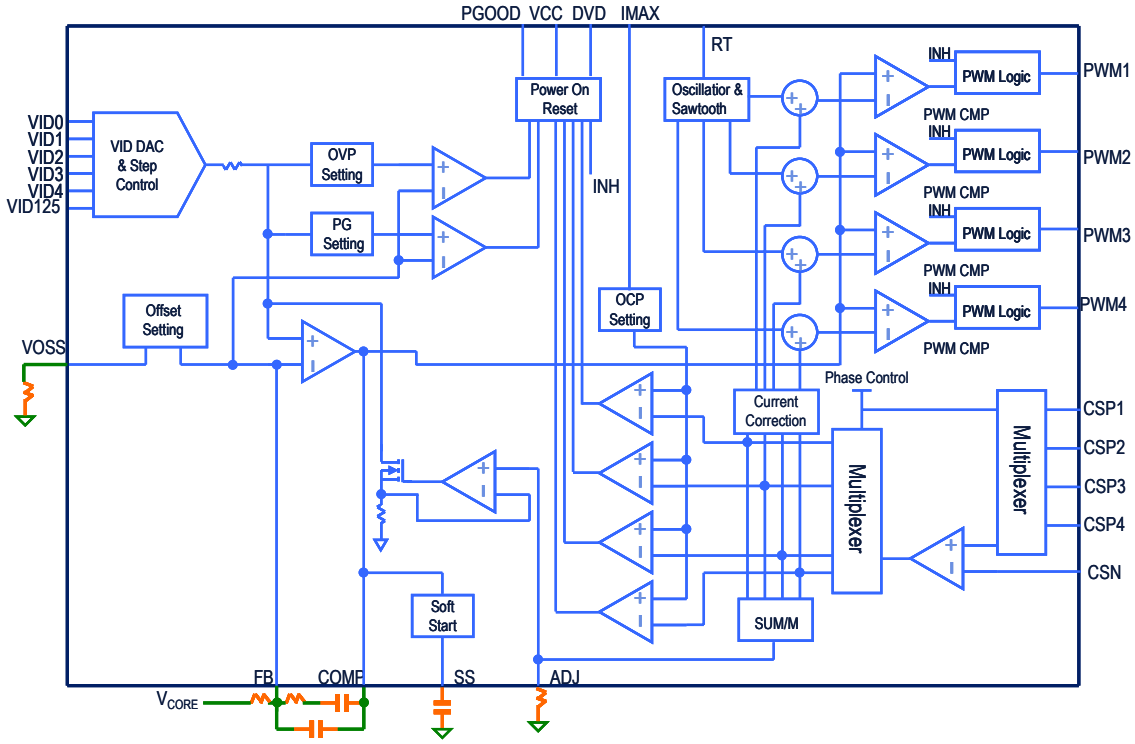
Note : “ 1 “ is open and “ 0 “ is connecting to ground.

Application Information :

TDA21301 is a multi-phase DC/DC controller that precisely regulates CPU core voltage and balances the current of different power channels. The converter consisting of TDA21301 and its companion CoreControl™ drivers, provides high quality CPU core power and all the protection functions to meet the requirement of the latest CPUs.

Voltage Control

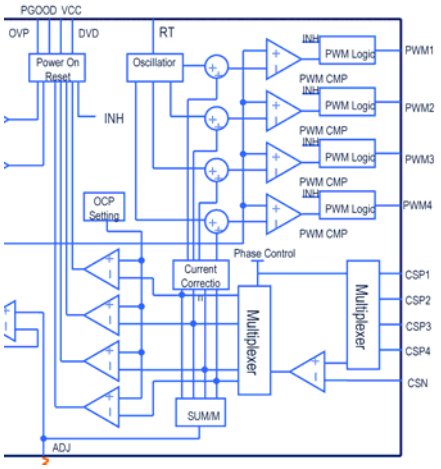
The TDA21301 senses the CPU V_{CORE} by SGND pin via a resistor connecting to Vss_sense pin of CPU and by FB pin via a resistor connecting to Vcc-sense of CPU to achieve the on-die voltage sense and to minimize the voltage drop on the PCB traces at heavy load condition. FB pin is also the input of the PGOOD & OVP sense. The internal highly accurate VID DAC provides the reference voltage for VRD10.X compliance. Control loop consists of an error amplifier, a pulse width modulator, external driver ICs and power elements. As a conventional voltage mode controller, the output voltage is locked at the V_{REF} of the error amplifier which is the output voltage of VID DAC plus setting offset and droop and the error signal is used as the control signal, Vc of the pulse width modulator. The PWM signals at different channels are generated by comparison of EA output and split-phase saw-tooth wave with additional current signal to achieve the balance current at each channel. Power stage transforms V_{IN} to output by PWM signal on-time ratio.



Current Balance

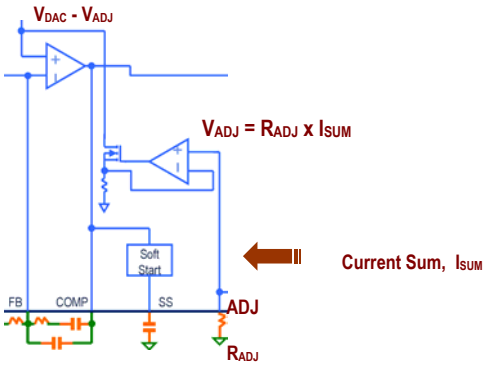
TDA21301 senses the inductor current directly via a RC network to emulate the voltage drop across the inductor's DCR in each phase when the synchronous MOSFETs are conducting for channel balance droop tuning and over current protection. The differential sensing GM amplifier converts the voltage accross the capacitor of the RC network which is qually the voltage drop at the inductor's DCR to current signal into internal current balance circuit. The current balance circuit sums and averages the current signals and then generates the balancing signals injected to pulse signal modulator. If some of the channel current is higher than average, the balancing signal shall decrease the pulse width at that channel to keep the current balance.

Single GM amplifier with time sharing technique has been used for reducing the offset errors and the linearity variation between different GM amplifiers. Thus with this technique it can greatly improve the accuracy of the sensed channel current with small voltage drop at the inductor's DCR.



Load Droop

The sensed channel current signals are summed. This summed current shall be sent to ADJ pin where there is a resistor connecting to ground. So the summed current and this resistor establish the droop voltage which is used to regulate the output of the DAC to form a output voltage droop proportional to the load current. The droop or so-called " Active Voltage Positioning " can reduce the output voltage ripple during the load transient and the size of the LC filters.



Fault Detection

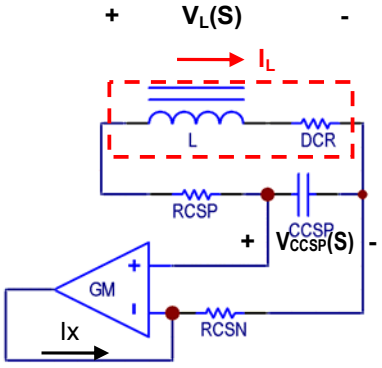
TDA21301 detects V_{CORE} for over voltage protection and power good signal indication. The " hiccup mode " operation of over-current and short circuit protection is adopted to reduce the short circuit current. The inrush current during the start up is suppressed by the soft start function which can be programmed by external capacitor at soft start pin through clamping the pulse width.

Phase Setting and Converter Start Up

The TDA21301 interfaces with companion CoreControl™ MOSFET drivers, TDA21106, TDA21107 (Single Channel) and TDA21102, TDA21103 (Dual Channel), for correct converter power sequence. The tri-state PWM outputs sense the interface voltage during IC POR period (both VCC and DVD trip). The channel is enabled if the voltage at the pin is 1.2V less than VCC. Tie the PWM outputs to VCC and the current sense pins to GND or leave them floating if the channel is unused. For 3 Phase application, connect PWM4 high.

Current Sensing Setting

TDA21301 senses the inductor current flowing through its DCR in each phase when synchronous MOSFETs are conducting for channel balance and droop tuning. The differential sensing GM amplifier converts the voltage accross the capacitor of the RC network which is qually the voltage drop at the inductor's DCR to current signal into internal current balance circuit.



$V_+ = V_{CCSP} = I_L \times DCR$, $V_- = I_X \times R_{CSN}$

Because $V_+ = V_-$ $\Rightarrow$ so, $I_X = \frac{I_L \times DCR}{R_{CSN}}$

Basic Theory

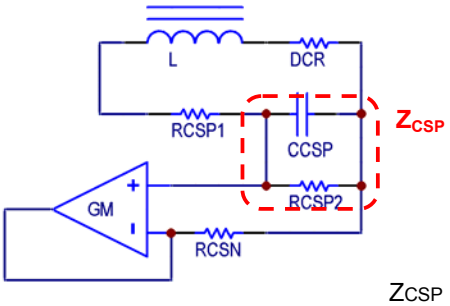
$$V_{CCSP}(s)=V_L(s)\times\frac{1/sC_{CSP}}{R_{CSP}+1/sC_{CSP}}=V_L(s)\times\frac{1}{sR_{CSP}C_{CSP}+1}=I_L(s)\times\frac{sL+DCR}{sR_{CSP}C_{CSP}+1}$$

We target to have $V_{CCSP}(s)=I_L(s)\times DCR$, then $I_L(s)\times DCR=I_L(s)\times\frac{sL+DCR}{sR_{CSP}C_{CSP}+1}$

so, $sR_{CSP}C_{CSP}+1=\frac{sL}{DCR}+1$

We can conclude now $V_{CCSP}(s)=I_L(s)\times DCR$ if $R_{CSP}C_{CSP}=\frac{L}{DCR}$

Proportional Current Setting



$$Z_{CSP} = \frac{R_{CSP2} \times \frac{1}{sC_{CSP}}}{R_{CSP2} + \frac{1}{sC_{CSP}}} = \frac{R_{CSP2}}{sR_{CSP2}C_{CSP} + 1}$$

$$V_{CCSP}(s) = V_L(s) \times \frac{Z_{CSP}}{R_{CSP1} + Z_{CSP}} = V_L(s) \times \frac{1}{\frac{R_{CSP1}}{Z_{CSP}} + 1}$$

$$= V_L(s) \times \frac{1}{\frac{R_{CSP1}}{\frac{R_{CSP2}}{sR_{CSP2}C_{CSP} + 1}} + 1} = V_L(s) \times \frac{1}{\frac{R_{CSP1}}{R_{CSP2}}(sR_{CSP2}C_{CSP} + 1) + 1}$$

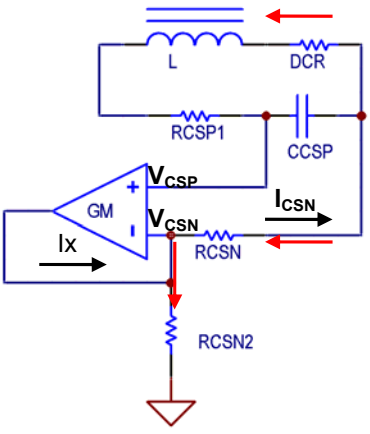
$$= V_L(s) \times \frac{R_{CSP2}}{sR_{CSP1}R_{CSP2}C_{CSP} + R_{CSP1} + R_{CSP2}} = I_L(s) \times \frac{(sL + DCR)R_{CSP2}}{sR_{CSP1}R_{CSP2}C_{CSP} + R_{CSP1} + R_{CSP2}}$$

$$= I_L(s) \times \frac{(sL + DCR)\frac{R_{CSP2}}{R_{CSP1} + R_{CSP2}}}{\frac{sR_{CSP1}R_{CSP2}C_{CSP}}{R_{CSP1} + R_{CSP2}} + 1}$$

$$If \ \frac{L}{DCR} = \frac{R_{CSP1}R_{CSP2}C_{CSP}}{R_{CSP1} + R_{CSP2}}, then \ V_{CCSP}(s) = I_L(s) \times DCR \times \frac{R_{CSP2}}{R_{CSP1} + R_{CSP2}}$$

With this technique, it is very easy to program the current ratio at each channel for achieving the current balance.

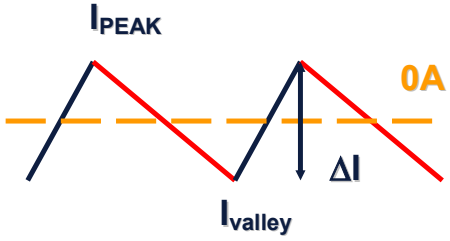
Voltage Hump Elimination



$$V_{CSP} = V_{CORE} + I_L \times DCR \text{ and } V_{CSN} = I_{CNS} \times R_{CSN} + V_{CORE}$$

$$\because V_{CSN} = V_{CSP}, \therefore I_{CNS} = \frac{I_L \times DCR}{R_{CSN}}$$

$$I_X = \frac{V_{CSN}}{R_{CSN2}} + \frac{I_L \times DCR}{R_{CSN}}$$



During the light load condition, the CoreControl converter is still working in the CCM but the valley of the inductor current is below 0A. This means that the inductor current is flowing from Vcore to PHASE and the voltage across on the C_{CSP} is reversed polarity. Now the GM amplifier should sink current but it is lack of the sinking current capability. A hump been observed on the load line at light load condition. In

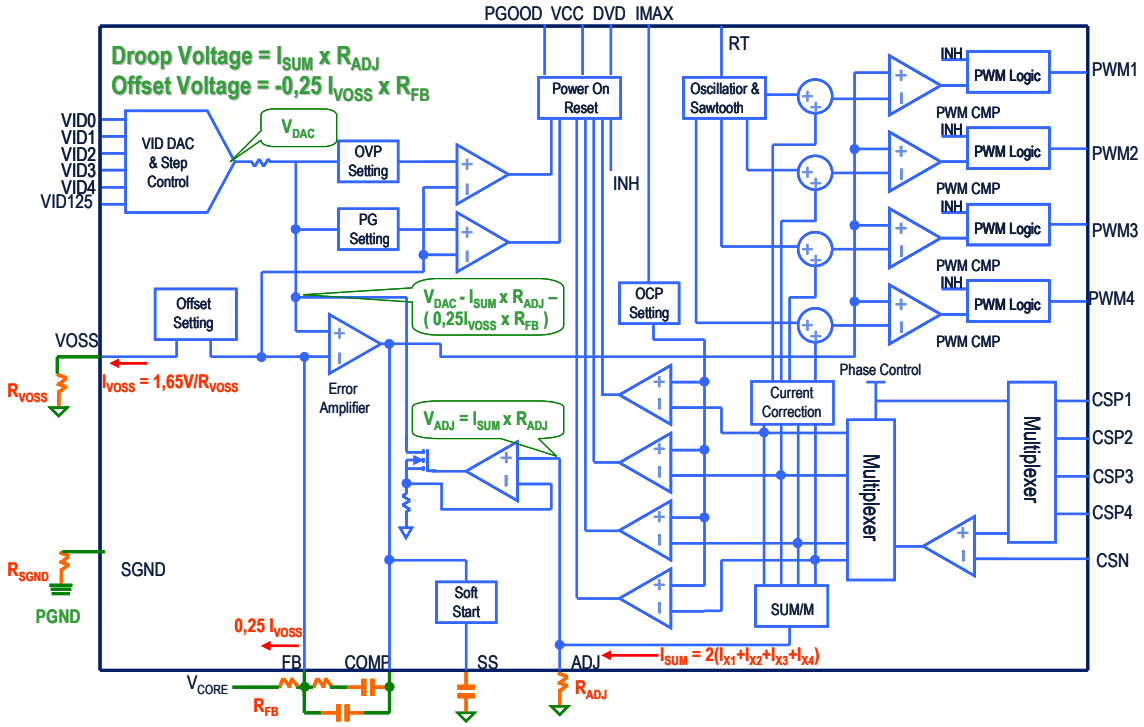
order to eliminate this hump, a resistor placed at CSN to GND has been introduced here. The value of this resistor can be calculated by the formula below.

$$\frac{V_{CSN}}{R_{CSN2}} \geq \frac{I_L \times DCR}{R_{CSN}} \Rightarrow R_{CSN2} \leq \frac{V_{CSN} \times R_{CSN}}{I_L \times DCR}$$

DAC Offset Voltage & Droop Setting

The DAC offset voltage is set by compensation network & external resistor at VOSS pin by $\frac{1.65V}{R_{VOSS}} \times \frac{R_{FB}}{4}$

The summed current signals from power channels are injected to ADJ pin to establish the droop voltage, $V_{ADJ}=R_{ADJ} \times \sum_{n=1}^{n=4} 2Ixn$. The DAC output voltage decreased by V_{ADJ} to generate the V_{CORE} load droop.

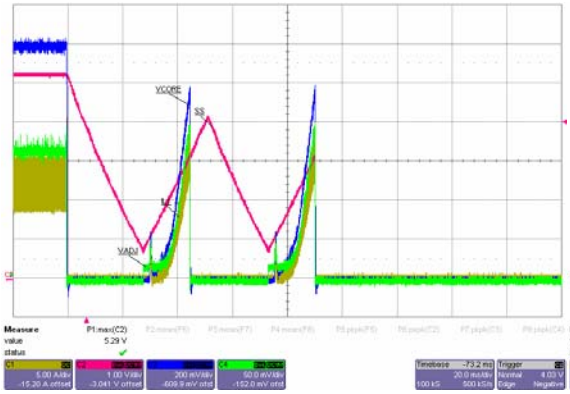


Protection and SS Function

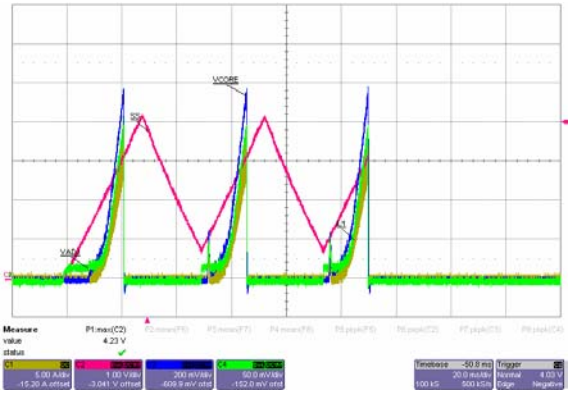
For OVP, the TDA21301 detects the V_{CORE} by FB pin voltage that is the inverting input of the error amplifier. This is to eliminate the delay caused by the compensation network for faster and more accurate detection. The trip point of OVP is 140% of the normal V_{CORE} voltage level. The PWM outputs are pulled low to turn on the Sync FET and to turn off the control FET while OVP is detected. The OVP latch can only be reset by either VCC or DVD. The PGOOD trip point is set at the 92% of the normal V_{CORE} voltage level. The open drain PGOOD pin shall be pulled low while V_{CORE} is lower than this trip point. During the VID on the fly condition, there is nothing able to change the status of the PGOOD.

Soft-start circuit generates a ramp by charging an external capacitor with a 13uA constant current source. This current source can start to charge the external soft start capacitor only when POR of IC and DVD reach their threshold and VIDs are set. The pulse width of PWM signal and V_{CORE} are clamped by rising ramp to reduce the inrush current and the stress on the power devices.

Over-current protection trip point is able to be programmed by an external resistor. OCP is triggered if one of the channels reaches this set current which is 1.6V / $0.5R_{IMAX}$. Controller forces PWM output latched at high impedance to turn off both control and Sync FETs in the power stage and initial the hiccup mode protection. The SS pin voltage is pulled low with a 13uA current after it is less than 90% VCC. The converter restarts after SS pin voltage is lower than 0.2V. Three times of OCP disable the converter and only release the latch by POR acts.



This is over current protection during operation



This is over current protection during startup

Design Process Suggestion :

Voltage Loop Setting

- Pole and Zero of output filter : Output inductor value, the capacitance and ESR value of the output capacitors
- Compensation Network : Error amplifier compensation & sawtooth wave amplitude.
- Kelvin sense for V_{CORE}

Current Loop Setting

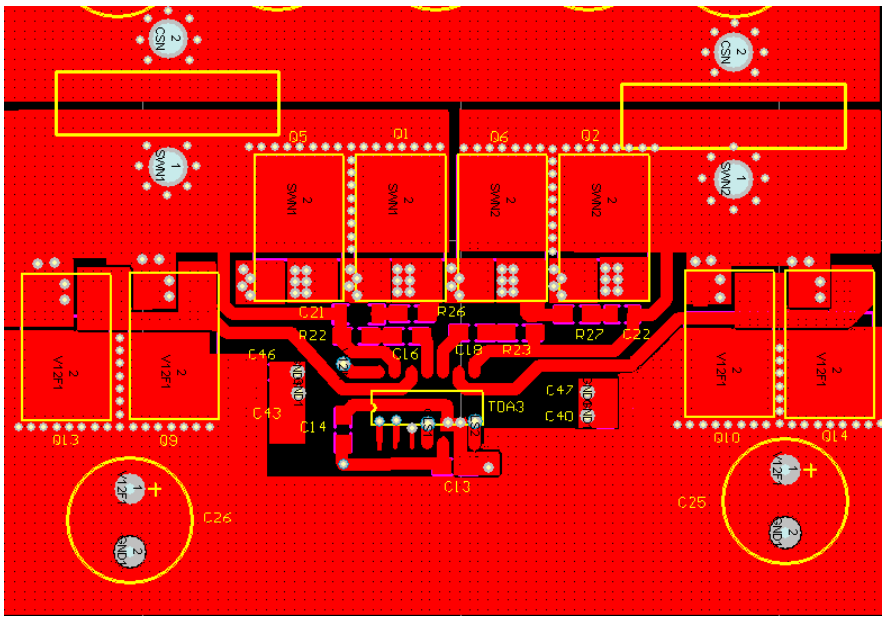
- GM amplifier current setting : Current sensing components (DCR of Inductors), the value of the resistors connecting to CSN. Do $Ix = \frac{I_L \times DCR}{R_{CSN}}$ < 60uA at full load condition for better load line linearity.
- Over current protection trip point : This can be programmed by external resistor at IMAX pin. $\frac{1}{2}\frac{1.6V}{R_{IMAX}} = \frac{1}{3}\frac{I_L \times DCR}{R_{CSN}}$

VRM Load Line Setting

- Droop amplitude : External ADJ pin resistor.
- Voltage hump elimination : $R_{CSN2} \le \frac{V_{CSN} \times R_{CSN}}{I_L \times DCR}$, I_L is the inductor valley current at no load and V_{CSN} is the VIDs setting voltage.
- DAC offset voltage seeting : VOSS pin external resistor programming the current source flowing through the feedback resistor to set the offset voltage & compensation network resistor.

$$V_{OFFSET} = 0.25 \times \frac{1.6V}{R_{VOSS}} \times R_{FB}$$

PCB Layout



Design Example :

Given

Apply for four phase converter

V_{IN} = 12V
V_{CORE} = 1.35V
I_{LOAD} = 100A
V_{DROOP} = 100 mV at full load
OCP set at 35A for each channel (S/H)
L_{OUT} = 0.6uH, DCR = 1.1 mΩ typical
C_{OUT} = 12.880 uH with 0.839 mΩ ESR (For bulk capacitors only)

1. Compensation Setting

- ***Modulator Gain, Pole and Zero :***

From the following formula ;

Modulator Gain = $\frac{V_{IN}}{V_{RAMP}} = \frac{12V}{1.9V \times \frac{3}{2}} = 4.2$ (12.46 dB)

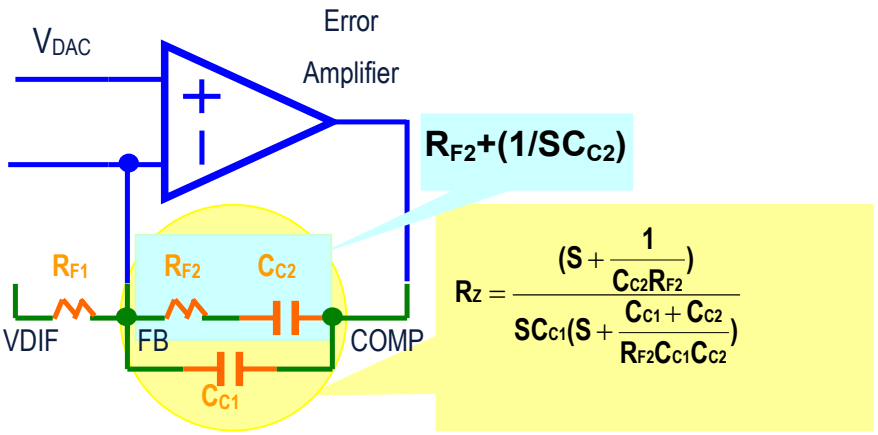
Where V_{RAMP} : ramp amplitude of the sawtooth waveform

LC Filter Pole = $\frac{1}{2\pi \times \sqrt{LC}}$ = 1.81 kHz and

ESR Zero = $\frac{1}{2\pi \times ESR \times C_{OUT}}$ = 14.73 kHz

- ***EA Compensation Network :***

Select R_{F1} = 3 kΩ, R_{F2} = 24 kΩ , C_{C2} = 10 nF, C_{C1} = 33 pF and Use type 2 compensation scheme shown in Figure 5.

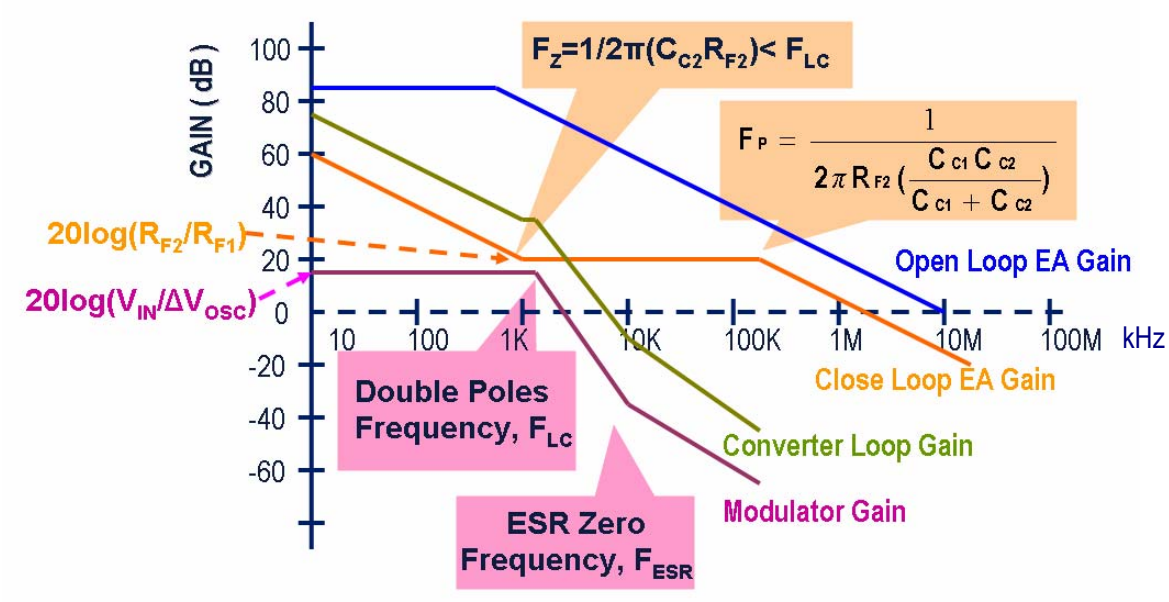


From the following formulas :

$$F_Z = \frac{1}{2\pi \times R_{F2} \times C_{C1}} = 633\ Hz\ ,\ F_P = \frac{1}{2\pi \times R_{F2} \times \frac{C_{C1} \times C_{C2}}{C_{C1}+C_{C2}}} = 321.5\ kHz$$

$$\text{Middle Band Gain} = \frac{R_{F2}}{R_{F1}} = 8\ \ (\ 18.06\ dB\ )$$

The asymptotic bode plot of EA compensation and PWM loop gain is shown as below.



2. Droop & DAC Offset Setting

For each channel the load current is 100A / 4 = 25A and DCR is 0.9 mΩ max at 25°C with temperature coefficient of copper is 3900 ppm/°C.

Assume that the copper temperature is 90°C at 100A output current. The DCR at 100A should be 0.9 mΩ x (1+ (90-25) x (3900 / 1000000)) = 1.12815 mΩ Max

Using the following formula to select the $I_{X(MAX)} \leq$ 90 uA for GM amplifier :

$$I_X = \frac{I_L \times DCR}{R_{CSN}}$$

Select R_{CSN} = 330Ω, then $I_{X(MAX)}$ would be 85.47 uA. V_{DROOP} = 100 mV = 85.47 uA X 2 X 4 X R_{ADJ}, therefore R_{ADJ} = 146.25 Ω. Select R_{ADJ} = 110Ω + 47Ω NTC resistor.

3. Over Current Protection Setting

OCP trip point is set by external resistor at IMAX pin. As above selected R_{CSN} 330 Ω, the OCP trip point is found using :

$$\frac{1}{2}\frac{1{,}6V}{R_{IMAX}} = \frac{1}{3}\frac{I_L \times DCR}{R_{CSN}} \Rightarrow R_{IMAX}=23.54k\Omega \text{ , so } 24k\Omega \text{ choosen}$$

4. Soft-start Capacitor Selection

C_{SS} = 100 nF is the suitable value for most application.

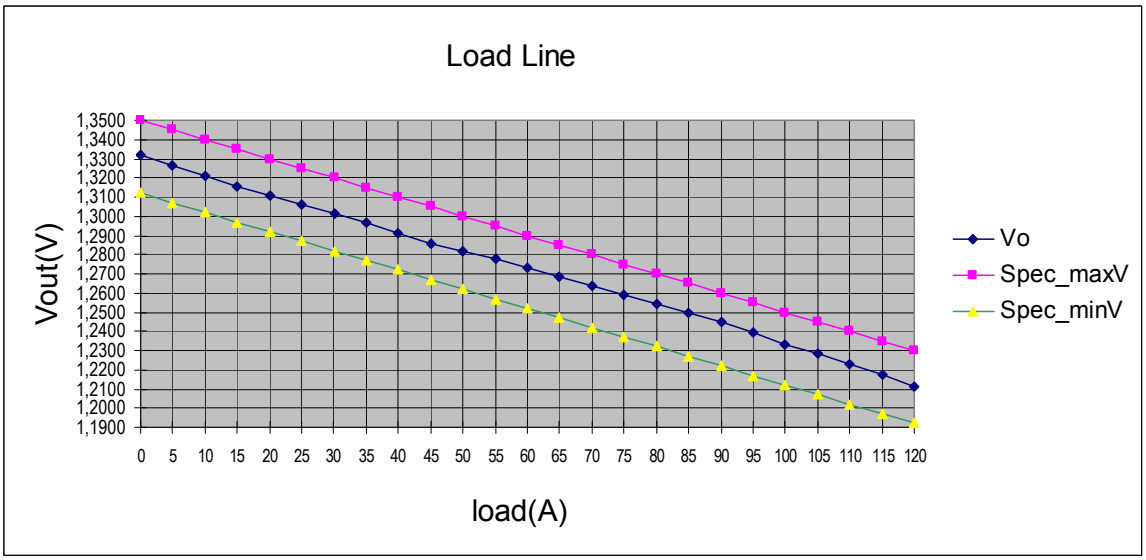
$$I_{SS} \times t_{SS} = V_{SS} \times C_{SS} \Rightarrow C_{SS} = \frac{I_{SS} \times t_{SS}}{V_{SS}}$$

I_{SS} = 13 uA , V_{SS} = 2V , t_{SS} = 10 mS

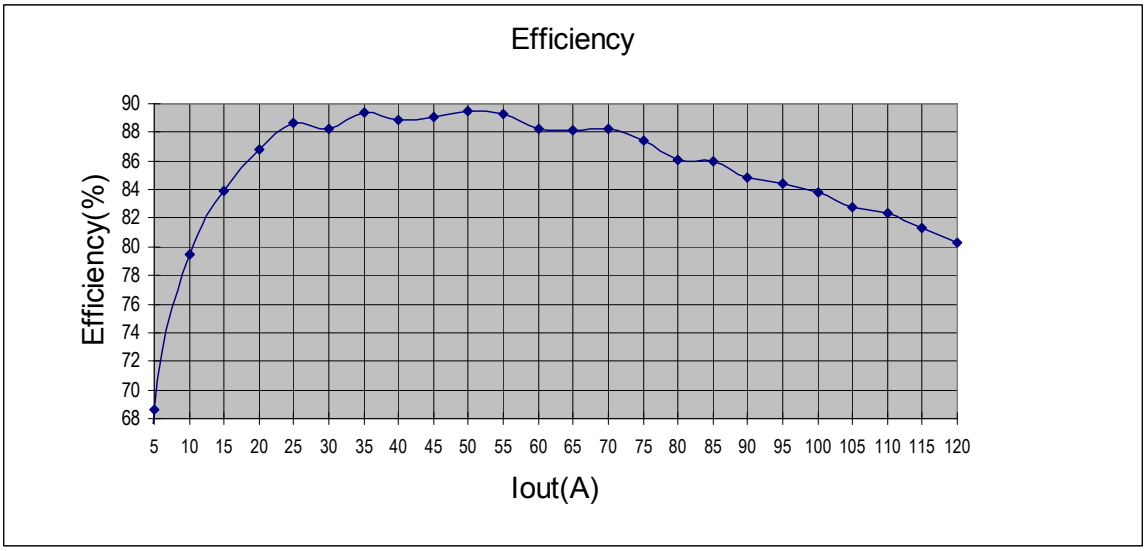
C_{SS} = 65 nF

Test Result

- ***Load Line***



- ***Efficiency (4 layer board, top and bottom layers : 1oz, inner layers : 0.5 oz)***



Layout Guide :

Place the high-power switching components first, and separate them from the sensitive nodes.

1. Switching Ripple Path :

- The best connection of the input capacitors is to place at the drain of the high side MOSFET and the source of the low side MOSFET.
- Low side MOSFET to the output capacitor.
- The return path of input and output capacitor.
- Separate the power and signal GND.
- The PHASE node, the conjunction of the high / low side MOSFETs and inductor, is the nosiy node. Keep them away from the sensitive small-signal node.
- Reducing the parasitic impedance and inductance is done by minimizing the length of the traces, offering enough copper area and avoiding the vias.

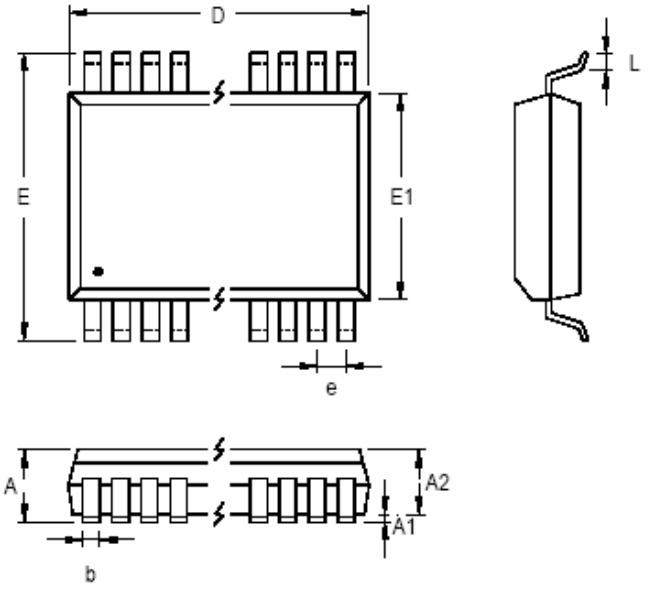
2. MOSFET drivers :

- Both of the decoupling capacitors for VCC and PVCC should be placed as close to the driver IC as possible.
- The bootstrap capacitor should be placed close to the **BOOT** pin.
- The traces of **$GATE_{HS}$** and **PHASE** should be routed in parallel and to keep it short and wide. The width of the trances should be no less than 40mils.
- High current loops from the input capacitor, high side MOSFET, output inductors and output capacitors back to the input capacitor negative terminal should be kept the distance minimized.
- The conjunction of high side MOSFET, low side MOSFET and output inductor should be kept as close as possible.

3. Other Path :

- The components from the compensation network, high frequency bypass capacitors and the setting resistors should be placed near controller IC and away from the noisy power path.
- The thermal compensation thermistor should be placed at the hottest point which is normally the MOSFETs located at the inner part of the power stage.

Outline Dimension :



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	---	1.20	---	0.047
A1	0.00	0.15	0.000	0.006
A2	0.79	1.05	0.031	0.041
b	0.18	0.30	0.007	0.012
D	9.60	9.80	0.378	0.386
e	0.65		0.026	
E	6.30	6.50	0.248	0.256
E1	4.29	4.50	0.169	0.177
L	0.45	0.76	0.018	0.030

28-Lead TSSOP Plastic Package

Revision History			
Datasheet DS-CoreControl-TDA21301			
Actual Release: V1.03 Date: 03.09.2004		Previous Release:V1.02	Date: 10.08.2004
Page of actual Rel.	Page of prev. Rel.	Subjects changed since last release	
3	3	Change " Frequency VS R_{RT} " diagram	
5	5	Change " Block Diagram ", Remove " OVP " and add " IMAX "	
11	11	Change " Block Diagram ", Remove " OVP " and add " IMAX "	
15	15	Change " Offset Diagram ", Remove " OVP " and add " IMAX "	

For questions on technology, delivery and prices please contact the Infineon Technologies Offices in Germany or the Infineon Technologies Companies and Representatives worldwide: see the address list on the last page or our webpage at

http://www.infineon.com/DCDC

CoreControl™, OptiMOS™ and **OptiMOS II™** are trademarks of Infineon Technologies AG.

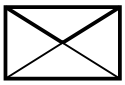
We listen to Your Comments

Any information within this dokument that you feel is wrong, unclear or missing at all?

Your feedback will help us to continously improve the quality of this dokument.

Please send your proposal (including a reference to this dokument) to:

mcdoku.comment@infineon.com



Edition 2004-09-03

Published by Infineon Technologies AG,
St.-Martin-Strasse 53,
D-81541 München

Attention please!

The information herein is given to describe certain components and shall not be considered as warranted characteristics.

Terms of delivery and rights to technical change reserved.

We hereby disclaim any and all warranties, including but not limited to warranties of non-infringement, regarding circuits, descriptions and charts stated herein.

Infineon Technologies is an approved CECC manufacturer.

Information

For further information on technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies Office in Germany or our Infineon Technologies Representatives worldwide (see address list).

Warnings

Due to technical requirements components may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies Office.

Infineon Technologies Components may only be used in life-support devices or systems with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system, or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body, or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.

Infineon Technologies AG sales offices worldwide – partly represented by Siemens AG

A
Siemens AG Österreich
Erdberger Lände 26
A-1031 Wien
T (+43)1-17 07-3 56 11
Fax (+43)1-17 07-5 59 73
AUS
Siemens Ltd.
885 Mountain Highway
Bayswater,Victoria 3153
T (+61)3-97 21 21 11
Fax (+61)3-97 21 72 75
B
Siemens Electronic Components
Benelux
Charleroisesteenweg 116/
Chaussée de Charleroi 116
B-1060 Brussel/Bruxelles
T (+32)2-5 36 69 05
Fax (+32)2-5 36 28 57
Email:components@siemens.nl
BR
Siemens Ltda.
Semiconductores
Avenida Mutinga,3800-Pirituba
05110-901 São Paulo-SP
T (+55)11-39 08 25 64
Fax (+55)11-39 08 27 28
CDN
Infineon Technologies Corporation
320 March Road,Suite 604
Canada,Ontario K2K 2E2
T (+1)6 13-5 91 63 86
Fax (+1)6 13-5 91 63 89
CH
Siemens Schweiz AG
Bauelemente
Freilagerstrasse 40
CH-8047 Zürich
T (+41)1-4 953065
Fax (+41)1-4 955050
D
Infineon Technologies AG
Völklinger Str.2
D-40219 Düsseldorf
T (+49)2 11-3 99 29 30
Fax (+49)2 11-3 99 14 81
Infineon Technologies AG
Werner-von-Siemens-Platz 1
D-30880 Laatzen (Hannover)
T (+49)5 11-8 77 22 22
Fax (+49)5 11-8 77 15 20
Infineon Technologies AG
Von-der-Tann-Straße 30
D-90439 Nürnberg
T (+49)9 11-6 54 76 99
Fax (+49)9 11-6 54 76 24
Infineon Technologies AG
Weissacher Straße 11
D-70499 Stuttgart
T (+49)7 11-1 37 33 14
Fax (+49)7 11-1 37 24 48
D
Infineon Technologies AG
Halbleiter Distribution
Richard-Strauss-Straße 76
D-81679 München
T (+49)89-92 21 40 86
Fax (+49)89-92 21 20 71
DK
Siemens A/S
Borupvang 3
DK-2750 Ballerup
T (+45)44 77-44 77
Fax (+45)44 77-40 17
E
Siemens S.A.
Dpto.Componentes
Ronda de Europa,5
E-28760 Tres Cantos-Madrid
T (+34)91-5 14 71 51
Fax (+34)91-5 14 70 13

F
Infineon Technologies France,
39/47,Bd.Ornano
F-93527 Saint-Denis CEDEX2
T (+33)1-49 22 31 00
Fax (+33)1-49 22 28 01
FIN
Siemens Components
Scandinavia
P.O .Bo x 6 0
FIN-02601 Espoo (Helsinki)
T (+3 58)10-5 11 51 51
Fax (+3 58)10-5 11 24 95
Email:
scs@components.siemens.se
GB
Infineon Technologies
Siemens House
Oldbury
GB-Bracknell,Berkshire
RG12 8FZ
T (+44)13 44-39 66 18
Fax (+44)13 44-39 66 32
H
Simacomp Kft.
Lajos u.103
H-1036 Budapest
T (+36)1-4 57 16 90
Fax (+36)1-4 57 16 92
HK
Infineon Technologies
Hong Kong Ltd.
Suite 302,Level 3,
Festival Walk,
80 Tat Chee Avenue,
Yam Yat Tsuen,
Kowloon Tong
Hong Kong
T (+8 52)28 32 05 00
Fax (+8 52)28 27 97 62
I
Siemens S..A.
Semiconductor Sales
Via Piero e Alberto Pirelli,10
I-20126 Milano
T (+39)02-66 76 -1
Fax (+39)02-66 76 43 95
IND
Siemens Ltd.
Components Division
No.84 Keonics Electronic City
Hosur Road
Bangalore 561 229
T (+91)80-8 52 11 22
Fax (+91)80-8 52 11 80
Siemens Ltd.
CMP Div,5th Floor
4A Ring Road,IP Estate
New Delhi 110 002
T (+91)11-3 31 99 12
Fax (+91)11-3 31 96 04
Siemens Ltd.
CMP Div,4th Floor
130,Pandurang Budhkar Marg,
Worli
Mumbai 400 018
T (+91)22-4 96 21 99
Fax (+91)22-4 96 22 01
IRL
Siemens Ltd.
Electronic Components Division
8,Raglan Road
IRL-Dublin 4
T (+3 53)1-2 16 23 42
Fax (+3 53)1-2 16 23 49
IL
Nisko Ltd.
2A,Habarzel St.
P.O.Box 58151
61580 Tel Aviv –Isreal
T (+9 72)3 -7 65 73 00
Fax (+9 72)3 -7 65 73 33

J
Siemens Components K.K.
Talanawa Park Tower 12F &17F
3-20-14,Higashi-Gotanda,
Shinagawa-ku
Tokyo
T (+81)3-54 49 64 11
Fax (+81)3 -54 49 64 01
MAL
Infineon Technologies AG
Sdn Bhd
Bayan Lepas Free Industrial Zone1
11900 Penang
T (+60)4 -6 44 99 75
Fax (+60)4 -6 41 48 72
N
Siemens Components
Scandinavia
Østre Aker vei 24
Postboks 10,Veitvet
N-0518 Oslo
T (+47)22-63 30 00
Fax (+47)22-68 49 13
Email:
scs@components.siemens.se
NL
Siemens Electronic Components
Benelux
Postbus 16068
NL-2500 BB Den Haag
T (+31)70-3 33 20 65
Fax (+31)70-3 33 28 15
Email:components@siemens.nl
NZ
Siemens Auckland
300 Great South Road
Greenland
Auckland
T (+64)9-5 20 30 33
Fax (+64)9-5 20 15 56
P
Siemens S.A.
an Componentes Electronicos
R.Irmaos Siemens,1
Alfragide
P-2720-093 Amadora
T (+351)1-4 17 85 90
Fax (+351)1-4 17 80 83
PK
Siemens Pakistan Engineering
Co.Ltd.
PO Box 1129,Islamabad 44000
23 West Jinnah Ave
Islamabad
T (+92)51-21 22 00
Fax (+92)51-21 16 10
PL
Siemens SP.z.o.o.
ul.Zupnicza 11
PL-03-821 Warszawa
T (+48)22-8 70 91 50
Fax (+48)22-8 70 91 59
ROK
Siemens Ltd.
Asia Tower,10th Floor
726 Yeoksam-dong,Kang-nam Ku
CPO Box 3001
Seoul 135-080
T (+82)2-5 27 77 00
Fax (+82)2-5 27 77 79
RUS
INTECH electronics
ul.Smolnaya,24/1203
RUS-125 445 Moskva
T (+7)0 95 -4 51 97 37
Fax (+7)0 95 -4 51 86 08
S
Siemens Components Scandinavia
Österögatan 1,Box 46
S-164 93 Kista
T (+46)8-7 03 35 00
Fax (+46)8-7 03 35 01
Email:
scs@components.siemens.se

ROC
Infineon Technologies
Taiwan.Ltd.
12F-1, No.3-2 Yuan Qu. St., Nan Kang Software Park, Taipei, 115
T (+8 86)2-2655 7500
Fax (+8 86)2-2655 7501
SGP
Infineon Technologies Asia
Pacific,Pte.Ltd.
168 Kallang Way
Singapore 349 253
T (+65)8 40 06 10
Fax (+65)7 42 62 39
USA
Infineon Technologies Corporation
1730 North First Street
San Jose,CA 95112
T (+1)4 08-5 01 60 00
Fax (+1)4 08-5 01 24 24
Siemens Components,Inc.
Optoelectronics Division
19000 Homestead Road
Cupertino,CA 95014
T (+1)4 08-2 57 79 10
Fax (+1)4 08-7 25 34 39
Siemens Components,Inc.
Special Products Division
186 Wood Avenue South
Iselin,NJ 08830-2770
T (+1)7 32-9 06 43 00
Fax (+1)7 32-6 32 28 30
VRC
Infineon Technologies
Hong Kong Ltd.
Beijing Office
Room 2106,Building A
Vantone New World Plaza
No.2 Fu Cheng Men Wai Da Jie
Jie
100037 Beijing
T (+86)10 -68 57 90 -06,-07
Fax (+86)10 -68 57 90 08
Infineon Technologies
Hong Kong Ltd.
Chengdu Office
Room14J1,Jinyang Mansion
58 Tidu Street
Chengdu,
Sichuan Province 610 016
T (+86)28-6 61 54 46 /79 51
Fax (+86)28 -6 61 01 59
Infineon Technologies
Hong Kong Ltd.
Shanghai Office
Room1101,Lucky Target Square
No.500 Chengdu Road North
Shanghai 200003
T (+86)21-63 6126 18 /19
Fax (+86)21-63 61 11 67
Infineon Technologies
Hong Kong Ltd.
Shenzhen Office
Room 1502,Block A
Tian An International Building
Renim South Road
Shenzhen 518 005
T (+86)7 55 -2 28 91 04
Fax (+86)7 55-2 28 02 17
ZA
Siemens Ltd.
Components Division
P.O.B.3438
Halfway House 1685
T (+27)11-6 52 -27 02
Fax (+27)11-6 52 20 42

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

- View TDA21301 on WIN SOURCE
- Infineon Technologies Information

Optimize Your Supply Chain with WIN SOURCE Solutions

- Global Sourcing Solution
- Obsolete Management
- Cost Control Management
- Shortage Management
- Alternative Solution
- Excess Inventory Management