THE DATASHEET OF

TPS61045ADRBT

TPS61045 Digitally Adjustable Boost Converter

1 Features

- Input Voltage Range from 1.8 to 6 V
- Output Voltage of up to 28 V Possible
- Up to 85% Efficiency
- Digitally Adjustable Output Voltage Control
- Disconnects Output From Input During Shutdown
- Switching Frequency up to 1 MHz
- No Load Quiescent Current 40 µA Typical
- Thermal Shutdown Mode
- Shutdown Current 0.1 µA Typical
- Available in Small 3-mm × 3-mm VSON Package

2 Applications

- LCD Bias Supply for Small to Medium LCD Displays
- OLED Display Power Supply
  - PDA, Pocket PC, Smart Phones
  - Handheld Devices
  - Cellular Phones

3 Description

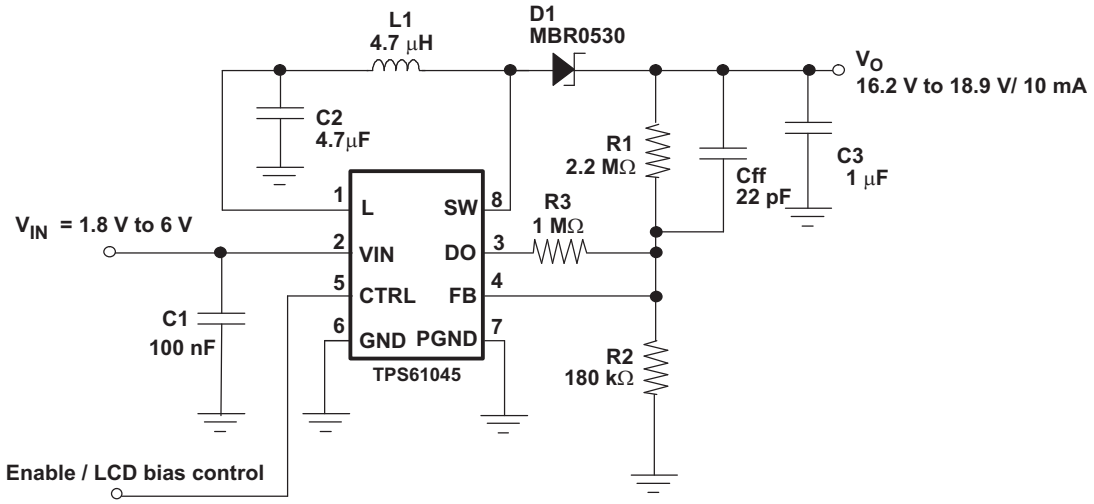
The TPS61045 device is a high-frequency boost converter with digitally-programmable output voltage and true shutdown. During shutdown, the output is disconnected from the input by opening the internal input switch. This allows a controlled power-up and power-down sequencing of the display. The output voltage can be increased or decreased in digital steps by applying a logic signal to the CTRL pin. The output voltage range, as well as the output voltage step size, can be programmed with the feedback divider network. With a high switching frequency of up to 1 MHz, the TPS61045 device allows the use of small external components, and together, with the small 8-pin VSON package, a minimum system solution size is achieved.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS61045	VSON (8)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



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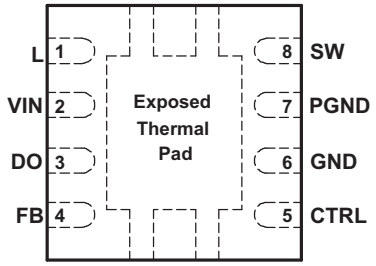
4 Revision History

Changes from Revision B (March 2009) to Revision C **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Updated Equation 10 ... 12
- Updated Equation 11 ... 13

5 Pin Configuration and Functions

DRB PACKAGE
(TOP VIEW)



(1) The exposed thermal pad is connected to PGND. Connect this pad directly with the GND pin.

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
CTRL	5	I	Combined enable and digital output voltage programming pin. Pulling CTRL constantly high enables the device. When CTRL is pulled to GND, the device is disabled and the input is disconnected from the output by opening the integrated switch Q1. Pulsing CTRL low increases or decreases the output voltage. Refer to *Application and Implementation* for further information.
DO	3	O	Internal DAC output. DO programs the output voltage through the CTRL pin. Refer to *Application and Implementation* for further information.
FB	4	I	Feedback. FB must be connected to the output voltage-feedback divider.
GND	6	—	Analog ground. GND must be directly connected to the PGND pin. Refer to *Application and Implementation* for further information.
L	1	O	Drain of the internal input switch (Q1). Connect L to the inductor.
PGND	7	—	Power ground
SW	8	I	Drain of the integrated main switch Q2. SW is connected to the inductor and anode of the Schottky rectifier diode.
VIN	2	I	Input supply pin

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage	V_{VIN} (2)	–0.3	7	V
Voltage	V_{CTRL}, $V_{(FB)}$, V_L, V_{DO} (2)	–0.3	V_{IN} + 0.3	V
Voltage	V_{SW} (2)	30		V
	Continuous power dissipation	See *Dissipation Rating*		
T_J	Operating junction temperature	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground pin.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±1500	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	TYP	MAX	UNIT
V_{VIN}	Input voltage range	1.8		6	V
V_{SW}	Switch voltage			30	V
L	Inductor (1)		4.7		µH
f	Switching frequency(1)			1	MHz
$C_{I(C2)}$	Input capacitor (C2) (1)		4.7		µF
$C_{O(C3)}$	Output capacitor (C3) (1)		1		µF
T_A	Operating ambient temperature	–40		85	°C
T_J	Operating junction temperature	–40		125	°C

(1) See application section for further information.

6.4 Thermal Information

over operating free-air temperature range (unless otherwise noted)

THERMAL METRIC(1)		TPS61045 VSON (8 PINS)	UNIT
$R_{\Theta JA}$ (2)	Junction-to-ambient thermal resistance	270	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) Standard 2-layer PCB without vias for the thermal pad. See the application section on how to improve the thermal resistance $R_{\Theta JA}$.

6.5 Dissipation Rating

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
8-pin VSON (DRB) (1)	370 mW	3.7 mW/°C	204 mW	148 mW

(1) See *Thermal Information* for the junction-to-ambient thermal resistance.

6.6 Electrical Characteristics

V_{IN} = 2.4 V, CTRL = V_{IN}, V_O = 18 V, I_O = 10 mA, T_A = –40°C to 85°C, typical values are at T_A = 25° C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
V_{IN}	Input voltage range		1.8		6	V
I_Q	Operating quiescent current	I_O = 0 mA, not switching		40	65	µA
$I_{O(SD)}$	Shutdown current	CTRL = GND		0.1	1	µA
UVLO	Undervoltage lockout (UVLO) threshold	V_{IN} falling		1.5	1.7	V
CTRL AND DAC OUTPUT						
V_{IH}	CTRL high-level input voltage		1.3			V
V_{IL}	CTRL low-level input voltage				0.3	V
I_{lkg}	CTRL input leakage current	CTRL = GND or V_{IN}			0.1	µA
$V_{O(DO)}$	DAC output voltage range		0		1.233	V
	DAC resolution	6 bit		19.6		mV
$V_{O(DO)}$	DAC center output voltage	CTRL = high		607		mV
$I_{O(SINK)}$	Maximum DAC sink current				30	µA
t_{UP}	Increase output voltage one step	CTRL = High to low to high	1		60	µs
t_{DWN}	Decrease the output voltage one step	CTRL = High to low to high	140		240	µs
t_{d1}	Delay time between up and down steps	CTRL = Low to high to low	1			µs
t_{OFF}	Shutdown	CTRL = High to low to high	560			µs
INPUT SWITCH (Q1), MAIN SWITCH (Q2), AND CURRENT LIMIT						
$V_{SW(Q2)}$	Main switch maximum voltage (Q2)				30	V
$r_{DS(on)}$	Main switch MOSFET on-resistance	V_{IN} = 2.4 V; I_S = 200 mA		400	800	mΩ
I_{lkg}	Main switch MOSFET leakage current	V_S = 28 V		0.1	10	µA
I_{LIM}	Main switch MOSFET current limit		300	375	450	mA
$r_{DS(on)}$	Input switch MOSFET on-resistance	V_{IN} = 2.4 V; I_S = 200 mA		1	2	Ω
I_{lkg}	Input switch MOSFET leakage current	V_L = GND, V_{IN} = 6 V		0.1	10	µA
OUTPUT						
V_O	Output voltage range		V_{IN}		28	V
V_{ref}	Internal voltage reference			1.233		V
I_{FB}	Feedback input bias current	$V_{(FB)}$ = 1.3 V		30	100	nA
V_{FB}	Feedback trip point voltage	1.8 V ≤ V_{IN} ≤ 6 V; V_O = 18 V, I_{LOAD} = 10 mA	1.208	1.233	1.258	V
	Feedback trip point voltage	1.8 V ≤ V_{IN}≤ 3.6 V; V_O = 18 V, I_{LOAD} = 10 mA , T_A = 0°C to 85°C	1.214	1.233	1.251	V

6.7 Typical Characteristics

Table 1. Table of Graphs

Graph Title		Figure
η	Efficiency vs Load Current	Figure 1
	Efficiency vs Input Voltage	Figure 2
$I_{DD(Q)}$	Quiescent Current vs Input Voltage	Figure 3
V_{FB}	Feedback Voltage vs Temperature	Figure 4
I_{FB}	Feedback Current vs Temperature	Figure 5
$r_{DS(on)}$	$r_{DS(on)}$ Main Switch Q2 vs Temperature	Figure 6
	$r_{DS(on)}$ Main Switch Q2 vs Input Voltage	Figure 7
	$r_{DS(on)}$ Input Switch Q1 vs Temperature	Figure 8
	$r_{DS(on)}$ Input Switch Q1 vs Input Voltage	Figure 9
V_{DO}	V_{DO} Voltage vs CTRL Input Step	Figure 10
	Line Transient Response	Figure 13
	Load Transient Response	Figure 14
	PFM Operation	Figure 15
	Softstart	Figure 16

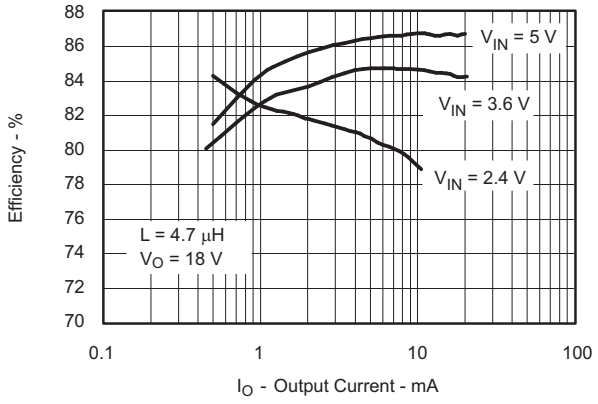


Figure 1. Efficiency vs Load Current

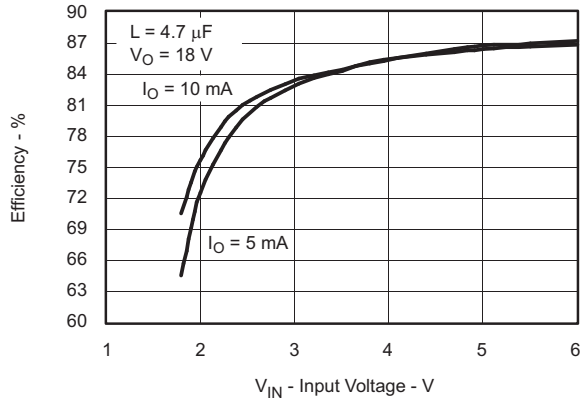


Figure 2. Efficiency vs Input Voltage

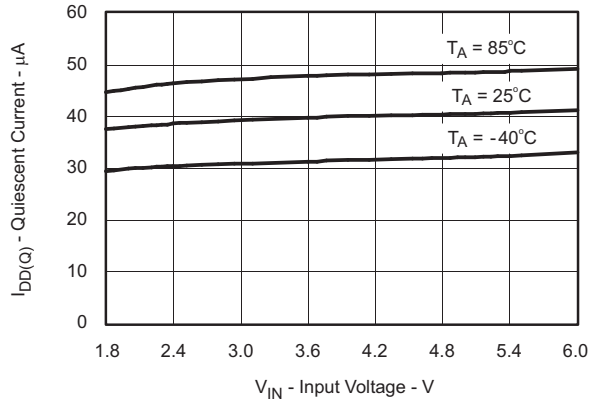


Figure 3. Quiescent Current vs Input Voltage

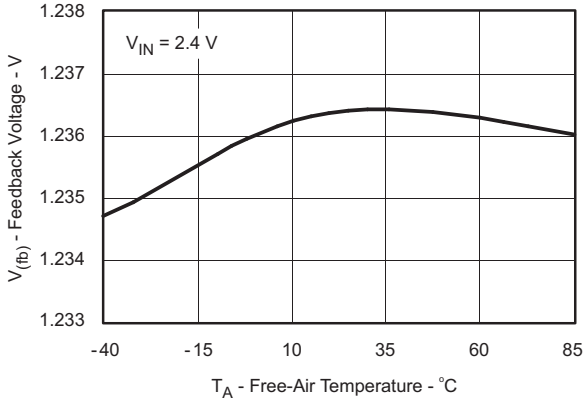


Figure 4. Feedback Voltage vs Temperature

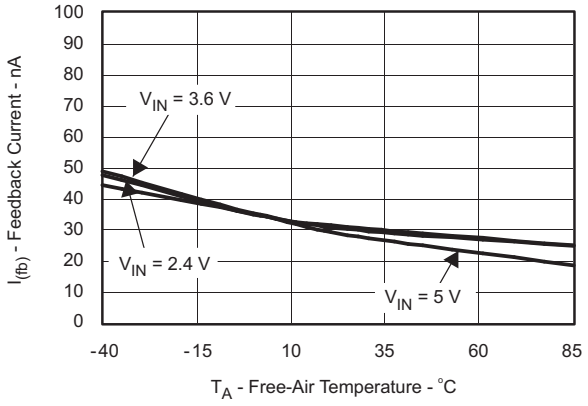


Figure 5. Feedback Current vs Temperature

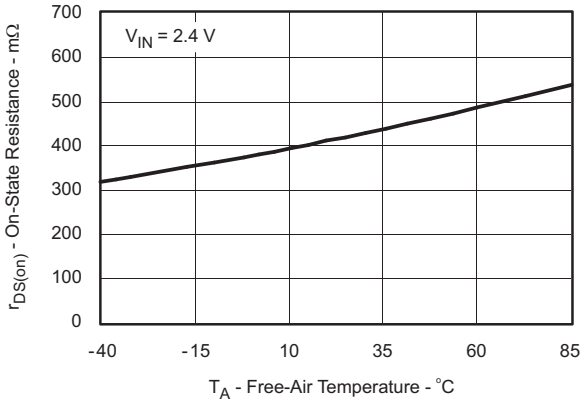


Figure 6. $r_{DS(on)}$ Main Switch Q2 vs Temperature

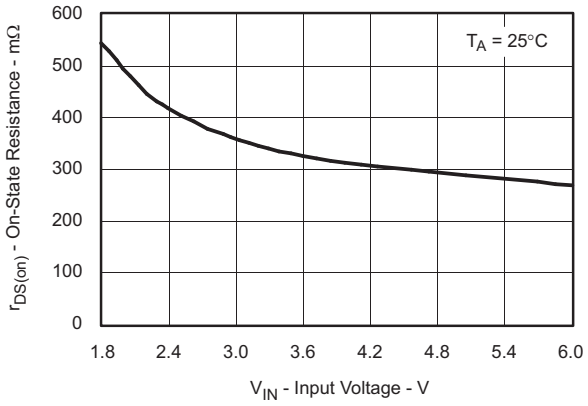


Figure 7. $r_{DS(on)}$ Main Switch Q2 vs Input Voltage

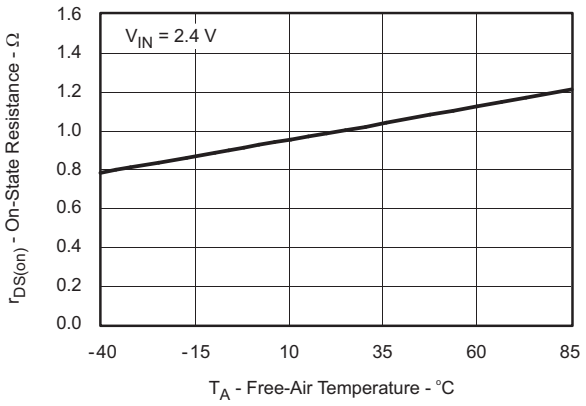


Figure 8. $r_{DS(on)}$ Input Switch Q1 vs Temperature

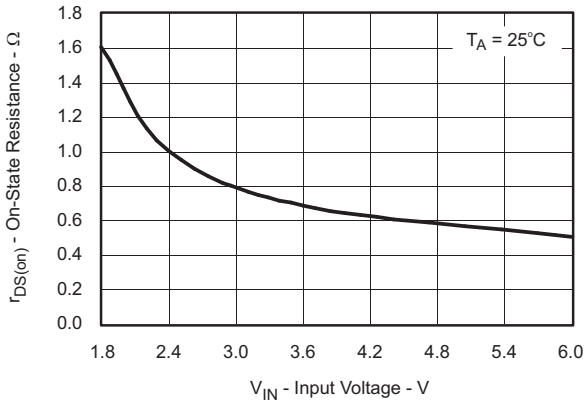


Figure 9. $r_{DS(on)}$ Input Switch Q1 vs Input Voltage

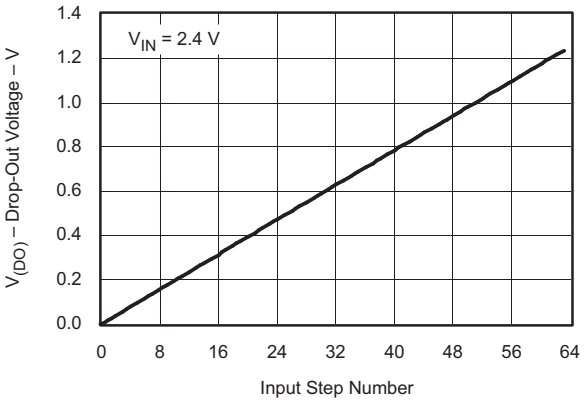


Figure 10. $V_{(DO)}$ Voltage vs CTRL Input Step

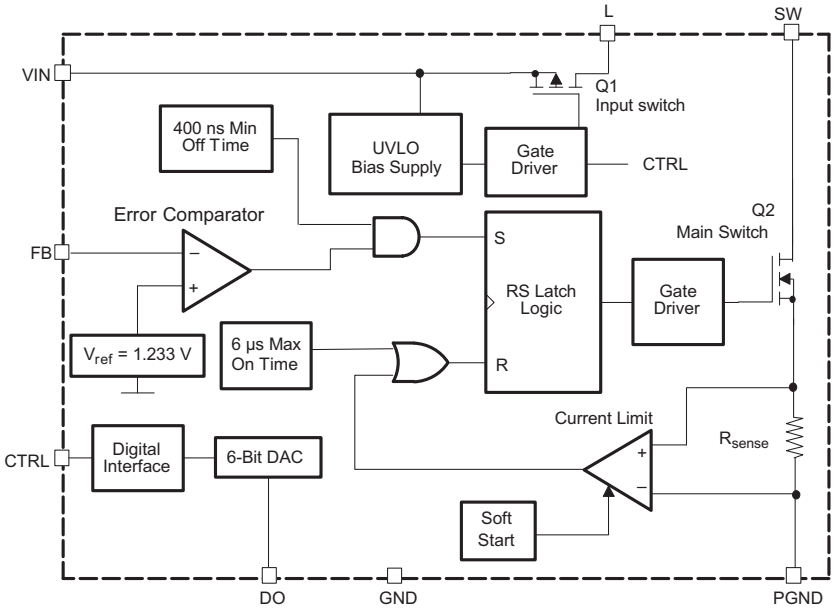
7 Detailed Description

7.1 Overview

The TPS61045 device operates with an input voltage range of 1.8 to 6 V and generates output voltages up to 28 V. The device operates in a pulse frequency modulation (PFM) scheme with constant peak current control. This control scheme maintains high efficiency over the entire load current range, and with a switching frequency of up to 1 MHz, the device enables the use of small external components.

The converter monitors the output voltage. When the feedback voltage falls below the reference voltage of 1.233 V (typical), the main switch turns on and the current ramps up. The main switch turns off when the inductor current reaches the internally set peak current of 375 mA (typical). See *Peak Current Control* for more information. The second criteria that turns off the main switch is the maximum on-time of 6 µs (typical). This limits the maximum on-time of the converter in extreme conditions. As the switch is turned off, the external Schottky diode is forward biased delivering the current to the output. The main switch remains off until the minimum off time of 400 ns (typical) has passed and the feedback voltage is below the reference voltage again. Using this PFM peak current control scheme, the converter operates in discontinuous conduction mode (DCM) where the switching frequency depends on the input voltage, output voltage, and output current. This gives a high efficiency over the entire load current range. This regulation scheme is inherently stable, which allows a wider range for the selection of the inductor and output capacitor.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Peak Current Control

The internal switch is turned on until the inductor current reaches the typical dc current limit (I_{LIM}) of 375 mA. Due to the internal current limit delay of 100 ns (typical), the actual current exceeds the dc current limit threshold by a small amount. The typical peak current limit can be calculated:

$$I_{P(typ)} = I_{(LIM)} + \frac{V_{IN}}{L} \times 100\ ns \quad (1)$$

$$I_{P(typ)} = 375\ mA + \frac{V_{IN}}{L} \times 100\ ns \quad (2)$$

The higher the input voltage and the lower the inductor value, the greater the current limit overshoot.

Feature Description (continued)

7.3.2 Softstart

If no special precautions are taken, all inductive step-up converters exhibit high inrush current during start up. This can cause voltage drops at the input rail during start-up, which may result in an unwanted or premature system shutdown.

When the device is enabled, the internal input switch (Q1) is slowly turned on to reduce the inrush current charging the capacitor (C2) connected to pin L. Furthermore, the TPS61045 device limits this inrush current during start-up by increasing the current limit in two steps starting from I_{LIM} / 4 for 256 switch cycles to I_{LIM} / 2 for the next 256 switch cycles.

7.3.3 Enable (CTRL Pin)

The CTRL pin serves two functions. One function is the enable and disable of the device. The other function is the output voltage programming of the device. If the digital interface is not required, the CTRL pin is used as a standard enable pin for the device.

Pulling the CTRL pin high enables the device beginning with the softstart cycle.

Pulling the CTRL pin to ground for a period of ≥560 µs shuts down the device, reducing the shutdown current to 0.1 µA (typical). During shutdown, the internal input switch (Q1) remains open and disconnects the load from the input supply of the device.

The user must terminate this pin. For more details on how to use the interface function, see *Digital Interface (CTRL)*.

7.3.4 DAC Output (DO)

The TPS61045 device allows digital adjustment of the output voltage using the digital CTRL interface, as described in *Digital Interface (CTRL)*. The DAC output pin (DO) drives an external resistor (R3) connected to the external feedback divider. The DO output has a typical output voltage range from 0 V to V_{ref} (1.233 V). If the DO output voltage is set to 0 V, the external resistor (R3) is more or less in parallel with the lower feedback resistor (R2), giving the highest output voltage. Programming the DO output to V_{ref} gives the lowest output voltage. Internally, a 6-bit DAC is used with 64 steps and 0 as the first step. This gives a typical voltage step of 19.6 mV, which is calculated as:

$$\left(V_{O(DO)} = \frac{V_{ref}}{2^6 - 1} \right) \quad (3)$$

See *Setting the Output Voltage* for further information.

After start-up, when the CTRL pin is pulled high, the DO output voltage is set to its center voltage, which is the 32nd step of typical $V_{(DO)}$ = 607 mV.

7.3.5 Digital Interface (CTRL)

When the CTRL pin is pulled high, the device starts up with softstart and the DAC output voltage (DO) sets to its center voltage with a typical output voltage of 607 mV.

The output voltage can be programmed by pulling the CTRL pin low for a certain period of time. Depending on this time period, the internal DAC voltage increases or decreases one digital step, as outlined in Table 2 and Figure 11. Programming the DAC output $V_{(DO)}$ to 0 V places R3 in parallel to R2, which gives the maximum output voltage. If the DAC is programmed to its maximum output voltage equal to the internal reference voltage, typically $V_{(DO)}$ = 1.233 V, then the output has its minimum output voltage.

Table 2. Timing Table

DAC OUTPUT DO	TIME	LOGIC LEVEL
Increase one step	t_{UP} = 1 to 60 µs	Low
Decrease one step	t_{DWN} = 140 to 240 µs	Low
Shutdown	t_{OFF} ≥ 560 µs	Low
Delay between steps	t_{d1} = 1 µs	High

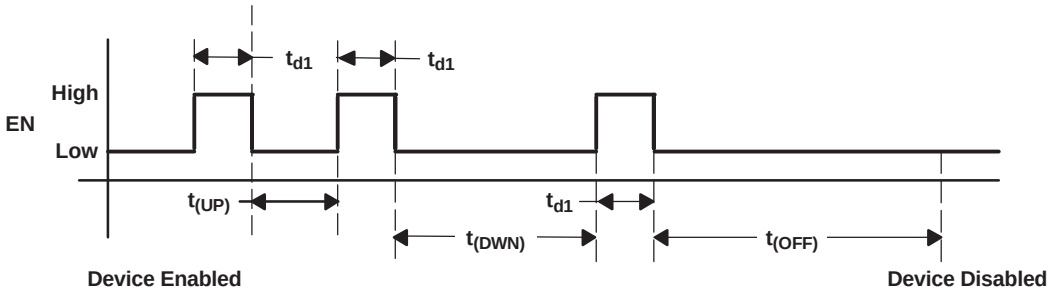


Figure 11. CTRL Timing Diagram

7.3.6 UVLO

An UVLO feature prevents misoperation of the device at input voltages below 1.5 V (typical). As long as the input voltage is below the undervoltage threshold, the device remains off, with the input switch (Q1) and the main switch (Q2) open.

7.3.7 Thermal Shutdown

An internal thermal shutdown is implemented in the TPS61045 device that shuts down the device if the typical junction temperature of 160°C is exceeded. If the device is in thermal shutdown mode, the input switch (Q1) and the main switch (Q2) are open.

7.4 Device Functional Modes

The device operates in a pulse frequency modulation (PFM) scheme with constant peak current control. This control scheme maintains high efficiency over the entire load current range, and with a switching frequency of up to 1 MHz, the device enables the use of small external components. The converter monitors the output voltage. When the feedback voltage falls below the reference voltage of 1.233 V (typical), the main switch turns on and the current ramps up. The main switch turns off when the inductor current reaches the internally set peak current of 375 mA (typical).

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS61045 device is a high-frequency boost converter with digitally-programmable output voltage and true shutdown. The TPS61045 device operates with an input voltage range of 1.8 to 6 V and generates output voltages up to 28 V. The device operates in a constant peak current control, which maintains high efficiency over the entire load current range, and with a typical switching frequency of up to 1 MHz.

8.2 Typical Application

The following section provides a step-by-step design approach for configuring the TPS61045 as a voltage regulating boost converter, as shown in Figure 12.

8.2.1 Analog Adjusted Output Voltage

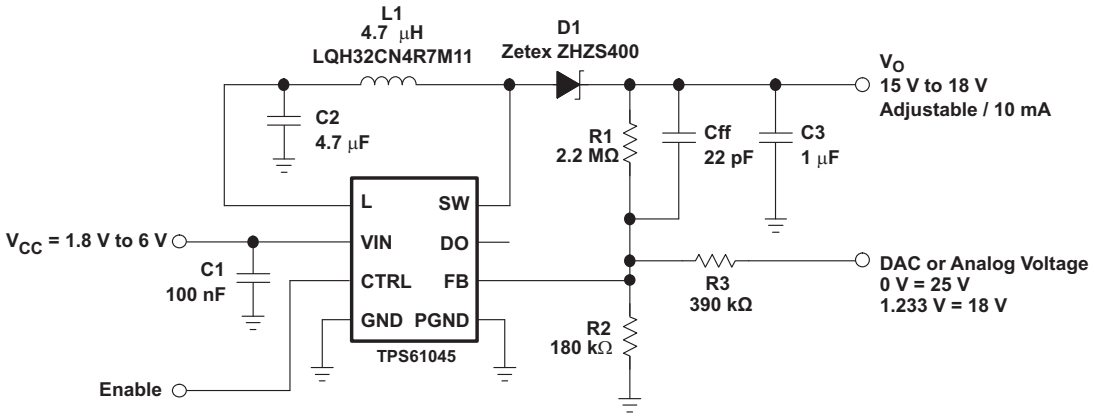


Figure 12. Typical Application With Analog Adjusted Output Voltage

8.2.1.1 Design Requirements

Table 3. Design Parameters

PARAMETERS	VALUES
Output voltage	18 V
Input voltage	1.8 to 6 V
Output current	10 mA

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Inductor Selection, Maximum Load Current

Because the PFM peak current control scheme is inherently stable, the inductor and capacitor value does not affect the stability of the regulator. The selection of the inductor together with the nominal load current, input, and output voltage of the application determines the switching frequency of the converter. Depending on the application, TI recommends inductor values between 2.2 to 47 µH. The maximum inductor value is determined by the maximum switch on-time of 6 µs (typical). The peak current limit of 375 mA (typical) must be reached within 6 µs for proper operation.

The inductor value determines the maximum switching frequency of the converter. Therefore, the user must select the inductor value for the maximum switching frequency at maximum load current of the converter and should not be exceeded. A good inductor value to start with is 4.7 µH. The maximum switching frequency is calculated as:

$$f_{s(max)} = \frac{V_{IN} \times (V_O - V_{IN})}{I_P \times L \times V_O} \quad (4)$$

where

- I_P = Peak current as described in *Peak Current Control*

$$I_{P(typ)} = 375\ mA + \frac{V_{IN}}{L} \times 100\ ns \quad (5)$$

where

- L = Selected inductor value; TI recommends inductor values between 2.2 to 47 µH

If the selected inductor does not exceed the maximum switching frequency of the converter, as a next step, the switching frequency at the nominal load current is estimated as follows:

$$f_{S(ILOAD)} = \frac{2 \times I_{LOAD} \times (V_O - V_{IN} + V_F)}{I_P^2 \times L} \quad (6)$$

where

- I_P = Peak current as described in *Peak Current Control*

$$I_{P(typ)} = 375\ mA + \frac{V_{IN}}{L} \times 100\ ns \quad (7)$$

where

- L = Selected inductor value
- $I_{(LOAD)}$ = Nominal load current
- V_F = Rectifier diode forward voltage (typically 0.3 V)

The smaller the inductor value, the higher the switching frequency of the converter, but the lower the efficiency.

The maximum load current of the converter is determined at the operation point where the converter starts to enter continuous conduction mode. The converter must always operate in DCM to maintain regulation.

Two conditions exist for determining the maximum output current of the converter. One condition is when the inductor current fall time is <400 ns, and the other condition is when the inductor current fall time is >400 ns.

One way to calculate the maximum available load current for certain operation conditions is to estimate the expected converter efficiency at the maximum load current. Find this number in the efficiency graphs shown in Figure 1 and Figure 2. Then, the maximum load current can be estimated:

Inductor fall time:

$$t_{fall} = \frac{I_P \times L}{V_O - V_{IN}} \quad (8)$$

For $t_f \geq 400$ ns:

$$I_{load\ max} = \eta \frac{I_P \times V_{IN}}{2 \times V_O} \quad (9)$$

For $t_f \leq 400$ ns:

$$I_{load\ max} = \eta \frac{I_P^2 \times L \times V_{IN}}{(V_O - V_{IN}) \times (2 \times I_P \times L + 2 \times 400\ ns \times V_{IN})} \quad (10)$$

where

- L = Selected inductor value
- η = Expected converter efficiency (typically between 70% to 85%)
- I_P = Peak current as described in *Peak Current Control*

$$I_P = 300\ mA + \frac{V_{IN}}{L} \times 100\ ns \quad (11)$$

Equation 10 contains the expected converter efficiency that allows calculating the expected maximum load current the converter can support. Find the efficiency in the efficiency graphs shown in Figure 1 and Figure 2, or 80% can be used as a good estimation.

The selected inductor must have a saturation current which meets the maximum peak current of the converter as calculated in *Peak Current Control*. Use the maximum value for I_{Lim} (450 mA) for this calculation.

Another important inductor parameter is the dc resistance. The lower the dc resistance, the higher the efficiency of the converter. See Table 4 and *Inductor Selection, Maximum Load Current*.

Table 4. Possible Inductor Selection

Inductor Value	Component Supplier	Comments
10 µH	Sumida CR32-100	High efficiency
10 µH	Sumida CDRH3D16-100	High efficiency
10 µH	Murata LQH43CN100K01	
4.7 µH	Sumida CDRH3D16-4R7	Small solution size
4.7 µH	Murata LQH32CN4R7M51	Small solution size

8.2.1.2.2 Setting the Output Voltage

See *Simplified Schematic*. When the converter is programmed to the minimum output voltage, the DAC output (DO) equals the reference voltage of 1.233 V (typical). Therefore, only the feedback resistor network (R1) and (R2) determines the output voltage under these conditions. This gives the minimum output voltage possible and can be calculated as:

$$V_{O(min)} = V_{(FB)} \times \left(\frac{R1}{R2} + 1\right) \quad (12)$$

The maximum output voltage is determined as the DAC output (DO) is set to 0 V:

$$V_{O(max)} = V_{(FB)} \times \frac{R1}{R3} + V_{(FB)} \times \left(\frac{R1}{R2} + 1\right) \quad (13)$$

The output voltage can be digitally programmed by pulling the CTRL pin low for a certain period of time as described in *Digital Interface (CTRL)*. Pulling the signal applied to the CTRL pin low and high again (for related timing see *Electrical Characteristics*) increases or decreases the DAC output DO (pin 3) one step where one step is typically 19.6 mV. A voltage step on DO of 19.6 mV (typical) changes the output voltage by one step and is calculated as:

$$V_{O(step)} = \frac{19.6\ mV \times R1}{R3} \quad (14)$$

The possible output voltage range is determined by selecting R1, R2, and R3. A possible larger output voltage range gives a larger output voltage step size. The smaller the possible output voltage range, the smaller the output voltage step size.

To reduce the overall operating quiescent current in battery-powered applications a high-impedance voltage divider must be used with a typical value for R2 of ≤200 kΩ and a maximum value for R1 of 2.2 MΩ.

Some applications may not need the digital interface to program the output voltage. In this case, the output DO can be left open as shown in Figure 12, and the output voltage is calculated as for any standard boost converter:

$$V_O = 1.233\ V \times \left(1 + \frac{R1}{R2}\right) \quad (15)$$

In such a configuration, a high-impedance voltage divider must also be used to minimize ground current, and TI recommends a typical value for R2 of ≤200 kΩ and a maximum value for R1 of 2.2 MΩ.

A feed-forward capacitor ($C_{(FF)}$), across the upper feedback resistor (R1), is required to provide sufficient overdrive for the error comparator. Without a feed-forward capacitor or with a too-small feed-forward capacitor value, the device shows double pulses or a pulse burst instead of single pulses at the switch node (SW). This can cause higher output voltage ripple. If a higher output voltage ripple is acceptable, the feed-forward capacitor can be left out also.

The lower the switching frequency of the converter, the larger the feed-forward capacitor value needs to be. A good starting point is to use a 10-pF feed-forward capacitor. As a first estimation, the required value for the feed-forward capacitor can be calculated at the operation point:

$$C_{(FF)} \approx \frac{1}{2 \times \pi \times \frac{f_S}{20} \times R1} \quad (16)$$

where

- R1 = Upper resistor of voltage divider
- f_S = Switching frequency of the converter at the nominal load current. (For the calculation of the switching frequency, see *Inductor Selection, Maximum Load Current*.)

For $C_{(FF)}$, choose a value which comes closest to the calculation result.

The larger the feed-forward capacitor, the worse the line regulation of the device. Therefore, select the feed-forward capacitor as small as possible if good line regulation is of concern.

8.2.1.2.3 Output Capacitor Selection

For better output voltage filtering, TI recommends a low-ESR output capacitor. Ceramic capacitors have low-ESR values, but depending on the application, tantalum capacitors can also be used. For the selection of the output capacitor, see Table 5.

Assuming the converter does not show double pulses or pulse bursts on the switch node (SW), the output voltage ripple is calculated as:

$$\Delta V_O = \frac{I_O}{C_O} \times \left(\frac{1}{f_{S(ILOAD)}} - \frac{I_P \times L}{V_O + V_F - V_{IN}} \right) + I_P \times ESR \quad (17)$$

where

- I_P = Peak current as described in *Peak Current Control*

$$I_P = 375\ mA + \frac{V_{IN}}{L} \times 100\ ns \quad (18)$$

where

- L = Selected inductor value
- $I_{O(LOAD)}$= Nominal load current
- $f_{S(ILoad)}$ = Switching frequency at the nominal load current as calculated previously.
- V_F = Rectifier diode forward voltage (typically 0.3 V)
- C_O = Selected output capacitor
- ESR = Output capacitor ESR value

8.2.1.2.4 Input Capacitor Selection

The input capacitor (C1) filters the high-frequency noise to the control circuit and must be directly connected to the input pin (VIN) of the device. The capacitor (C2) connected to the L pin of the device is the input capacitor for the power stage.

The main purpose of the capacitor (C2), that is connected directly to the L pin, is to smooth the inductor current. A larger capacitor reduces the inductor ripple current present at the L pin. The smaller the ripple current at the L pin, the higher the efficiency of the converter. If a sufficiently large capacitor is used, the input switch must carry only the dc current, filtered by the capacitor (C2), and not the high switching currents of the converter. A 4.7- or 10-µF ceramic capacitor (C2) is sufficient for most applications. For better filtering, this value can be increased without limit. See Table 5 for input capacitor recommendations.

Table 5. Possible Input and Output Capacitor Selection

Capacitor	Voltage Rating	Component Supplier	Comments
4.7 F/X5R/0805	6.3 V	Tayo Yuden JMK212BY475MG	C_I / C_O
10 µF/X5R/0805	6.3 V	Tayo Yuden JMK212BJ106MG	C_I / C_O
1 µF/X7R/1206	25 V	Tayo Yuden TMK316BJ105KL	C_O
1 µF/X7R/1206	35 V	Tayo Yuden GMK316BJ105KL	C_O
4.7 µF/X5R/1210	25 V	Tayo Yuden TMK325BJ475MG	C_O

8.2.1.2.5 Diode Selection

To achieve high efficiency, use a Schottky diode. The current rating of the diode must meet the peak current rating of the converter as it is calculated in *Peak Current Control*. Use the maximum value for $I_{(LIM)}$ (450 mA) for this calculation. For the selection of the Schottky diode, see Table 6.

Table 6. Possible Schottky Diode Selection

Component Supplier	Reverse Voltage
ON Semiconductor MBR0530	30 V
ON Semiconductor MBR0520	20 V
ON Semiconductor MBRM120L	20 V
Toshiba CRS02	30 V
Zetex ZHZS400	40 V

8.2.1.3 Application Curves

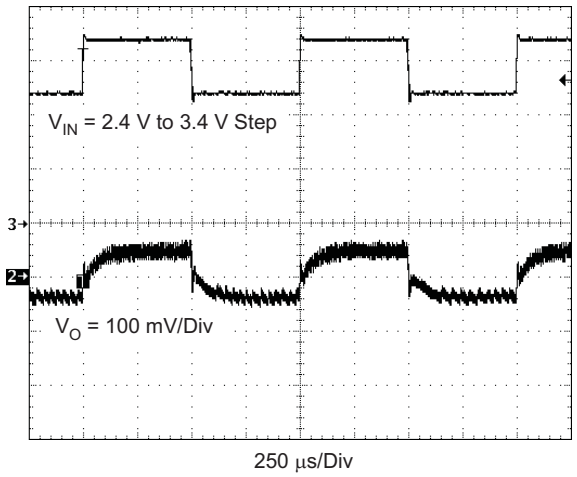


Figure 13. Line Transient Response

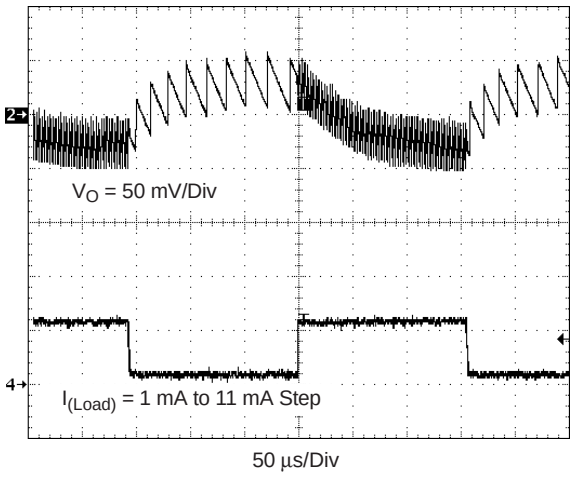


Figure 14. Load Transient Response

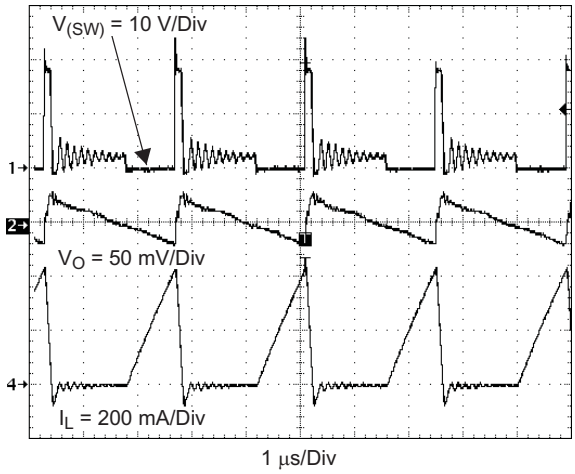


Figure 15. PFM Operation

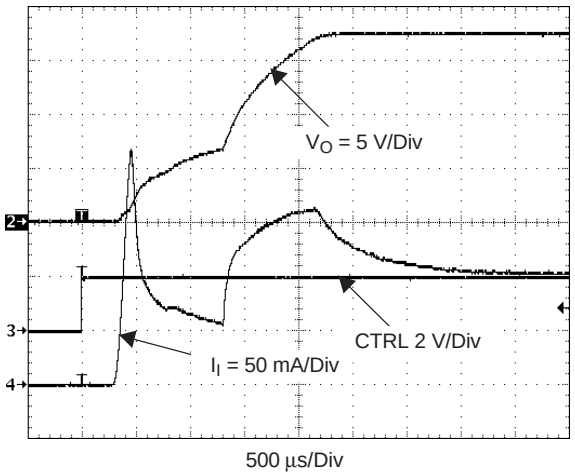


Figure 16. Softstart

8.2.2 OLED Supply with Higher Output Current

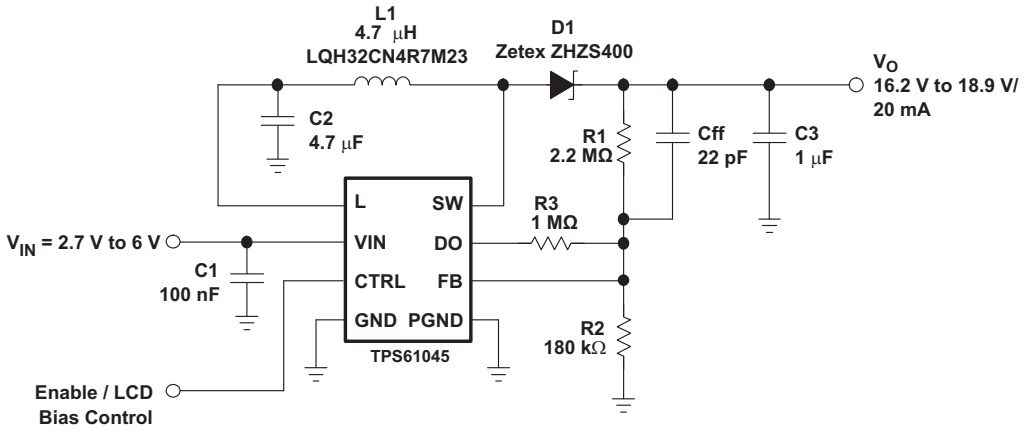


Figure 17. OLED Supply Providing Higher Output Current

8.2.2.1 Design Requirements

Table 7. Design Parameters

PARAMETERS	VALUES
Output voltage	16.2 to 18.9 V
Input voltage	2.7 to 6 V
Output current	20 mA

8.2.2.2 Detailed Design Procedure

Refer to the prior *Detailed Design Procedure*.

8.2.2.3 Application Curves

Refer to waveforms in the prior *Application Curves*.

9 Power Supply Recommendations

The device is designed to operate from an input voltage supply range between 1.8 to 6 V. This input supply must be well regulated. If the input supply is located more than a few inches from the converter, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. An electrolytic or tantalum capacitor with a value of 47 µF is a typical choice.

10 Layout

10.1 Layout Guidelines

As for all switching power supplies, the layout is an important step in the design, especially at high peak currents and switching frequencies. If the layout is not carefully implemented, the regulator can show noise problems and duty cycle jitter.

The inductor and diode must be placed as close as possible to the switch pin (SW) to minimize noise coupling into other circuits. Because the feedback pin and network is a high-impedance circuit, the feedback network must be routed away from the inductor. Also, the input capacitor must be placed as close as possible to the input pin for good input-voltage filtering. If space is critical and these guidelines can not be followed completely, the user must give the highest priority to the close placement of the diode to the switch pin (SW).

10.2 Layout Example

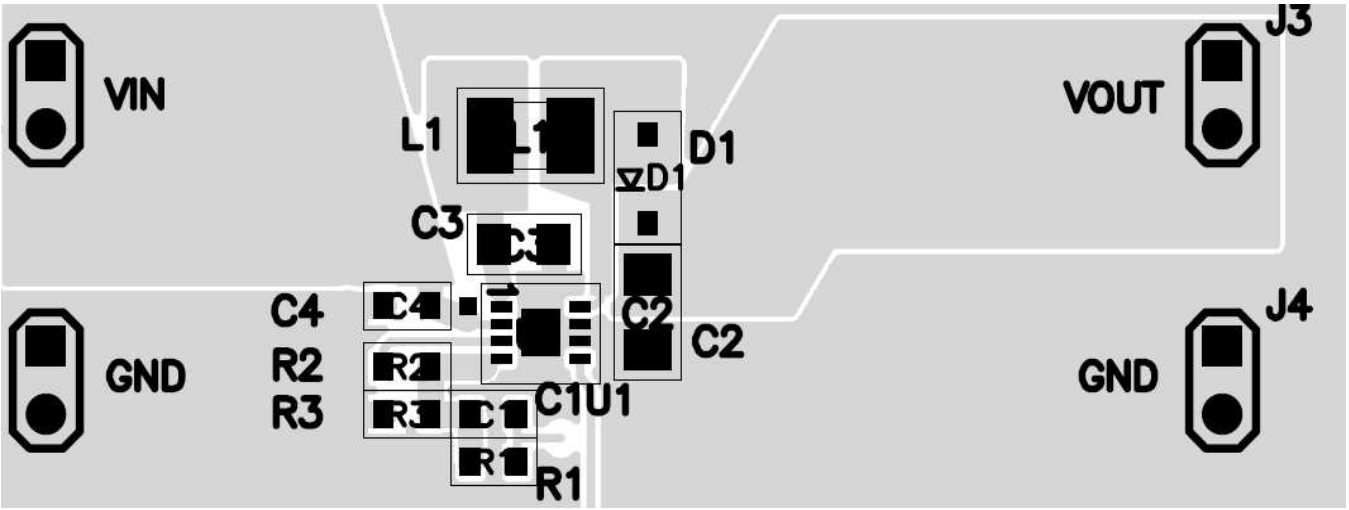


Figure 18. Board Layout Example

10.3 Thermal Considerations

The TPS61045 device is available in a thermally-enhanced VSON package. The package includes a thermal pad, improving the thermal capabilities of the package. See VSON PCB attachment application note (SLUA271).

The thermal resistance junction to ambient ($R_{\Theta JA}$) of the VSON package depends on the PCB layout. Use thermal vias and wide PCB traces to improve thermal resistance ($R_{\Theta JA}$). Under normal operation conditions, no PCB vias are required for the thermal pad. However, the thermal pad must be soldered to the PCB.

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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11.2 Trademarks

All trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS61045DRBR	ACTIVE	SON	DRB	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BHT	Samples
TPS61045DRBRG4	ACTIVE	SON	DRB	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BHT	Samples
TPS61045DRBT	ACTIVE	SON	DRB	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BHT	Samples
TPS61045DRBTG4	ACTIVE	SON	DRB	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BHT	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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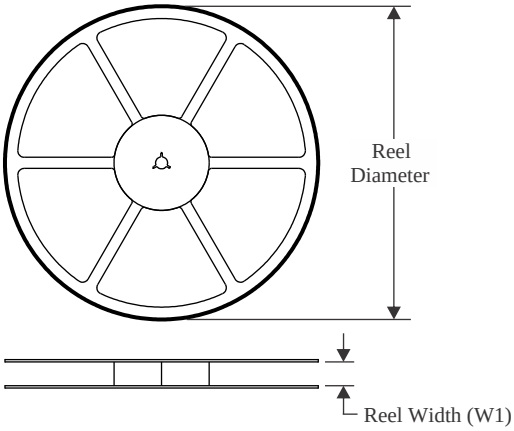
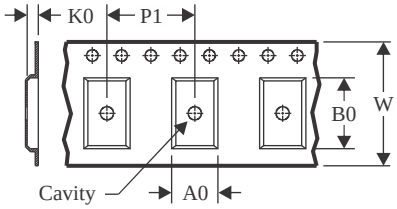
TAPE AND REEL INFORMATION

REEL DIMENSIONS

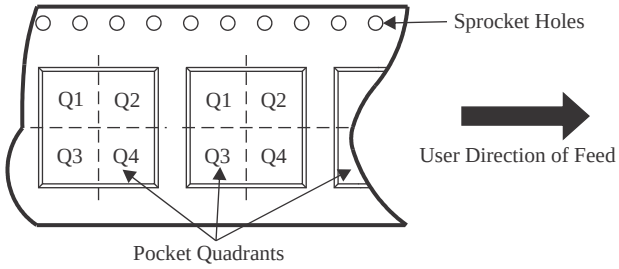


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

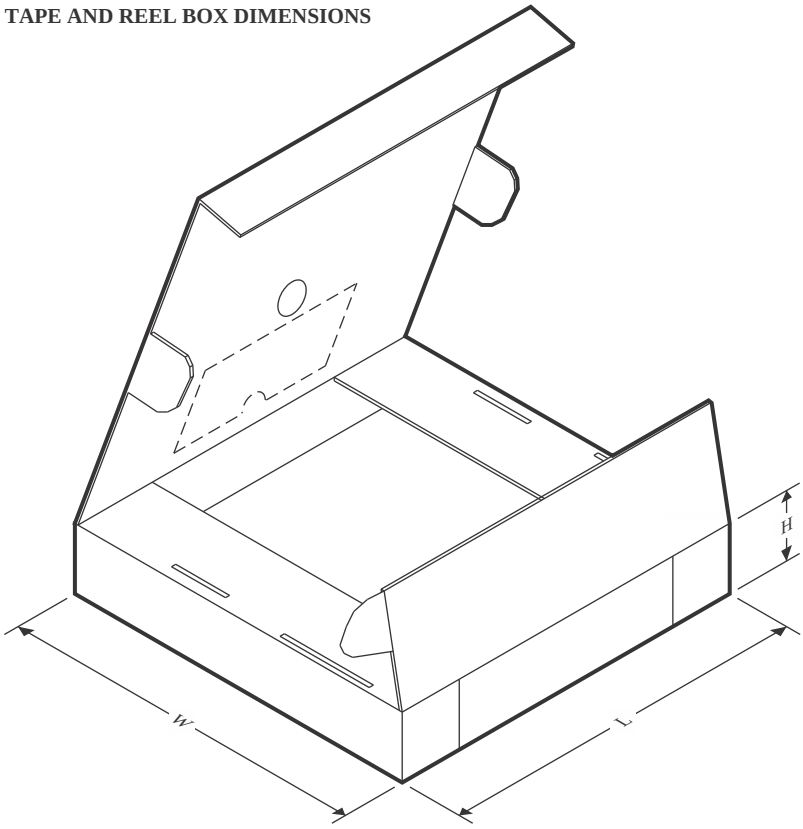
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS61045DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS61045DRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS61045DRBR	SON	DRB	8	3000	356.0	356.0	35.0
TPS61045DRBT	SON	DRB	8	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

DRB 8

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

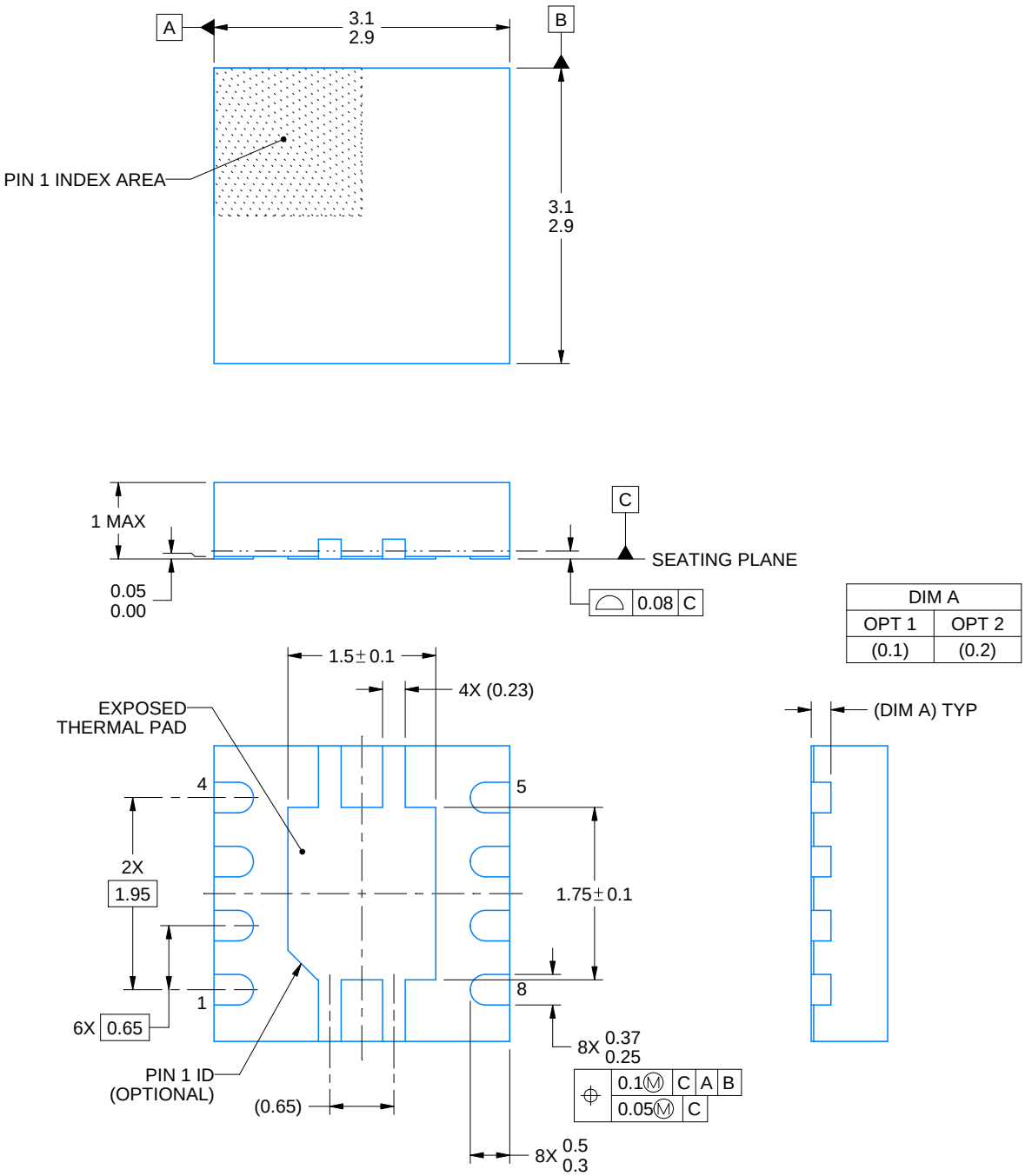
4203482/L

PACKAGE OUTLINE

DRB0008A

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES:

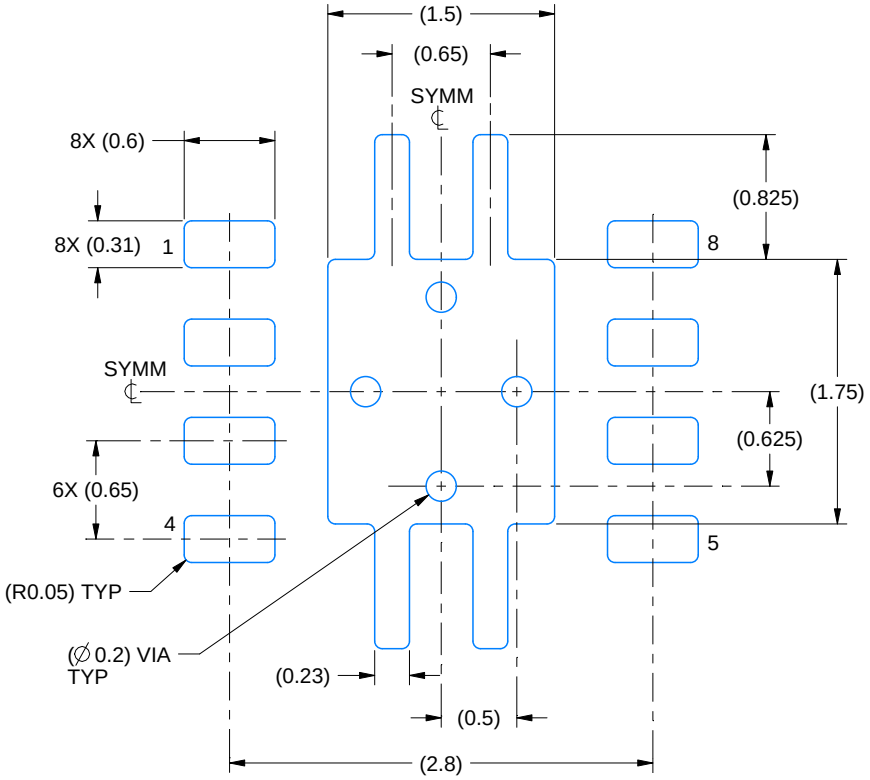
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

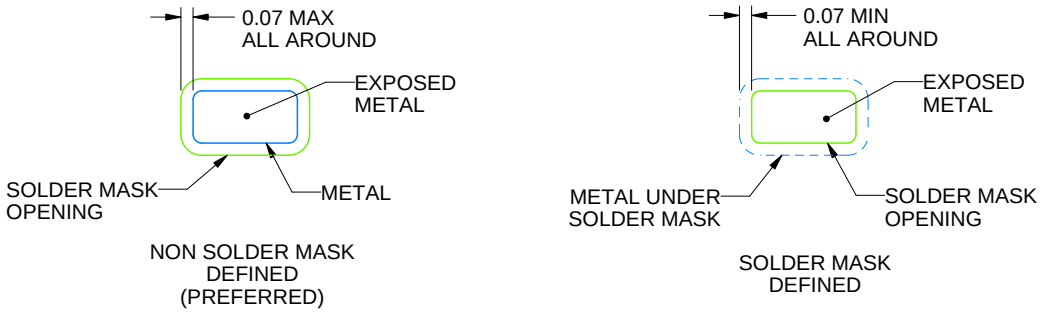
DRB0008A

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

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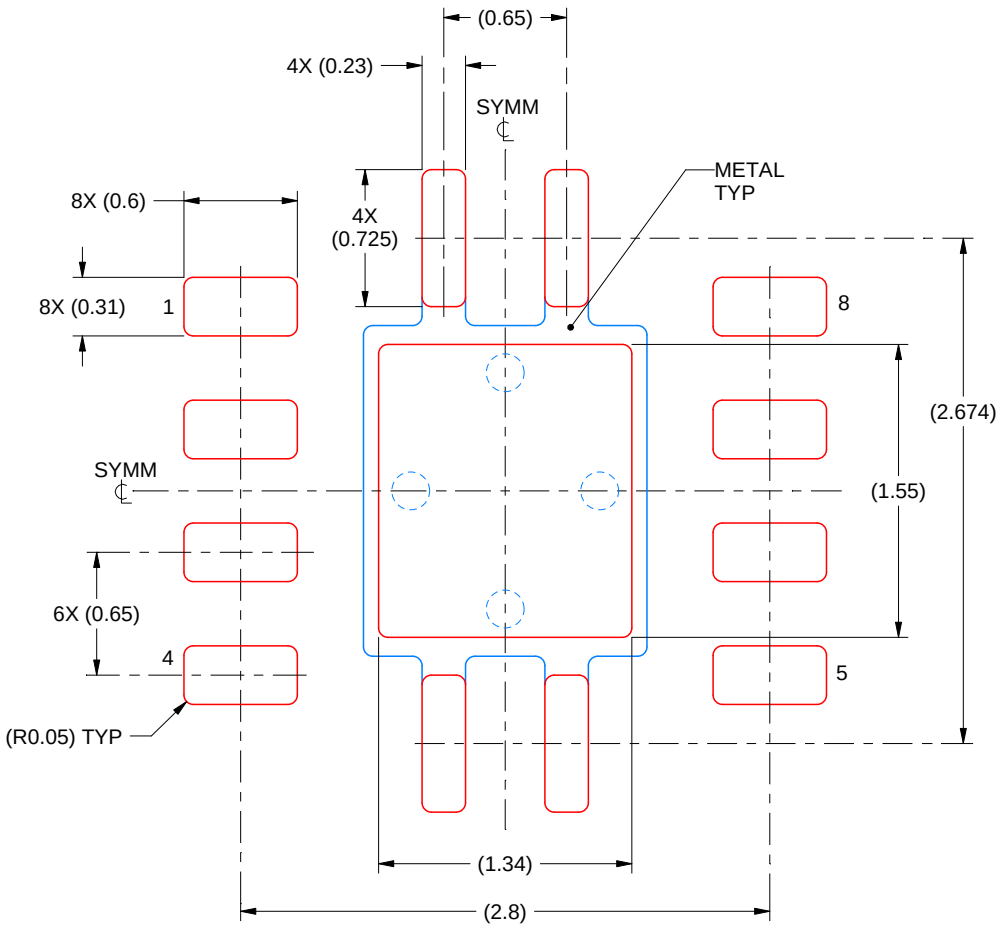
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
84% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218875/A 01/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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