THE DATASHEET OF

TPS79147DBVT

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TPS791
Ultralow Noise, High PSRR, Fast RF 100-mA Low-Dropout Linear Regulators

1 Features

- 100-mA Low-Dropout Regulator With $\overline{EN}$
- Available in 1.8-V, 3.3-V, 4.7-V, and Adj.
- High PSRR (70 dB at 10 kHz)
- Ultralow Noise (15 μV_{RMS})
- Fast Start-Up Time (63 µs)
- Stable With Any 1-µF Ceramic Capacitor
- Excellent Load, Line Transient
- Very Low Dropout Voltage (38 mV at Full Load, TPS79147)
- 5-Pin SOT23 (DBV) Package
- TPS792xx Provides EN Options

2 Applications

- Powering VCOs and PLLs
- Bluetooth and Wireless LAN
- Portable and Battery Operated

3 Description

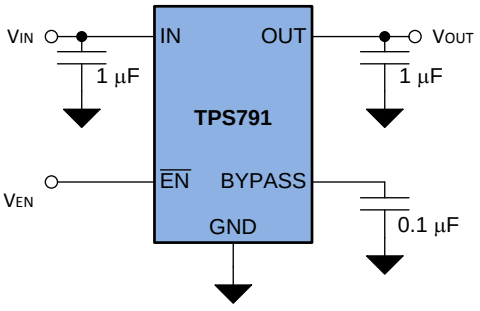
The TPS791 device is a low-dropout (LDO) low-power linear voltage regulator that features high power-supply rejection ratio (PSRR), ultralow noise, fast start-up, and excellent line and load transient responses in a small outline, SOT23 package. The device is stable, with a small 1-µF ceramic capacitor on the output. The TPS791 uses an advanced, proprietary BiCMOS fabrication process to yield extremely low dropout voltages (for example, 38 mV at 100 mA, TPS79147). This device achieves fast start-up times (approximately 63 µs with a 0.001-µF bypass capacitor) while consuming very low quiescent current (170 µA typical). Moreover, when the device is placed in standby mode, the supply current is reduced to less than 1 µA. The TPS79118 exhibits approximately 15 μV_{RMS} of output voltage noise with a 0.1-µF bypass capacitor. Applications with analog components that are noise sensitive, such as portable RF electronics, benefit from the high PSRR and low noise features as well as the fast response time.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS791	SOT23 (5)	2.90 mm × 1.60 mm
	SOT23 (6)	2.90 mm × 1.60 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic: Fixed Output



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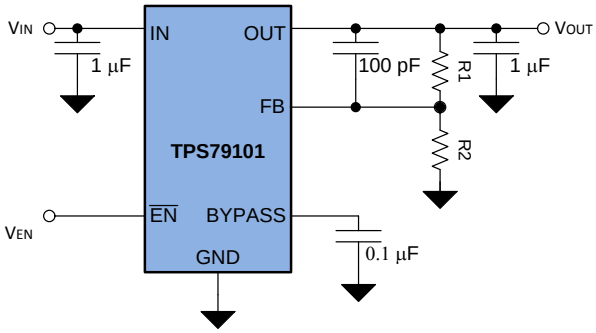
Simplified Schematic: Adjustable Output



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (May 2002) to Revision D **Page**

- Added *Device Information* table, *Simplified Schematic* figures to page 1, *ESD Ratings* table, *Thermal Information* table, *Pin Configuration and Functions* section, *Overview* section, *Feature Description* section, *Device Functional Modes* section, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Changed *TPS791xx* to *TPS791* throughout document ... 1
- Changed *Applications* section ... 1
- Changed *Description* section ... 1
- Deleted *Ordering Information* table ... 3
- Changed $\overline{EN}$ pin description ... 3
- Added I/O data for GND pin ... 3
- Deleted *Package Dissipation Rating* table ... 3
- Changed V_I to V_{IN}, I_O to I_{OUT}, C_O to C_{OUT}, $C_{o(byp)}$ and $C_{(byp)}$ to C_{BYPASS} throughout document ... 3
- Changed formula in footnote 1 of *Recommended Operating Conditions* table ... 4
- Added VREF parameter to *Electrical Characteristics* table ... 5
- Changed V_{CC} to V_{IN} in test conditions of *UVLO threshold* and *UVLO hysteresis* parameters ... 5
- Added PSRR and V_{DO} symbols to *Power-supply ripple rejection* and *Dropout voltage* parameters ... 5
- Added conditions statement to *Typical Characteristics* section ... 6
- Changed I_{OUT} to C_{BYPASS} in *TPS79118 Output Spectral Noise Density vs Frequency* figure ... 7
- Changed I_{OUT} to C_{BYPASS} in *TPS79133 Output Spectral Noise Density vs Frequency* figure ... 7
- Changed third bullet in *Normal Operation* section ... 15
- Changed first bullet in *Disabled* section ... 15
- Changed V_{EN} column in *Device Functional Mode Comparison* table ... 15
- Added *active-low* to *Application Information* description ... 16

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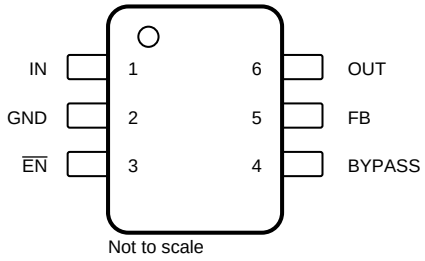
5 Pin Configuration and Functions

DBV Package: Adjustable Output
6-Pin SOT23
Top View



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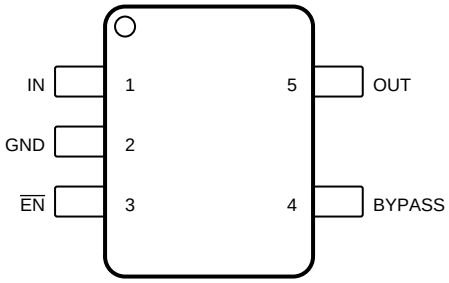
DBV Package: Fixed Output
5-Pin SOT23
Top View



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Pin Functions

PIN			I/O	DESCRIPTION
NAME	ADJ	FIXED		
BYPASS	4	4	—	An external bypass capacitor connected to this pin, in conjunction with an internal resistor, creates a low-pass filter to further reduce regulator noise.
$\overline{EN}$	3	3	I	The $\overline{EN}$ pin is an input which enables or shuts down the device. The enable signal is an active-low digital control that enables the device, so when $\overline{EN}$ is a logic high (> 2 V), the device is in shutdown mode. When $\overline{EN}$ is logic low (< 0.7 V), the device is enabled.
FB	5	N/A	I	This pin is the feedback input voltage for the adjustable device.
GND	2	2	—	Regulator ground.
IN	1	1	I	The IN pin is the input to the device.
OUT	6	5	O	The OUT pin is the regulated output of the device.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Input voltage range(2)	–0.3	6	V
Voltage range at $\overline{EN}$	–0.3	V_{IN} + 0.3	V
Voltage on OUT	–0.3	6	V
Peak output current	Internally limited		
Continuous total power dissipation	See *Thermal Information* table		
Operating virtual junction temperature, T_J	–40	150	°C
Operating ambient temperature, T_A	–40	85	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the network ground pin.

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6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage[1]	2.7		5.5	V
I_{OUT}	Continuous output current[2]	0		100	mA
T_J	Operating junction temperature	–40		125	°C

(1) To calculate the minimum input voltage for your maximum output current, use the following formula:
$V_{IN}(min) = V_{OUT}(max) + \text{dropout voltage } (V_{DO})$ at maximum load.
(2) Continuous output current and operating junction temperature are limited by internal protection circuitry, but the device is not recommended to be operated under conditions beyond those specified in this table for extended periods of time.

6.4 Thermal Information

THERMAL METRIC[1]		TPS791		UNIT
		DBV (SOT23)	DBV (SOT23)	
		5 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	192.6	168.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	104.2	87.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	55.2	36.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	24.1	17.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	54.8	36.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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6.5 Electrical Characteristics

over recommended operating free-air temperature range, (T_J = –40°C to 125°C), V_{IN} = $V_{OUT(typ)}$ + 1 V, I_{OUT}= 1 mA, $\overline{EN}$ = 0 V, C_{OUT} = 10 µF, C_{BYPASS}= 0.01 µF (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
	Output voltage	TPS79101	T_J = 25°C, 1.22 V ≤ V_{OUT} ≤ 5.2 V			V_{OUT}		V
			0 µA < I_{OUT} < 100 mA(1) ,1.22 V ≤ V_{OUT} ≤ 5.2 V		0.98 V_{OUT}		1.02 V_{OUT}	
		TPS79118	T_J = 25°C			1.8		
			0 µA < I_{OUT} < 100 mA, 2.8 V < V_{IN} < 5.5 V		1.764		1.836	
		TPS79133	T_J = 25°C			3.3		
			0 µA < I_{OUT} < 100 mA, 4.3 V < V_{IN} < 5.5 V		3.234		3.366	
		TPS79147	T_J = 25°C			4.7		
			0 µA < I_{OUT} < 100 mA, 5.2 V < V_{IN} < 5.5 V		4.606		4.794	
VREF	Reference voltage					1.2246		V
	Quiescent current (GND current)		0 µA < I_{OUT} < 100 mA, T_J = 25°C			170		µA
			0 µA < I_{OUT} < 100 mA				250	
	Load regulation		0 µA < I_{OUT} < 100 mA, T_J = 25°C			5		mV
$\Delta V_{OUT}/V_{OUT}$	Output voltage line regulation(2)		V_{OUT} + 1 V < V_{IN} ≤ 5.5 V, T_J = 25°C			0.05		%/V
			V_{OUT} + 1 V < V_{IN} ≤ 5.5 V				0.12	
	Output noise voltage (TPS79118)		BW = 100 Hz to 100 kHz, I_{OUT} = 100 mA, T_J = 25°C	C_{BYPASS} = 0.001 µF		32		μV_{RMS}
				C_{BYPASS} = 0.0047 µF		17		
				C_{BYPASS} = 0.01 µF		16		
				C_{BYPASS} = 0.1 µF		15		
	Time, start-up (TPS79133)		R_L = 33 Ω, C_{OUT} = 1 µF, T_J = 25°C	C_{BYPASS} = 0.001 µF		53		µs
				C_{BYPASS} = 0.0047 µF		67		
				C_{BYPASS} = 0.01 µF		98		
	Output current limit		V_{OUT} = 0 V(1)		285		600	mA
	UVLO threshold		V_{IN} rising		2.25		2.65	V
	UVLO hysteresis		T_J = 25°C, V_{IN} rising			100		mV
	Standby current		$\overline{EN}$ = V_{IN}, 2.7 V < V_{IN} < 5.5 V			0.07	1	µA
	High level enable input voltage		2.7 V < V_{IN} < 5.5 V		2			V
	Low level enable input voltage		2.7 V < V_{IN} < 5.5 V				0.7	V
	Input current ($\overline{EN}$)		$\overline{EN}$ = V_{IN}		–1		1	µA
PSRR	Power-supply ripple rejection	TPS79118	f = 100 Hz, T_J = 25°C, I_{OUT} = 10 mA			80		dB
			f = 100 Hz, T_J = 25°C, I_{OUT} = 100 mA			75		
			f = 10 kHz, T_J = 25°C, I_{OUT} = 100 mA			72		
			f = 100 kHz, T_J = 25°C, I_{OUT} = 100 mA			45		
		TPS79133	f = 100 Hz, T_J = 25°C, I_{OUT} = 10 mA			70		
			f = 100 Hz, T_J = 25°C, I_{OUT} = 100 mA			75		
			f = 10 kHz, T_J = 25°C, I_{OUT} = 100 mA			73		
			f = 100 kHz, T_J = 25°C, I_{OUT} = 100 mA			37		
V_{DO}	Dropout voltage(3)	TPS79133	I_{OUT} = 100 mA, T_J = 25°C			50		mV
			I_{OUT} = 100 mA				90	
		TPS79147	I_{OUT} = 100 mA, T_J = 25°C			38		
			I_{OUT} = 100 mA				70	

(1) The minimum V_{IN} operating voltage is 2.7 V or $V_{OUT(typ)}$ + 1 V, whichever is greater. The maximum V_{IN} voltage is 5.5 V. The maximum output current is 100 mA.
(2) If V_{OUT} ≤ 1.8 V then V_{INmin} = 2.7 V and V_{INmax} = 5.5 V.
(3) Equals V_{IN} voltage – V_{OUT}(typ) – 100 mV; the TPS79118 dropout voltage is limited by the minimum input voltage range limitations.

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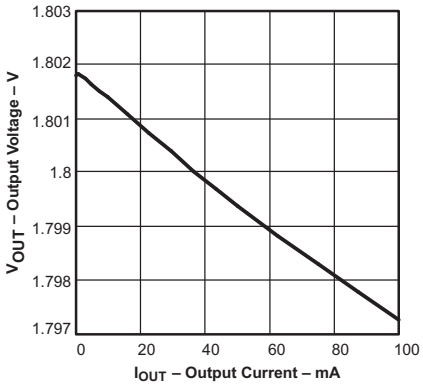
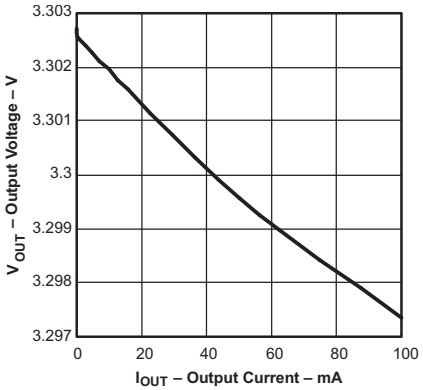
6.6 Typical Characteristics

at T_J = 25°C, V_{IN} = $V_{OUT(typ)}$ + 1 V, I_{OUT} = 1 mA, EN = 0 V, C_{OUT} = 10 µF, and C_{BYPASS} = 0.01 µF (unless otherwise noted)



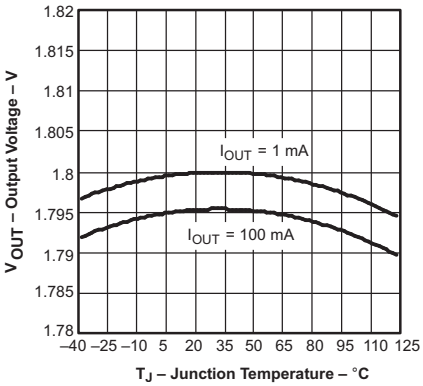
V_{IN} = 2.8 V, C_{OUT} = 10 µF, T_J = 25°C

Figure 1. TPS79118 Output Voltage vs Output Current



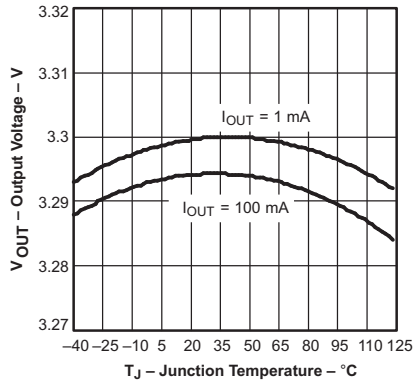
V_{IN} = 4.3 V, C_{OUT} = 10 µF, T_J = 25°C

Figure 2. TPS79133 Output Voltage vs Output Current



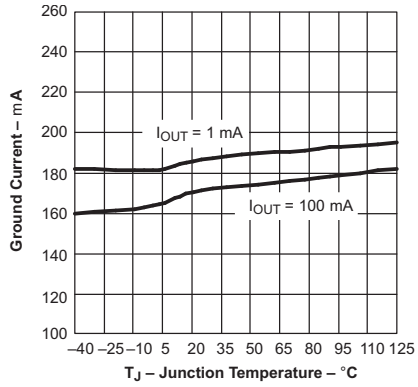
V_{IN} = 2.8 V, C_{OUT} = 10 µF

Figure 3. TPS79118 Output Voltage vs Junction Temperature



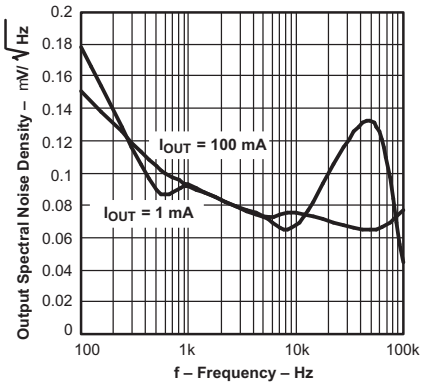
V_{IN} = 4.3 V, C_{OUT} = 10 µF

Figure 4. TPS79133 Output Voltage vs Junction Temperature



V_{IN} = 4.3 V, C_{OUT} = 10 µF

Figure 5. TPS79133 Ground Current vs Junction Temperature



V_{IN} = 2.8 V, C_{OUT} = 1 µF, C_{BYPASS} = 0.1 µF

Figure 6. TPS79118 Output Spectral Noise Density vs Frequency

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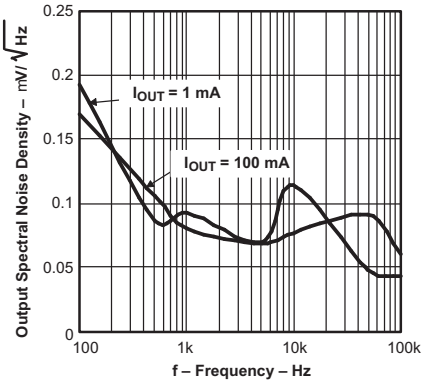
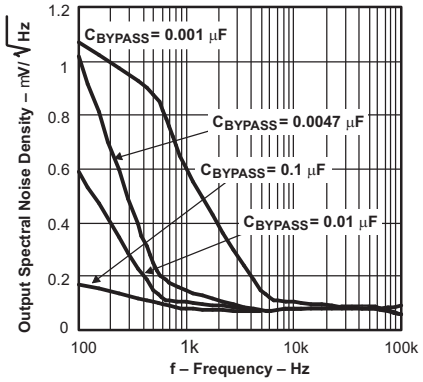
Typical Characteristics (continued)

at T_J = 25°C, V_{IN} = $V_{OUT(typ)}$ + 1 V, I_{OUT} = 1 mA, EN = 0 V, C_{OUT} = 10 µF, and C_{BYPASS} = 0.01 µF (unless otherwise noted)



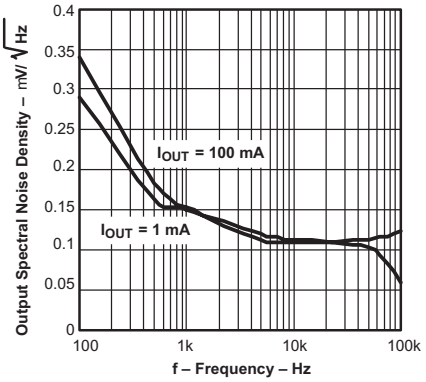
V_{IN} = 2.8 V, C_{OUT} = 10 µF, C_{BYPASS} = 0.1 µF

Figure 7. TPS79118 Output Spectral Noise Density vs Frequency



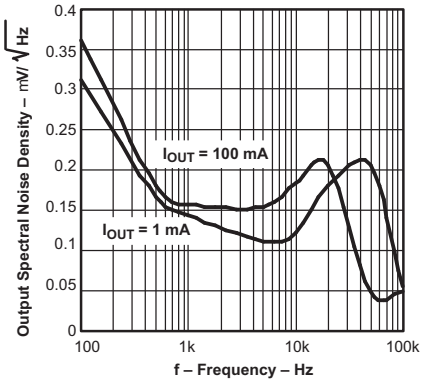
V_{IN} = 2.8 V, I_{OUT} = 100 mA, C_{OUT} = 10 µF

Figure 8. TPS79118 Output Spectral Noise Density vs Frequency



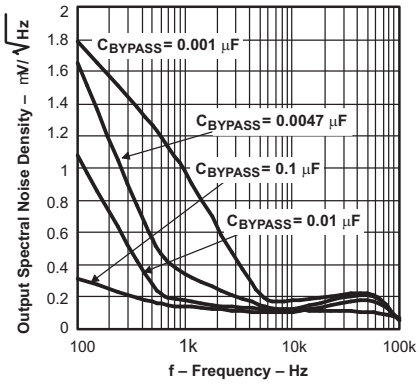
V_{IN} = 4.3 V, C_{OUT} = 1 µF, C_{BYPASS} = 0.1 µF

Figure 9. TPS79133 Output Spectral Noise Density vs Frequency



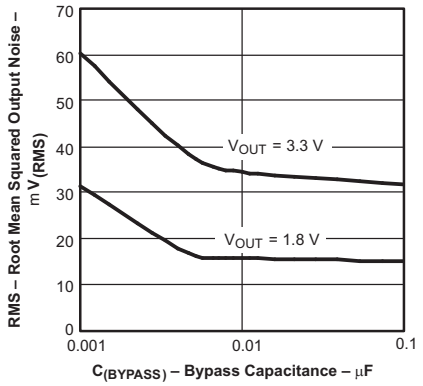
V_{IN} = 4.3 V, C_{OUT} = 10 µF, C_{BYPASS} = 0.1 µF

Figure 10. TPS79133 Output Spectral Noise Density vs Frequency



V_{IN} = 4.3 V, I_{OUT} = 100 mA, C_{OUT} = 10 µF

Figure 11. TPS79133 Output Spectral Noise Density vs Frequency



BW = 100 Hz to 100 kHz

Figure 12. Root Mean Squared Output Noise vs Bypass Capacitance

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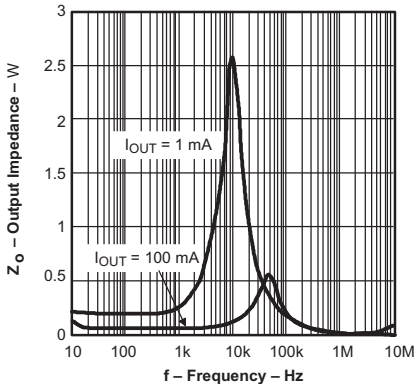
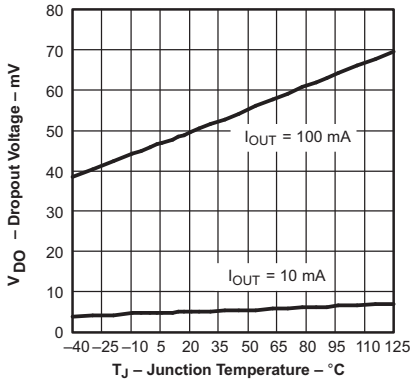
Typical Characteristics (continued)

at T_J = 25°C, V_{IN} = $V_{OUT(typ)}$ + 1 V, I_{OUT} = 1 mA, EN = 0 V, C_{OUT} = 10 µF, and C_{BYPASS} = 0.01 µF (unless otherwise noted)



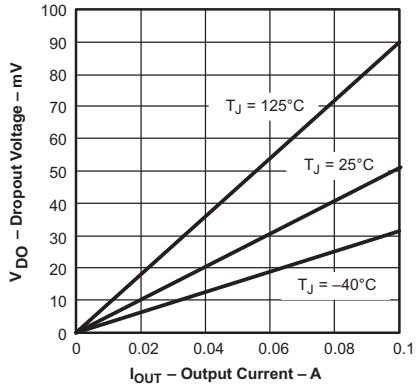
V_{IN} = 4.3 V, C_{OUT} = 10 µF, T_J = 25°C

Figure 13. TPS79133 Output Impedance vs Frequency



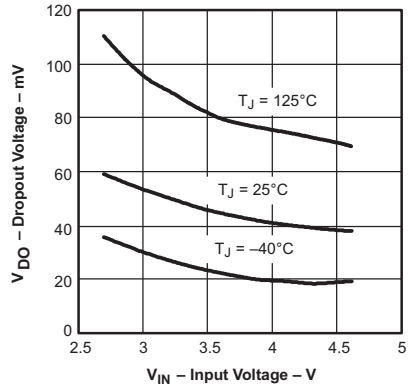
V_{IN} = 3.2 V, C_{OUT} = 10 µF

Figure 14. TPS79133 Dropout Voltage vs Junction Temperature



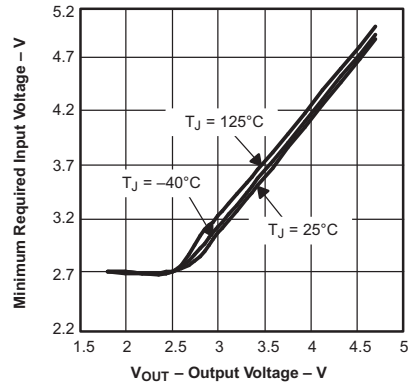
V_{IN} = 3.2 V, C_{OUT} = 10 µF

Figure 15. TPS79133 Dropout Voltage vs Output Current



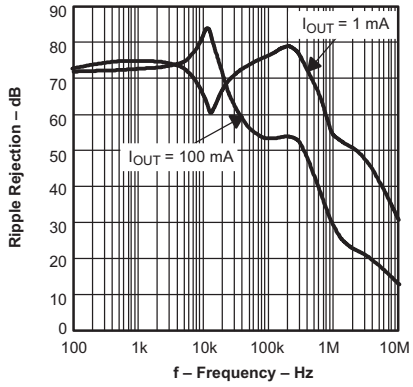
I_{OUT} = 100 mA

Figure 16. TPS79101 Dropout Voltage vs Input Voltage



V_{IN} = 3.2 V, C_{OUT} = 10 µF

Figure 17. Minimum Required Input Voltage vs Output Voltage



V_{IN} = 2.8 V, C_{OUT} = 10 µF, C_{BYPASS} = 0.01 µF

Figure 18. TPS79118 Ripple Rejection vs Frequency

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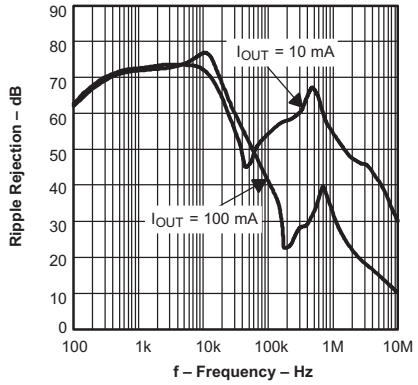
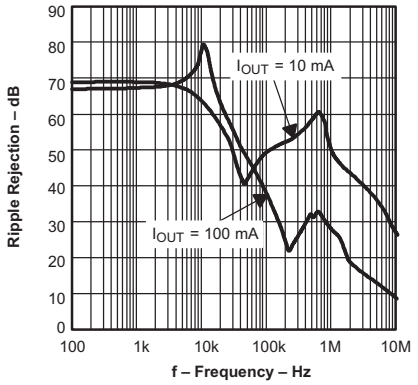
Typical Characteristics (continued)

at T_J = 25°C, V_{IN} = $V_{OUT(typ)}$ + 1 V, I_{OUT} = 1 mA, EN = 0 V, C_{OUT} = 10 µF, and C_{BYPASS} = 0.01 µF (unless otherwise noted)



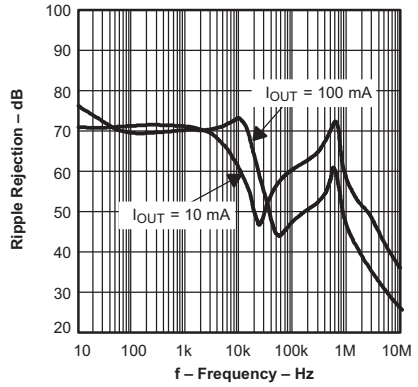
V_{IN} = 2.8 V, C_{OUT} = 1 µF, C_{BYPASS} = 0.01 µF

Figure 19. TPS79118 Ripple Rejection vs Frequency



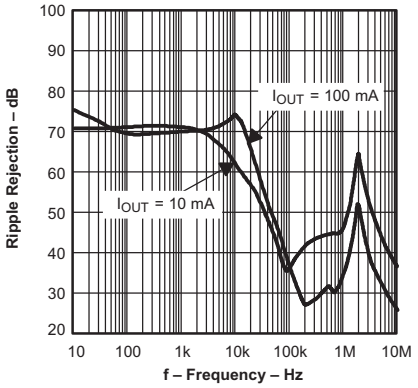
V_{IN} = 2.8 V, C_{OUT} = 1 µF, C_{BYPASS} = 0.1 µF

Figure 20. TPS79118 Ripple Rejection vs Frequency



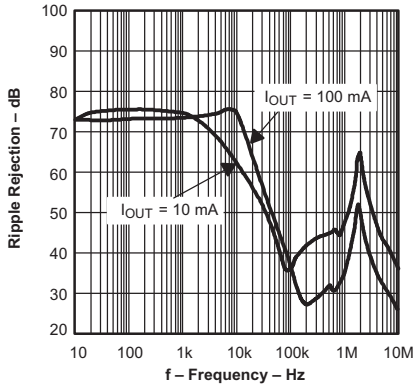
V_{IN} = 4.3 V, C_{OUT} = 10 µF, C_{BYPASS} = 0.01 µF

Figure 21. TPS79133 Ripple Rejection vs Frequency



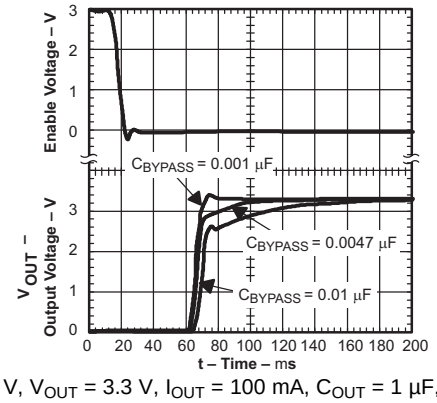
V_{IN} = 4.3 V, C_{OUT} = 1 µF, C_{BYPASS} = 0.01 µF

Figure 22. TPS79133 Ripple Rejection vs Frequency



V_{IN} = 4.3 V, C_{OUT} = 1 µF, C_{BYPASS} = 0.1 µF

Figure 23. TPS79133 Ripple Rejection vs Frequency



V_{IN} = 4.3 V, V_{OUT} = 3.3 V, I_{OUT} = 100 mA, C_{OUT} = 1 µF, T_J = 25°C

Figure 24. TPS79133 Output Voltage, Enable Voltage vs Time (Start-Up)

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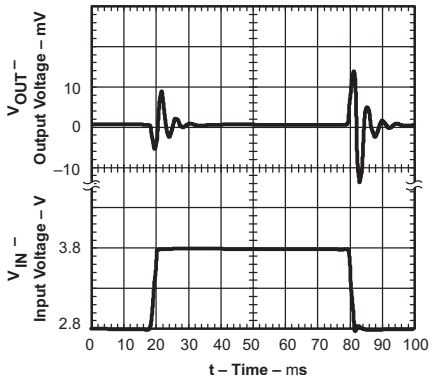
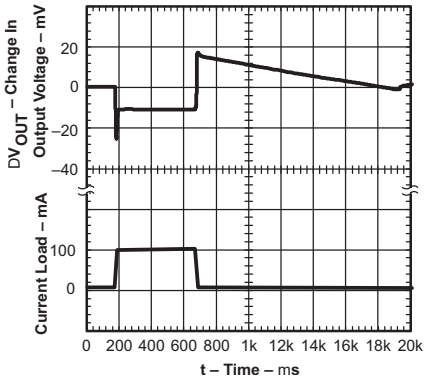
Typical Characteristics (continued)

at T_J = 25°C, V_{IN} = $V_{OUT(typ)}$ + 1 V, I_{OUT} = 1 mA, EN = 0 V, C_{OUT} = 10 µF, and C_{BYPASS} = 0.01 µF (unless otherwise noted)



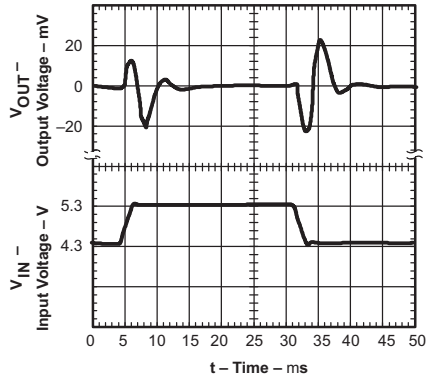
I_{OUT} = 100 mA, C_{OUT} = 1 µF, C_{BYPASS} = 0.01 µF

Figure 25. TPS79118 Line Transient Response



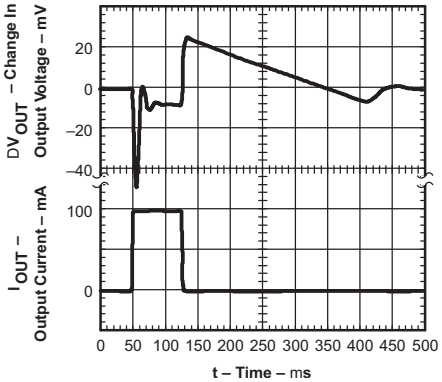
V_{IN} = 2.8 V, C_{OUT} = 10 µF

Figure 26. TPS79118 Load Transit Response



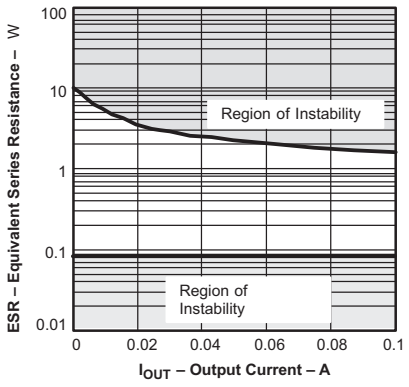
I_{OUT} = 100 mA, C_{OUT} = 1 µF, C_{BYPASS} = 0.01 µF,
dv / dt = 0.4 V / m_s

Figure 27. TPS79133 Line Transient Response



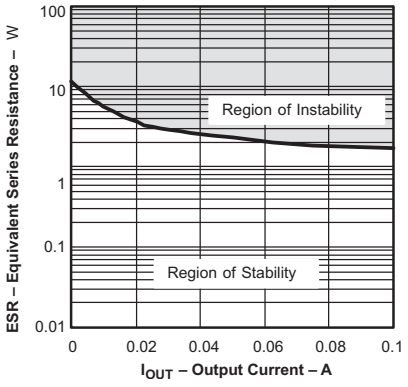
V_{IN} = 4.3 V, C_{OUT} = 10 µF

Figure 28. TPS79133 Load Transit Response



V_{IN} = 5.5 V, C_{OUT} = 0.47 µF, T_J = –40°C to 125°C

Figure 29. TPS79118 Typical Regions of Stability Equivalent Series Resistance (ESR) vs Output Current



V_{IN} = 5.5 V, C_{OUT} = 1 µF, T_J = –40°C to 125°C

Figure 30. TPS79118 Typical Regions of Stability Equivalent Series Resistance (ESR) vs Output Current

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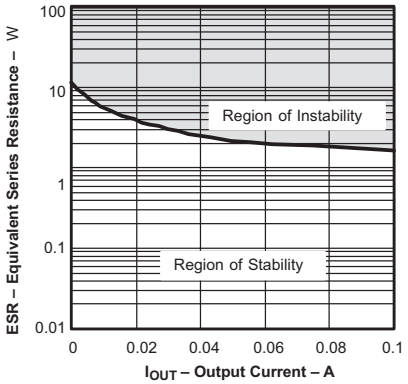
Typical Characteristics (continued)

at T_J = 25°C, V_{IN} = $V_{OUT(typ)}$ + 1 V, I_{OUT} = 1 mA, EN = 0 V, C_{OUT} = 10 µF, and C_{BYPASS} = 0.01 µF (unless otherwise noted)



V_{IN} = 5.5 V, C_{OUT} = 10 µF, T_J = –40°C to 125°C

Figure 31. TPS79118 Typical Regions of Stability Equivalent Series Resistance (ESR) vs Output Current

7 Detailed Description

7.1 Overview

The TPS791 device is a high PSRR, ultra-low noise, 100-mA linear regulator (LDO). The fast start-up time and the excellent load and line transient behavior of this device qualify the TPS791 to be an ideal solution for signal RF and signal-chain applications.

7.2 Functional Block Diagrams

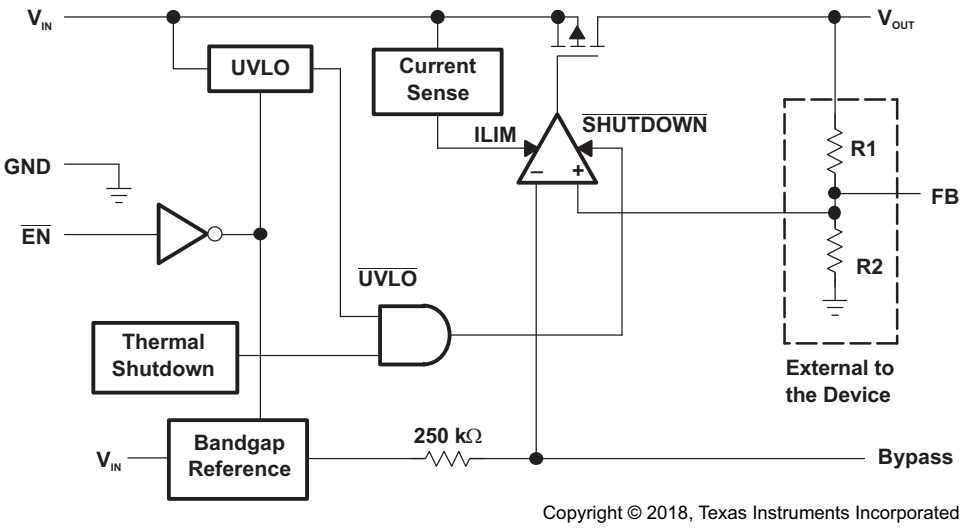


Figure 32. Functional Block Diagram: Adjustable Version

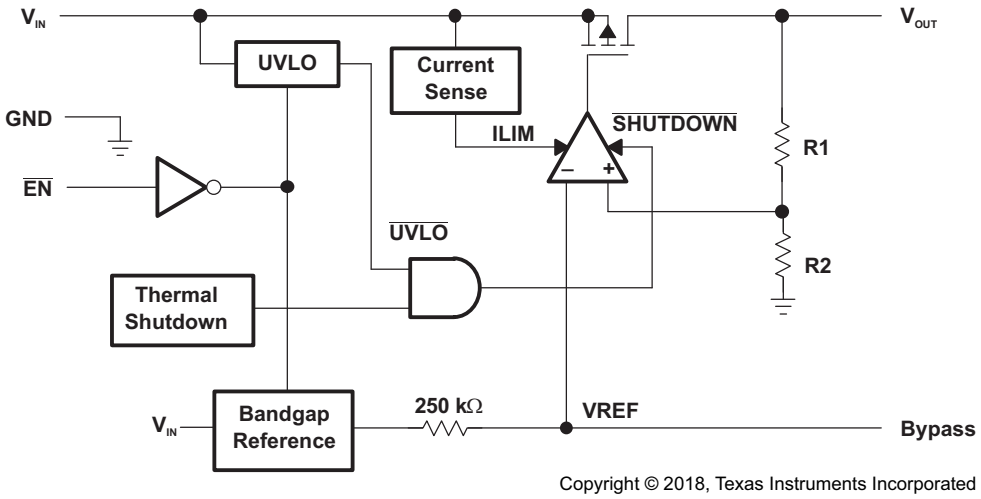


Figure 33. Functional Block Diagram: Fixed Version

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7.3 Feature Description

7.3.1 Power Dissipation and Junction Temperature

Specified regulator operation is confirmed at a junction temperature of 125°C; restrict the maximum junction temperature to 125°C under normal operating conditions. This restriction limits the power dissipation the regulator can handle in any given application. To ensure the junction temperature is within acceptable limits, calculate the maximum allowable dissipation, $P_{D(max)}$, and the actual dissipation, P_D, which must be less than or equal to $P_{D(max)}$.

The maximum-power-dissipation limit is determined using the following equation:

$$P_D(max) = \frac{T_J max - T_A}{R_{\theta JA}} \quad (1)$$

where

- $T_J$max is the maximum allowable junction temperature
- $R_{\theta JA}$ is the thermal resistance junction-to-ambient for the package (see the *Thermal Information* table)
- T_A is the ambient temperature

The regulator dissipation is calculated using:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (2)$$

Power dissipation resulting from quiescent current is negligible. Excessive power dissipation triggers the thermal protection circuit.

7.3.2 Programming the TPS79101 Adjustable Regulator

The output voltage of the TPS79101 adjustable regulator is programmed using an external resistor divider; see Figure 32. The output voltage is calculated using:

$$V_{OUT} = VREF \times \left(1 + \frac{R1}{R2}\right) \quad (3)$$

where

- VREF = 1.2246 V typ (the internal reference voltage)

Select resistors R1 and R2 for approximately a 50-µA divider current. Lower value resistors can be used for improved noise performance, but the solution consumes more power. Avoid higher resistor values because leakage current into or out of FB across R1, R2 creates an offset voltage that artificially increases or decreases the feedback voltage and thus erroneously decreases or increases V_{OUT}. The recommended design procedure is to choose R2 = 30.1 kΩ to set the divider current at 50 µA, C1 = 15 pF for stability, and then calculate R1 using:

$$R1 = \left(\frac{V_{OUT}}{VREF} - 1\right) \times R2 \quad (4)$$

In order to improve the stability of the adjustable version, a small compensation capacitor is suggested to be placed between OUT and FB. For voltages < 1.8 V, the value of this capacitor must be 100 pF. For voltages > 1.8 V, the approximate value of this capacitor can be calculated as:

$$C1 = \frac{\left(3 \times 10^{-7}\right) \times (R1 + R2)}{(R1 \times R2)} \quad (5)$$

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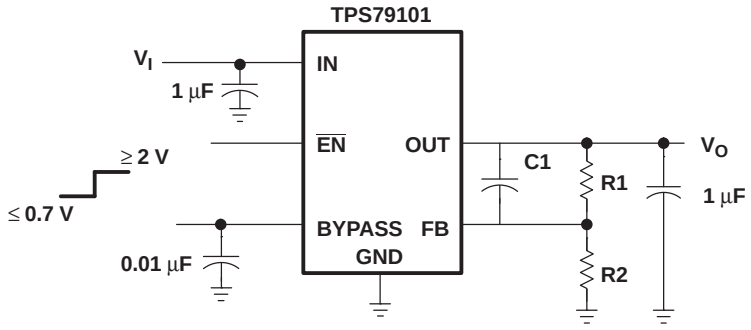
Feature Description (continued)

The table in Figure 34 shows the suggested value of this capacitor for several resistor ratios. If this capacitor is not used (such as in a unity-gain configuration) or if an output voltage < 1.8 V is chosen, then the minimum recommended output capacitor is 2.2 µF instead of 1 µF.



OUTPUT VOLTAGE PROGRAMMING GUIDE

OUTPUT VOLTAGE	R1	R2	C1
2.5 V	31.6 kΩ	30.1 kΩ	22 pF
3.3 V	51 kΩ	30.1 kΩ	15 pF
3.6 V	59 kΩ	30.1 kΩ	15 pF

Figure 34. TPS79101 Adjustable LDO Regulator Programming

7.3.3 Regulator Protection

The TPS791 PMOS-pass transistor has a built-in back diode that conducts reverse current when the input voltage drops below the output voltage (for example, during power-down). Current is conducted from the output to the input and is not internally limited. If extended reverse voltage operation is anticipated, external limiting may be appropriate.

The TPS791 features internal current limiting and thermal protection. During normal operation, the TPS791 limits output current to approximately 400 mA. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. Although current limiting is designed to prevent gross device failure, care must be taken not to exceed the power dissipation ratings of the package or the absolute maximum voltage ratings of the device. If the temperature of the device exceeds approximately 165°C, thermal-protection circuitry shuts the device down. When the device cools down to below approximately 140°C, regulator operation resumes.

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7.4 Device Functional Modes

7.4.1 Normal Operation

The device regulates to the nominal output voltage under the following conditions:

- The input voltage is at least as high as the $|V_{IN(min)}|$
- The input voltage magnitude is greater than the nominal output voltage magnitude added to the dropout voltage
- $|V_{EN}|$ < low-level enable pin input voltage (0.7 V)
- The output current is less than the current limit
- The device junction temperature is less than the maximum specified junction temperature

7.4.2 Dropout Operation

If the input voltage magnitude is lower than the nominal output voltage magnitude plus the specified dropout voltage magnitude, but all other conditions are met for normal operation, the device operates in dropout mode. In this mode of operation, the output voltage magnitude is the same as the input voltage magnitude minus the dropout voltage magnitude. The transient performance of the device is significantly degraded because the pass device (such as a bipolar junction transistor, or BJT) is in saturation and no longer controls the current through the LDO. Line or load transients in dropout can result in large output voltage deviations.

7.4.3 Disabled

The device is disabled under the following conditions:

- $|V_{EN}|$ > high-level enable pin input voltage (2 V)
- The device junction temperature is greater than the thermal shutdown temperature

Table 1 shows the conditions that lead to the different modes of operation.

Table 1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER			
	V_{IN}	V_{EN}	I_{OUT}	T_J
Normal mode	$\|V_{IN}\| > \{ \|V_{OUT(nom)}\| + \|V_{DO}\|, \|V_{IN(min)}\| \}$	$\|V_{EN}\| < 0.7$ V	$I_{OUT} < I_{CL}$	$T_J < 125°C$
Dropout mode	$\|V_{IN(min)}\| < \|V_{IN}\| < \|V_{OUT(nom)}\| + \|V_{DO}\|$	$\|V_{EN}\| < 0.7$ V	—	$T_J < 125°C$
Disabled mode (any true condition disables the device)	—	$\|V_{EN}\| > 2$ V	—	$T_J > 170°C$

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS791 low-dropout (LDO) regulator is optimized for use in noise-sensitive battery-operated equipment. The device features extremely low dropout voltages, high PSRR, ultralow output noise, low quiescent current (170 µA typically), and an active-low, enable input to reduce supply currents to less than 1 µA when the regulator is turned off.

8.1.1 External Capacitor Requirements

A 0.1-µF or larger ceramic input bypass capacitor, connected between IN and GND and located close to the TPS791, is required for stability and to improve transient response, noise rejection, and ripple rejection. A higher-value electrolytic input capacitor may be necessary if large, fast-rise-time load transients are anticipated and the device is located several inches from the power source.

Like all low dropout regulators, the TPS791 requires an output capacitor connected between OUT and GND to stabilize the internal control loop. The minimum recommended capacitance is 1 µF. Any 1-µF or larger ceramic capacitor is suitable. The device is also stable with a 0.47-µF ceramic capacitor with at least 75 mΩ of ESR.

The internal voltage reference is a key source of noise in an LDO regulator. The TPS791 has a BYPASS pin that is connected to the voltage reference through a 250-kΩ internal resistor. The 250-kΩ internal resistor, in conjunction with an external bypass capacitor connected to the BYPASS pin, creates a low-pass filter to reduce the voltage reference noise and, therefore, the noise at the regulator output. In order for the regulator to operate properly, the current flow out of the BYPASS pin must be at a minimum because any leakage current creates an IR drop across the internal resistor thus creating an output error. Therefore, the bypass capacitor must have minimal leakage current.

For example, the TPS79118 exhibits approximately 15 μV_{RMS} of output voltage noise using a 0.1-µF ceramic bypass capacitor and a 1-µF ceramic output capacitor. The output starts up slower as the bypass capacitance increases because of the RC time constant at the bypass pin that is created by the internal 250-kΩ resistor and external capacitor.

8.2 Typical Application

Figure 35 shows a typical application circuit.

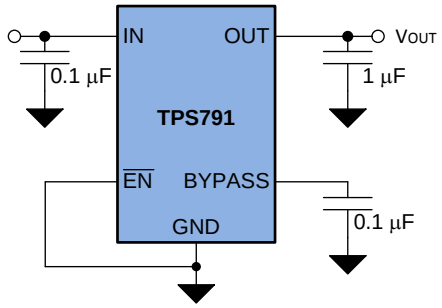

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Figure 35. Typical Application Circuit

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Typical Application (continued)

8.2.1 Design Requirements

Table 2 shows the parameters used for this design example.

Table 2. Design Parameters

PARAMETER	DESIGN REQUIREMENT
Input voltage	4.3 V to 3.5 V (Lithium Ion battery)
Output voltage	3.3 V
DC output current	10 mA
Peak output current	100 mA
Maximum ambient temperature	60°C

8.2.2 Detailed Design Procedure

Select the desired output voltage option. An input capacitor of 0.1 µF is used because the battery is connected to the input through a via and a short 10-mil (0.01-in) trace. An output capacitor of 1 mF is used in this design example. A smaller size output capacitor can be used up to a minimum of 1 µF to stabilize the internal control loop.

8.2.3 Application Curves

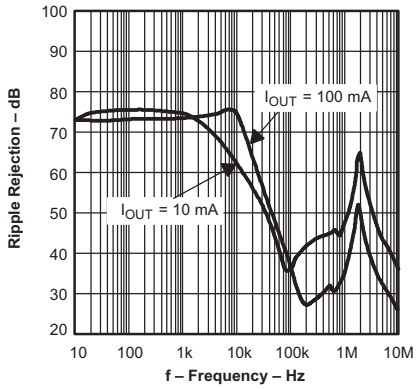

Figure 36. TPS79133 Ripple Rejection vs Frequency

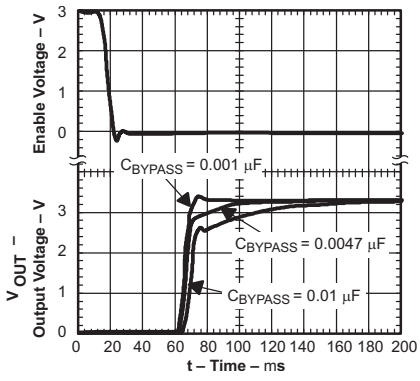

Figure 37. TPS79133 Output Voltage, Enable Voltage vs Time (Start-Up)

8.3 Do's and Don'ts

Do place at least one, low-ESR, 1-µF capacitor as close as possible between the OUT pin of the regulator and the GND pin.

Do place at least one, low-ESR, 0.1-µF capacitor as close as possible between the IN pin of the regulator and the GND pin.

Do provide adequate thermal paths away from the device.

Do not place the input or output capacitor more than 10 mm away from the regulator.

Do not exceed the absolute maximum ratings.

Do not float the Enable (EN) pin.

Do not resistively or inductively load the BYPASS pin.

Do not let the output voltage get more than 0.3 V above the input voltage.

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9 Power Supply Recommendations

This device is designed to operate from an input voltage supply range from 2.7 V to 5.5 V. The input voltage range must provide adequate headroom in order for the device to have a regulated output. This input supply must be well-regulated and stable. A 0.1-µF input capacitor is required for stability; if the input supply is noisy, additional input capacitors with low ESR can help improve the output noise performance.

10 Layout

10.1 Layout Guidelines

Layout is a critical part of good power-supply design. There are several signal paths that conduct fast-changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade the power-supply performance. To help eliminate these problems, bypass the IN pin to ground with a low ESR ceramic bypass capacitor with an X5R or X7R dielectric.

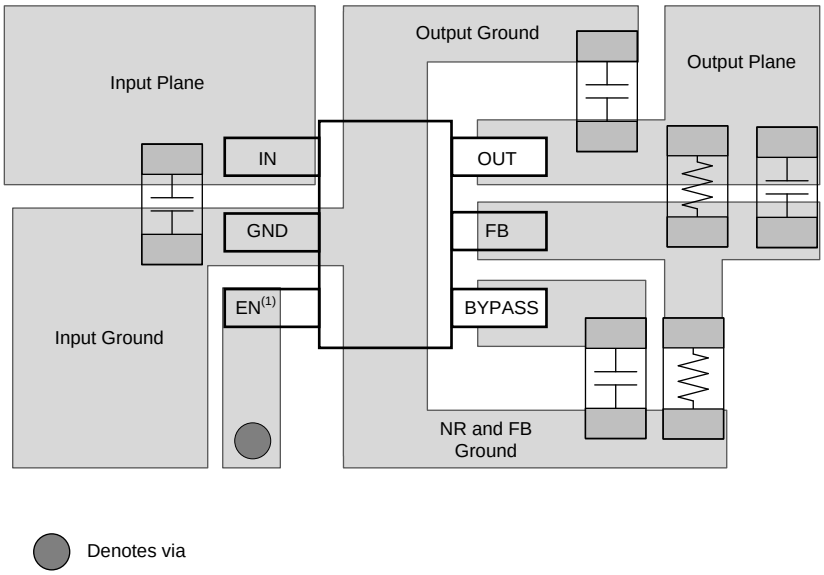
Equivalent series inductance (ESL) and equivalent series resistance (ESR) must be minimized to maximize performance and ensure stability. Every capacitor (C_{IN}, C_{OUT}, C_{BYPASS}, and C_1) must be placed as close as possible to the device and on the same side of the PCB as the regulator itself.

Do not place any capacitors on the opposite side of the PCB from where the regulator is installed. The use of vias and long traces is strongly discouraged because these circuits can impact system performance negatively, and even cause instability.

10.1.1 Board Layout Recommendation to Improve PSRR and Noise Performance

To improve ac measurements such as PSRR, output noise, and transient response, TI recommends that the board be designed with separate ground planes for V_{IN} and V_{OUT}, with each ground plane connected only at the ground pin of the device. In addition, connect the ground connection for the bypass capacitor directly to the ground pin of the device.

10.2 Layout Example



(1) The EN pin is active low.

Figure 38. Layout Example (6-Pin DBV Package)

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11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

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All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS79101DBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	PEUI	Samples
TPS79101DBVRG4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	PEUI	Samples
TPS79101DBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	PEUI	Samples
TPS79118DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	PERI	Samples
TPS79118DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	PERI	Samples
TPS79118DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	PERI	Samples
TPS79133DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	PESI	Samples
TPS79133DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	PESI	Samples
TPS79133DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	PESI	Samples
TPS79147DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	PETI	Samples
TPS79147DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	PETI	Samples
TPS79147DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	PETI	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF TPS791 :

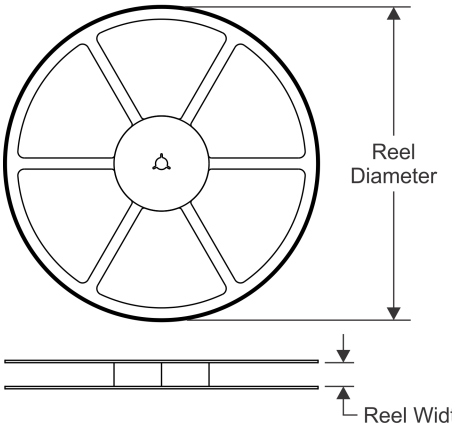
- Automotive: TPS791-Q1

NOTE: Qualified Version Definitions:

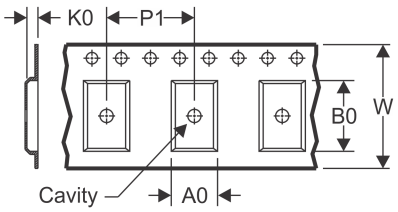
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

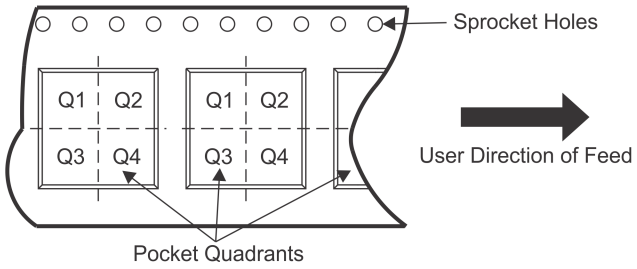


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

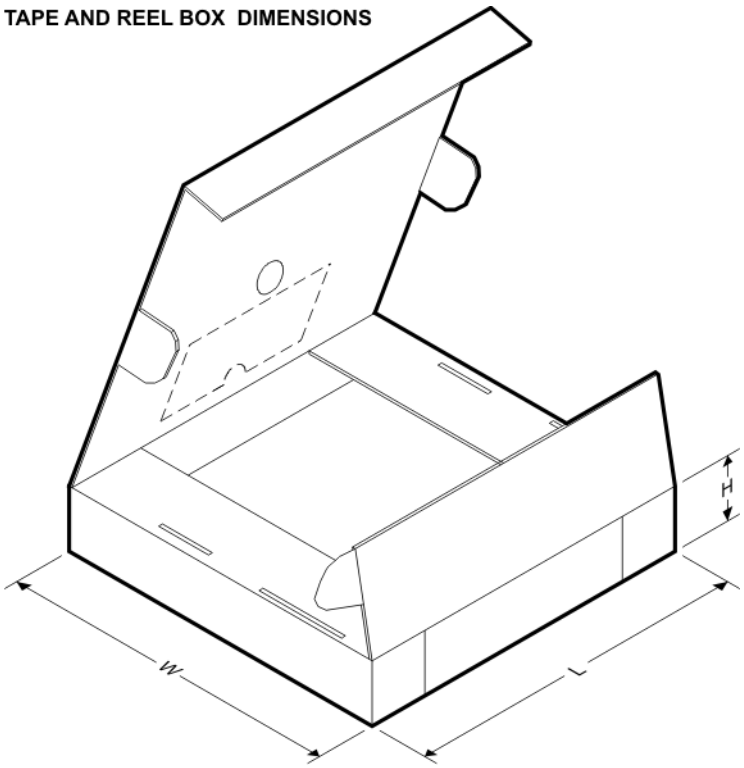
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS79101DBVR	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS79101DBVT	SOT-23	DBV	6	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS79118DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS79118DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS79133DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS79133DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS79147DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TPS79147DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

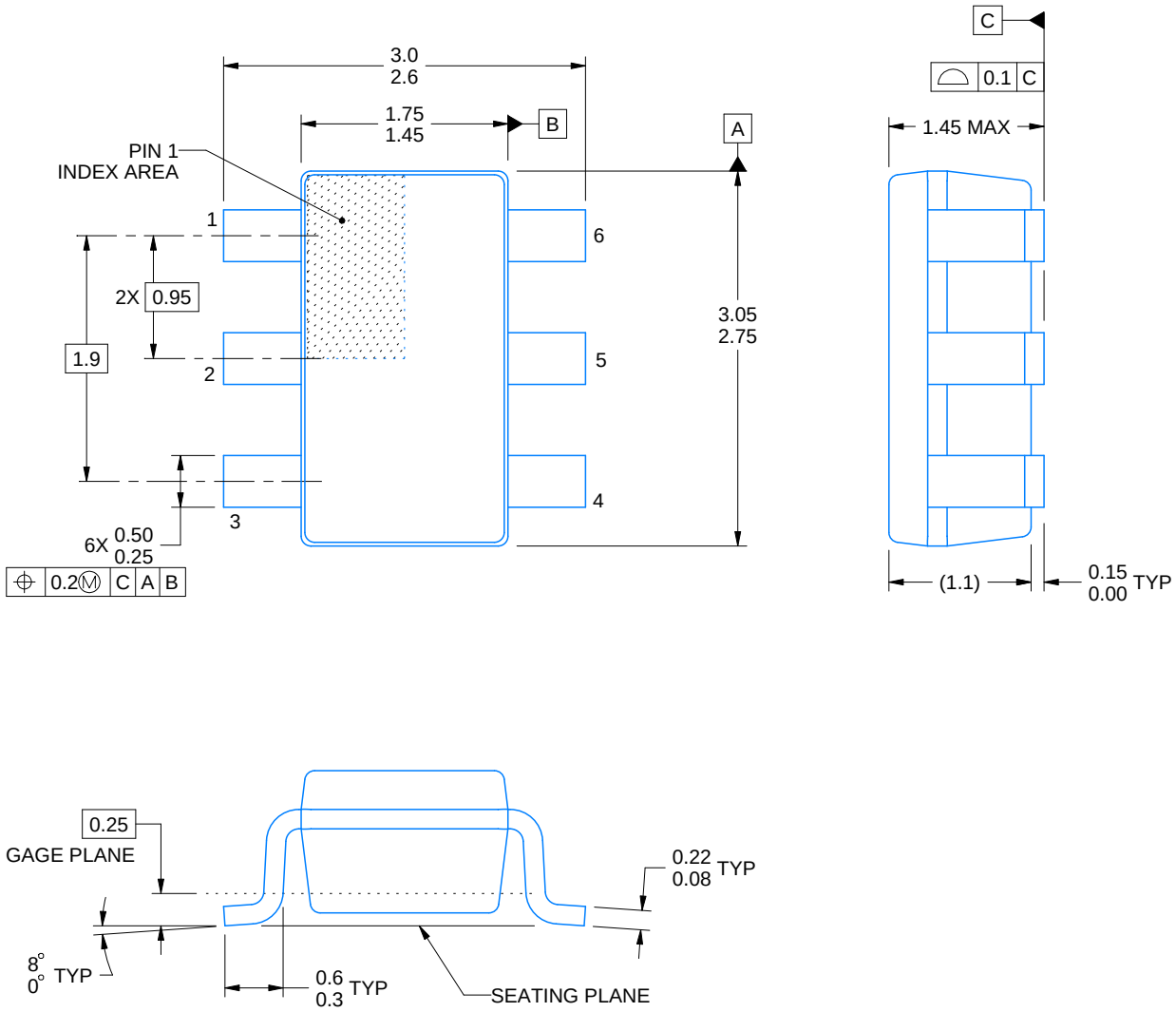
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS79101DBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0
TPS79101DBVT	SOT-23	DBV	6	250	180.0	180.0	18.0
TPS79118DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS79118DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS79133DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS79133DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS79147DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS79147DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

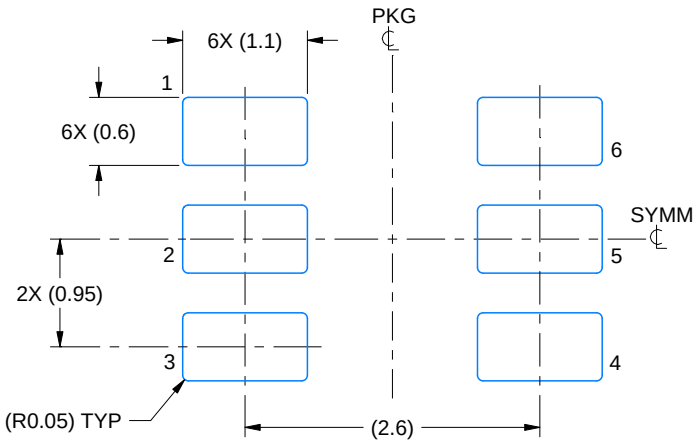
SMALL OUTLINE TRANSISTOR



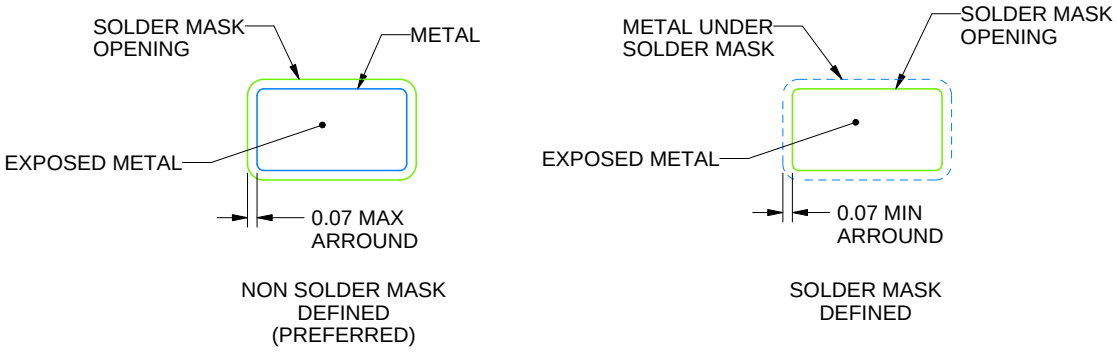
4214840/B 03/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

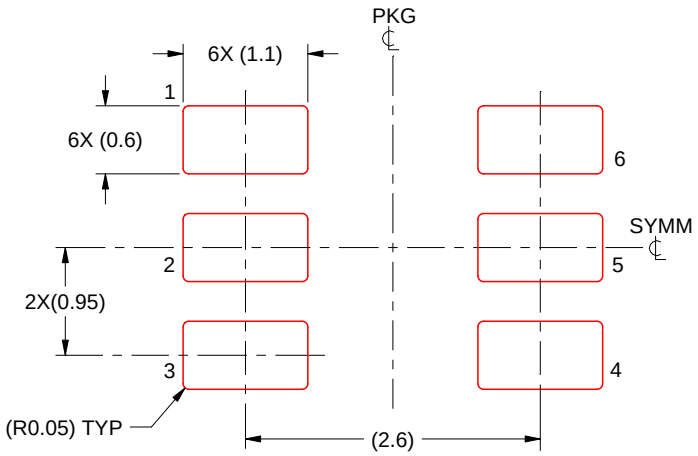


SOLDER MASK DETAILS

4214840/B 03/2018

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/B 03/2018

NOTES: (continued)

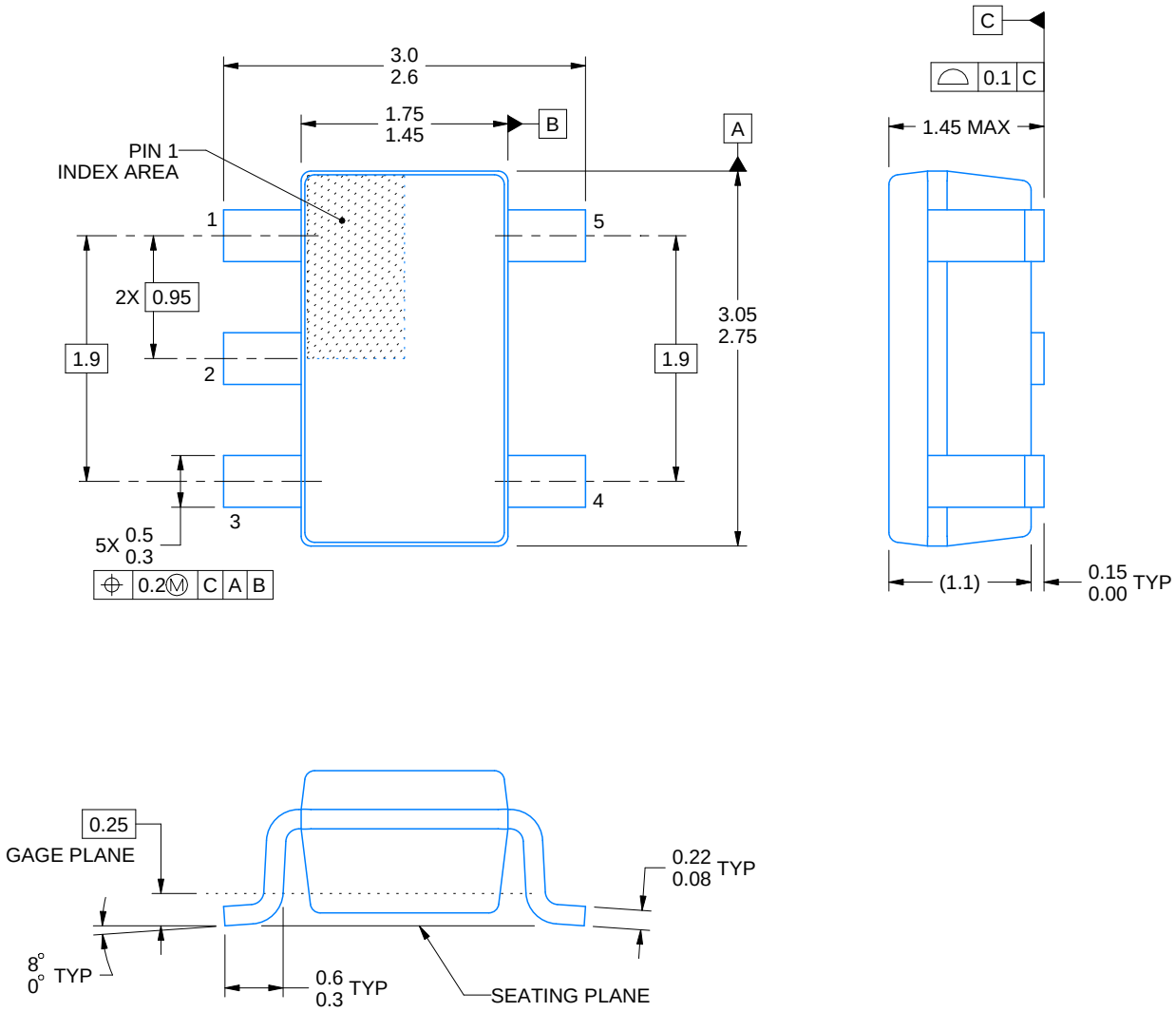
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

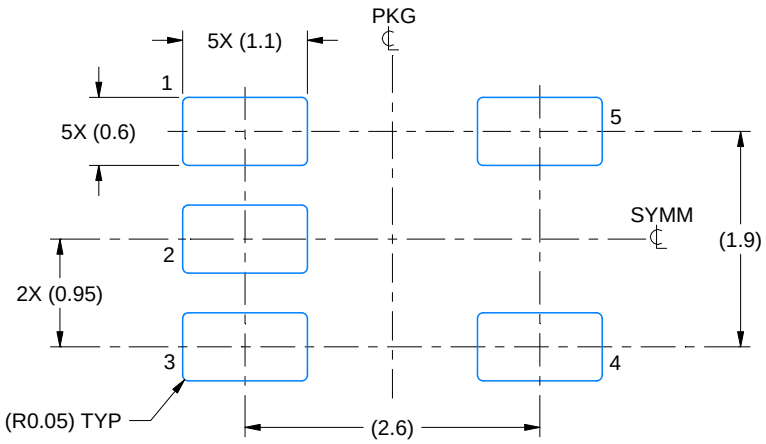
SMALL OUTLINE TRANSISTOR



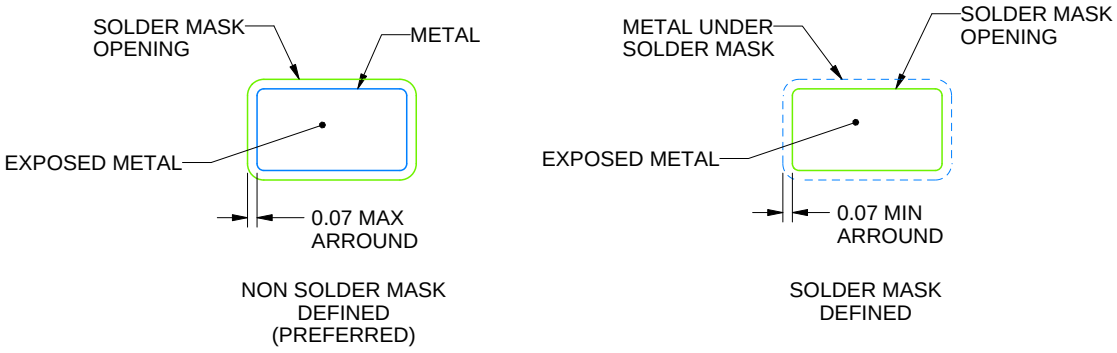
4214839/D 11/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/D 11/2018

NOTES: (continued)

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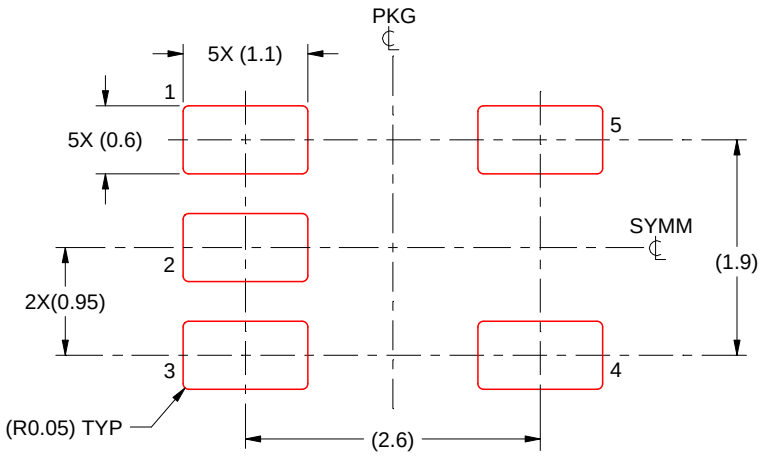
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/D 11/2018

NOTES: (continued)

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8. Board assembly site may have different recommendations for stencil design.

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