THE DATASHEET OF

TPS82675SIPT

TEXAS INSTRUMENTS

TPS82670, TPS82671, TPS82672, TPS82673, TPS82674, TPS82675, TPS82676
TPS82677, TPS826711, TPS826716, TPS826721, TPS826745, TPS826765, TPS8267195

SLVSAI0J – OCTOBER 2010 – REVISED MAY 2016

TPS8267x 600-mA, High-Efficiency MicroSiP™ Step-Down Converter (Profile <1.0mm)

1 Features

- 90% Efficiency at 5.5 MHz Operation
- 17µA Quiescent Current
- Wide V_{IN} Range From 2.3 V to 4.8 V
- 5.5MHz Regulated Frequency Operation
- Spread Spectrum, PWM Frequency Dithering
- *Best in Class* Load and Line Transient
- ±2% Total DC Voltage Accuracy
- Automatic PFM/PWM Mode Switching
- Low Ripple Light-Load PFM Mode
- ≥35dB V_{IN} PSRR (1kHz to 10kHz)
- Internal Soft Start, 120-µs Start-Up Time
- Integrated Active Power-Down Sequencing (Optional)
- Current Overload and Thermal Shutdown Protection
- Sub 1-mm Profile Solution
- Total Solution Size <6.7 mm^2

2 Applications

- Cell Phones, Smart-Phones
- Camera Module, Optical Data Module
- Wearable Electronics
- Digital TV, WLAN, GPS and Bluetooth™ Applications
- POL Applications

3 Description

The TPS8267x device is a complete 600mA, DC/DC step-down power supply intended for low-power applications. Included in the package are the switching regulator, inductor and input/output capacitors. No additional components are required to finish the design.

The TPS8267x is based on a high-frequency synchronous step-down dc-dc converter optimized for battery-powered portable applications. The MicroSiP™ DC/DC converter operates at a regulated 5.5-MHz switching frequency and enters the power-save mode operation at light load currents to maintain high efficiency over the entire load current range.

The PFM mode extends the battery life by reducing the quiescent current to 17µA (typ) during light load operation. For noise-sensitive applications, the device has PWM spread spectrum capability providing a lower noise regulated output, as well as low noise at the input. These features, combined with high PSRR and AC load regulation performance, make this device suitable to replace a linear regulator to obtain better power conversion efficiency.

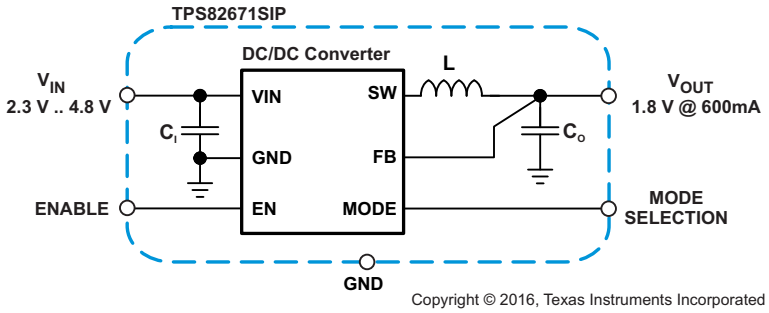
The TPS8267x is packaged in a compact (2.3mm x 2.9mm) and low profile (1.0mm) BGA package suitable for automated assembly by standard surface mount equipment.

Device Information[(1)]

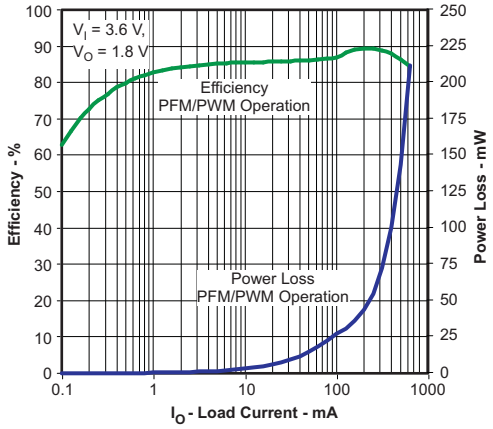
PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS8267x	µSIP (8)	2.30 x 2.90 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

4 Simplified Schematic



Efficiency vs Output Current



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5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision I (November 2014) to Revision J — **Page**

- Added TPS8267195 part number to data sheet ... 1
- Added TPS8267195 to Electrical Characteristics table ... 7
- Changed Layout Example figure, Note 4 value from "...less than 0.5 mm.." to "...less than 0.5 µm.." ... 21

Changes from Revision H (October 2014) to Revision I — **Page**

- Moved T_{stg} spec to Absolute Maximum Ratings table for clarification ... 5
- Changed Handling Ratings to ESD Ratings and replaced MIN/MAX values with ± VALUE for clarification ... 6
- Added TPS826716 data and removed Product Preview note. ... 7

Changes from Revision G (September 2014) to Revision H — **Page**

- Added TPS826716 to Device Comparison Table as Product Preview. ... 4

Changes from Revision F (November 2012) to Revision G — **Page**

- Added Device Information and Handling Rating tables, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section. ... 1
- Added device TPS826721 ... 4

Changes from Revision E (October 2012) to Revision F — **Page**

- Added TPS826745 to Header ... 1

Changes from Revision D (April 2012) to Revision E **Page**

- Added TPS826765 to Header 1

Changes from Revision C (November 2011) to Revision D **Page**

- Added devices TPS82670, TPS82673, and TPS82674 to Header 1

Changes from Revision B (August 2011) to Revision C **Page**

- Added device TPS82672 to Header info 1

Changes from Revision A (April 2011) to Revision B **Page**

- Added TPS82676 part number to data sheet header 1

Changes from Original (October 2010) to Revision A **Page**

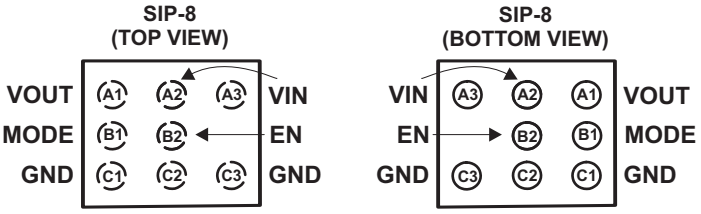
- Added devices TPS82677 and TPS82678 to Header info 1
- Added copyright attribution for spectrum illustrations 11

6 Device Comparison Table

PART NUMBER (1)	OUTPUT VOLTAGE	DEVICE SPECIFIC FEATURE	PACKAGE MARKING
TPS82670	1.86V	PWM Spread Spectrum Modulation Low PFM Output Ripple Voltage Output Capacitor Discharge	YK
TPS82671	1.8V	PWM Spread Spectrum Modulation Low PFM Output Ripple Voltage	RA
TPS826711	1.8V	PWM Spread Spectrum Modulation Low PFM Output Ripple Voltage Output Capacitor Discharge	YW
TPS826716	1.6V	PWM Spread Spectrum Modulation Low PFM Output Ripple Voltage	GS
TPS82672	1.5V	PWM Spread Spectrum Modulation Low PFM Output Ripple Voltage	WD
TPS826721	2.1V	PWM Spread Spectrum Modulation Low PFM Output Ripple Voltage	EO
TPS82673	1.26V	PWM Spread Spectrum Modulation Low PFM Output Ripple Voltage Output Capacitor Discharge	YL
TPS82674	1.2V	PWM Spread Spectrum Modulation Low PFM Output Ripple Voltage Output Capacitor Discharge	SW
TPS826745	1.225V	PWM Spread Spectrum Modulation Low PFM Output Ripple Voltage Output Capacitor Discharge	B5
TPS82675	1.2V	PWM Spread Spectrum Modulation Low PFM Output Ripple Voltage	RB
TPS82676	1.1V	PWM Spread Spectrum Modulation Low PFM Output Ripple Voltage Output Capacitor Discharge	TU
TPS826765	1.05V	PWM Spread Spectrum Modulation Low PFM Output Ripple Voltage Output Capacitor Discharge	AN
TPS82677	1.2V	Output Capacitor Discharge	SK
TPS8267195	1.95V	PWM Spread Spectrum Modulation Low PFM Output Ripple Voltage	4A

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com

7 Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
VOUT	A1	O	Power output pin. Apply output load between this pin and GND.
VIN	A2, A3	I	The VIN pins supply current to the TPS8267x internal regulator.
EN	B2	I	This is the enable pin of the device. Connect this pin to ground to force the converter into shutdown mode. Pull this pin to V_I to enable the device. This pin must not be left floating and must be terminated.
MODE	B1	I	This is the mode selection pin of the device. This pin must not be left floating and must be terminated.
			MODE = LOW: The device is operating in regulated frequency pulse width modulation mode (PWM) at high-load currents and in pulse frequency modulation mode (PFM) at light load currents.
			MODE = HIGH: Low-noise mode is enabled and regulated frequency PWM operation is forced.
GND	C1, C2, C3	–	Ground pin.

8 Specifications

8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_I (2)	Voltage at VIN(3)	–0.3	6	V
	Voltage at VIN (TPS826721)(3)	-0.3	5.5	
	Voltage at VOUT	–0.3	3.6	V
	Voltage at EN, MODE	–0.3	V_{IN} + 0.3	V
	Power dissipation	Internally limited		
T_A	Operating temperature range(4)	–40	85	°C
T_{INT} (max)	Maximum internal operating temperature		125	°C
T_{stg}	Storage temperature	–55	125	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.
(3) Operation above 4.8V input voltage for extended periods may affect device reliability.
(4) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature ($T_{A(max)}$) is dependent on the maximum operating temperature ($T_{INT(max)}$), the maximum power dissipation of the device in the application ($P_{D(max)}$), and the junction-to-ambient thermal resistance of the part/package in the application ($R_{\theta JA}$), as given by the following equation: $T_{A(max)} = T_{J(max)} - (R_{\theta JA} \times P_{D(max)})$. To achieve optimum performance, it is recommended to operate the device with a maximum internal temperature of 105°C.

8.2 ESD Ratings

		VALUE	UNIT
V_{ESD} (1)	Human body model (HBM) ESD stress voltage (2)	±2000	V
	Charge device model (CDM) ESD stress voltage (3)	±1000	
	Machine model (MM) ESD stress voltage (4)	±200	V

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges in to the device.
(2) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(3) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.
(4) The machine model is a 200-pF capacitor discharged directly into each pin.

8.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{IN}	Input voltage range		2.3		4.8 (1)	V
I_O	Output current range	TPS82671 to TPS826765	0		600	mA
	Additional output capacitance (PFM/PWM operation) (2)	TPS82670 to TPS82676 TPS826711, TPS826716, TPS826721, TPS826765, TPS8267195		0	2.5	µF
		TPS82677		0	4	µF
	Additional output capacitance (PWM operation) (2)			0	7	µF
T_A	Ambient temperature		–40		+85	°C
T_J	Operating junction temperature		–40		+125	°C

(1) Operation above 4.8V input voltage for extended periods may affect device reliability.
(2) In certain applications larger capacitor values can be tolerable, see *Output Capacitor Selection* section for more details.

8.4 Thermal Information

THERMAL METRIC (1)		TPS8267x SIP 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient (top) thermal resistance	125	°C/W
	Junction-to-ambient (bottom) thermal resistance	70	
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance	-	
$R_{\theta JB}$	Junction-to-board thermal resistance	-	
ψ_{JT}	Junction-to-top characterization parameter	-	
ψ_{JB}	Junction-to-board characterization parameter	-	
$R_{\theta JCbot}$	Junction-to-case (bottom) thermal resistance	-	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

8.5 Electrical Characteristics

Minimum and maximum values are at V_{IN} = 2.3V to 5.5V, V_{OUT} = 1.8V, EN = 1.8V, AUTO mode and T_A = –40°C to 85°C; Circuit of Parameter Measurement Information section (unless otherwise noted). Typical values are at V_{IN} = 3.6V, V_{OUT} = 1.8V, EN = 1.8V, AUTO mode and T_A = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
I_Q	Operating quiescent current	I_O = 0mA. Device not switching		17	40	µA
		I_O = 0mA. PWM operation		5.8		mA
I_{SD}	Shutdown current	EN = GND		0.5	5	µA
UVLO	Undervoltage lockout threshold	TPS8267195 only		2.08	2.14	V
		all other versions		2.05	2.1	

Electrical Characteristics (continued)

Minimum and maximum values are at V_{IN} = 2.3V to 5.5V, V_{OUT} = 1.8V, EN = 1.8V, AUTO mode and T_A = –40°C to 85°C; Circuit of Parameter Measurement Information section (unless otherwise noted). Typical values are at V_{IN} = 3.6V, V_{OUT} = 1.8V, EN = 1.8V, AUTO mode and T_A = 25°C (unless otherwise noted).

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
PROTECTION							
	Thermal shutdown				140		°C
	Thermal shutdown hysteresis				10		°C
I_{LIM}	Peak Input Current Limit				1100		mA
I_{SC}	Input current limit under short-circuit conditions		V_O shorted to ground		13.5		mA
ENABLE, MODE							
V_{IH}	High-level input voltage			1.0			V
V_{IL}	Low-level input voltage					0.4	V
I_{lkg}	Input leakage current		Input connected to GND or VIN		0.01	1.5	µA
OSCILLATOR							
f_{SW}	Oscillator frequency		I_O = 0mA. PWM operation	4.9	5.45	6.0	MHz
OUTPUT							
V_{OUT}	Regulated DC output voltage	TPS82670 TPS82671 TPS826711 TPS826716 TPS82672 TPS826721 TPS82673 TPS82674 TPS826745 TPS82675 TPS82676 TPS826765	2.5V ≤ V_I ≤ 4.8V, 0mA ≤ I_O ≤ 600 mA PFM/PWM operation	0.98×V_{NOM}	V_{NOM}	1.03×V_{NOM}	V
			2.5V ≤ V_I ≤ 5.5V, 0mA ≤ I_O ≤ 600 mA PFM/PWM operation	0.98×V_{NOM}	V_{NOM}	1.04×V_{NOM}	V
			2.5V ≤ V_I ≤ 5.5V, 0mA ≤ I_O ≤ 600 mA PWM operation	0.98×V_{NOM}	V_{NOM}	1.02×V_{NOM}	V
		TPS8267195	2.5V ≤ V_I ≤ 4.8V, 0mA ≤ I_O ≤ 600 mA PFM/PWM operation	0.975×V_{NOM}	V_{NOM}	1.035×V_{NOM}	V
			2.5V ≤ V_I ≤ 5.5V, 0mA ≤ I_O ≤ 600 mA PFM/PWM operation	0.975×V_{NOM}	V_{NOM}	1.045×V_{NOM}	V
			2.5V ≤ V_I ≤ 5.5V, 0mA ≤ I_O ≤ 600 mA PWM operation	0.975×V_{NOM}	V_{NOM}	1.025×V_{NOM}	V
		TPS82677	2.5V ≤ V_I ≤ 4.8V, 0mA ≤ I_O ≤ 600 mA PFM/PWM operation	0.98×V_{NOM}	V_{NOM}	1.04×V_{NOM}	V
			2.5V ≤ V_I ≤ 5.5V, 0mA ≤ I_O ≤ 600 mA PWM operation	0.98×V_{NOM}	V_{NOM}	1.02×V_{NOM}	V
	Line regulation		V_I = V_O + 0.5V (min 2.5V) to 5.5V, I_O = 200 mA		0.23		%/V
	Load regulation		I_O = 0mA to 600 mA. PWM operation		–0.00085		%/mA
	Feedback input resistance				480		kΩ
ΔV_O	Power-save mode ripple voltage	TPS82671 TPS826711	I_O = 1mA, V_O = 1.8V		19		mV_{PP}
		TPS826716	I_O = 1mA, V_O = 1.6V		19		mV_{PP}
		TPS826721	I_O = 1mA, V_O = 2.1V		19		mV_{PP}
		TPS82673 TPS82674 TPS826745 TPS82675	I_O = 1mA, V_O = 1.2V		16		mV_{PP}
		TPS82676	I_O = 1mA, V_O = 1.1V		16		mV_{PP}
		TPS826765	I_O = 1mA, V_O = 1.05V		16		mV_{PP}
		TPS82677	I_O = 1mA, V_O = 1.2V		25		mV_{PP}
	Start-up time	TPS82671 TPS826711	I_O = 0mA, Time from active EN to V_O		120		µs
r_{DIS}	Discharge resistor for power-down sequence		Devices featuring active discharge		70	150	Ω

8.6 Typical Characteristics

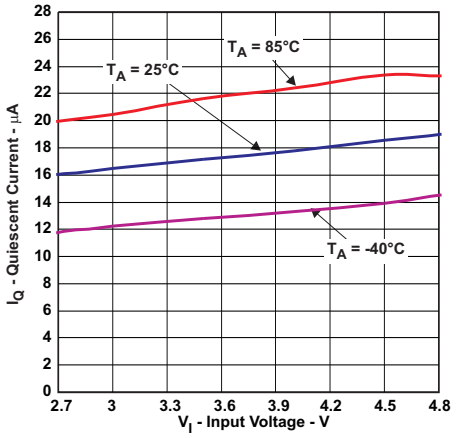
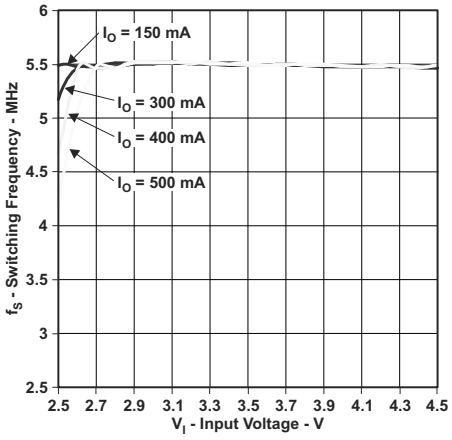
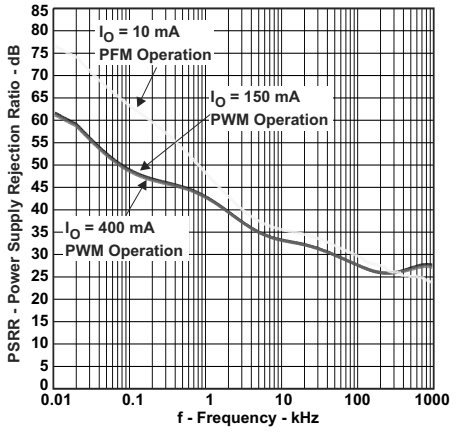


Figure 1. Quiescent Current vs. Input Voltage



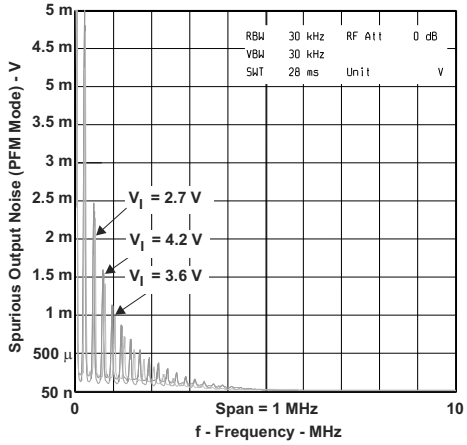
V_O = 1.8 V

Figure 2. PWM Switching Frequency vs. Input Voltage



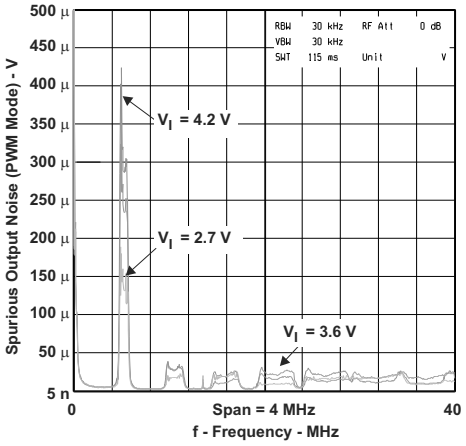
V_I = 3.6 V V_O = 1.8 V (TPS82671)

Figure 3. Power Supply Rejection Ratio vs. Frequency



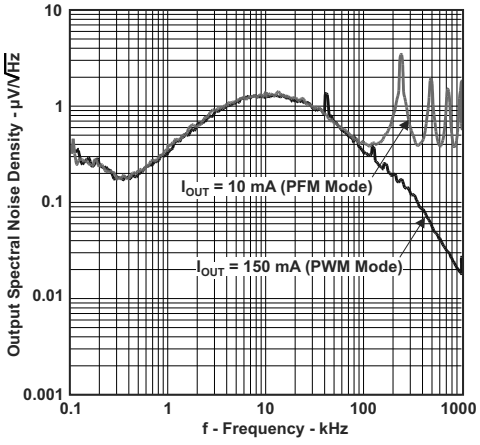
V_O = 1.8 V R_L = 150 Ω (TPS82671)

Figure 4. Spurious Output Noise (PFM Mode) vs. Frequency



V_O = 1.8 V R_L = 12 Ω (TPS82671)

Figure 5. Spurious Output Noise (PWM Mode) vs. Frequency



V_I = 3.6 V V_O = 1.8 V (TPS82671)

Figure 6. Output Spectral Noise Density vs. Frequency

9 Detailed Description

9.1 Overview

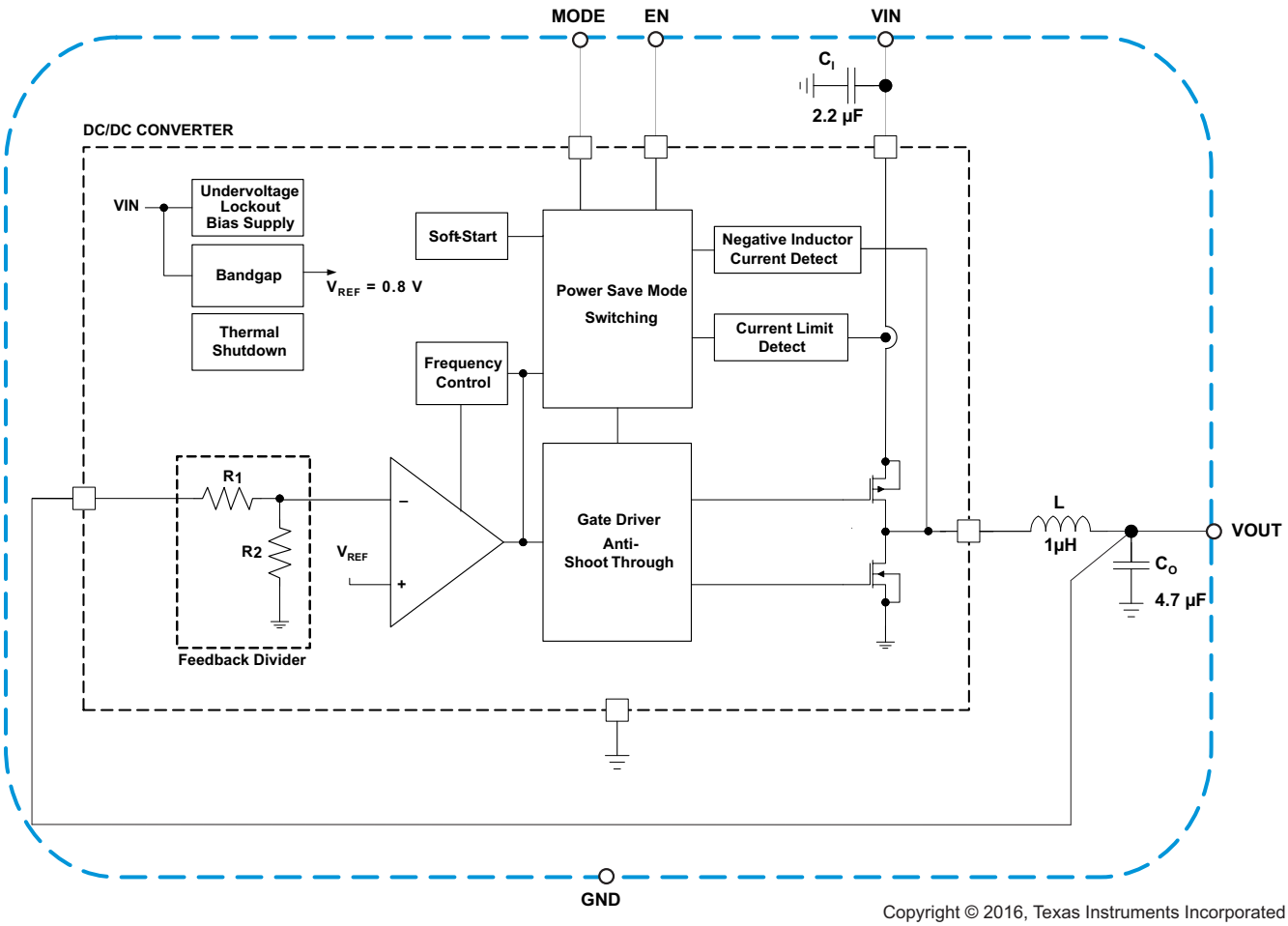
The TPS8267x is a stand-alone, synchronous, step-down converter. The converter operates at a regulated 5.5-MHz frequency pulse width modulation (PWM) at moderate to heavy load currents. At light load currents, the TPS8267x converter operates in power-save mode with pulse frequency modulation (PFM).

The converter uses a unique frequency-locked ring-oscillating modulator to achieve *best-in-class* load and line response. One key advantage of the non-linear architecture is that there is no traditional feed-back loop. The loop response to change in V_O is essentially instantaneous, which explains the transient response. Although this type of operation normally results in a switching frequency that varies with input voltage and load current, an internal frequency lock loop (FLL) holds the switching frequency constant over a large range of operating conditions.

Combined with *best-in-class* load and line-transient response characteristics, the low quiescent current of the device (approximately 17µA) helps to maintain high efficiency at light load while that current preserves a fast transient response for applications that require tight output regulation.

The TPS8267x integrates an input current limit to protect the device against heavy load or short circuits and features an undervoltage lockout circuit to prevent the device from misoperation at low input voltages. Fully functional operation is permitted down to 2.1V input voltage.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Power-Save Mode

If the load current decreases, the converter enters power-save mode automatically. During power-save mode, the converter operates in discontinuous current, (DCM) single-pulse PFM mode, which produces a low output ripple compared with other PFM architectures.

When in power-save mode, the converter resumes its operation when the output voltage falls below the nominal voltage. The converter ramps up the output voltage with a minimum of one pulse and goes into power-save mode when the output voltage is within its regulation limits.

The IC exits PFM mode and enters PWM mode when the output current can no longer be supported in PFM mode. As a consequence, the DC output voltage is typically positioned approximately 0.5% above the nominal output voltage. The transition between PFM and PWM is seamless.

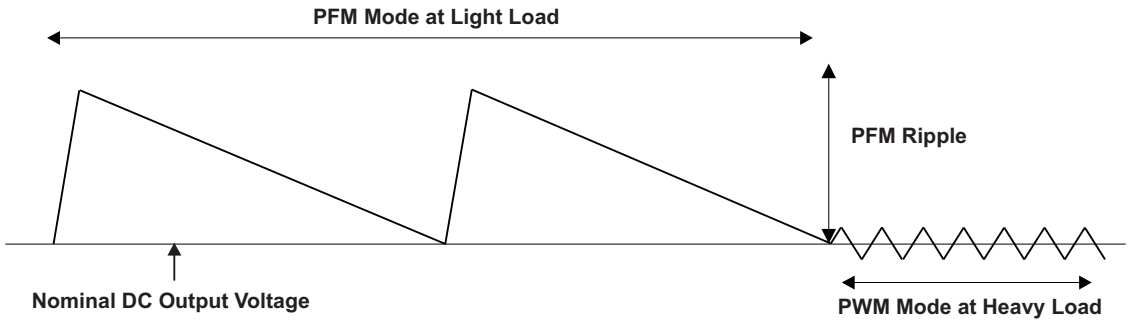


Figure 7. Operation In PFM Mode And Transfer To PWM Mode

9.3.2 Mode Selection

The MODE pin selects the operating mode of the device. Connecting the MODE pin to GND enables the automatic PWM and power-save mode operation. The converter operates in regulated frequency PWM mode at moderate to heavy loads, and operates in PFM mode during light loads. This type of operation maintains high efficiency over a wide load current range.

Pulling the MODE pin high forces the converter to operate in PWM mode even at light-load currents. The advantage is that the converter modulates its switching frequency according to a spread spectrum PWM modulation technique that allows simple filtering of the switching harmonics in noise-sensitive applications. In this mode, the efficiency is lower when compared to the power-save mode during light loads.

For additional flexibility, it is possible to switch from power-save mode to PWM mode during operation. This type of operation allows efficient power management by adjusting the operation of the converter to the specific system requirements.

9.3.3 Spread Spectrum, PWM Frequency Dithering

The goal of spread spectrum architecture is to spread out the emitted RF energy over a larger frequency range so that any resulting electromagnetic interference (EMI) is similar to white noise. The end result is a spectrum that is continuous and lower in peak amplitude. Spread spectrum makes it easier to comply with EMI standards. It also makes it easier to comply with the power supply ripple requirements in cellular and non-cellular wireless applications. Radio receivers are typically susceptible to narrowband noise that is focused on specific frequencies.

Switching regulators can be particularly troublesome in applications where electromagnetic interference (EMI) is a concern. Switching regulators operate on a cycle-by-cycle basis to transfer power to an output. In most cases, the frequency of operation is either fixed or regulated, based on the output load. This method of conversion creates large components of noise at the frequency of operation (fundamental) and multiples of the operating frequency (harmonics).

Feature Description (continued)

The spread spectrum architecture varies the switching frequency by approximately ±10% of the nominal switching frequency, thereby significantly reduces the peak radiated and conducting noise on both the input and output supplies. The frequency dithering scheme is modulated with a triangle profile and a modulation frequency f_m.

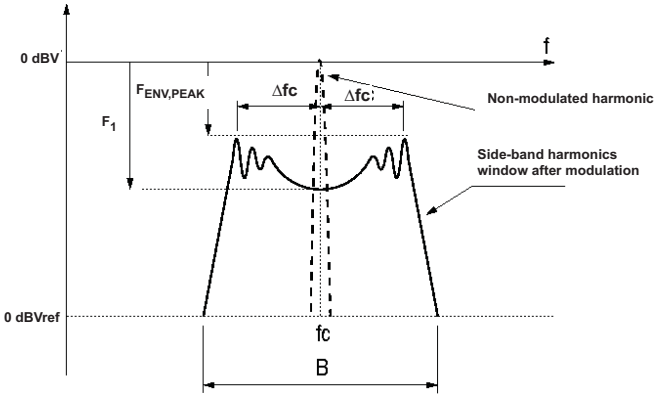


Figure 8. Spectrum Of A Frequency Modulated Sin. Wave With Sinusoidal Variation In Time

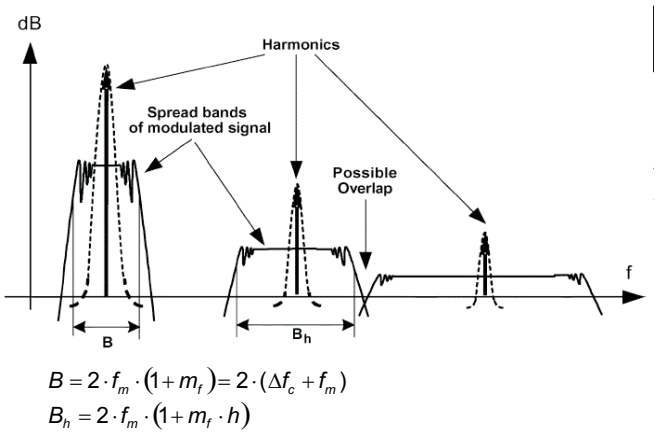


Figure 9. Spread Bands Of Harmonics In Modulated Square Signals (1)

Figure 8 and Figure 9 show that after modulation the sideband harmonic is attenuated when compared to the non-modulated harmonic, and when the harmonic energy is spread into a certain frequency band. The higher the modulation index (*mf*) the larger the attenuation.

$$m_f = \frac{\delta \times f_c}{f_m} \tag{1}$$

With:

- f_c is the carrier frequency (i.e. nominal switching frequency)
- f_m is the modulating frequency (approx. 0.016*f_c)
- δ is the modulation ratio (approx 0.1)

$$\delta = \frac{\Delta f_c}{f_c} \tag{2}$$

The maximum switching frequency is limited by the process and by the parameter modulation ratio (δ), together with f_m, which is the bandwidth of the side-band harmonics around the carrier frequency f_c. The bandwidth of a frequency modulated waveform is approximately given by the Carson's rule and can be summarized as:

$$B = 2 \times f_m \times (1 + m_f) = 2 \times (\Delta f_c + f_m) \tag{3}$$

f_m < RBW: The receiver is not able to distinguish individual side-band harmonics; so, several harmonics are added in the input filter and the measured value is higher than expected in theoretical calculations.

f_m > RBW: The receiver is able to properly measure each individual side-band harmonic separately, so that the measurements match the theoretical calculations.

(1) Spectrum illustrations and formulae (Figure 8 and Figure 9) copyright *IEEE TRANSACTIONS ON ELECTROMAGNETIC COMPATIBILITY, VOL. 47, NO.3, AUGUST 2005.* See References Section for full citation.

9.4 Device Functional Modes

9.4.1 Enable

The TPS8267x device starts operation when EN is set high and starts up with the soft start as previously described. For proper operation, the EN pin must be terminated and must not be left floating.

Pulling the EN pin low forces the device into shutdown. In this mode, all internal circuits are turned off and the V_{IN} current reduces to the device leakage current, which is typically a few hundred nanoamps.

The TPS8267x device can actively discharge the output capacitor when it turns off. The integrated discharge resistor has a typical resistance of 100 Ω. The required time to ramp down the output voltage depends on the load current and the capacitance present at the output node.

9.4.2 Soft Start

The TPS8267x has an internal soft-start circuit that limits the in-rush current during start-up. This circuit limits input voltage drop when a battery or a high-impedance power source is connected to the input of the MicroSiP™ DC/DC converter.

The soft-start system progressively increases the switching on-time from a minimum pulse-width of 35ns as a function of the output voltage. This mode of operation continues for approximately 100µs after the enable. If the output voltage does not reach its target value within the soft-start time, the soft-start transitions to a second mode of operation.

If the output voltage rises above approximately 0.5V, the converter increases the input current limit and thus enables the power supply to come up properly. The start-up time mainly depends on the capacitance present at the output node and the load current.

10 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The TPS8267x devices are complete power supply modules, not needing further external devices. The devices are optimized to work best with the components populated. However application conditions might demand for different input and/or output capacitance values.

10.2 Typical Application

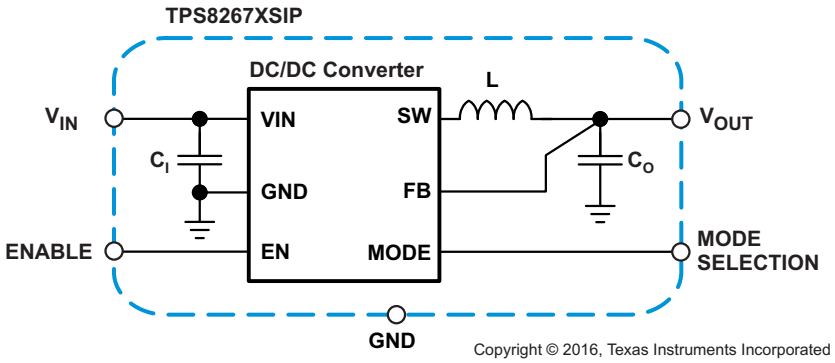


Figure 10. MicroSIP Converter Module Schematic

10.2.1 Design Requirements

For applications requiring additional input and/or output capacitance, the following procedures should be considered. For the maximum recommended values see *Recommended Operating Conditions*.

10.2.2 Detailed Design Procedure

10.2.2.1 Input Capacitor Selection

Because of the pulsating input current nature of the buck converter, a low ESR input capacitor is required to prevent large voltage transients that can cause misbehavior of the device or interference in other circuits in the system.

For most applications, the input capacitor that is integrated into the TPS8267x should be sufficient. If the application exhibits a noisy or erratic switching frequency, experiment with additional input ceramic capacitance to find a remedy.

The TPS8267x uses a tiny ceramic input capacitor. When a ceramic capacitor is combined with trace or cable inductance, such as from a wall adapter, a load step at the output can induce ringing at the VIN pin. This ringing can couple to the output and be mistaken as loop instability or can even damage the part. In this circumstance, additional "bulk" capacitance, such as electrolytic or tantalum, should be placed between the input of the converter and the power source lead to reduce ringing that can occur between the inductance of the power source leads and C_I.

10.2.2.2 Output Capacitor Selection

The advanced, fast-response, voltage mode, control scheme of the TPS8267x allows the use of a tiny ceramic output capacitor (C_O). For most applications, the output capacitor integrated in the TPS8267x is sufficient.

Typical Application (continued)

At nominal load current, the device operates in PWM mode; the overall output voltage ripple is the sum of the voltage step that is caused by the output capacitor ESL and the ripple current that flows through the output capacitor impedance. At light loads, the output capacitor limits the output ripple voltage and provides holdup during large load transitions.

The TPS8267x is designed as a Point-Of-Load (POL) regulator, to operate stand-alone without requiring any additional capacitance. Adding a 2.2µF ceramic output capacitor (X7R or X5R dielectric) generally works from a converter stability point of view, but does not necessarily help to minimize the output ripple voltage.

For best operation (i.e. optimum efficiency over the entire load current range, proper PFM/PWM auto transition), the TPS8267xSIP requires a minimum output ripple voltage in PFM mode. The typical output voltage ripple is ca. 1% of the nominal output voltage V_O. The PFM pulses are time controlled resulting in a PFM output voltage ripple and PFM frequency that depends (first order) on the capacitance seen at the MicroSiP™ DC/DC converter's output.

In applications requiring additional output bypass capacitors located close to the load, care should be taken to ensure proper operation. If the converter exhibits marginal stability or erratic switching frequency, experiment with additional low value series resistance (e.g. 50 to 100mΩ) in the output path to find a remedy.

Because the damping factor in the output path is directly related to several resistive parameters (e.g. inductor DCR, power-stage $r_{DS(on)}$, PWB DC resistance, load switches $r_{DS(on)}$ …) that are temperature dependant, the converter small and large signal behavior must be checked over the input voltage range, load current range and temperature range.

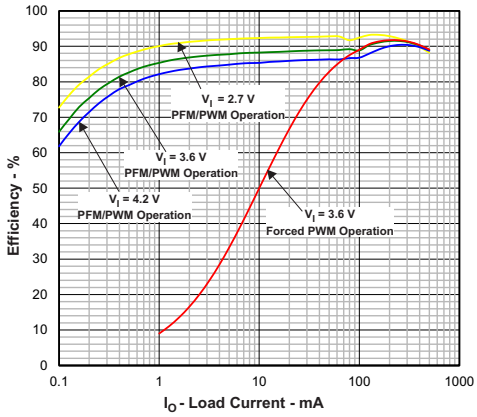
The easiest sanity test is to evaluate, directly at the converter’s output, the following aspects:

- PFM/PWM efficiency
- PFM/PWM and forced PWM load transient response

During the recovery time from a load transient, the output voltage can be monitored for settling time, overshoot or ringing that helps judge the converter’s stability. Without any ringing, the loop has usually more than 45° of phase margin.

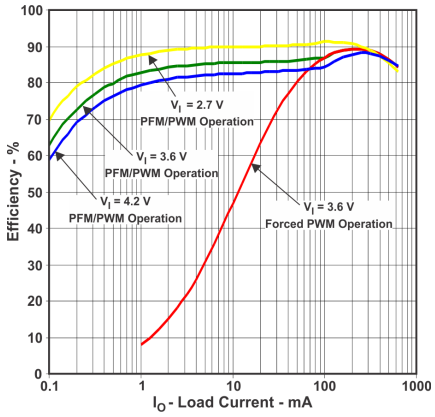
Typical Application (continued)

10.2.3 Application Curves



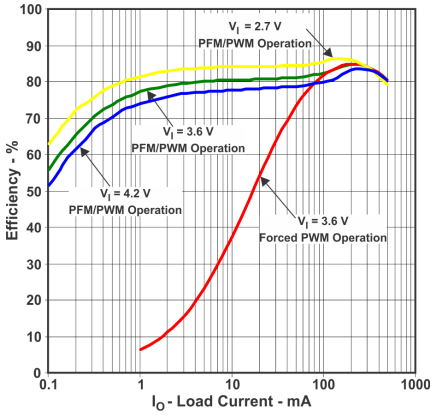
V_O = 1.95V

Figure 11. Efficiency vs. Load Current



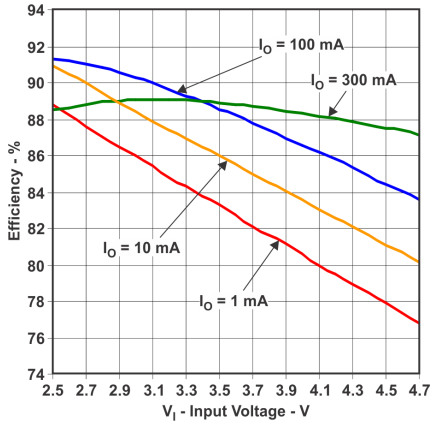
V_O = 1.8 V

Figure 12. Efficiency vs. Load Current



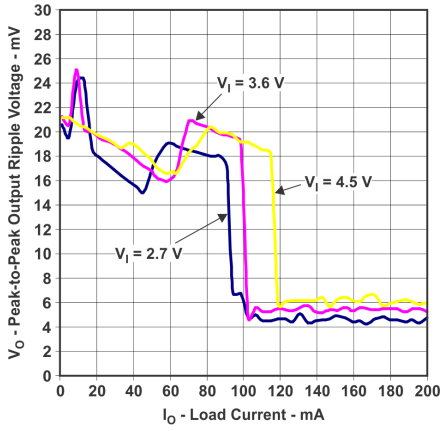
V_O = 1.2 V

Figure 13. Efficiency vs. Load Current



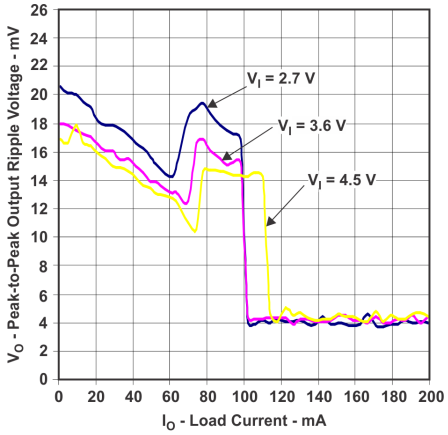
V_O = 1.8 V PFM/PWM Operation

Figure 14. Efficiency vs. Input Voltage



V_O = 1.8 V PFM/PWM Operation (TPS82671)

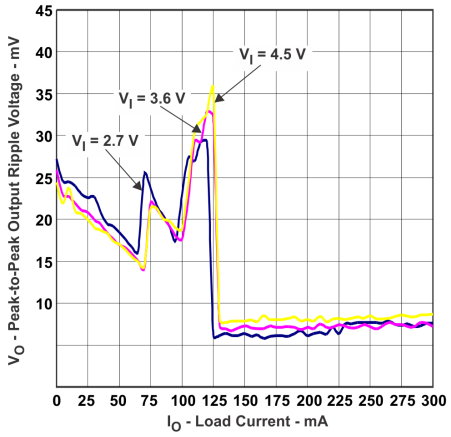
Figure 15. Peak-to-Peak Output Ripple Voltage vs. Load Current



V_O = 1.2 V PFM/PWM Operation (TPS82675)

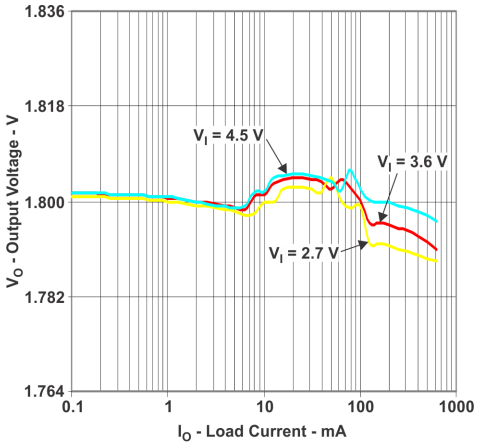
Figure 16. Peak-to-Peak Output Ripple Voltage vs. Load Current

Typical Application (continued)



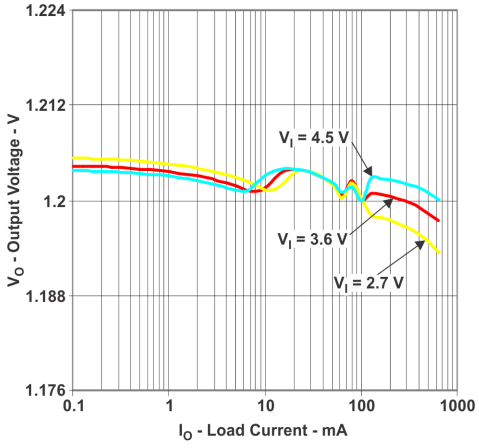
V_O = 1.2 V (TPS82671)

Figure 17. Peak-to-Peak Output Ripple Voltage vs. Load Current



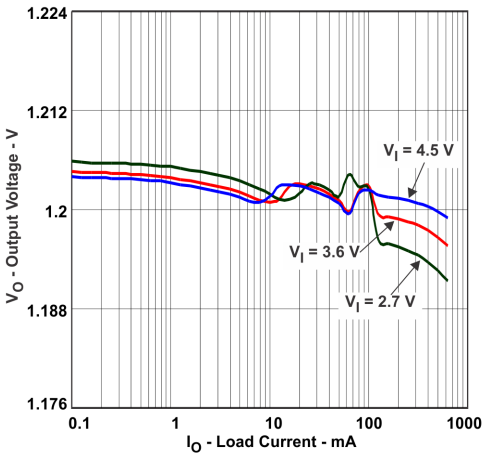
V_O = 1.8 V PFM/PWM Operation (TPS82671)

Figure 18. DC Output Voltage vs. Load Current



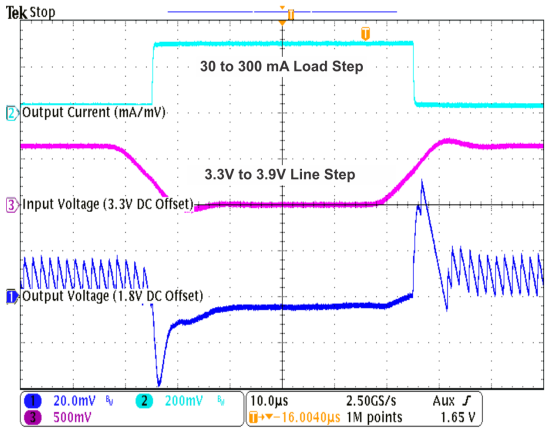
V_O = 1.2 V (TPS82675)

Figure 19. DC Output Voltage vs. Load Current



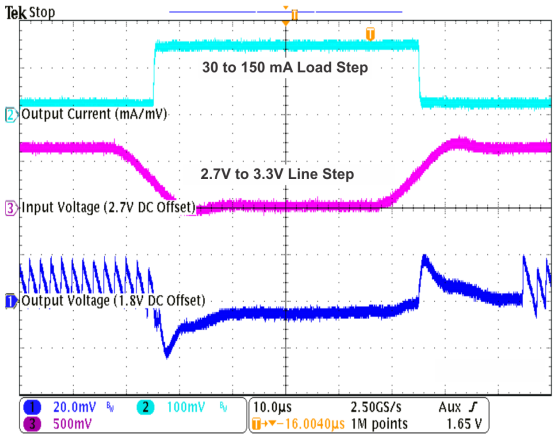
V_O = 1.2 V PFM/PWM Operation (TPS82677)

Figure 20. DC Output Voltage vs. Load Current



V_O = 1.8 V MODE = Low (TPS82671)

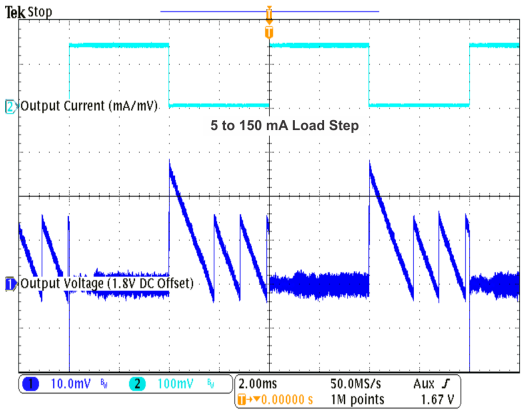
Figure 21. Combined Line/Load Transient Response



V_O = 1.8 V MODE = Low (TPS82671)

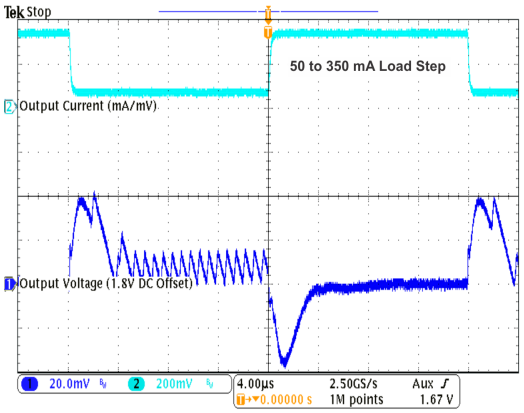
Figure 22. Combined Line/Load Transient Response

Typical Application (continued)



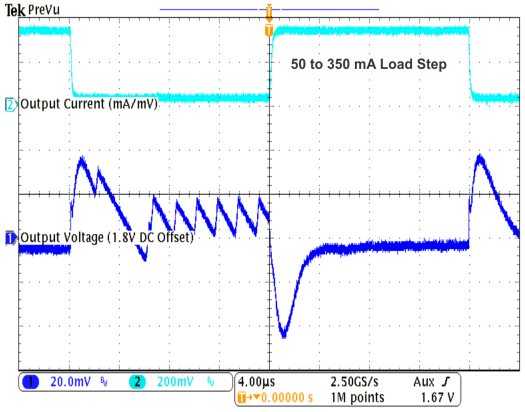
V_O = 1.8 V V_I = 3.6 V MODE = Low (TPS82671)

Figure 23. Load Transient Response in PFM/PWM Operation



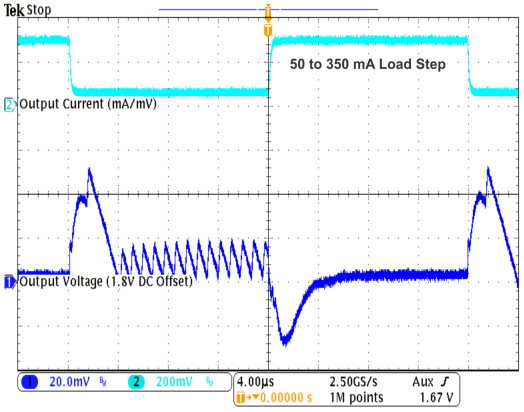
V_O = 1.8 V V_I = 3.6 V MODE = Low (TPS82671)

Figure 24. Load Transient Response in PFM/PWM Operation



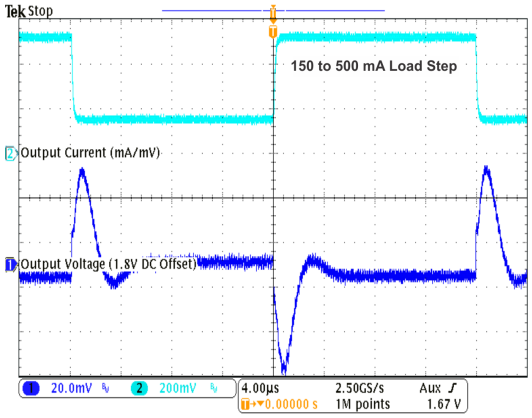
V_O = 1.8 V V_I = 2.7 V MODE = Low (TPS82671)

Figure 25. Load Transient Response in PFM/PWM Operation



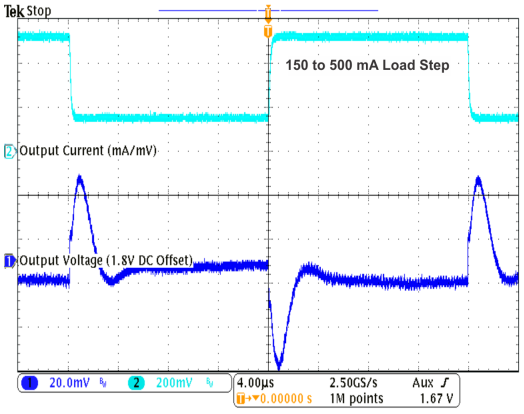
V_O = 1.8 V V_I = 4.5 V MODE = Low (TPS82671)

Figure 26. Load Transient Response in PFM/PWM Operation



V_O = 1.8 V V_I = 3.6 V MODE = Low (TPS82671)

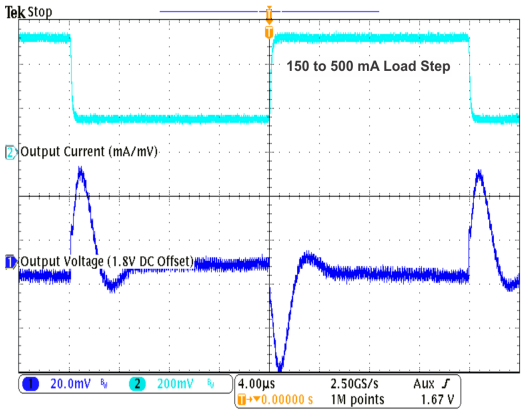
Figure 27. Load Transient Response in PFM/PWM Operation



V_O = 1.8 V V_I = 2.7 V MODE = Low (TPS82671)

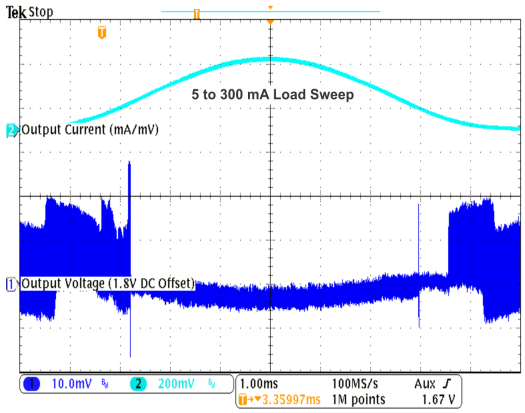
Figure 28. Load Transient Response in PFM/PWM Operation

Typical Application (continued)



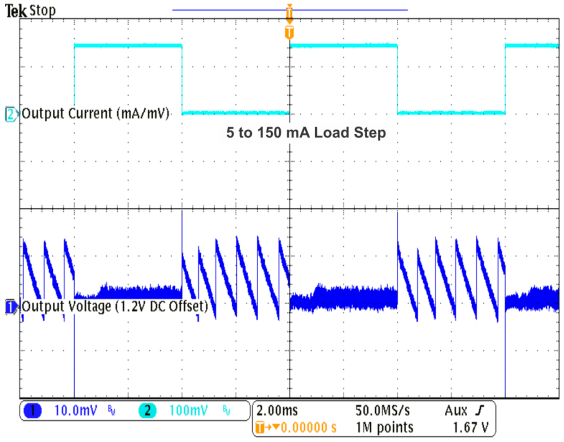
V_O = 1.8 V V_I = 4.5 V MODE = Low (TPS82671)

Figure 29. Load Transient Response in PFM/PWM Operation



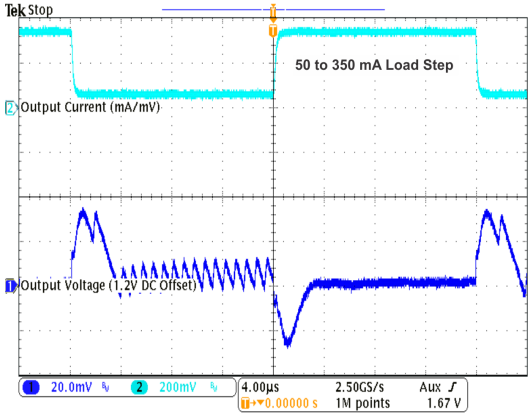
V_O = 1.8 V V_I = 3.6 V MODE = Low (TPS82671)

Figure 30. AC Load Transient Response



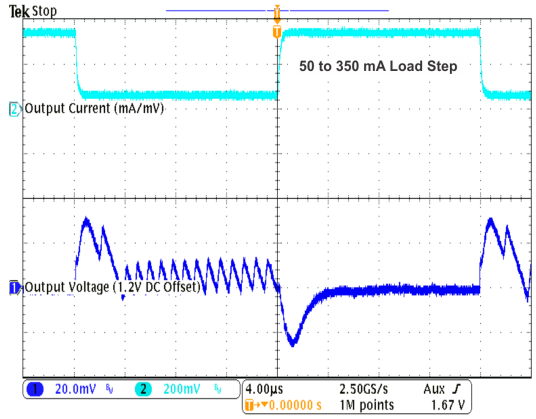
V_O = 1.2 V V_I = 3.6 V MODE = Low

Figure 31. Load Transient Response in PFM/PWM Operation



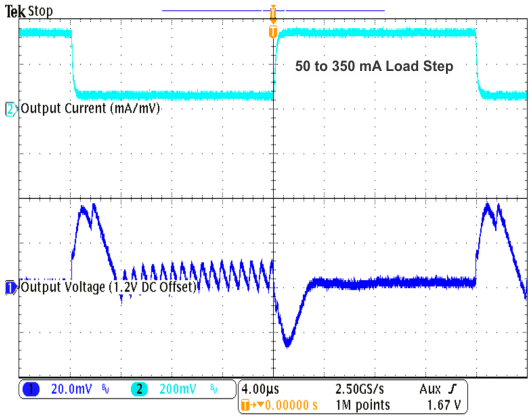
V_O = 1.2 V V_I = 3.6 V MODE = Low

Figure 32. Load Transient Response in PFM/PWM Operation



V_O = 1.2 V V_I = 2.7 V MODE = Low

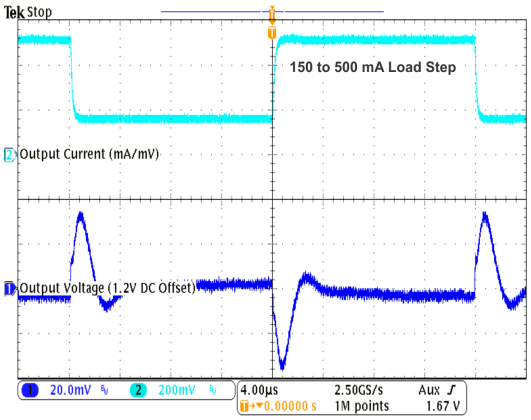
Figure 33. Load Transient Response in PFM/PWM Operation



V_O = 1.2 V V_I = 4.5 V MODE = Low

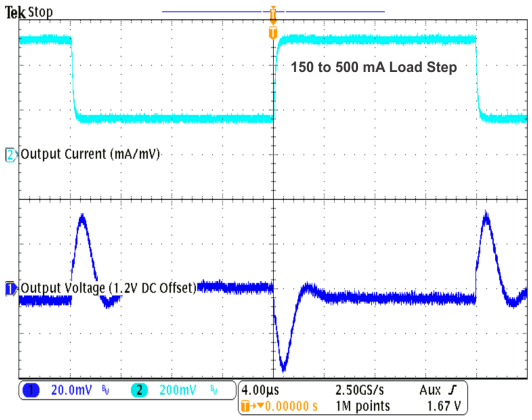
Figure 34. Load Transient Response in PFM/PWM Operation

Typical Application (continued)



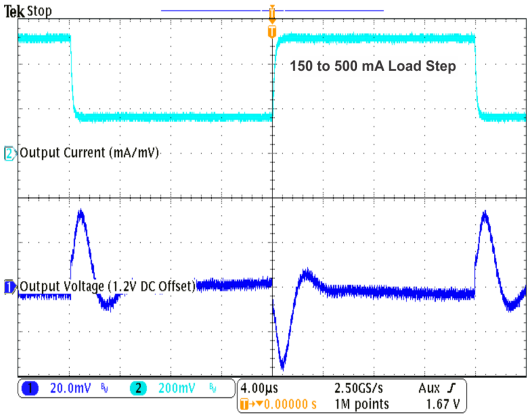
V_O = 1.2 V V_I = 3.6 V MODE = Low

Figure 35. Load Transient Response in PFM/PWM Operation



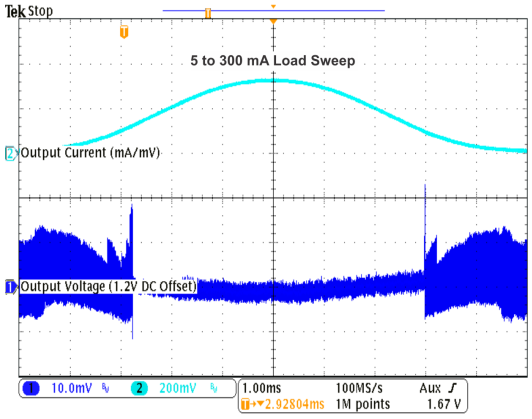
V_O = 1.2 V V_I = 2.7 V MODE = Low

Figure 36. Load Transient Response in PFM/PWM Operation



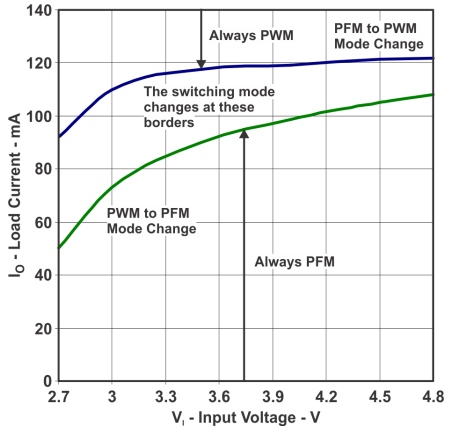
V_O = 1.2 V V_I = 4.5 V MODE = Low (TPS82671)

Figure 37. Load Transient Response in PFM/PWM Operation



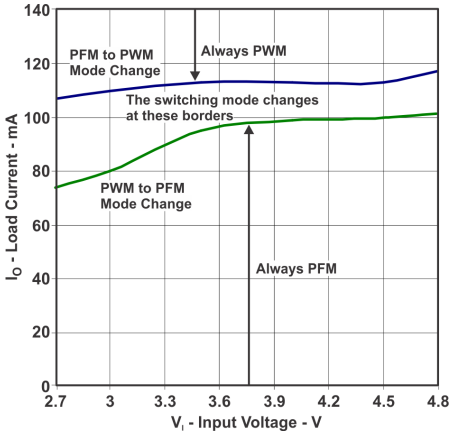
V_O = 1.2 V V_I = 3.6 V MODE = Low (TPS82671)

Figure 38. AC Load Transient Response



V_O = 1.8 V (TPS82671)

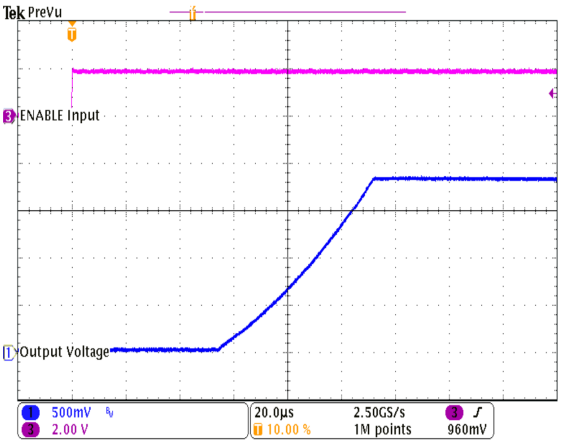
Figure 39. PFM/PWM Boundaries



V_O = 1.2 V (TPS82674)

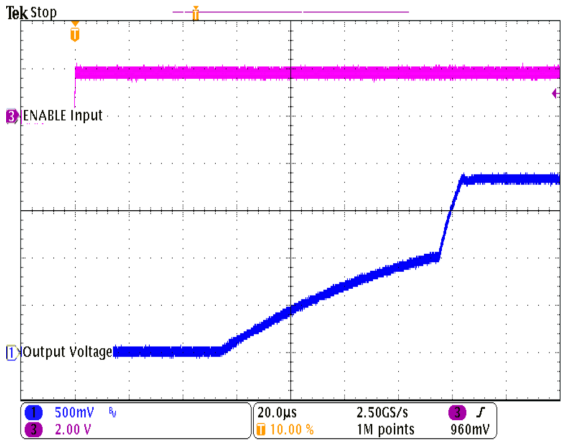
Figure 40. PFM/PWM Boundaries

Typical Application (continued)



V_O = 1.8 V V_I = 3.6 V I_O = 0 mA
MODE = Low

Figure 41. Start-Up



V_O = 1.8 V V_I = 3.6 V (TPS82671)
R_L = 100 Ω MODE = Low

Figure 42. Start-Up

11 Power Supply Recommendations

The TPS8267X devices are designed to operate from a 2.3-V to 4.8-V input voltage supply. The input power supply's output current needs to be rated according to the output voltage and the output current of the power rail application.

12 Layout

12.1 Layout Guidelines

In making the pad size for the µSiP LGA balls, it is recommended that the layout use non-solder-mask defined (NSMD) land. With this method, the solder mask opening is made larger than the desired land area, and the opening size is defined by the copper pad width. Figure 43 shows the appropriate diameters for a MicroSiP™ layout.

12.2 Layout Example

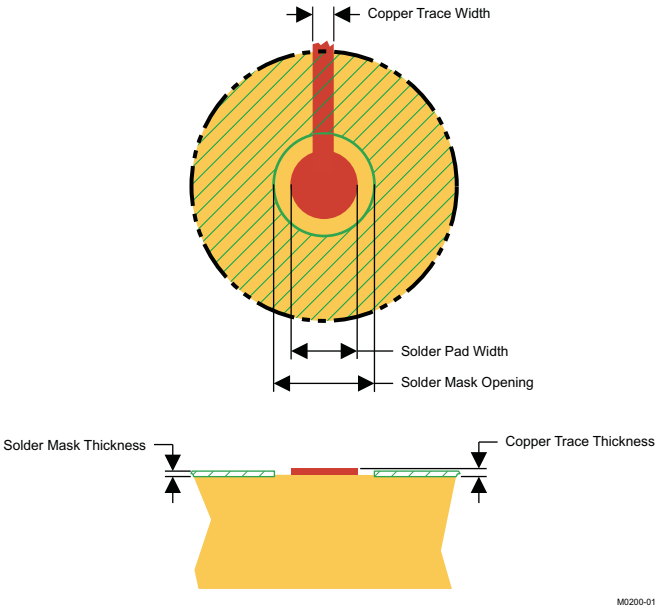


Figure 43. Recommended Land Pattern Image And Dimensions

SOLDER PAD DEFINITIONS (1)(2)(3)(4)	COPPER PAD	SOLDER MASK (5) OPENING	COPPER THICKNESS	STENCIL (6) OPENING	STENCIL THICKNESS
Non-solder-mask defined (NSMD)	0.30mm	0.360mm	1oz max (0.032mm)	0.34mm diameter	0.1mm thick

(1) Circuit traces from non-solder-mask defined PWB lands should be 75 µm to 100 µm wide in the exposed area inside the solder mask opening. Wider trace widths reduce device stand off and affect reliability.
(2) Best reliability results are achieved when the PWB laminate glass transition temperature is above the operating the range of the intended application.
(3) Recommend solder paste is Type 3 or Type 4.
(4) For a PWB using a Ni/Au surface finish, the gold thickness should be less than 0.5 µm to avoid a reduction in thermal fatigue performance.
(5) Solder mask thickness should be less than 20 µm on top of the copper circuit pattern.
(6) For best solder stencil performance use laser cut stencils with electro polishing. Chemically etched stencils give inferior solder paste volume control.

12.3 Surface Mount Information

The TPS8267x MicroSiP™ DC/DC converter uses an open frame construction that is designed for a fully automated assembly process and that features a large surface area for pick and place operations. See the "Pick Area" in the package drawings.

Package height and weight have been kept to a minimum thereby to allow the MicroSiP™ device to be handled similarly to a 0805 component.

See JEDEC/IPC standard J-STD-20b for reflow recommendations.

13 Device and Documentation Support

13.1 Documentation Support

13.1.1 References

"EMI Reduction in Switched Power Converters Using Frequency Modulation Techniques", in *IEEE TRANSACTIONS ON ELECTROMAGNETIC COMPATIBILITY, VOL. 4, NO. 3, AUGUST 2005, pp 569-576* by Josep Balcells, Alfonso Santolaria, Antonio Orlandi, David González, Javier Gago.

13.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS82670	Click here	Click here	Click here	Click here	Click here
TPS82671	Click here	Click here	Click here	Click here	Click here
TPS82672	Click here	Click here	Click here	Click here	Click here
TPS82673	Click here	Click here	Click here	Click here	Click here
TPS82674	Click here	Click here	Click here	Click here	Click here
TPS82675	Click here	Click here	Click here	Click here	Click here
TPS82676	Click here	Click here	Click here	Click here	Click here
TPS82677	Click here	Click here	Click here	Click here	Click here
TPS826711	Click here	Click here	Click here	Click here	Click here
TPS826716	Click here	Click here	Click here	Click here	Click here
TPS826721	Click here	Click here	Click here	Click here	Click here
TPS826745	Click here	Click here	Click here	Click here	Click here
TPS826765	Click here	Click here	Click here	Click here	Click here
TPS8267195	Click here	Click here	Click here	Click here	Click here

13.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.4 Trademarks

MicroSiP, E2E are trademarks of Texas Instruments.
Bluetooth is a trademark of Bluetooth SIG, Inc.
All other trademarks are the property of their respective owners.

13.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS82670SIPR	ACTIVE	uSiP	SIP	8	3000	RoHS & Green			-40 to 85	YK TXI670	Samples
TPS82670SIPT	ACTIVE	uSiP	SIP	8	250	RoHS & Green	SNAGCU	Level-2-260C-1 YEAR	-40 to 85	YK	Samples
TPS826711SIPR	ACTIVE	uSiP	SIP	8	3000	RoHS & Green	SNAGCU	Level-2-260C-1 YEAR	-40 to 85	YW	Samples
TPS826711SIPT	ACTIVE	uSiP	SIP	8	250	RoHS & Green	SNAGCU	Level-2-260C-1 YEAR	-40 to 85	YW	Samples
TPS826716SIPR	ACTIVE	uSiP	SIP	8	3000	RoHS & Green	SNAGCU	Level-2-260C-1 YEAR	-40 to 85	GS	Samples
TPS826716SIPT	ACTIVE	uSiP	SIP	8	250	RoHS & Green	SNAGCU	Level-2-260C-1 YEAR	-40 to 85	GS	Samples
TPS82671SIPR	ACTIVE	uSiP	SIP	8	3000	RoHS & Green	SNAGCU	Level-2-260C-1 YEAR	-40 to 85	RA	Samples
TPS82671SIPT	ACTIVE	uSiP	SIP	8	250	RoHS & Green	SNAGCU	Level-2-260C-1 YEAR	-40 to 85	RA	Samples
TPS826721SIPR	ACTIVE	uSiP	SIP	8	3000	RoHS & Green	SNAGCU	Level-2-260C-1 YEAR	-40 to 85	EO	Samples
TPS826721SIPT	ACTIVE	uSiP	SIP	8	250	RoHS & Green	SNAGCU	Level-2-260C-1 YEAR	-40 to 85	EO	Samples
TPS82672SIPR	ACTIVE	uSiP	SIP	8	3000	RoHS & Green	SNAGCU	Level-2-260C-1 YEAR	-40 to 85	WD	Samples
TPS82672SIPT	ACTIVE	uSiP	SIP	8	250	RoHS & Green	SNAGCU	Level-2-260C-1 YEAR	-40 to 85	WD	Samples
TPS82673SIPR	ACTIVE	uSiP	SIP	8	3000	RoHS & Green	SNAGCU	Level-2-260C-1 YEAR	-40 to 85	YL	Samples
TPS82673SIPT	ACTIVE	uSiP	SIP	8	250	RoHS & Green	SNAGCU	Level-2-260C-1 YEAR	-40 to 85	YL	Samples
TPS826745SIPR	ACTIVE	uSiP	SIP	8	3000	RoHS & Green	SNAGCU	Level-2-260C-1 YEAR	-40 to 85	B5	Samples
TPS826745SIPT	ACTIVE	uSiP	SIP	8	250	RoHS & Green	SNAGCU	Level-2-260C-1 YEAR	-40 to 85	B5	Samples
TPS82674SIPR	ACTIVE	uSiP	SIP	8	3000	RoHS & Green	SNAGCU	Level-2-260C-1 YEAR	-40 to 85	SW	Samples
TPS82674SIPT	ACTIVE	uSiP	SIP	8	250	RoHS & Green	SNAGCU	Level-2-260C-1 YEAR	-40 to 85	SW	Samples
TPS82675SIPR	ACTIVE	uSiP	SIP	8	3000	RoHS & Green	SNAGCU	Level-2-260C-1 YEAR	-40 to 85	RB	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS82675SIPT	ACTIVE	uSiP	SIP	8	250	RoHS (In Work) & Green (In Work)	SNAGCU	Level-2-260C-1 YEAR	-40 to 85	RB	Samples
TPS826765SIPR	ACTIVE	uSiP	SIP	8	3000	RoHS & Green	SNAGCU	Level-2-260C-1 YEAR	-40 to 85	AN	Samples
TPS826765SIPT	ACTIVE	uSiP	SIP	8	250	RoHS & Green	SNAGCU	Level-2-260C-1 YEAR	-40 to 85	AN	Samples
TPS82676SIPR	ACTIVE	uSiP	SIP	8	3000	RoHS & Green	SNAGCU	Level-2-260C-1 YEAR	-40 to 85	TU	Samples
TPS82676SIPT	ACTIVE	uSiP	SIP	8	250	RoHS & Green	SNAGCU	Level-2-260C-1 YEAR	-40 to 85	TU	Samples
TPS82677SIPR	ACTIVE	uSiP	SIP	8	3000	RoHS & Green	SNAGCU	Level-2-260C-1 YEAR	-40 to 85	SK	Samples
TPS82677SIPT	ACTIVE	uSiP	SIP	8	250	RoHS & Green	SNAGCU	Level-2-260C-1 YEAR	-40 to 85	SK	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

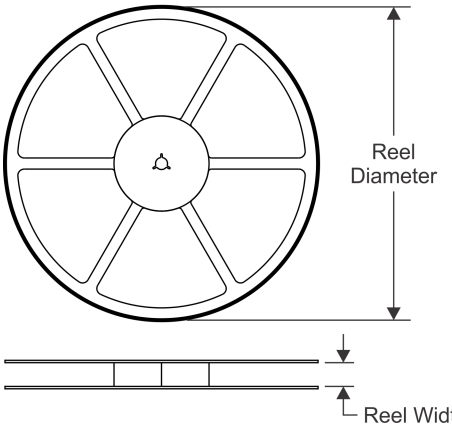
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

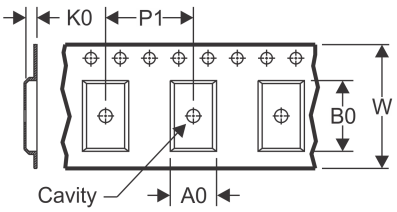
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

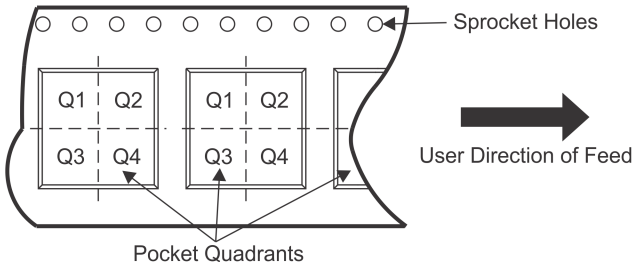


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

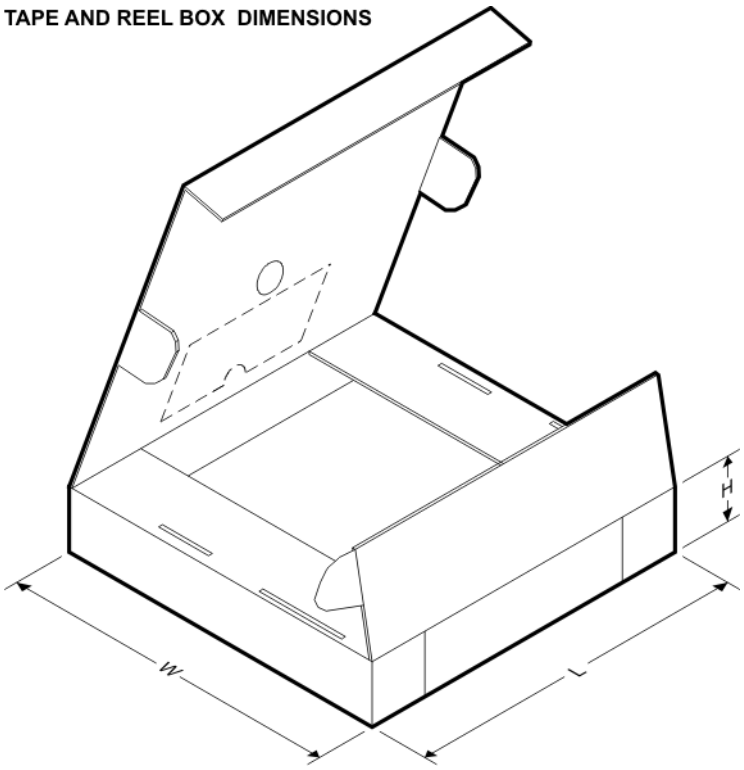


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS82670SIPT	uSiP	SIP	8	250	178.0	9.0	2.45	3.05	1.1	4.0	8.0	Q2
TPS826711SIPR	uSiP	SIP	8	3000	178.0	9.0	2.45	3.05	1.1	4.0	8.0	Q2
TPS826711SIPT	uSiP	SIP	8	250	178.0	9.0	2.45	3.05	1.1	4.0	8.0	Q2
TPS826716SIPR	uSiP	SIP	8	3000	178.0	9.0	2.45	3.05	1.1	4.0	8.0	Q2
TPS826716SIPT	uSiP	SIP	8	250	178.0	9.0	2.45	3.05	1.1	4.0	8.0	Q2
TPS82671SIPR	uSiP	SIP	8	3000	178.0	9.0	2.45	3.05	1.1	4.0	8.0	Q2
TPS82671SIPT	uSiP	SIP	8	250	178.0	9.0	2.45	3.05	1.1	4.0	8.0	Q2
TPS826721SIPR	uSiP	SIP	8	3000	178.0	9.0	2.45	3.05	1.1	4.0	8.0	Q2
TPS826721SIPT	uSiP	SIP	8	250	178.0	9.0	2.45	3.05	1.1	4.0	8.0	Q2
TPS82672SIPR	uSiP	SIP	8	3000	178.0	9.0	2.45	3.05	1.1	4.0	8.0	Q2
TPS82672SIPT	uSiP	SIP	8	250	178.0	9.0	2.45	3.05	1.1	4.0	8.0	Q2
TPS82673SIPR	uSiP	SIP	8	3000	178.0	9.0	2.45	3.05	1.1	4.0	8.0	Q2
TPS82673SIPT	uSiP	SIP	8	250	178.0	9.0	2.45	3.05	1.1	4.0	8.0	Q2
TPS826745SIPR	uSiP	SIP	8	3000	178.0	9.0	2.45	3.05	1.1	4.0	8.0	Q2
TPS826745SIPT	uSiP	SIP	8	250	178.0	9.0	2.45	3.05	1.1	4.0	8.0	Q2
TPS82674SIPR	uSiP	SIP	8	3000	178.0	9.0	2.45	3.05	1.1	4.0	8.0	Q2
TPS82674SIPT	uSiP	SIP	8	250	178.0	9.0	2.45	3.05	1.1	4.0	8.0	Q2
TPS82675SIPR	uSiP	SIP	8	3000	178.0	9.0	2.45	3.05	1.1	4.0	8.0	Q2

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS82675SIPT	uSiP	SIP	8	250	178.0	9.0	2.45	3.05	1.1	4.0	8.0	Q2
TPS826765SIPR	uSiP	SIP	8	3000	178.0	9.0	2.45	3.05	1.1	4.0	8.0	Q2
TPS826765SIPT	uSiP	SIP	8	250	178.0	9.0	2.45	3.05	1.1	4.0	8.0	Q2
TPS82676SIPR	uSiP	SIP	8	3000	178.0	9.0	2.45	3.05	1.1	4.0	8.0	Q2
TPS82676SIPT	uSiP	SIP	8	250	178.0	9.0	2.45	3.05	1.1	4.0	8.0	Q2
TPS82677SIPR	uSiP	SIP	8	3000	178.0	9.0	2.45	3.05	1.1	4.0	8.0	Q2
TPS82677SIPT	uSiP	SIP	8	250	178.0	9.0	2.45	3.05	1.1	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS

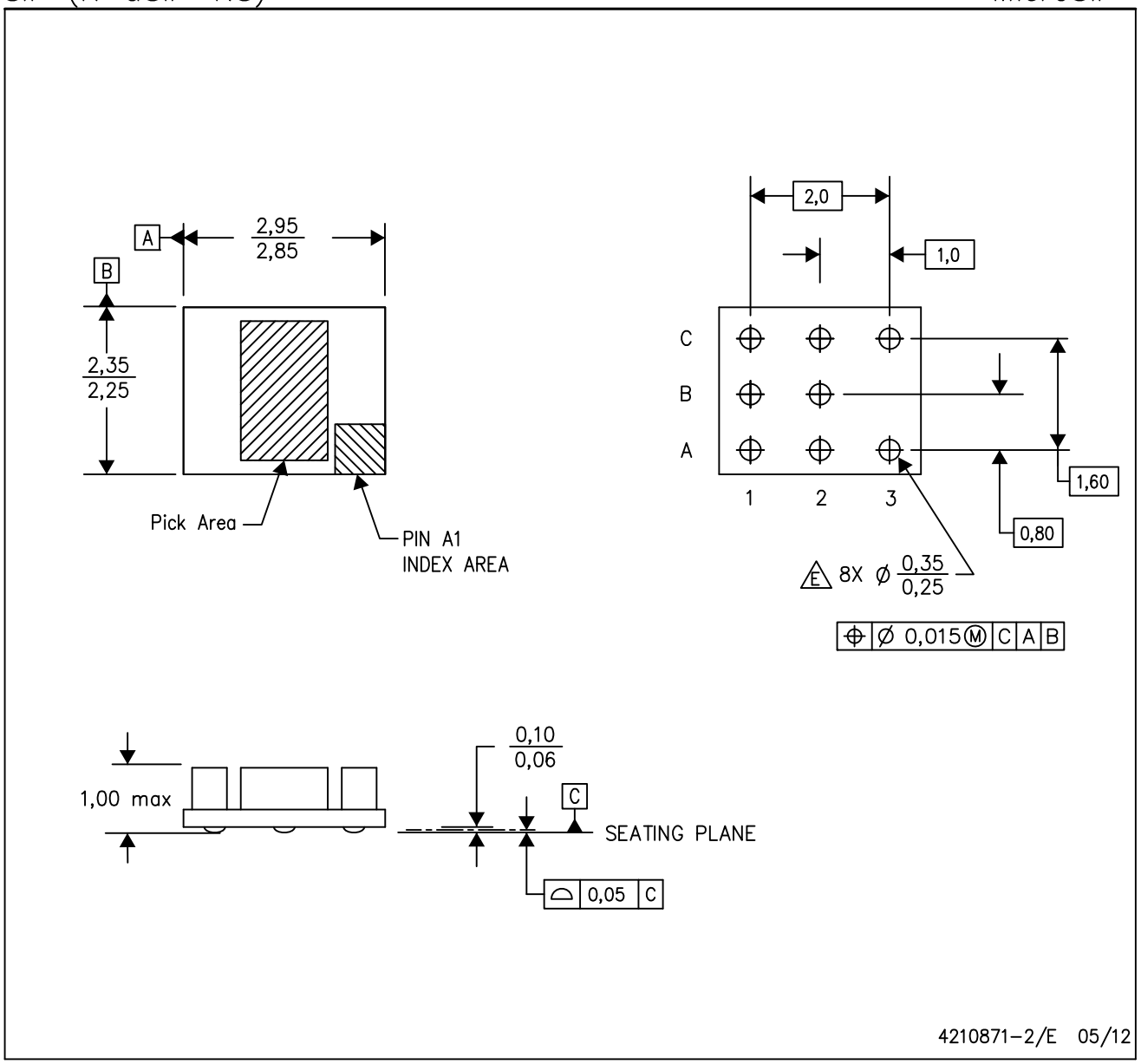


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS82670SIPT	uSiP	SIP	8	250	223.0	194.0	35.0
TPS826711SIPR	uSiP	SIP	8	3000	223.0	194.0	35.0
TPS826711SIPT	uSiP	SIP	8	250	223.0	194.0	35.0
TPS826716SIPR	uSiP	SIP	8	3000	223.0	194.0	35.0
TPS826716SIPT	uSiP	SIP	8	250	223.0	194.0	35.0
TPS82671SIPR	uSiP	SIP	8	3000	223.0	194.0	35.0
TPS82671SIPT	uSiP	SIP	8	250	223.0	194.0	35.0
TPS826721SIPR	uSiP	SIP	8	3000	223.0	194.0	35.0
TPS826721SIPT	uSiP	SIP	8	250	223.0	194.0	35.0
TPS82672SIPR	uSiP	SIP	8	3000	223.0	194.0	35.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS82672SIPT	uSiP	SIP	8	250	223.0	194.0	35.0
TPS82673SIPR	uSiP	SIP	8	3000	223.0	194.0	35.0
TPS82673SIPT	uSiP	SIP	8	250	223.0	194.0	35.0
TPS826745SIPR	uSiP	SIP	8	3000	223.0	194.0	35.0
TPS826745SIPT	uSiP	SIP	8	250	223.0	194.0	35.0
TPS82674SIPR	uSiP	SIP	8	3000	223.0	194.0	35.0
TPS82674SIPT	uSiP	SIP	8	250	223.0	194.0	35.0
TPS82675SIPR	uSiP	SIP	8	3000	223.0	194.0	35.0
TPS82675SIPT	uSiP	SIP	8	250	223.0	194.0	35.0
TPS826765SIPR	uSiP	SIP	8	3000	223.0	194.0	35.0
TPS826765SIPT	uSiP	SIP	8	250	223.0	194.0	35.0
TPS82676SIPR	uSiP	SIP	8	3000	223.0	194.0	35.0
TPS82676SIPT	uSiP	SIP	8	250	223.0	194.0	35.0
TPS82677SIPR	uSiP	SIP	8	3000	223.0	194.0	35.0
TPS82677SIPT	uSiP	SIP	8	250	223.0	194.0	35.0

SIP (R–uSiP–N8) MicroSiP™



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. MicroSiP™ package configuration – Micro System in Package.
D. Reference Product Data Sheet for array population. 3 x 3 matrix pattern is shown for illustration only.
E. This package contains Pb–free balls.

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