

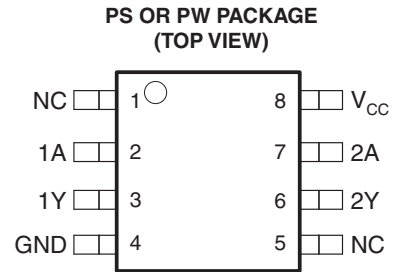


**THE DATASHEET OF
SN74HCU7204PW**



FEATURES

- Wide Operating Voltage Range of 2 V to 6 V
- Outputs Can Drive up to 10 LSTTL Loads
- Low Power Consumption, 20- μ A Max I_{CC}
- Typical $t_{pd} = 7$ ns
- ± 4 -mA Output Drive at 5 V
- Low Input Current of 1 μ A Max
- Unbuffered Outputs



DESCRIPTION/ORDERING INFORMATION

The SN74HCU7204 contains two independent unbuffered inverters. The device performs the Boolean function $Y = \bar{A}$ in positive logic.

ORDERING INFORMATION

| T _A | PACKAGE ⁽¹⁾ | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|------------------------|--------------------------------|------------------|
| -40°C to 85°C | SOP – PS | SN74HCU7204PS | HU7204 |
| | | Reel of 2000 SN74HCU7204PSR | |
| | TSSOP – PW | Tube of 90 SN74HCU7204PW | HU7204 |
| | | Reel of 2000 SN74HCU7204PWR | |
| | | Reel of 250 SN74HCU7204PWT | |

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE (EACH INVERTER)

| INPUT A | OUTPUT Y |
|------------|-------------|
| H | L |
| L | H |

LOGIC DIAGRAM (POSITIVE LOGIC)



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SN74HCU7204 DUAL INVERTERS

SCLS700–MAY 2006

Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|--|--|-----------------------------|-----|--------|
| V_{CC} | Supply voltage range | -0.5 | 7 | V |
| I_{IK} | Input clamp current ⁽²⁾ | $V_I < 0$ or $V_I > V_{CC}$ | | ±20 mA |
| I_{OK} | Output clamp current ⁽²⁾ | $V_O < 0$ or $V_O > V_{CC}$ | | ±20 mA |
| I_O | Continuous output current | $V_O = 0$ to V_{CC} | | ±25 mA |
| Continuous current through V_{CC} or GND | | | | ±50 mA |
| θ_{JA} | Package thermal impedance ⁽³⁾ | PS package | | TBD |
| | | PW package | | TBD |
| T_{stg} | Storage temperature range | -65 | 150 | °C |

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions⁽¹⁾

| | | MIN | NOM | MAX | UNIT | |
|----------|--------------------------------|------------------|-----|----------|------|----|
| V_{CC} | Supply voltage | 2 | 5 | 6 | V | |
| V_{IH} | High-level input voltage | $V_{CC} = 2$ V | | 1.7 | V | |
| | | $V_{CC} = 4.5$ V | | 3.6 | | |
| | | $V_{CC} = 6$ V | | 4.8 | | |
| V_{IL} | Low-level input voltage | $V_{CC} = 2$ V | | 0.3 | V | |
| | | $V_{CC} = 4.5$ V | | 0.8 | | |
| | | $V_{CC} = 6$ V | | 1.1 | | |
| V_I | Input voltage | 0 | | V_{CC} | V | |
| V_O | Output voltage | 0 | | V_{CC} | V | |
| I_{OH} | High-level output current | $V_{CC} = 4.5$ V | | -4 | mA | |
| | | $V_{CC} = 6$ V | | -5.2 | | |
| I_{OL} | Low-level output current | $V_{CC} = 4.5$ V | | 4 | mA | |
| | | $V_{CC} = 6$ V | | 5.2 | | |
| t_t | Transition time | $V_{CC} = 2$ V | | 0 | 1000 | ns |
| | | $V_{CC} = 4.5$ V | | 0 | 500 | |
| | | $V_{CC} = 6$ V | | 0 | 400 | |
| T_A | Operating free-air temperature | -40 | | 85 | °C | |

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | V _{CC} | T _A = 25°C | | | MIN | MAX | UNIT |
|-----------------|---|--------------------------|-----------------|-----------------------|-----|-----|------|-----|------|
| | | | | MIN | TYP | MAX | | | |
| V _{OH} | V _I = V _{CC} or GND | I _{OH} = -20 μA | 2 V | 1.8 | | | 1.8 | | V |
| | | | 4.5 V | 4 | | | 4 | | |
| | | | 6 V | 5.5 | | | 5.5 | | |
| | | I _{OH} = -4 mA | 4.5 V | 3.86 | | | 3.76 | | |
| | | | 6 V | 5.36 | | | 5.26 | | |
| V _{OL} | V _I = V _{CC} or GND | I _{OL} = 20 μA | 2 V | | | | 0.2 | | V |
| | | | 4.5 V | | | | 0.5 | | |
| | | | 6 V | | | | 0.5 | | |
| | | I _{OL} = 4 mA | 4.5 V | | | | 0.32 | | |
| | | | 6 V | | | | 0.32 | | |
| I _I | V _I = V _{CC} or 0 | I _O = 0 | 6 V | | | | ±100 | | nA |
| | | | I _{CC} | 6 V | | | | 2 | |
| C _i | | | 2 V to 6 V | | | | 3 10 | | pF |

Switching Characteristics

over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see [Figure 1](#))

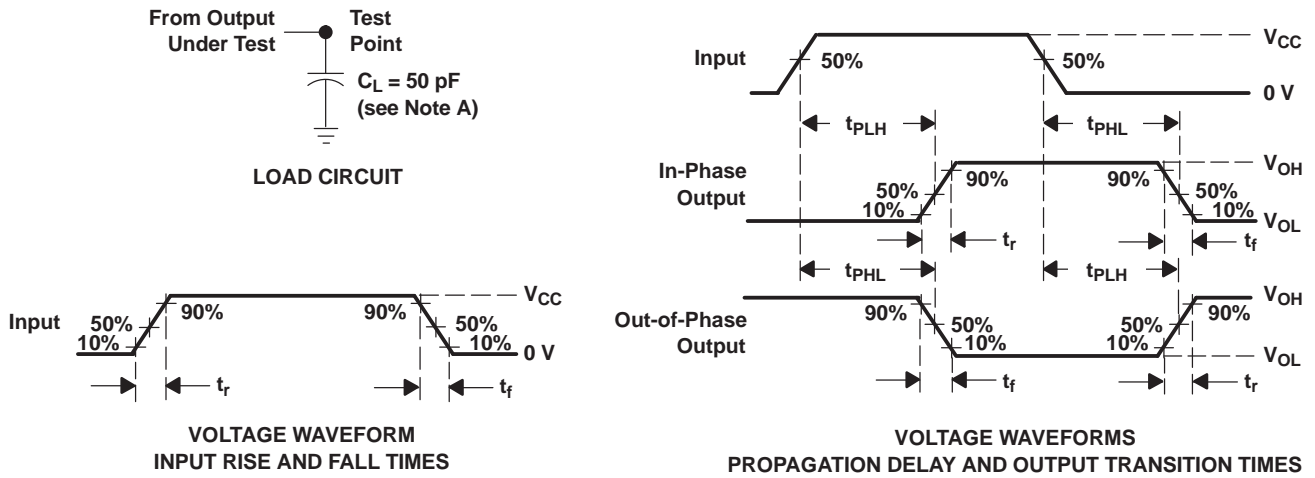
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | V _{CC} | T _A = 25°C | | | MIN | MAX | UNIT |
|--------------------------------|--------------|-------------|-----------------|-----------------------|-----|-----|-----|-----|------|
| | | | | MIN | TYP | MAX | | | |
| t _{pd} | A | Y | 2 V | 40 80 | | | 100 | | ns |
| | | | 4.5 V | 8 16 | | | 20 | | |
| | | | 6 V | 7 14 | | | 17 | | |
| t _r /t _f | | Y | 2 V | 38 75 | | | 95 | | ns |
| | | | 4.5 V | 8 15 | | | 19 | | |
| | | | 6 V | 6 13 | | | 16 | | |

Operating Characteristics

T_A = 25°C

| PARAMETER | TEST CONDITIONS | TYP | UNIT |
|--|-----------------|-----|------|
| C _{pd} Power dissipation capacitance per inverter | No load | 20 | pF |

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and test-fixture capacitance.
 B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r = 6 \text{ ns}$, $t_f = 6 \text{ ns}$.
 C. The outputs are measured one at a time, with one input transition per measurement.
 D. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|--------------------|------|----------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|---------|
| SN74HCU7204PW | ACTIVE | TSSOP | PW | 8 | 150 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | | HU7204 | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

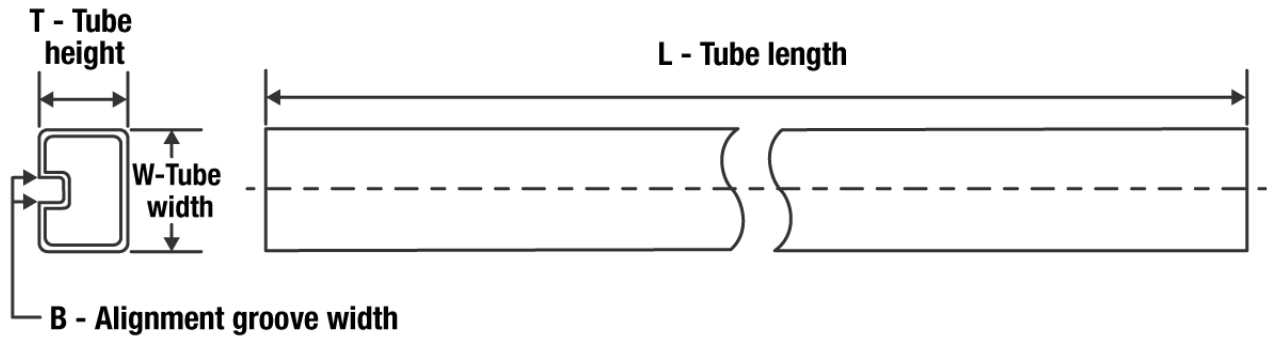
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TUBE


*All dimensions are nominal

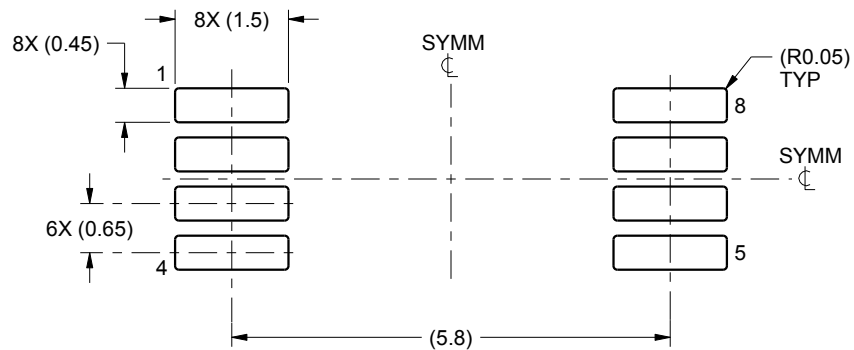
| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|---------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| SN74HCU7204PW | PW | TSSOP | 8 | 150 | 530 | 10.2 | 3600 | 3.5 |

EXAMPLE BOARD LAYOUT

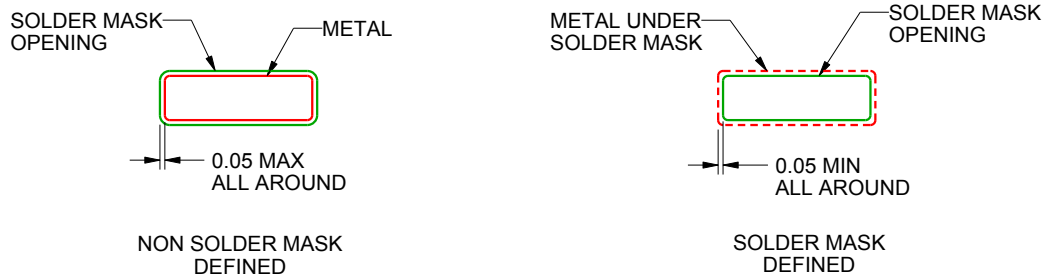
PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
NOT TO SCALE

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NOTES: (continued)

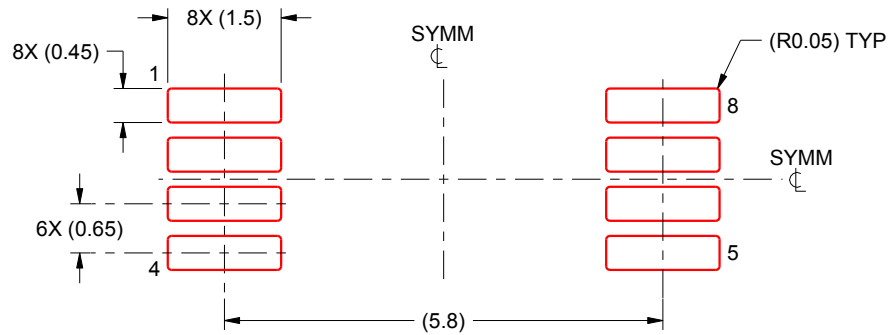
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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