



**THE DATASHEET OF
Z0853004PSG**





Z08030/8530

***Serial Communications
Controller***

Customer Procurement Specification

PS011301-0601



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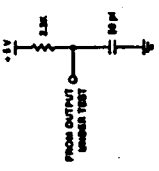
DC Characteristics

Symbol	Parameter	Min	Max	Unit	Condition
V_{IH}	Input High Voltage	2.0 ^a	$V_{CC} + 0.3^c$	V	
V_{IL}	Input Low Voltage	-0.3 ^c	0.8 ^a	V	$I_{OL} = -250 \mu A$
V_{OH}	Output High Voltage	2.4 ^b		V	$I_{OL} = +2.0 mA$
V_{OL}	Output Low Voltage	0.4 ^b		V	$0.4 \leq V_{IH} \leq +2.4V$
I_{IL}	Input Leakage	± 10.00		μA	$0.4 \leq V_{OH} \leq +2.4V$
I_{OL}	Output Leakage		± 10.00	μA	
I_{CC}	V _{CC} Supply Current	250		mA	

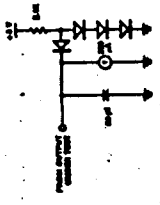
- ^a $V_{CC} = 5V \pm 0.1V$, unless otherwise specified, over specified temperature range.
- ^b Tested
- ^c Guaranteed by Design
- ^d Guaranteed by Characterization

Standard Test Conditions

- The DC characteristics and capacitance section below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to GND. Positive current flows into the referenced pin.
- Standard conditions are as follows:
 - $V_{CC} = 5V \pm 0.1V$
 - $GND = 0V$
 - T_A as specified in Ordering Information
- All ac parameters assume a load capacitance of 50 pF max.



Open-Drain Test Load

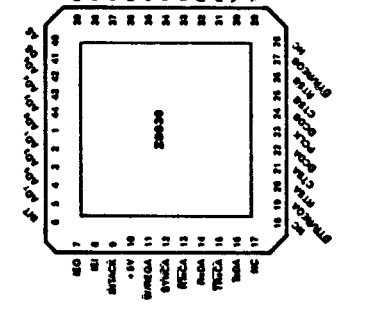
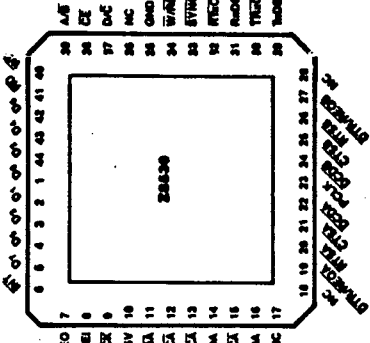


Standard Test Load

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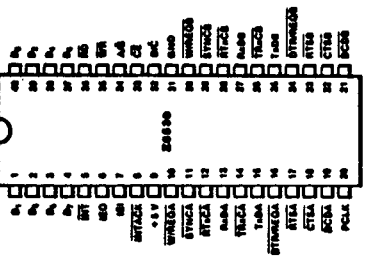
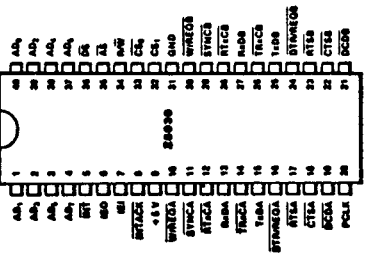
Absolute Maximum Ratings
 Voltages on all pins with respect to GND -0.3V to +7.0V
 Operating Ambient Temperature See Ordering Information

Storage Temperature -65°C to +150°C
 Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



Chip Carrier Pin Assignments: Z8000

Chip Carrier Pin Assignments: Z8000



DIP Pin Assignments: Z8000

DIP Pin Assignments: Z8000

Z8030 AC CHARACTERISTICS

Z8030 AC CHARACTERISTICS (Continued)

Number	Symbol	Parameter	4 MHz		6 MHz		8 MHz		Notes*†
			Min	Max	Min	Max	Min	Max	
1	TwAS	AS Low Width	70 ^a		50 ^a		35 ^a		
2	TdS(AS)	DS ↑ to AS ↓ Delay	50 ^c		25 ^c		15 ^c		
3	TcSO(AS)	CS ₀ to AS ↑ Setup Time	0 ^a		0 ^a		0 ^a		1
4	ThCS(AS)	CS ₀ to AS ↑ Hold Time	60 ^a		40 ^a		30 ^a		1
5	TcS1(DS)	CS ₁ to DS ↓ Setup Time	100 ^a		80 ^a		65 ^a		1
6	ThCS1(DS)	CS ₁ to DS ↓ Hold Time	55 ^c		40 ^c		30 ^c		1
7	ThA(AS)	RTACK to AS ↑ Setup Time	10 ^c		10 ^c		10 ^c		
8	ThA(AS)	RTACK to AS ↑ Hold Time	250 ^a		200 ^a		150 ^a		
9	TcRW(DS)	RW (Read) to DS ↓ Setup Time	100 ^a		80 ^a		65 ^a		
10	ThRW(DS)	RW to DS ↓ Hold Time	55 ^a		40 ^a		35 ^a		
11	TcRW(DS)	RW (Write) to DS ↓ Setup Time	0 ^c		0 ^c		0 ^c		
12	TcAS(DS)	AS ↑ to DS ↓ Delay	60 ^c		40 ^c		30 ^c		
13	TcDS	DS Low Width	240 ^a		200 ^a		150 ^a		
14	Tc	Valid Access Recovery Time	4TcPC ^a		4TcPC ^a		4TcPC ^a		2
15	ThA(AS)	Address to AS ↑ Setup Time	30 ^a		10 ^a		10 ^a		1
16	ThA(AS)	Address to AS ↑ Hold Time	50 ^a		30 ^a		25 ^a		1
17	ThDW(DS)	Write Data to DS ↓ Setup Time	30 ^a		20 ^a		15 ^a		
18	ThDW(DS)	Write Data to DS ↑ Hold Time	30 ^a		20 ^a		20 ^a		
19	TcDS(DA)	DS ↓ to Data Active Delay	0 ^c		0 ^c		0 ^c		
20	TcDS(DR)	DS ↑ to Read Data Not Valid Delay	0 ^a		0 ^a		0 ^a		
21	TcDS(DR)	DS ↓ to Read Data Valid Delay	250 ^a		180 ^a		140 ^a		
22	TcAS(DR)	AS ↑ to Read Data Valid Delay	520 ^a		300 ^a		250 ^a		

NOTES:

1. Parameter does not apply to interrupt acknowledge transactions.
 2. Parameter applies only between transactions involving the SCC.
- *Times are preliminary and subject to change.
†Units in nanoseconds (ns).

- a Tested
- b Guaranteed by Design
- c Guaranteed by Characterization

Number	Symbol	Parameter
23	TcDS(DR)	DS ↑ to Read Data Post Delay
24	TcADR	Address Required Valid to Read Data Valid Delay
25	TcDS(W)	DS ↓ to Wait Valid Delay
26	TcDS(WEC)	DS ↑ to W/REC Not Valid Delay
27	TcDS(WEC)	DS ↓ to DTR/REC Not Valid Delay
28	TcDS(WT)	AS ↑ to RT Valid Delay
29	TcAS(DSA)	AS ↑ to DS ↓ (Acknowledge) Delay
30	TcDS(A)	DS (Acknowledge) Low Width
31	TcDS(ADR)	DS ↓ (Acknowledge) to Read Data Valid Delay
32	TcDS(DSA)	EI to DS ↓ (Acknowledge) Setup Time
33	TcDS(DSA)	EI to DS ↑ (Acknowledge) Hold Time
34	TcDS(WEC)	EI to EIO Delay
35	TcAS(WEC)	AS ↑ to EIO Delay
36	TcDS(WT)	DS ↓ (Acknowledge) to RT Inactive Delay
37	TcDS(ASQ)	DS ↑ to AS ↓ Delay for No Reset
38	TcDS(DS)	AS ↑ to DS ↓ Delay for No Reset
39	TcDS(W)	AS and DS Concurrent Low for Reset
40	TcPC	PCLK Low Width
41	TcPC	PCLK High Width
42	TcPC	PCLK Cycle Time
43	TcPC	PCLK Rise Time
44	TcPC	PCLK Fall Time

- NOTES:
 1. Post delay is defined as the time required for a 5.0V change in the output signal.
 2. Operation output, measured with open-drain load.
 3. Parameter is system dependent. For any Z80C in the delay chain, TcAS(DSA) or TcDS(WEC) for the Z80C, and TcDS(WEC) for the Z80C.
 4. Parameter applies only to Z80C pulling I/O Lines at the beginning of the internal clock period.
 5. Internal circuitry subject to the reset provided by the Z80 to be acceptable.
 *Times are preliminary and subject to change. †Units in nanoseconds (ns).

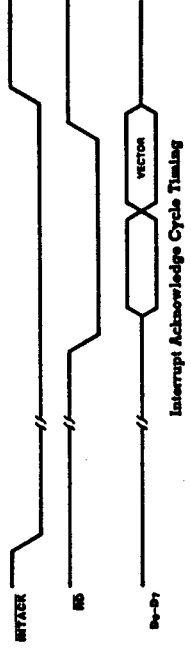
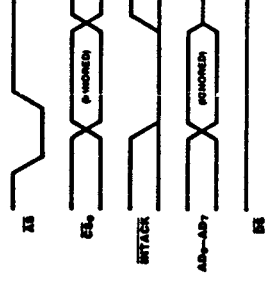
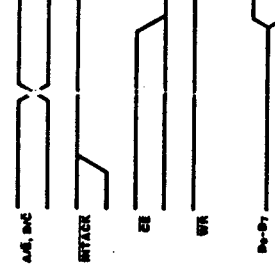
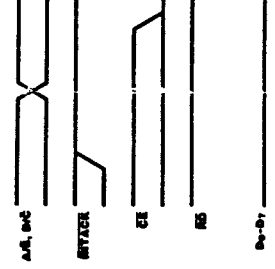
Z80S3/Z80S30 SYSTEM TIMING AC CHARACTERISTICS

Number	Symbol	Parameter	4 MHz		6 MHz		8 MHz		Notes†‡
			Min	Max	Min	Max	Min	Max	
1	TdRXQ(REQ)	RXC ↓ to W/REQ Valid Delay	8	12	8	12	8	12	2
2	TdRXQ(W)	RXC ↑ to Wait Inactive Delay	8	14	8	14	8	14	1,2
3	TdRXQ(SY)	RXC ↑ to SYNC Valid Delay	4	7	4	7	4	7	2
4a.	TdRXQ(INT), Z80S30	RXC ↑ to INT Valid Delay	10	16	10	16	10	16	1,2
4b.	TdRXQ(INT), Z8030		8	12	8	12	8	12	1,2
			+2	+3	+2	+3	+2	+3	4
5	TdTXQ(REQ)	TRC ↓ to W/REQ Valid Delay	5	8	5	8	5	8	3
6	TdTXQ(W)	TRC ↓ to Wait Inactive Delay	5	11	5	11	5	11	1,3
7	TdTXQ(DRC)	TRC ↓ DTR/REQ Valid Delay	4	7	4	7	4	7	3
8a.	TdTXQ(INT), Z80S30	TRC ↓ to INT Valid Delay	6	10	6	10	6	10	1,3
8b.	TdTXQ(INT), Z8030		4	6	4	6	4	6	1,3
			+2	+3	+2	+3	+2	+3	4
9a.	TdSY(INT), Z80S30	SYNC Transition to INT Valid Delay	2	6	2	6	2	6	1
9b.	TdSY(INT), Z8030		2	3	2	3	2	3	1,4
10a.	TdEXT(INT), Z80S30	DOD or CTS Transition to INT Valid Delay	2	6	2	6	2	6	1
10b.	TdEXT(INT), Z8030		2	3	2	3	2	3	1,4

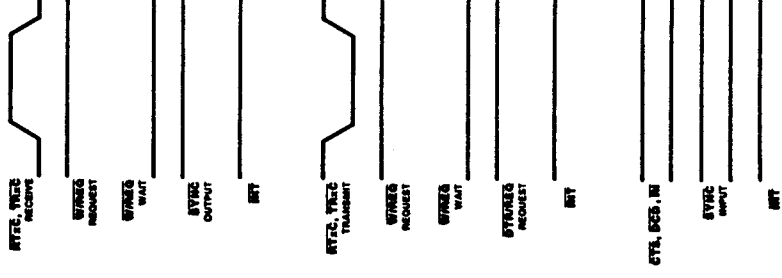
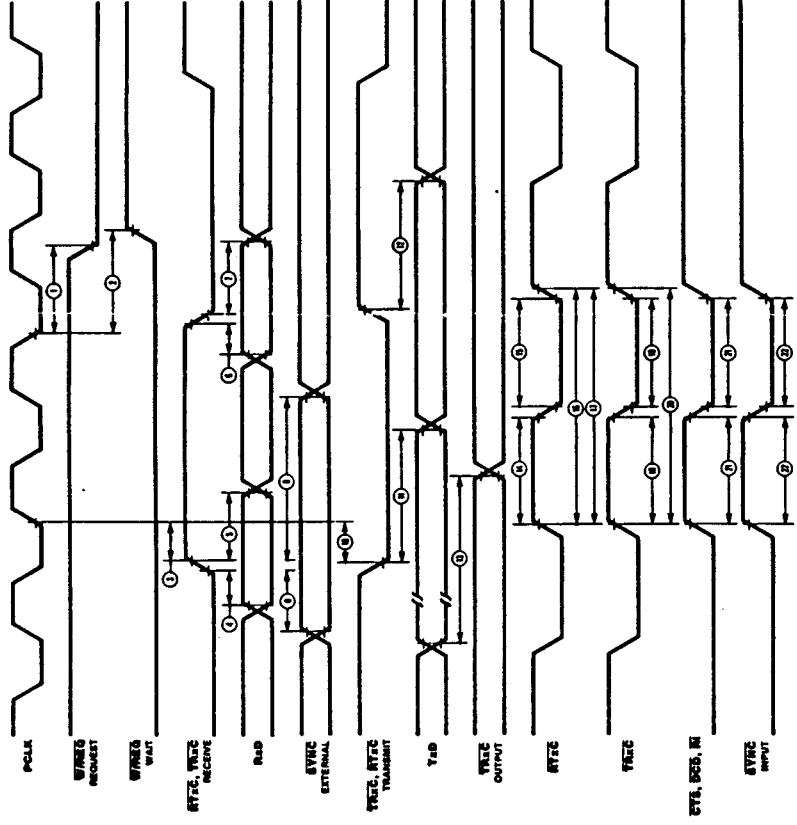
NOTES:

- Open-drain output, measured with open-drain test load
- RxC is RTrxC or TRxC, whichever is supplying the receive clock.
- TrC is TRxC or RTxC, whichever is supplying the transmit clock.
- Units equal to NS.

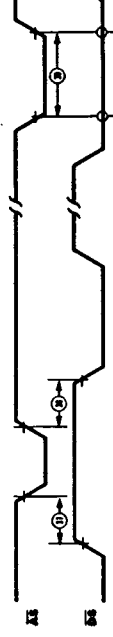
†Timings are preliminary and subject to change.
‡Units equal to TdPC.



**General
Timing**



**Reset
Timing
Z8030**



Z8530 AC CHARACTERISTICS

Z8530 AC CHARACTERISTICS (Continued)

Number	Symbol	Parameter	4 MHz		6 MHz		8 MHz		Notes ^{††}
			Min	Max	Min	Max	Min	Max	
1	TwPCI	PCLK Low Width	105 ^a	2000 ^a	70 ^a	1000 ^a	50 ^a	1000 ^a	
2	TwPCh	PCLK High Width	105 ^a	2000 ^a	70 ^a	1000 ^a	50 ^c	1000 ^a	
3	TIPC	PCLK Fall Time		20 ^a		10 ^a		10 ^a	
4	TrPC	PCLK Rise Time		20 ^a		10 ^a		10 ^a	
5	TcPC	PCLK Cycle Time	250 ^a	4000 ^a	165 ^a	2000 ^a	125 ^a	2000 ^a	
6	TsA(WR)	Address to \overline{WR} ↓ Setup Time	80 ^a		80 ^a		70 ^a		
7	TtA(WR)	Address to \overline{WR} ↑ Hold Time	0 ^c		0 ^c		0 ^c		
8	TsA(RD)	Address to \overline{RD} ↓ Setup Time	80 ^a		80 ^a		70 ^a		
9	TtA(RD)	Address to \overline{RD} ↑ Hold Time	0 ^c		0 ^c		0 ^c		
10	TsA(PC)	INTACK to PCLK ↑ Setup Time	10 ^a		10 ^a		10 ^a		
11	TsA(WR)	INTACK to \overline{WR} ↓ Setup Time	200 ^a		160 ^a		145 ^a		1
12	TtA(WR)	INTACK to \overline{WR} ↑ Hold Time	0 ^c		0 ^c		0 ^c		
13	TsA(RD)	INTACK to \overline{RD} ↓ Setup Time	200 ^a		160 ^a		145 ^a		1
14	TtA(RD)	INTACK to \overline{RD} ↑ Hold Time	0 ^a		0 ^a		0 ^a		
15	TtA(PC)	INTACK to PCLK ↑ Hold Time	100 ^a		100 ^a		85 ^a		
16	TsCE(WR)	\overline{CE} Low to \overline{WR} ↓ Setup Time	0 ^a		0 ^a		0 ^a		
17	TtCE(WR)	\overline{CE} to \overline{WR} ↑ Hold Time	0 ^a		0 ^a		0 ^a		
18	TsCE(WR)	\overline{CE} High to \overline{WR} ↓ Setup Time	100 ^a		70 ^a		60 ^a		
19	TsCE(RD)	\overline{CE} Low to \overline{RD} ↓ Setup Time	0 ^a		0 ^a		0 ^a		1
20	TtCE(RD)	\overline{CE} to \overline{RD} ↑ Hold Time	0 ^a		0 ^a		0 ^a		1
21	TsCE(RD)	\overline{CE} High to \overline{RD} ↓ Setup Time	100 ^a		70 ^a		60 ^a		1
22	TwRD	\overline{RD} Low Width	390 ^a		200 ^a		150 ^a		1
23	TdRD(DRA)	\overline{RD} ↓ to Read Data Active Delay	0 ^c		0 ^c		0 ^c		
24	TdRD(DR)	\overline{RD} ↑ to Read Data Not Valid Delay	0 ^a		0 ^a		0 ^a		
25	TdRD(DR)	\overline{RD} ↓ to Read Data Valid Delay	250 ^a		180 ^a		140 ^a		
26	TdRD(DRz)	\overline{RD} ↑ to Read Data Float Delay	70 ^a		45 ^a		40 ^a		2

NOTES:

1. Parameter does not apply to Interrupt Acknowledge transactions.
2. Float delay is defined as the time required for a ±0.5V change at the output with a maximum dc load and minimum ac load.
- ^aTimings are preliminary and subject to change.
- [†]Units in nanoseconds (ns).

Number	Symbol	Parameter
27	TsA(DR)	Address Required Valid to Valid Delay [†]
28	TwWR	\overline{WR} Low Width
29	Td(WR)	Write Data to \overline{WR} ↓ Setup
30	Td(WR)	Write Data to \overline{WR} ↑ Hold Time
31	Td(WR)	\overline{WR} ↓ to Wait [†] Valid Delay
32	Td(WR)	\overline{RD} ↓ to Wait [†] Valid Delay
33	Td(WR(REQ))	\overline{WR} ↓ to \overline{WR} (REQ) Not Valid
34	Td(WR(REQ))	\overline{RD} ↓ to \overline{WR} (REQ) Not Valid
35	Td(WR(REQ))	\overline{WR} ↓ DTR(REQ) Not Valid
36	Td(WR(REQ))	\overline{RD} ↓ to DTR(REQ) Not Valid
37	Td(PCINT)	PCLK ↓ to INT Valid Delay
38	TsA(RD)	INTACK to \overline{RD} ↓ (Acknowledge)
39	TwRDA	\overline{RD} (Acknowledge) Width
40	Td(RD(DR))	\overline{RD} ↓ (Acknowledge) to Read Valid Delay
41	TtE(RDA)	EI to \overline{RD} ↓ (Acknowledge) to Read Time
42	TtE(RDA)	EI to \overline{RD} ↓ (Acknowledge) to Read Time
43	TdE(REQ)	EI to REQ Delay Time
44	Td(PCREQ)	PCLK ↑ to REQ Delay
45	Td(RD(NT))	\overline{RD} ↓ to INT [†] Inactive Delay
46	Td(WR(REQ))	\overline{RD} ↓ to \overline{WR} ↓ Delay for Not Valid
47	Td(WR(REQ))	\overline{WR} ↓ to \overline{RD} ↓ Delay for Not Valid
48	TwRES	\overline{WR} and \overline{RD} coincident L ₁ Valid Access Recovery Time
49	Ttc	Valid Access Recovery Time

- NOTES:
1. Parameter applies only between transactions involving the output.
 2. Parameter applies only between transactions involving the output, measured with open-circuit test load.
 3. Parameter is system dependent. For any FCC in the delay chain, TtE(RDA) for the SCC, and TdE(REQ) for the delay chain, TtE(RDA) for the SCC, and TdE(REQ) for the delay chain.
 4. Timings are preliminary and subject to change.
 5. Units in nanoseconds (ns).

- a Tested
- b Guaranteed by Design
- c Guaranteed by Character

Z8030/Z8530 GENERAL TIMING AC CHARACTERISTICS

Number	Symbol	Parameter	4 MHz			6 MHz			8 MHz			Notes*†
			Min	Max	Typ	Min	Max	Typ	Min	Max	Typ	
1	TdPC(REQ)	PCLK ↓ to $\overline{W}/\overline{REQ}$ Valid Delay	250 ^a	350 ^a	250 ^a	250 ^a	350 ^a	250 ^a	350 ^a	250 ^a	350 ^a	
2	TdPC(W)	PCLK ↓ to Wait Inactive Delay										
3	TsRXC(PC)	RxC ↑ to PCLK ↑ Setup Time (PCLK + 4 case only)	80	0 ^a	70	70	0 ^a	60	0 ^a	60	0 ^a	1, 4
4	TsRXD(RXC)	RxD to RxC ↑ Setup Time (X1 Mode)	0 ^a	0 ^a	0 ^a	0 ^a	0 ^a	0 ^a	0 ^a	0 ^a	0 ^a	1
5	TsRXD(RXC)	RxD to RxC ↑ Hold Time (X1 Mode)	150 ^a	150 ^a	150 ^a	150 ^a	150 ^a	150 ^a	150 ^a	150 ^a	150 ^a	1
6	TsRXD(RXC)	RxD to \overline{RxC} ↓ Setup Time (X1 Mode)	0 ^a	0 ^a	0 ^a	0 ^a	0 ^a	0 ^a	0 ^a	0 ^a	0 ^a	1, 5
7	TsRXD(RXC)	RxD to \overline{RxC} ↓ Hold Time (X1 Mode)	150 ^c	150 ^c	150 ^c	150 ^c	150 ^c	150 ^c	150 ^c	150 ^c	150 ^c	1, 5
8	TsY(RXC)	SYNC to RxC ↑ Setup Time	-200 ^a	-200 ^a	-200 ^a	-200 ^a	-200 ^a	-200 ^a	-200 ^a	-200 ^a	-200 ^a	1
9	TsY(RXC)	SYNC to RxC ↑ Hold Time	3TcPC ^c	3TcPC ^c	3TcPC ^c	3TcPC ^c	3TcPC ^c	3TcPC ^c	3TcPC ^c	3TcPC ^c	3TcPC ^c	
10	TsTXC(PC)	\overline{TxC} ↓ to PCLK ↑ Setup Time	+400	+320	0 ^a	+320	+250	0 ^a	+250	0 ^a	+250	1
10	TsTXC(PC)	\overline{TxC} ↓ to PCLK ↑ Setup Time	0 ^a	0 ^a	0 ^a	0 ^a	0 ^a	0 ^a	0 ^a	0 ^a	0 ^a	2, 4
11	TdTXC(TXD)	\overline{TxC} ↓ to TxD Delay (X1 Mode)	300 ^a	300 ^a	300 ^a	230 ^a	200 ^a	200 ^a	200 ^a	200 ^a	200 ^a	2
12	TdTxCr(TXD)	TxC ↑ to TxD Delay (X1 Mode)	300 ^a	300 ^a	300 ^a	230 ^a	200 ^a	200 ^a	200 ^a	200 ^a	200 ^a	2, 5
13	TdTXD(TRX)	TxD to \overline{TRxC} Delay (Send Clock Echo)	200 ^a	200 ^a	200 ^a	200 ^a	200 ^a	200 ^a	200 ^a	200 ^a	200 ^a	
14	TwRTXh	\overline{RTxC} High Width	180 ^a	180 ^a	180 ^a	180 ^a	150 ^a	150 ^a	150 ^a	150 ^a	150 ^a	6
15	TwRTXl	\overline{RTxC} Low Width	180 ^a	180 ^a	180 ^a	180 ^a	150 ^a	150 ^a	150 ^a	150 ^a	150 ^a	6
16	TcRTX	\overline{RTxC} Cycle Time (RxD, TxD)	1000 ^a	1000 ^a	1000 ^a	640 ^a	500 ^a	500 ^a	500 ^a	500 ^a	500 ^a	6, 7
17	TcRTXX	Crystal Oscillator Period	250 ^c	1000 ^c	165 ^c	1000 ^c	125 ^c	1000 ^c	1000 ^c	1000 ^c	1000 ^c	3
18	TwTRXh	\overline{TRxC} High Width	180 ^a	180 ^a	180 ^a	180 ^a	150 ^a	150 ^a	150 ^a	150 ^a	150 ^a	6
19	TwTRXl	\overline{TRxC} Low Width	180 ^a	180 ^a	180 ^a	180 ^a	150 ^a	150 ^a	150 ^a	150 ^a	150 ^a	6
20	TcTRX	\overline{TRxC} Cycle Time	1000 ^a	1000 ^a	1000 ^a	640 ^a	500 ^a	500 ^a	500 ^a	500 ^a	500 ^a	6, 7
21	TwEXT	\overline{DCD} or \overline{CTS} Pulse Width	200 ^a	200 ^a	200 ^a	200 ^a	200 ^a	200 ^a	200 ^a	200 ^a	200 ^a	
22	TwSY	SYNC Pulse Width	200 ^a	200 ^a	200 ^a	200 ^a	200 ^a	200 ^a	200 ^a	200 ^a	200 ^a	

NOTES

- RxC is \overline{RTxC} or \overline{TRxC} , whichever is supplying the receive clock.
- TxC is \overline{TRxC} or \overline{RTxC} , whichever is supplying the transmit clock.
- Both \overline{RTxC} and \overline{TRxC} have 30 pF capacitors to ground connected to them.
- Parameter applies only if the data rate is one-fourth the PCLK rate. In all other cases, no phase relationship between RxC and PCLK or TxC and PCLK is required.
- Parameter applies only to FM encoding/decoding.
- Parameter applies only for transmitter and receiver; DPLL and baud rate generator timing requirements are identical to case PCLK requirements.
- The maximum receive or transmit data is 1/4 PCLK.
- Timings are preliminary and subject to change.

*Units in nanoseconds (ns).

- a Tested
- b Guaranteed by Design
- c Guaranteed by Characterization

Z8

Z8

RTXCR

AD₀-AD₇

CS₀

CS₁

CS

Z8

Z8

RTXCR

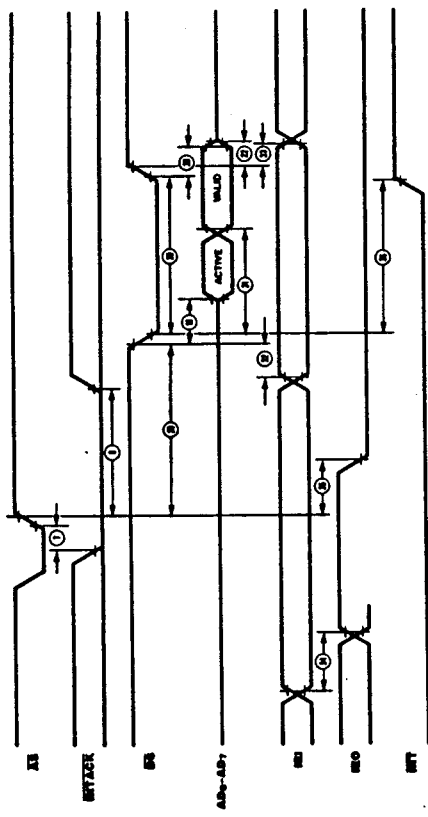
AD₀-AD₇

CS₀

CS₁

CS

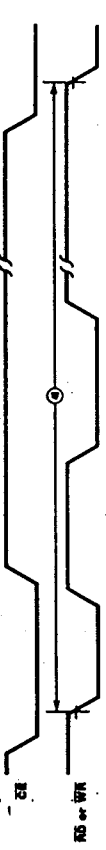
**Interrupt
Acknowledge
Timing
Z8030**



**Reset
Timing
Z8530**



**Cycle
Timing
Z8530**



Looking for pricing, stock, or lifecycle information?

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-  Alternative Solution
-  Excess Inventory Management