THE DATASHEET OF

LPC812M101JDH20FP

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LPC81xM

32-bit ARM® Cortex®-M0+ microcontroller; up to 16 kB flash and 4 kB SRAM

Rev. 4.7 — 19 March 2021 Product data sheet

1. General description

The LPC81xM are an ARM Cortex-M0+ based, low-cost 32-bit MCU family operating at CPU frequencies of up to 30 MHz. The LPC81xM support up to 16 kB of flash memory and 4 kB of SRAM.

The peripheral complement of the LPC81xM includes a CRC engine, one I^2C-bus interface, up to three USARTs, up to two SPI interfaces, one multi-rate timer, self wake-up timer, and state-configurable timer, one comparator, function-configurable I/O ports through a switch matrix, an input pattern match engine, and up to 18 general-purpose I/O pins.

2. Features and benefits

- System:
  - ARM Cortex-M0+ processor, running at frequencies of up to 30 MHz with single-cycle multiplier and fast single-cycle I/O port.
  - ARM Cortex-M0+ built-in Nested Vectored Interrupt Controller (NVIC).
  - System tick timer.
  - Serial Wire Debug (SWD) and JTAG boundary scan modes supported.
  - Micro Trace Buffer (MTB) supported.
- Memory:
  - Up to 16 kB on-chip flash programming memory with 64 Byte page write and erase.
  - Up to 4 kB SRAM.
- ROM API support:
  - Boot loader.
  - USART drivers.
  - I2C drivers.
  - Power profiles.
  - Flash In-Application Programming (IAP) and In-System Programming (ISP).
- Digital peripherals:
  - High-speed GPIO interface connected to the ARM Cortex-M0+ IO bus with up to 18 General-Purpose I/O (GPIO) pins with configurable pull-up/pull-down resistors, programmable open-drain mode, input inverter, and glitch filter.
  - High-current source output driver (20 mA) on four pins.
  - High-current sink driver (20 mA) on two true open-drain pins.
  - GPIO interrupt generation capability with boolean pattern-matching feature on eight GPIO inputs.
  - Switch matrix for flexible configuration of each I/O pin function.

- State Configurable Timer/PWM (SCTimer/PWM) with input and output functions (including capture and match) assigned to pins through the switch matrix.
- Multiple-channel multi-rate timer (MRT) for repetitive interrupt generation at up to four programmable, fixed rates.
- Self Wake-up Timer (WKT) clocked from either the IRC or a low-power, low-frequency internal oscillator.
- CRC engine.
- Windowed Watchdog timer (WWDT).

- Analog peripherals:
  - Comparator with internal and external voltage references with pin functions assigned or enabled through the switch matrix.
- Serial interfaces:
  - Three USART interfaces with pin functions assigned through the switch matrix.
  - Two SPI controllers with pin functions assigned through the switch matrix.
  - One I^2C-bus interface with pin functions assigned through the switch matrix.
- Clock generation:
  - 12 MHz internal RC oscillator trimmed to 1.5 % accuracy that can optionally be used as a system clock.
  - Crystal oscillator with an operating range of 1 MHz to 25 MHz.
  - Programmable watchdog oscillator with a frequency range of 9.4 kHz to 2.3 MHz.
  - 10 kHz low-power oscillator for the WKT.
  - PLL allows CPU operation up to the maximum CPU rate without the need for a high-frequency crystal. May be run from the system oscillator, the external clock input CLKIN, or the internal RC oscillator.
  - Clock output function with divider that can reflect the crystal oscillator, the main clock, the IRC, or the watchdog oscillator.
- Power control:
  - Integrated PMU (Power Management Unit) to minimize power consumption.
  - Reduced power modes: Sleep mode, Deep-sleep mode, Power-down mode, and Deep power-down mode.
  - Wake-up from Deep-sleep and Power-down modes on activity on USART, SPI, and I2C peripherals.
  - Timer-controlled self wake-up from Deep power-down mode.
  - Power-On Reset (POR).
  - Brownout detect.
- Unique device serial number for identification.
- Single power supply.
- Operating temperature range −40 °C to 105 °C except for the DIP8 package, which is available for a temperature range of −40 °C to 85 °C.
- Available as DIP8, TSSOP16, SO20, TSSOP20, and XSON16 package.

3. Applications

- 8/16-bit applications
- Consumer
- Climate control
- Lighting
- Motor control
- Fire and security applications

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4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
LPC810M021FN8	DIP8	plastic dual in-line package; 8 leads (300 mil)	SOT097-2
LPC811M001JDH16	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
LPC812M101JDH16	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
LPC812M101JD20	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
LPC812M101JDH20	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1
LPC812M101JTB16	XSON16	plastic extremely thin small outline package; no leads; 16 terminals; body 2.5 × 3.2 × 0.5 mm	SOT1341-1

4.1 Ordering options

Table 2. Ordering options

Type number	Flash/kB	SRAM/kB	USART	I^2C-bus	SPI	Comparator	GPIO	Package
LPC810M021FN8	4	1	2	1	1	1	6	DIP8
LPC811M001JDH16	8	2	2	1	1	1	14	TSSOP16
LPC812M101JDH16	16	4	3	1	2	1	14	TSSOP16
LPC812M101JD20	16	4	2	1	1	1	18	SO20
LPC812M101JDH20	16	4	3	1	2	1	18	TSSOP20
LPC812M101JTB16	16	4	3	1	2	1	14	XSON16

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5. Marking

The LPC81xM devices typically have the following top-side marking:

LPC81x

xxxxx

xxxxxxxx

xxYWWxR[x]

The last two letters in the last line (field ‘xR’) identify the boot code version and device revision.

Table 3. Device revision table

Revision identifier (xR)	Revision description
‘1A’	Initial device revision with boot code version 13.1
‘2A’	Device revision with boot code version 13.2
’4C’	Device revision with boot code version 13.4

Field ‘Y’ states the year the device was manufactured. Field ‘WW’ states the week the device was manufactured during that year.

Remark: On the TSSOP16 package, the last line includes only the date code xxYWW.

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6. Block diagram

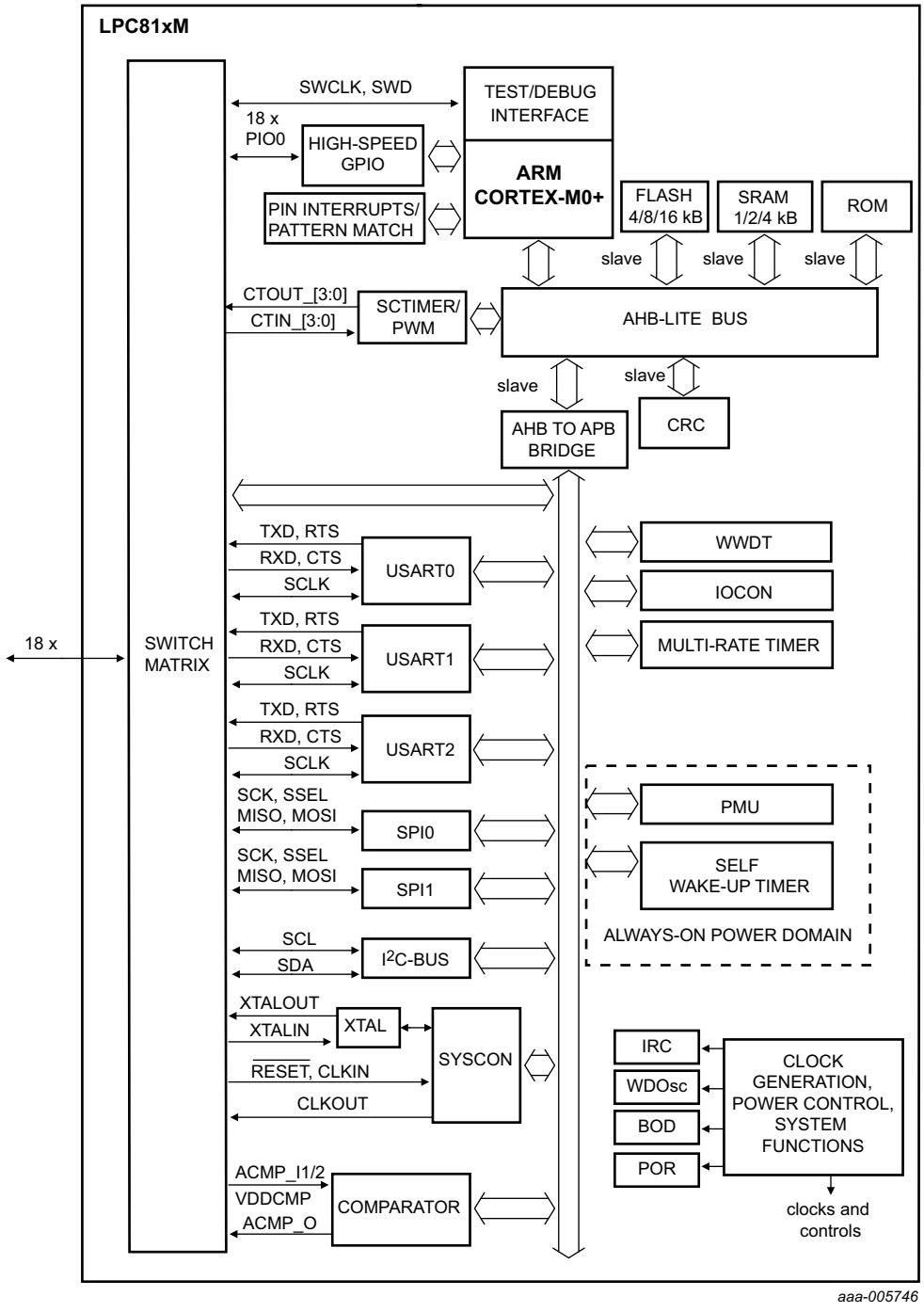

Fig 1. LPC81xM block diagram

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7. Pinning information

7.1 Pinning

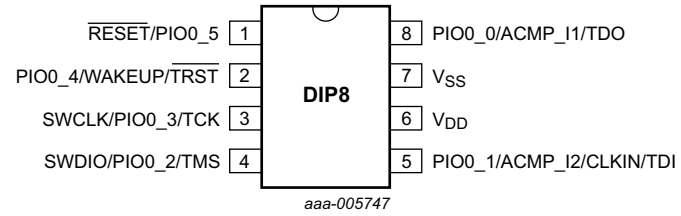

Fig 2. Pin configuration DIP8 package (LPC810M021JN8)

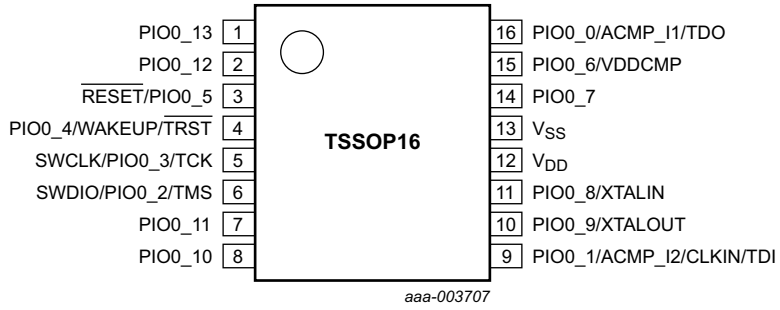

Fig 3. Pin configuration TSSOP16 package (LPC811M001JDH16 and LPC812M101JDH16)

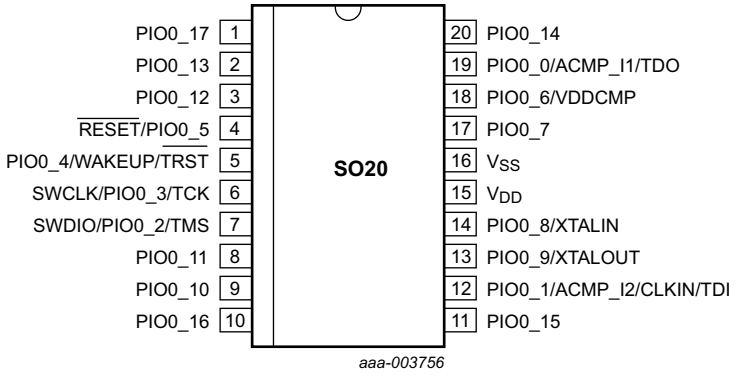

Fig 4. Pin configuration SO20 package (LPC812M101JD20)

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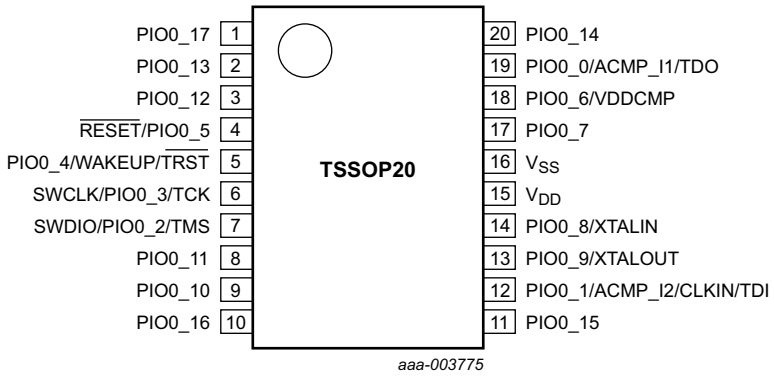

Fig 5. Pin configuration TSSOP20 package (LPC812M101JDH20)

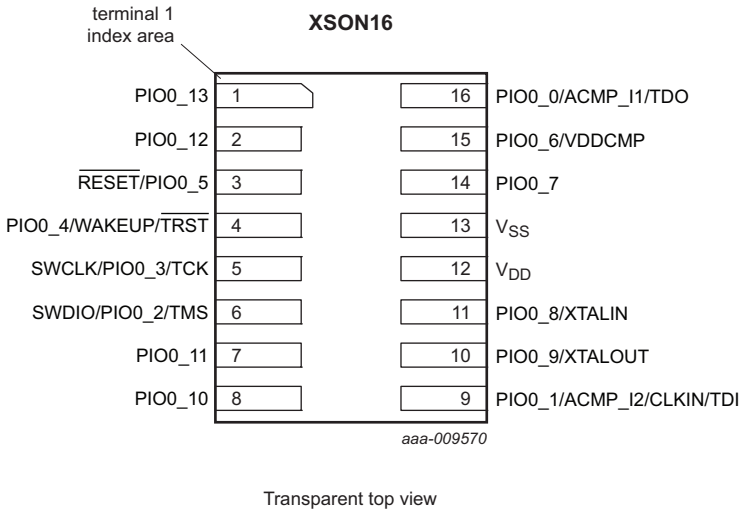

Fig 6. Pin configuration XSON16 package (LPC812M101JTB16)

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7.2 Pin description

The pin description consists of two parts showing pin functions that are fixed to a certain package pin (see Table 4) and showing pin functions that can be assigned to any pin on the package through the switch matrix (see Table 5).

The pin description table in Table 4 shows the pin functions that are fixed to specific pins on each package. These fixed-pin functions are selectable between GPIO and the comparator inputs, SWD, $\overline{\text{RESET}}$, and the XTAL pins. By default, the GPIO function is selected except on pins PIO0_2, PIO0_3, and PIO0_5. JTAG functions are available in boundary scan mode only.

Table 5 shows the the I2C, USART, SPI, and SCT pin functions, which can be assigned through the switch matrix to any pin that is not power or ground in place of the pin's fixed functions.

The following exceptions apply:

For full I2C-bus compatibility, assign the I2C functions to the open-drain pins PIO0_11 and PIO0_10.

Do not assign more than one output to any pin. However, more than one input can be assigned to a pin. Once any function is assigned to a pin, the pin's GPIO functionality is disabled.

Pin PIO0_4 triggers a wake-up from Deep power-down mode. If you need to wake up from Deep power-down mode via an external pin, do not assign any movable function to this pin.

The JTAG functions TDO, TDI, TCK, TMS, and $\overline{\text{TRST}}$ are selected on pins PIO0_0 to PIO0_4 by hardware when the part is in boundary scan mode.

Table 4. Pin description table (fixed pins)

Symbol	SO20/ TSSOP20	TSSOP16	XSON16	DIP8		Type	Reset state [1]	Description
PIO0_0/ACMP_I1/ TDO	19	16	16	8	[5]	I/O	I; PU	**PIO0_0 —** General purpose digital input/output port 0 pin 0. In ISP mode, this is the USART0 receive pin U0_RXD. In boundary scan mode: TDO (Test Data Out).
						AI	-	**ACMP_I1 —** Analog comparator input 1.
PIO0_1/ACMP_I2/ CLKIN/TDI	12	9	9	5	[5]	I/O	I; PU	**PIO0_1 —** General purpose digital input/output pin. In boundary scan mode: TDI (Test Data In). ISP entry pin on chip versions 1A and 2A and on the DIP8 package (see Table 6). For these chip versions and packages, a LOW level on this pin during reset starts the ISP command handler. See PIO0_12 for all other packages.
						AI	-	**ACMP_I2 —** Analog comparator input 2.
						I	-	**CLKIN —** External clock input.

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Table 4. Pin description table (fixed pins)

Symbol	SO20/ TSSOP20	TSSOP16	XSON16	DIP8		Type	Reset state [1]	Description
SWDIO/PIO0_2/TMS	7	6	6	4	[2]	I/O	I; PU	**SWDIO —** Serial Wire Debug I/O. SWDIO is enabled by default on this pin. In boundary scan mode: TMS (Test Mode Select).
						I/O	-	**PIO0_2 —** General purpose digital input/output pin.
SWCLK/PIO0_3/ TCK	6	5	5	3	[2]	I/O	I; PU	**SWCLK —** Serial Wire Clock. SWCLK is enabled by default on this pin. In boundary scan mode: TCK (Test Clock).
						I/O	-	**PIO0_3 —** General purpose digital input/output pin.
PIO0_4/WAKEUP/ $\overline{\text{TRST}}$	5	4	4	2	[6]	I/O	I; PU	**PIO0_4 —** General purpose digital input/output pin. In ISP mode, this is the USART0 transmit pin U0_TXD. In boundary scan mode: $\overline{\text{TRST}}$ (Test Reset). This pin triggers a wake-up from Deep power-down mode. If you need to wake up from Deep power-down mode via an external pin, do not assign any movable function to this pin. This pin should be pulled HIGH externally before entering Deep power-down mode. A LOW-going pulse as short as 50 ns causes the chip to exit Deep power-down mode and wakes up the part.
$\overline{\text{RESET}}$/PIO0_5	4	3	3	1	[4]	I/O	I; PU	**$\overline{\text{RESET}}$ —** External reset input: A LOW-going pulse as short as 50 ns on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0. In deep power-down mode, this pin must be pulled HIGH externally. The $\overline{\text{RESET}}$ pin can be left unconnected or be used as a GPIO or for any movable function if an external $\overline{\text{RESET}}$ function is not needed and the Deep power-down mode is not used.
						I	-	**PIO0_5 —** General purpose digital input/output pin.
PIO0_6/VDDCMP	18	15	15	-	[9]	I/O	I; PU	**PIO0_6 —** General purpose digital input/output pin.
						AI	-	**VDDCMP —** Alternate reference voltage for the analog comparator.
PIO0_7	17	14	14	-	[2]	I/O	I; PU	**PIO0_7 —** General purpose digital input/output pin.
PIO0_8/XTALIN	14	11	11	-	[8]	I/O	I; PU	**PIO0_8 —** General purpose digital input/output pin.
						I	-	**XTALIN —** Input to the oscillator circuit and internal clock generator circuits. Input voltage must not exceed 1.95 V.
PIO0_9/XTALOUT	13	10	10	-	[8]	I/O	I; PU	**PIO0_9 —** General purpose digital input/output pin.
						O	-	**XTALOUT —** Output from the oscillator circuit.
PIO0_10	9	8	8	-	[3]	I	IA	**PIO0_10 —** General purpose digital input/output pin. Assign I2C functions to this pin when true open-drain pins are needed for a signal compliant with the full I2C specification.
PIO0_11	8	7	7	-	[3]	I	IA	**PIO0_11 —** General purpose digital input/output pin. Assign I2C functions to this pin when true open-drain pins are needed for a signal compliant with the full I2C specification.

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Table 4. Pin description table (fixed pins)

Symbol	SO20/ TSSOP20	TSSOP16	XSON16	DIP8		Type	Reset state [1]	Description
PIO0_12	3	2	2	-	[2]	I/O	I; PU	**PIO0_12 —** General purpose digital input/output pin. ISP entry pin on the SO20/TSSOP20/TSSOP16/XSON16 packages starting with chip version 4C (see Table 6). A LOW level on this pin during reset starts the ISP command handler. See pin PIO0_1 for the DIP8 package and chip versions 1A and 2A.
PIO0_13	2	1	1	-	[2]	I/O	I; PU	**PIO0_13 —** General purpose digital input/output pin.
PIO0_14	20	-	-	-	[7]	I/O	I; PU	**PIO0_14 —** General purpose digital input/output pin.
PIO0_15	11	-	-	-	[7]	I/O	I; PU	**PIO0_15 —** General purpose digital input/output pin.
PIO0_16	10	-	-	-	[7]	I/O	I; PU	**PIO0_16 —** General purpose digital input/output pin.
PIO0_17	1	-	-	-	[7]	I/O	I; PU	**PIO0_17 —** General purpose digital input/output pin.
V_{DD}	15	12	12	6		-	-	3.3 V supply voltage.
V_{SS}	16	13	13	7		-	-	Ground.

[1] Pin state at reset for default function: I = Input; AI = Analog Input; O = Output; PU = internal pull-up enabled (pins pulled up to full V_{DD} level); IA = inactive, no pull-up/down enabled.

[2] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis; includes high-current output driver.

[3] True open-drain pin. I^2C-bus pins compliant with the I^2C-bus specification for I^2C standard mode, I^2C Fast-mode, and I^2C Fast-mode Plus. Do not use this pad for high-speed applications such as SPI or USART. The pin requires an external pull-up to provide output functionality. When power is switched off, this pin is floating and does not disturb the I2C lines. Open-drain configuration applies to all functions on this pin.

Remark: If this pin is not available on the package, prevent it from internally floating as follows: Set bits 10 and 11 in the GPIO DIR0 register to 1 to enable the output driver and write 1 to bits 10 and 11 in the GPIO CLR0 register to drive the outputs LOW internally.

[4] See Figure 11 for the reset pad configuration. $\overline{\text{RESET}}$ functionality is not available in Deep power-down mode. Use the WAKEUP pin to reset the chip and wake up from Deep power-down mode. An external pull-up resistor is required on this pin for the Deep power-down mode.

[5] 5 V tolerant pin providing standard digital I/O functions with configurable modes, configurable hysteresis, and analog input. When configured as an analog input, the digital section of the pin is disabled, and the pin is not 5 V tolerant.

[6] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis. In Deep power-down mode, pulling this pin LOW wakes up the chip. The wake-up pin function can be disabled and the pin can be used for other purposes, if the WKT low power oscillator is enabled for waking up the part from Deep power-down mode.

[7] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis.

[8] 5 V tolerant pin providing standard digital I/O functions with configurable modes, configurable hysteresis, and analog I/O for the system oscillator. When configured as an analog I/O, the digital section of the pin is disabled, and the pin is not 5 V tolerant.

[9] The digital part of this pin is 3 V tolerant pin due to special analog functionality. Pin provides standard digital I/O functions with configurable modes, configurable hysteresis, and an analog input. When configured as an analog input, the digital section of the pin is disabled.

Table 5. Movable functions (assign to pins PIO0_0 to PIO_17 through switch matrix)

Function name	Type	Description
U0_TXD	O	Transmitter output for USART0.
U0_RXD	I	Receiver input for USART0.
$\overline{\text{U0_RTS}}$	O	Request To Send output for USART0.
$\overline{\text{U0_CTS}}$	I	Clear To Send input for USART0.

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Table 5. Movable functions (assign to pins PIO0_0 to PIO_17 through switch matrix)

Function name	Type	Description
U0_SCLK	I/O	Serial clock input/output for USART0 in synchronous mode.
U1_TXD	O	Transmitter output for USART1.
U1_RXD	I	Receiver input for USART1.
$\overline{\text{U1_RTS}}$	O	Request To Send output for USART1.
$\overline{\text{U1_CTS}}$	I	Clear To Send input for USART1.
U1_SCLK	I/O	Serial clock input/output for USART1 in synchronous mode.
U2_TXD	O	Transmitter output for USART2.
U2_RXD	I	Receiver input for USART2.
$\overline{\text{U2_RTS}}$	O	Request To Send output for USART2.
$\overline{\text{U2_CTS}}$	I	Clear To Send input for USART2.
U2_SCLK	I/O	Serial clock input/output for USART2 in synchronous mode.
SPI0_SCK	I/O	Serial clock for SPI0.
SPI0_MOSI	I/O	Master Out Slave In for SPI0.
SPI0_MISO	I/O	Master In Slave Out for SPI0.
SPI0_SSEL	I/O	Slave select for SPI0.
SPI1_SCK	I/O	Serial clock for SPI1.
SPI1_MOSI	I/O	Master Out Slave In for SPI1.
SPI1_MISO	I/O	Master In Slave Out for SPI1.
SPI1_SSEL	I/O	Slave select for SPI1.
CTIN_0	I	SCT input 0.
CTIN_1	I	SCT input 1.
CTIN_2	I	SCT input 2.
CTIN_3	I	SCT input 3.
CTOUT_0	O	SCT output 0.
CTOUT_1	O	SCT output 1.
CTOUT_2	O	SCT output 2.
CTOUT_3	O	SCT output 3.
I2C0_SCL	I/O	I^2C-bus clock input/output (open-drain if assigned to pin PIO0_10). High-current sink only if assigned to PIO0_10 and if I^2C Fast-mode Plus is selected in the I/O configuration register.
I2C0_SDA	I/O	I^2C-bus data input/output (open-drain if assigned to pin PIO0_11). High-current sink only if assigned to pin PIO0_11 and if I^2C Fast-mode Plus is selected in the I/O configuration register.
ACMP_O	O	Analog comparator digital output.
CLKOUT	O	Clock output.
GPIO_INT_BMAT	O	Output of the pattern match engine.

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Table 6. Pin location in ISP mode

ISP entry pin	USART RXD	USART TXD	Marking	Boot loader version	Package
PIO0_1	PIO0_0	PIO0_4	1A	v 13.1	TSSOP20; SO20; TSSOP16; DIP8; XSON16
PIO0_1	PIO0_0	PIO0_4	2A	v 13.2	TSSOP20; SO20; TSSOP16; DIP8; XSON16
PIO0_1	PIO0_0	PIO0_4	4C and later	v 13.4 and later	DIP8
PIO0_12	PIO0_0	PIO0_4	4C and later	v 13.4 and later	TSSOP20; SO20; TSSOP16; XSON16

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8. Functional description

8.1 ARM Cortex-M0+ core

The ARM Cortex-M0+ core runs at an operating frequency of up to 30 MHz using a two-stage pipeline. Integrated in the core are the NVIC and Serial Wire Debug with four breakpoints and two watchpoints. The ARM Cortex-M0+ core supports a single-cycle I/O enabled port for fast GPIO access.

The core includes a single-cycle multiplier and a system tick timer.

8.2 On-chip flash program memory

The LPC81xM contain up to 16 kB of on-chip flash program memory. The flash memory supports a 64 Byte page size with page write and erase.

8.3 On-chip SRAM

The LPC81xM contain a total of up to 4 kB on-chip static RAM data memory.

8.4 On-chip ROM

The 8 kB on-chip ROM contains the boot loader and the following Application Programming Interfaces (API):

- In-System Programming (ISP) and In-Application Programming (IAP) support for flash programming
- Power profiles for configuring power consumption and PLL settings
- USART driver API routines
- I^2C-bus driver API routines

8.5 Nested Vectored Interrupt Controller (NVIC)

The Nested Vectored Interrupt Controller (NVIC) is an integral part of the Cortex-M0+. The tight coupling to the CPU allows for low interrupt latency and efficient processing of late arriving interrupts.

8.5.1 Features

- Controls system exceptions and peripheral interrupts.
- On the LPC81xM, the NVIC supports 32 vectored interrupts including up to 8 external interrupt inputs selectable from all GPIO pins.
- Four programmable interrupt priority levels with hardware priority level masking.
- Software interrupt generation using the ARM exceptions SVCall and PendSV.
- Relocatable interrupt vector table using vector table offset register.

8.5.2 Interrupt sources

Each peripheral device has one interrupt line connected to the NVIC but may have several interrupt flags. Individual interrupt flags may also represent more than one interrupt source.

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Up to eight pins, regardless of the selected function, can be programmed to generate an interrupt on a level, a rising or falling edge, or both. The interrupt generating pins can be selected from all digital or mixed digital/analog pins. The pin interrupt/pattern match block controls the edge or level detection mechanism.

8.6 System tick timer

The ARM Cortex-M0+ includes a 24-bit system tick timer (SysTick) that is intended to generate a dedicated SysTick exception at a fixed time interval (typically 10 ms).

8.7 Memory map

The LPC81xM incorporates several distinct memory regions. Figure 7 shows the overall map of the entire address space from the user program viewpoint following reset. The interrupt vector area supports address remapping.

The ARM private peripheral bus includes the ARM core registers for controlling the NVIC, the system tick timer (SysTick), and the reduced power modes.

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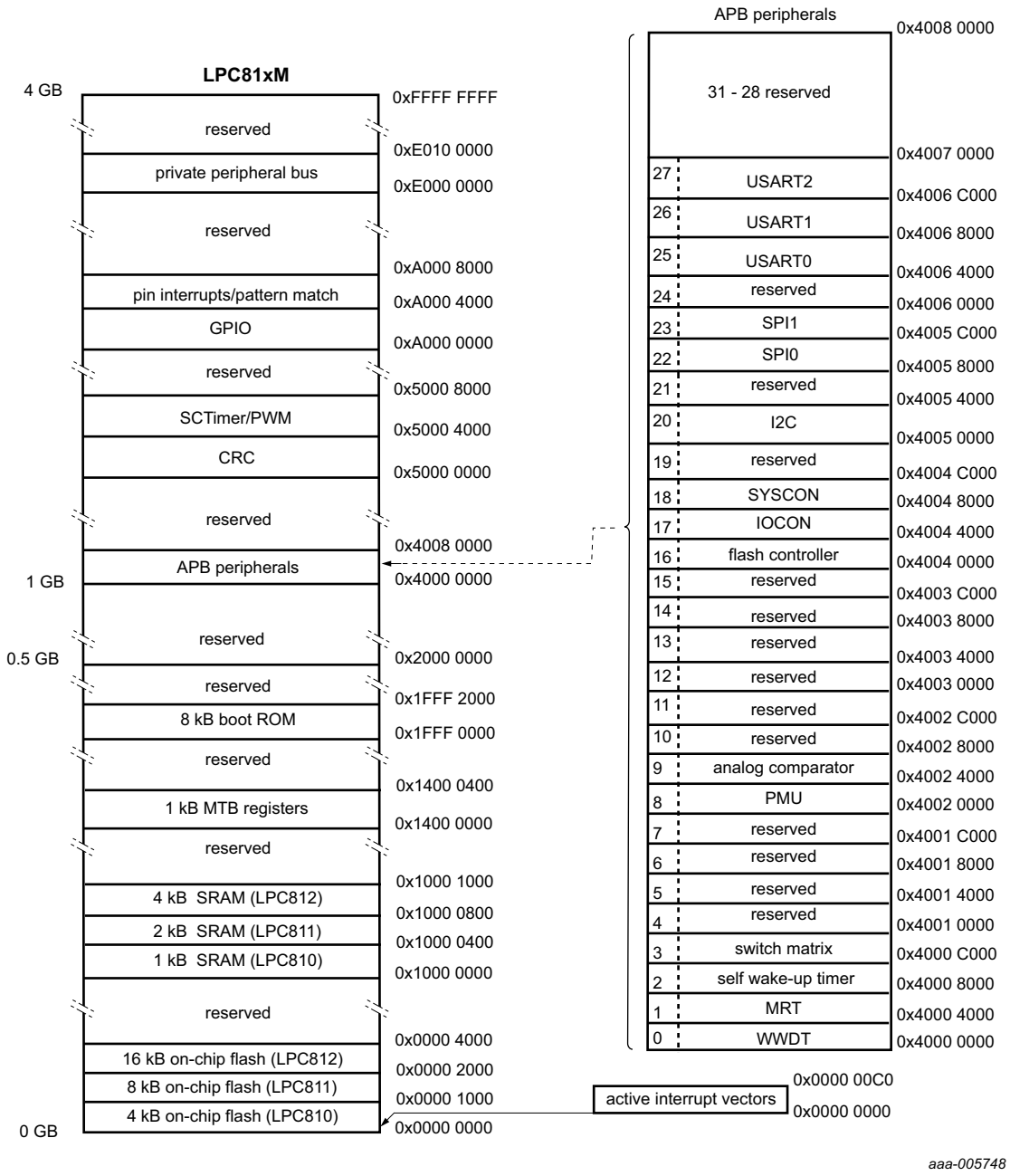

Fig 7. LPC81xM Memory map

8.8 I/O configuration

The IOCON block controls the configuration of the I/O pins. Each digital or mixed digital/analog pin with the PIO0_n designator (except the true open-drain pins PIO0_10 and PIO0_11) in Table 4 can be configured as follows:

- Enable or disable the weak internal pull-up and pull-down resistors.
- Select a pseudo open-drain mode. The input cannot be pulled up above V_{DD}. This pin is not 5 V tolerant when V_{DD} = 0.

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- Program the input glitch filter with different filter constants using one of the IOCON divided clock signals (IOCONCLKCDIV, see Figure 10 “LPC81xM clock generation”). You can also bypass the glitch filter.
- Invert the input signal.
- Hysteresis can be enabled or disabled.
- For pins PIO0_10 and PIO0_11, select the I2C-mode and output driver for standard digital operation, for I2C standard and fast modes, or for I2C Fast mode+.
- On mixed digital/analog pins, enable the analog input mode. Enabling the analog mode disconnects the digital functionality.

Remark: The functionality of each I/O pin is flexible and is determined entirely through the switch matrix. See Section 8.9 for details.

8.8.1 Standard I/O pad configuration

Figure 8 shows the possible pin modes for standard I/O pins with analog input function:

- Digital output driver with configurable open-drain output
- Digital input: Weak pull-up resistor (PMOS device) enabled/disabled
- Digital input: Weak pull-down resistor (NMOS device) enabled/disabled
- Digital input: Repeater mode enabled/disabled
- Digital input: Input glitch filter selectable on all pins
- Analog input

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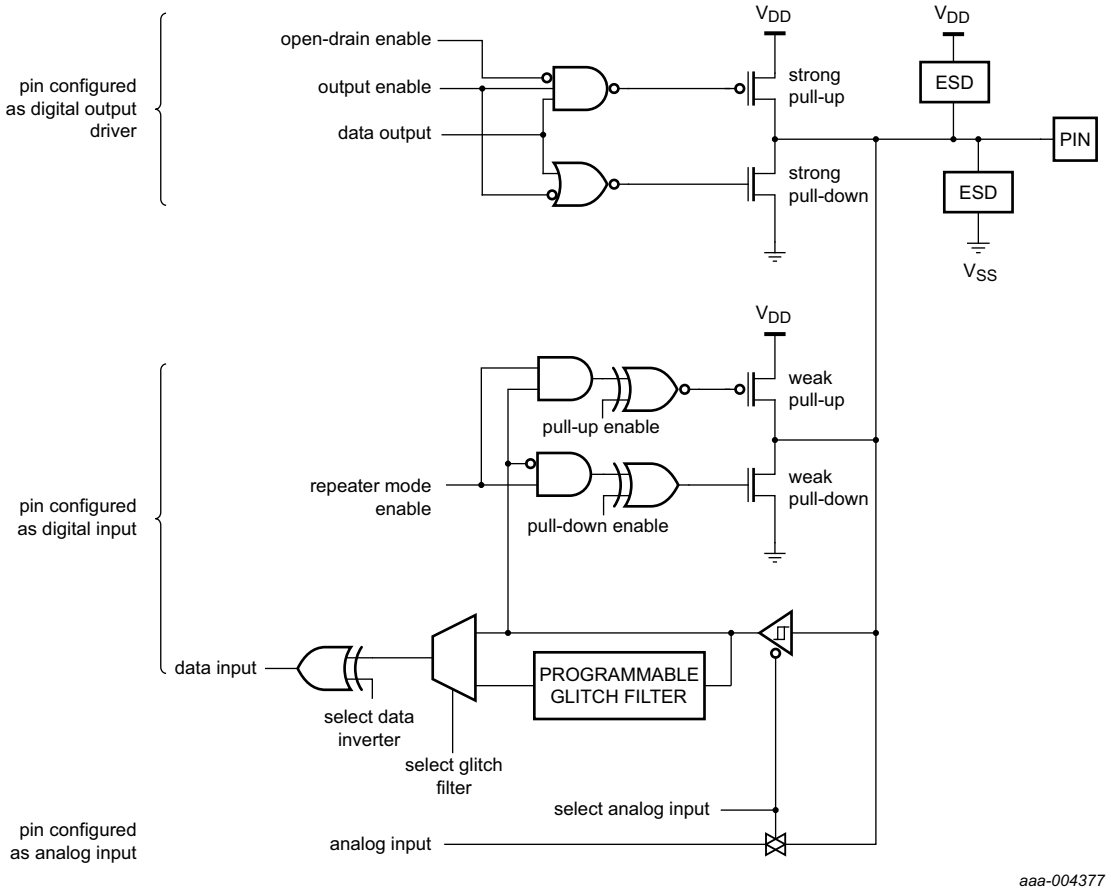

Fig 8. Standard I/O pad configuration

8.9 Switch Matrix (SWM)

The switch matrix controls the function of each digital or mixed analog/digital pin in a highly flexible way by allowing to connect many functions like the USART, SPI, SCT, and I2C functions to any pin that is not power or ground. These functions are called movable functions and are listed in Table 5.

Functions that need specialized pads like the oscillator pins XTALIN and XTALOUT can be enabled or disabled through the switch matrix. These functions are called fixed-pin functions and cannot move to other pins. The fixed-pin functions are listed in Table 4. If a fixed-pin function is disabled, any other movable function can be assigned to this pin.

8.10 Fast General-Purpose parallel I/O (GPIO)

Device pins that are not connected to a specific peripheral function are controlled by the GPIO registers. Pins may be dynamically configured as inputs or outputs. Multiple outputs can be set or cleared in one write operation.

LPC81xM use accelerated GPIO functions:

- GPIO registers are located on the ARM Cortex M0+ IO bus for fastest possible single-cycle I/O timing, allowing GPIO toggling with rates of up to 15 MHz.

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- An entire port value can be written in one instruction.
- Mask, set, and clear operations are supported for the entire port.

All GPIO port pins are fixed-pin functions that are enabled or disabled on the pins by the switch matrix. Therefore each GPIO port pin is assigned to one specific pin and cannot be moved to another pin. Except for pins SWDIO/PIO0_2, SWCLK/PIO0_3, and RESET/PIO0_5, the switch matrix enables the GPIO port pin function by default.

8.10.1 Features

- Bit level port registers allow a single instruction to set and clear any number of bits in one write operation.
- Direction control of individual bits.
- All I/O default to inputs with internal pull-up resistors enabled after reset - except for the I^2C-bus true open-drain pins PIO0_2 and PIO0_3.
- Pull-up/pull-down configuration, repeater, and open-drain modes can be programmed through the IOCON block for each GPIO pin (see Figure 8).
-

8.11 Pin interrupt/pattern match engine

The pin interrupt block configures up to eight pins from all digital pins for providing eight external interrupts connected to the NVIC.

The pattern match engine can be used, in conjunction with software, to create complex state machines based on pin inputs.

Any digital pin, independently of the function selected through the switch matrix, can be configured through the SYSCON block as input to the pin interrupt or pattern match engine. The registers that control the pin interrupt or pattern match engine are located on the IO+ bus for fast single-cycle access.

8.11.1 Features

- Pin interrupts
  - Up to eight pins can be selected from all digital pins as edge- or level-sensitive interrupt requests. Each request creates a separate interrupt in the NVIC.
  - Edge-sensitive interrupt pins can interrupt on rising or falling edges or both.
  - Level-sensitive interrupt pins can be HIGH- or LOW-active.
  - Pin interrupts can wake up the LPC81xM from sleep mode, deep-sleep mode, and power-down mode.
- Pin interrupt pattern match engine
  - Up to eight pins can be selected from all digital pins to contribute to a boolean expression. The boolean expression consists of specified levels and/or transitions on various combinations of these pins.
  - Each minterm (product term) comprising the specified boolean expression can generate its own, dedicated interrupt request.
  - Any occurrence of a pattern match can be programmed to also generate an RXEV notification to the ARM CPU. The RXEV signal can be connected to a pin.

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– The pattern match engine does not facilitate wake-up.

8.12 USART0/1/2

Remark: USART0 and USART1 are available on all LPC800 parts. USART2 is available on parts LPC812M101JTB16, LPC812M101JDH16, and LPC812M101JDH20 only.

All USART functions are movable functions and are assigned to pins through the switch matrix.

8.12.1 Features

- Maximum bit rates of 1.875 Mbit/s in asynchronous mode and 10 Mbit/s in synchronous mode for USART functions connected to all digital pins except PIO0_10 and PIO0_11.
- 7, 8, or 9 data bits and 1 or 2 stop bits
- Synchronous mode with master or slave operation. Includes data phase selection and continuous clock option.
- Multiprocessor/multidrop (9-bit) mode with software address compare. (RS-485 possible with software address detection and transceiver direction control.)
- Parity generation and checking: odd, even, or none.
- One transmit and one receive data buffer.
- RTS/CTS for hardware signaling for automatic flow control. Software flow control can be performed using Delta CTS detect, Transmit Disable control, and any GPIO as an RTS output.
- Received data and status can optionally be read from a single register
- Break generation and detection.
- Receive data is 2 of 3 sample "voting". Status flag set when one sample differs.
- Built-in Baud Rate Generator.
- A fractional rate divider is shared among all UARTs.
- Interrupts available for Receiver Ready, Transmitter Ready, Receiver Idle, change in receiver break detect, Framing error, Parity error, Overrun, Underrun, Delta CTS detect, and receiver sample noise detected.
- Separate data and flow control loopback modes for testing.
- Supported by on-chip ROM API.

8.13 SPI0/1

Remark: SPI0 is available on all LPC800 parts. SPI1 is available on parts LPC812M101JDH16 and LPC812M101JDH20 only.

All SPI functions are movable functions and are assigned to pins through the switch matrix.

8.13.1 Features

- Maximum data rates of 30 Mbit/s in master mode and 25 Mbit/s in slave mode for SPI functions connected to all digital pins except PIO0_10 and PIO0_11.

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- Data frames of 1 to 16 bits supported directly. Larger frames supported by software.
- Master and slave operation.
- Data can be transmitted to a slave without the need to read incoming data. This can be useful while setting up an SPI memory.
- Control information can optionally be written along with data. This allows very versatile operation, including “any length” frames.
- One Slave Select input/output with selectable polarity and flexible usage.

Remark: Texas Instruments SSI and National Microwire modes are not supported.

8.14 I2C-bus interface

The I^2C-bus is bidirectional for inter-IC control using only two wires: a serial clock line (SCL) and a serial data line (SDA). Each device is recognized by a unique address and can operate as either a receiver-only device (e.g., an LCD driver) or a transmitter with the capability to both receive and send information (such as memory). Transmitters and/or receivers can operate in either master or slave mode, depending on whether the chip has to initiate a data transfer or is only addressed. The I^2C is a multi-master bus and can be controlled by more than one bus master connected to it.

The I2C-bus functions are movable functions and can be assigned through the switch matrix to any pin. However, only the true open-drain PIO0_10 and PIO0_11 provide the electrical characteristics to support the full I2C-bus specification (see Ref. 1).

8.14.1 Features

- Supports standard and fast mode with data rates of up to 400 kbit/s.
- Independent Master, Slave, and Monitor functions.
- Supports both Multi-master and Multi-master with Slave functions.
- Multiple I^2C slave addresses supported in hardware.
- One slave address can be selectively qualified with a bit mask or an address range in order to respond to multiple I^2C bus addresses.
- 10-bit addressing supported with software assist.
- Supports SMBus.
- Supported by on-chip ROM API.
- If the I2C functions are connected to the true open-drain pins (PIO0_10 and PIO0_11), the I2C supports the full I2C-bus specification:
  - Fail-safe operation: When the power to an I^2C-bus device is switched off, the SDA and SCL pins connected to the I^2C-bus are floating and do not disturb the bus.
  - Supports Fast-mode Plus with bit rates up to 1 Mbit/s.

8.15 State-Configurable Timer/PWM (SCTimer/PWM)

The state configurable timer (SCTimer/PWM or SCT) can perform basic 16-bit and 32-bit timer/counter functions with match outputs and external and internal capture inputs. In addition, the SCTimer/PWM can employ up to two different programmable states, which can change under the control of events, to provide complex timing patterns.

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All inputs and outputs of the SCTimer/PWM are movable functions and are assigned to pins through the switch matrix.

8.15.1 Features

- Two 16-bit counters or one 32-bit counter.
- Counters clocked by bus clock or selected input.
- Up counters or up-down counters.
- State variable allows sequencing across multiple counter cycles.
- The following conditions define an event: a counter match condition, an input (or output) condition, a combination of a match and/or and input/output condition in a specified state, and the count direction.
- Events control outputs, interrupts, and the SCT states.
  - Match register 0 can be used as an automatic limit.
  - In bi-directional mode, events can be enabled based on the count direction.
  - Match events can be held until another qualifying event occurs.
- Selected events can limit, halt, start, or stop a counter.
- Supports:
  - 4 inputs
  - 4 outputs
  - 5 match/capture registers
  - 6 events
  - 2 states

8.16 Multi-Rate Timer (MRT)

The Multi-Rate Timer (MRT) provides a repetitive interrupt timer with four channels. Each channel can be programmed with an independent time interval, and each channel operates independently from the other channels.

8.16.1 Features

- 31-bit interrupt timer
- Four channels independently counting down from individually set values
- Bus stall, repeat and one-shot interrupt modes

8.17 Windowed WatchDog Timer (WWDT)

The watchdog timer resets the controller if software fails to periodically service it within a programmable time window.

8.17.1 Features

- Internally resets chip if not periodically reloaded during the programmable time-out period.
- Optional windowed operation requires reload to occur between a minimum and maximum time period, both programmable.

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- Optional warning interrupt can be generated at a programmable time prior to watchdog time-out.
- Enabled by software but requires a hardware reset or a watchdog reset/interrupt to be disabled.
- Incorrect feed sequence causes reset or interrupt if enabled.
- Flag to indicate watchdog reset.
- Programmable 24-bit timer with internal prescaler.
- Selectable time period from ($T_{cy(WDCLK)} \times 256 \times 4$) to ($T_{cy(WDCLK)} \times 2^{24} \times 4$) in multiples of $T_{cy(WDCLK)} \times 4$.
- The Watchdog Clock (WDCLK)is generated by a the dedicated watchdog oscillator (WDOSC).

8.18 Self Wake-up Timer (WKT)

The self wake-up timer is a 32-bit, loadable down-counter. Writing any non-zero value to this timer automatically enables the counter and launches a count-down sequence. When the counter is used as a wake-up timer, this write can occur just prior to entering a reduced power mode.

8.18.1 Features

- 32-bit loadable down-counter. Counter starts automatically when a count value is loaded. Time-out generates an interrupt/wake up request.
- The WKT resides in a separate, always-on power domain.
- The WKT supports two clock sources: the low-power oscillator and the IRC. The low-power oscillator is located in the always-on power domain, so it can be used as the clock source in Deep power-down mode.
- The WKT can be used for waking up the part from any reduced power mode, including Deep power-down mode, or for general-purpose timing.

8.19 Analog comparator (ACMP)

The analog comparator with selectable hysteresis can compare voltage levels on external pins and internal voltages.

After power-up and after switching the input channels of the comparator, the output of the voltage ladder must be allowed to settle to its stable value before it can be used as a comparator reference input. Settling times are given in Table 23.

The analog comparator output is a movable function and is assigned to a pin through the switch matrix. The comparator inputs and the voltage reference are enabled or disabled on pins PIO0_0 and PIO0_1 through the switch matrix.

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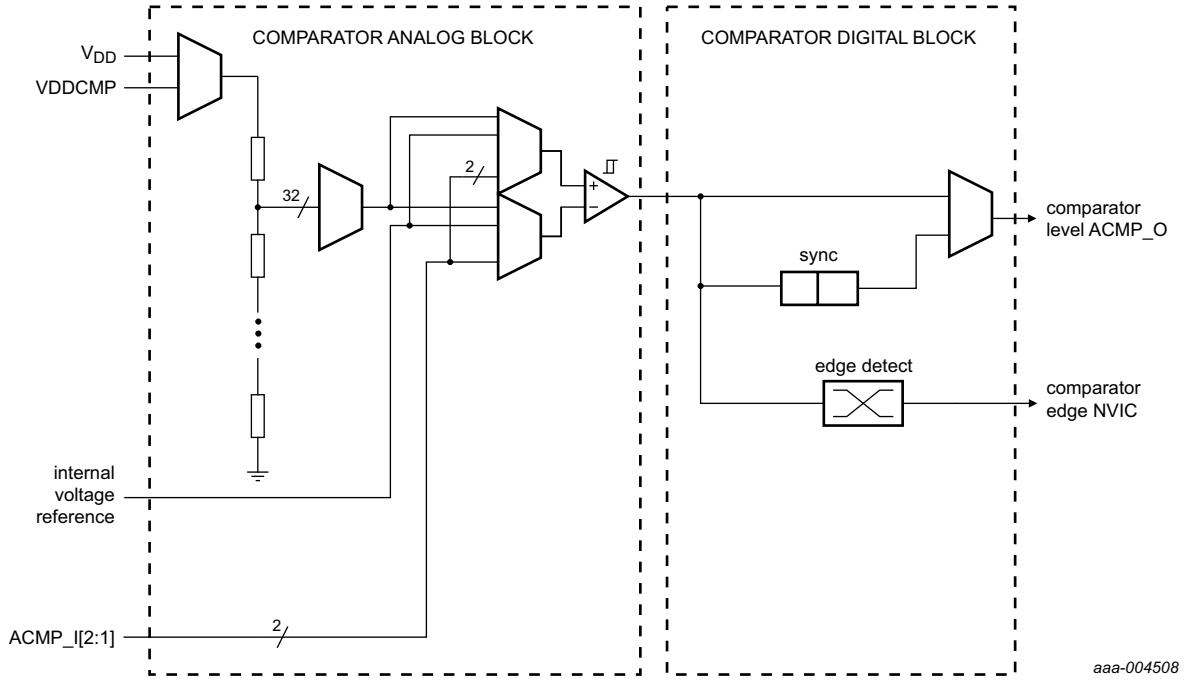

Fig 9. Comparator block diagram

8.19.1 Features

- Selectable 0 mV, 10 mV (± 5 mV), and 20 mV (± 10 mV), 40 mV (± 20 mV) input hysteresis.
- Two selectable external voltages (V_{DD} or VDDCMP on pin PIO0_6); fully configurable on either positive or negative input channel.
- Internal voltage reference from band gap selectable on either positive or negative input channel.
- 32-stage voltage ladder with the internal reference voltage selectable on either the positive or the negative input channel.
- Voltage ladder source voltage is selectable from an external pin or the main 3.3 V supply voltage rail.
- Voltage ladder can be separately powered down for applications only requiring the comparator function.
- Interrupt output is connected to NVIC.
- Comparator level output is connected to output pin ACMP_O.
- The comparator output can be routed internally to the SCT input through the switch matrix.

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8.20 Clocking and power control

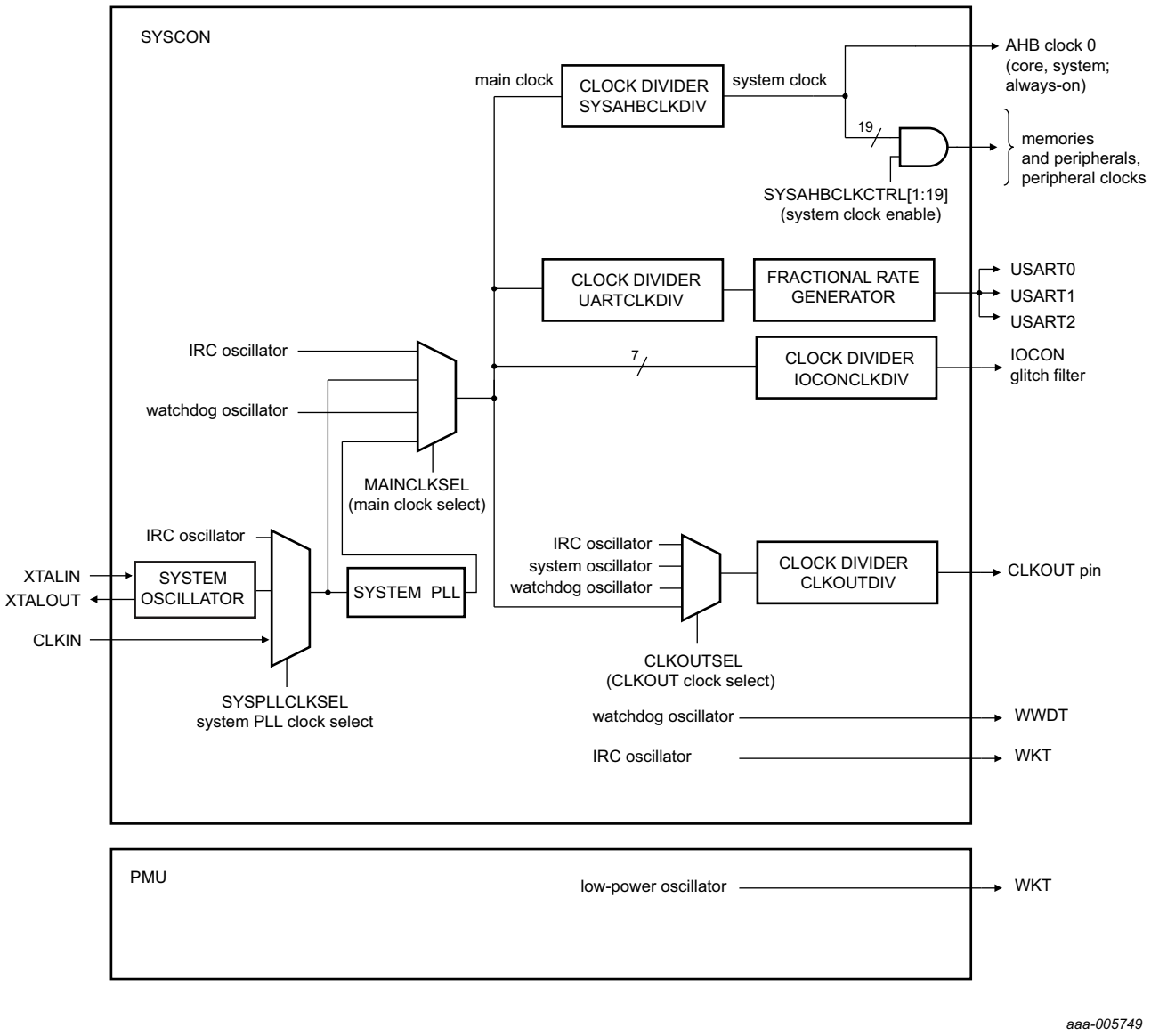

Fig 10. LPC81xM clock generation

8.20.1 Crystal and internal oscillators

The LPC81xM include four independent oscillators:

1. The crystal oscillator (SysOsc) operating at frequencies between 1 MHz and 25 MHz.
2. The internal RC Oscillator (IRC) with a fixed frequency of 12 MHz, trimmed to 1% accuracy.
3. The internal low-power, low-frequency Oscillator with a nominal frequency of 10 kHz with 40% accuracy for use with the self wake-up timer.
4. The dedicated Watchdog Oscillator (WDOsc) with a programmable nominal frequency between 9.4 kHz and 2.3 MHz with 40% accuracy.

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Each oscillator, except the low-frequency oscillator, can be used for more than one purpose as required in a particular application.

Following reset, the LPC81xM will operate from the IRC until switched by software. This allows systems to operate without any external crystal and the bootloader code to operate at a known frequency.

See Figure 10 for an overview of the LPC81xM clock generation.

8.20.1.1 Internal RC Oscillator (IRC)

The IRC may be used as the clock source for the WWDT, and/or as the clock that drives the PLL and subsequently the CPU. The nominal IRC frequency is 12 MHz. The IRC is trimmed to 1.5 % accuracy over the entire voltage and temperature range.

The IRC can be used as a clock source for the CPU with or without using the PLL. The IRC frequency can be boosted to a higher frequency, up to the maximum CPU operating frequency, by the system PLL.

Upon power-up or any chip reset, the LPC81xM use the IRC as the clock source. Software may later switch to one of the other available clock sources.

8.20.1.2 Crystal Oscillator (SysOsc)

The crystal oscillator can be used as the clock source for the CPU, with or without using the PLL.

The SysOsc operates at frequencies of 1 MHz to 25 MHz. This frequency can be boosted to a higher frequency, up to the maximum CPU operating frequency, by the system PLL.

8.20.1.3 Internal Low-power Oscillator and Watchdog Oscillator (WDOsc)

The nominal frequency of the WDOsc is programmable between 9.4 kHz and 2.3 MHz. The frequency spread over silicon process variations is ± 40%.

The WDOsc is a dedicated oscillator for the windowed WWDT.

The internal low-power 10 kHz (± 40% accuracy) oscillator serves a the clock input to the WKT. This oscillator can be configured to run in all low power modes.

8.20.2 Clock input

An external clock source can be supplied on the selected CLKIN pin. When selecting a clock signal for the CLKIN pin, follow the specifications for digital I/O pins in Table 9 “Static characteristics” and Table 16 “Dynamic characteristics: I/O pins[1]”.

An 1.8 V external clock source can be supplied on the XTALIN pins to the system oscillator limiting the voltage of this signal ((see Section 14.2).

The maximum frequency for both clock signals is 25 MHz.

8.20.3 System PLL

The PLL accepts an input clock frequency in the range of 10 MHz to 25 MHz. The input frequency is multiplied up to a high frequency with a Current Controlled Oscillator (CCO). The multiplier can be an integer value from 1 to 32. The CCO operates in the range of 156 MHz to 320 MHz, so there is an additional divider in the loop to keep the CCO within its frequency range while the PLL is providing the desired output frequency. The output

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divider may be set to divide by 2, 4, 8, or 16 to produce the output clock. Since the minimum output divider value is 2, it is insured that the PLL output has a 50 % duty cycle. The PLL is turned off and bypassed following a chip reset and may be enabled by software. The program must configure and activate the PLL, wait for the PLL to lock, and then connect to the PLL as a clock source. The PLL settling time is nominally 100 μs.

8.20.4 Clock output

The LPC81xM features a clock output function that routes the IRC, the SysOsc, the watchdog oscillator, or the main clock to the CLKOUT function. The CLKOUT function can be connected to any digital pin through the switch matrix.

8.20.5 Wake-up process

The LPC81xM begin operation at power-up by using the IRC as the clock source. This allows chip operation to resume quickly. If the SysOsc, the external clock source, or the PLL is needed by the application, software must enable these features and wait for them to stabilize before they are used as a clock source.

8.20.6 Power control

The LPC81xM supports the ARM Cortex-M0 Sleep mode. The CPU clock rate may also be controlled as needed by changing clock sources, reconfiguring PLL values, and/or altering the CPU clock divider value. This allows a trade-off of power versus processing speed based on application requirements. In addition, a register is provided for shutting down the clocks to individual on-chip peripherals, allowing to fine-tune power consumption by eliminating all dynamic power use in any peripherals that are not required for the application. Selected peripherals have their own clock divider which provides even better power control.

8.20.6.1 Power profiles

The power consumption in Active and Sleep modes can be optimized for the application through simple calls to the power profile API. The API is accessible through the on-chip ROM.

The power configuration routine configures the LPC81xM for one of the following power modes:

- Default mode corresponding to power configuration after reset.
- CPU performance mode corresponding to optimized processing capability.
- Efficiency mode corresponding to optimized balance of current consumption and CPU performance.
- Low-current mode corresponding to lowest power consumption.

In addition, the power profile includes routines to select the optimal PLL settings for a given system clock and PLL input clock.

8.20.6.2 Sleep mode

When Sleep mode is entered, the clock to the core is stopped. Resumption from the Sleep mode does not need any special sequence but re-enabling the clock to the ARM core.

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In Sleep mode, execution of instructions is suspended until either a reset or interrupt occurs. Peripheral functions continue operation during Sleep mode and may generate interrupts to cause the processor to resume execution. Sleep mode eliminates dynamic power used by the processor itself, memory systems and related controllers, and internal buses.

8.20.6.3 Deep-sleep mode

In Deep-sleep mode, the LPC81xM is in Sleep-mode and all peripheral clocks and all clock sources are off except for the IRC and watchdog oscillator or low-power oscillator if selected. The IRC output is disabled. In addition all analog blocks are shut down and the flash is in stand-by mode. In Deep-sleep mode, the application can keep the watchdog oscillator and the BOD circuit running for self-timed wake-up and BOD protection.

The LPC81xM can wake up from Deep-sleep mode via a reset, digital pins selected as inputs to the pin interrupt block, a watchdog timer interrupt, or an interrupt from the USART (if the USART is configured in synchronous slave mode), the SPI, or the I2C blocks (in slave mode).

Any interrupt used for waking up from Deep-sleep mode must be enabled in one of the SYSCON wake-up enable registers and the NVIC.

Deep-sleep mode saves power and allows for short wake-up times.

8.20.6.4 Power-down mode

In Power-down mode, the LPC81xM is in Sleep-mode and all peripheral clocks and all clock sources are off except for watchdog oscillator or low-power oscillator if selected. In addition all analog blocks and the flash are shut down. In Power-down mode, the application can keep the watchdog oscillator and the BOD circuit running for self-timed wake-up and BOD protection.

The LPC81xM can wake up from Power-down mode via a reset, digital pins selected as inputs to the pin interrupt block, a watchdog timer interrupt, or an interrupt from the USART (if the USART is configured in synchronous slave mode), the SPI, or the I2C blocks (in slave mode).

Any interrupt used for waking up from Power-down mode must be enabled in one of the SYSCON wake-up enable registers and the NVIC.

Power-down mode reduces power consumption compared to Deep-sleep mode at the expense of longer wake-up times.

8.20.6.5 Deep power-down mode

In Deep power-down mode, power is shut off to the entire chip except for the WAKEUP pin and the self wake-up timer if enabled. Four general-purpose registers are available to store information during Deep power-down mode. The LPC81xM can wake up from Deep power-down mode via the WAKEUP pin, or without an external signal by using the time-out of the self wake-up timer (see Section 8.18).

The LPC81xM can be prevented from entering Deep power-down mode by setting a lock bit in the PMU block. Locking out Deep power-down mode enables the application to keep the watchdog timer or the BOD running at all times.

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When entering Deep power-down mode, an external pull-up resistor is required on the WAKEUP pin to hold it HIGH. Pull the $\overline{\text{RESET}}$ pin HIGH to prevent it from floating while in Deep power-down mode.

8.21 System control

8.21.1 Reset

Reset has four sources on the LPC81xM: the $\overline{\text{RESET}}$ pin, the Watchdog reset, power-on reset (POR), and the BrownOut Detection (BOD) circuit. The $\overline{\text{RESET}}$ pin is a Schmitt trigger input pin. Assertion of chip reset by any source, once the operating voltage attains a usable level, starts the IRC and initializes the flash controller.

A LOW-going pulse as short as 50 ns resets the part.

When the internal Reset is removed, the processor begins executing at address 0, which is initially the Reset vector mapped from the boot block. At that point, all of the processor and peripheral registers have been initialized to predetermined values.

In Deep power-down mode, an external pull-up resistor is required on the $\overline{\text{RESET}}$ pin.

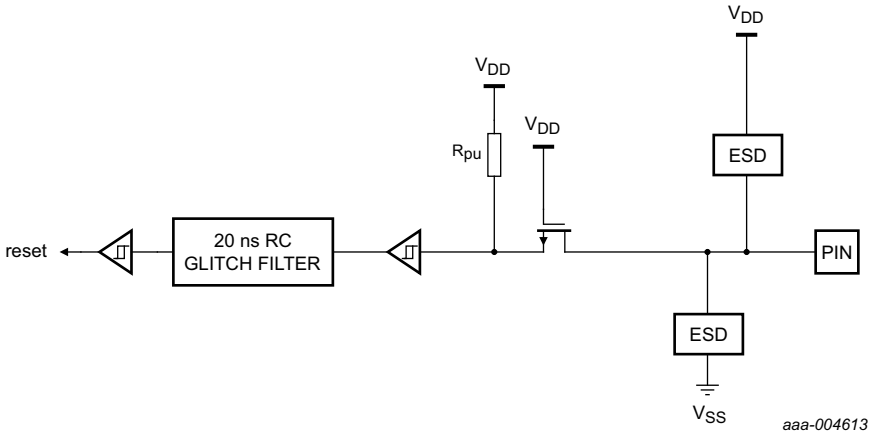

Fig 11. Reset pad configuration

8.21.2 Brownout detection

The LPC81xM includes up to four levels for monitoring the voltage on the V_{DD} pin. If this voltage falls below one of the selected levels, the BOD asserts an interrupt signal to the NVIC. This signal can be enabled for interrupt in the Interrupt Enable Register in the NVIC to cause a CPU interrupt. Alternatively, software can monitor the signal by reading a dedicated status register. Four threshold levels can be selected to cause a forced reset of the chip.

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8.21.3 Code security (Code Read Protection - CRP)

CRP provides different levels of security in the system so that access to the on-chip flash and use of the Serial Wire Debugger (SWD) and In-System Programming (ISP) can be restricted. Programming a specific pattern into a dedicated flash location invokes CRP. IAP commands are not affected by the CRP.

In addition, ISP entry via the ISP entry pin can be disabled without enabling CRP. For details, see the *LPC800 user manual*.

There are three levels of Code Read Protection:

1. CRP1 disables access to the chip via the SWD and allows partial flash update (excluding flash sector 0) using a limited set of the ISP commands. This mode is useful when CRP is required and flash field updates are needed but all sectors cannot be erased.
2. CRP2 disables access to the chip via the SWD and only allows full flash erase and update using a reduced set of the ISP commands.
3. Running an application with level CRP3 selected, fully disables any access to the chip via the SWD pins and the ISP. This mode effectively disables ISP override using the ISP entry pin as well. If necessary, the application must provide a flash update mechanism using IAP calls or using a call to the reinvoke ISP command to enable flash update via the USART.

CAUTION

If level three Code Read Protection (CRP3) is selected, no future factory testing can be performed on the device.

In addition to the three CRP levels, sampling of the ISP entry pin for valid user code can be disabled. For details, see the *LPC800 user manual*.

8.21.4 APB interface

The APB peripherals are located on one APB bus.

8.21.5 AHBLite

The AHBLite connects the CPU bus of the ARM Cortex-M0+ to the flash memory, the main static RAM, the CRC, and the ROM.

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8.22 Emulation and debugging

Debug functions are integrated into the ARM Cortex-M0+. Serial wire debug functions are supported in addition to a standard JTAG boundary scan. The ARM Cortex-M0+ is configured to support up to four breakpoints and two watch points.

The Micro Trace Buffer is implemented on the LPC81xM.

The $\overline{\text{RESET}}$ pin selects between the JTAG boundary scan ($\overline{\text{RESET}}$ = LOW) and the ARM SWD debug ($\overline{\text{RESET}}$ = HIGH). The ARM SWD debug port is disabled while the LPC81xM is in reset. The JTAG boundary scan pins are selected by hardware when the part is in boundary scan mode on pins PIO0_0 to PIO0_3 (see Table 4).

To perform boundary scan testing, follow these steps:

1. Erase any user code residing in flash.
2. Power up the part with the $\overline{\text{RESET}}$ pin pulled HIGH externally.
3. Wait for at least 250 μs.
4. Pull the $\overline{\text{RESET}}$ pin LOW externally.
5. Perform boundary scan operations.
6. Once the boundary scan operations are completed, assert the $\overline{\text{TRST}}$ pin to enable the SWD debug mode, and release the $\overline{\text{RESET}}$ pin (pull HIGH).

Remark: The JTAG interface cannot be used for debug purposes.

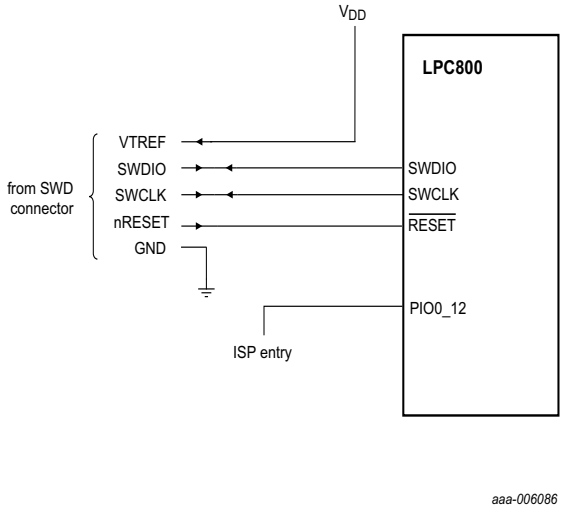

Fig 12. Connecting the SWD pins to a standard SWD connector

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9. Limiting values

Table 7. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage (core and external rail)		[2]	−0.5	+4.6	V
V_I	input voltage	5 V tolerant I/O pins; $V_{DD} \geq 1.8$ V	[3]	−0.5	+5.5	V
		5 V tolerant open-drain pins PIO0_10 and PIO0_11	[4]	−0.5	+5.5	V
V_{IA}	analog input voltage		[5] [6]	−0.5	4.6	V
$V_{i(xtal)}$	crystal input voltage		[2]	−0.5	+2.5	V
I_{DD}	supply current	per supply pin		-	100	mA
I_{SS}	ground current	per ground pin		-	100	mA
I_{latch}	I/O latch-up current	$-(0.5V_{DD}) < V_I < (1.5V_{DD})$; $T_j < 125$ °C		-	100	mA
T_{stg}	storage temperature	non-operating	[7]	−65	+150	°C
$T_{j(max)}$	maximum junction temperature			-	150	°C
$P_{tot(pack)}$	total power dissipation (per package)	based on package heat transfer, not device power consumption		-	1.5	W
V_{ESD}	electrostatic discharge voltage	human body model; all pins	[8]	-	5500	V
		charged device model; TSSOP20 and SOP20 packages		-	1200	V
		charged device model; TSSOP16 package		-	1000	V
		charged device model; XSON16 package		-	800	V

[1] The following applies to the limiting values:

a) This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.

b) Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

c) The limiting values are stress ratings only. Operating the part at these values is not recommended and proper operation is not guaranteed. The conditions for functional operation are specified in Table 9.

[2] Maximum/minimum voltage above the maximum operating voltage (see Table 9) and below ground that can be applied for a short time (< 10 ms) to a device without leading to irrecoverable failure. Failure includes the loss of reliability and shorter lifetime of the device.

[3] Including voltage on outputs in tri-state mode. Does not apply to pin PIO0_6.

[4] V_{DD} present or not present. Compliant with the I^2C-bus standard. 5.5 V can be applied to this pin when V_{DD} is powered down.

[5] If the comparator is configured with the common mode input $V_{IC} = V_{DD}$, the other comparator input can be up to 0.2 V above or below V_{DD} without affecting the hysteresis range of the comparator function.

[6] It is recommended to connect an overvoltage protection diode between the analog input pin and the voltage supply pin.

[7] The maximum non-operating storage temperature is different than the temperature for required shelf life which should be determined based on required shelf lifetime. Please refer to the JEDEC spec (J-STD-033B.1) for further details.

[8] Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

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10. Thermal characteristics

The average chip junction temperature, T_j (°C), can be calculated using the following equation:

$$T_j = T_{amb} + (P_D \times R_{th(j-a)}) \quad (1)$$

- T_{amb} = ambient temperature (°C),
- $R_{th(j-a)}$ = the package junction-to-ambient thermal resistance (°C/W)
- P_D = sum of internal and I/O power dissipation

The internal power dissipation is the product of I_{DD} and V_{DD}. The I/O power dissipation of the I/O pins is often small and many times can be negligible. However it can be significant in some applications.

Table 8. Thermal resistance

Symbol	Parameter	Conditions	Max/Min	Unit
DIP8				
$R_{th(j-a)}$	thermal resistance from junction to ambient	JEDEC (4.5 in × 4 in); still air	60 ± 15 %	°C/W
		Single-layer (4.5 in × 3 in); still air	81 ± 15 %	°C/W
$R_{th(j-c)}$	thermal resistance from junction to case		38 ± 15 %	°C/W
TSSOP16				
$R_{th(j-a)}$	thermal resistance from junction to ambient	JEDEC (4.5 in × 4 in); still air	133 ± 15 %	°C/W
		Single-layer (4.5 in × 3 in); still air	182 ± 15 %	°C/W
$R_{th(j-c)}$	thermal resistance from junction to case		33 ± 15 %	°C/W
TSSOP20				
$R_{th(j-a)}$	thermal resistance from junction to ambient	JEDEC (4.5 in × 4 in); still air	110 ± 15 %	°C/W
		Single-layer (4.5 in × 3 in); still air	153 ± 15 %	°C/W
$R_{th(j-c)}$	thermal resistance from junction to case		23 ± 15 %	°C/W
SO20				
$R_{th(j-a)}$	thermal resistance from junction to ambient	JEDEC (4.5 in × 4 in); still air	87 ± 15 %	°C/W
		Single-layer (4.5 in × 3 in); still air	112 ± 15 %	°C/W
$R_{th(j-c)}$	thermal resistance from junction to case		50 ± 15 %	°C/W
XSON16				
$R_{th(j-a)}$	thermal resistance from junction to ambient	JEDEC (4.5 in × 4 in); still air	92 ± 15 %	°C/W
		Single-layer (4.5 in × 3 in); still air	180 ± 15 %	°C/W
$R_{th(j-c)}$	thermal resistance from junction to case		27 ± 15 %	°C/W

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11. Static characteristics

Table 9. Static characteristics

T_{amb} = −40 °C to +105 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
V_{DD}	supply voltage (core and external rail)			1.8	3.3	3.6	V
I_{DD}	supply current	Active mode; code `while(1){}` executed from flash;					
		system clock = 12 MHz; default mode; V_{DD} = 3.3 V	[2][3][4][5]	-	1.4	-	mA
		system clock = 12 MHz; low-current mode; V_{DD} = 3.3 V	[2][3][4][5][6]	-	1.0	-	mA
		system clock = 24 MHz; low-current mode; V_{DD} = 3.3 V	[2][4][5][6][7]	-	2.2	-	mA
		system clock = 30 MHz; default mode; V_{DD} = 3.3 V	[2][4][5][8]	-	3.3	-	mA
		system clock = 30 MHz; low-current mode; V_{DD} = 3.3 V	[2][4][5][6][8]	-	3	-	mA
		Sleep mode					
		system clock = 12 MHz; default mode; V_{DD} = 3.3 V	[2][3][4][5]	-	0.8	-	mA
		system clock = 12 MHz; low-current mode; V_{DD} = 3.3 V	[2][3][4][5][6]	-	0.7	-	mA
		system clock = 24 MHz; low-current mode; V_{DD} = 3.3 V	[2][4][5][6][7]	-	1.3	-	mA
		system clock = 30 MHz; default mode; V_{DD} = 3.3 V	[2][4][5][8]	-	1.8	-	mA
		system clock = 30 MHz; low-current mode; V_{DD} = 3.3 V	[2][4][5][6][8]	-	1.7	-	mA
		Deep-sleep mode					
		V_{DD} = 3.3 V, T_{amb} = 25 °C	[2][9]	-	150	300	µA
		V_{DD} = 3.3 V, T_{amb} = 105 °C	[2][9]	-	-	400	µA
		Power-down mode					
		V_{DD} = 3.3 V, T_{amb} = 25 °C	[2][9]	-	0.9	5	µA
		V_{DD} = 3.3 V, T_{amb} = 105 °C	[2][9]	-	-	40	µA
		Deep power-down mode; Low-power oscillator and self wakeup timer (WKT) disabled					
		V_{DD} = 3.3 V, T_{amb} = 25 °C	[10]	-	170	1000	nA
		V_{DD} = 3.3 V, T_{amb} = 105 °C	[10]	-	-	4	µA
		Deep power-down mode; Low-power oscillator and self wakeup timer (WKT) enabled		-	1	-	µA

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Table 9. Static characteristics *...continued*

T_{amb} = −40 °C to +105 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
Standard port pins configured as digital pins, RESET; see Figure 13							
I_{IL}	LOW-level input current	V_I = 0 V; on-chip pull-up resistor disabled		-	0.5	10	nA
I_{IH}	HIGH-level input current	$V_I = V_{DD}$; on-chip pull-down resistor disabled		-	0.5	10	nA
I_{OZ}	OFF-state output current	V_O = 0 V; $V_O = V_{DD}$; on-chip pull-up/down resistors disabled		-	0.5	10	nA
V_I	input voltage	$V_{DD} \geq 1.8$ V; 5 V tolerant pins	[11] [12]	0	-	5.0	V
		V_{DD} = 0 V		0	-	3.6	V
V_O	output voltage	output active		0	-	V_{DD}	V
V_{IH}	HIGH-level input voltage			$0.7V_{DD}$	-	-	V
V_{IL}	LOW-level input voltage			-	-	$0.3V_{DD}$	V
V_{hys}	hysteresis voltage			-	0.4	-	V
V_{OH}	HIGH-level output voltage	$2.5 \text{ V} \leq V_{DD} \leq 3.6$ V; I_{OH} = 4 mA		$V_{DD} - 0.4$	-	-	V
		$1.8 \text{ V} \leq V_{DD} < 2.5$ V; I_{OH} = 3 mA		$V_{DD} - 0.4$	-	-	V
V_{OL}	LOW-level output voltage	$2.5 \text{ V} \leq V_{DD} \leq 3.6$ V; I_{OL} = 4 mA		-	-	0.4	V
		$1.8 \text{ V} \leq V_{DD} < 2.5$ V; I_{OL} = 3 mA		-	-	0.4	V
I_{OH}	HIGH-level output current	$V_{OH} = V_{DD} - 0.4$ V; $2.5 \text{ V} \leq V_{DD} \leq 3.6$ V		4	-	-	mA
		$1.8 \text{ V} \leq V_{DD} < 2.5$ V		3	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V $2.5 \text{ V} \leq V_{DD} \leq 3.6$ V		4	-	-	mA
		$1.8 \text{ V} \leq V_{DD} < 2.5$ V		3	-	-	mA
I_{OHS}	HIGH-level short-circuit output current	V_{OH} = 0 V	[13]	-	-	45	mA
I_{OLS}	LOW-level short-circuit output current	$V_{OL} = V_{DD}$	[13]	-	-	50	mA
I_{pd}	pull-down current	V_I = 5 V		10	50	150	µA
I_{pu}	pull-up current	V_I = 0 V; $2.0 \text{ V} \leq V_{DD} \leq 3.6$ V		15	50	85	µA
		$1.8 \text{ V} \leq V_{DD} < 2.0$ V		10	50	85	µA
		$V_{DD} < V_I < 5$ V		0	0	0	µA
High-drive output pins configured as digital pins (PIO0_2, PIO0_3, PIO0_7, PIO0_12, PIO0_13); see Figure 13							
I_{IL}	LOW-level input current	V_I = 0 V; on-chip pull-up resistor disabled		-	0.5	10	nA
I_{IH}	HIGH-level input current	$V_I = V_{DD}$; on-chip pull-down resistor disabled		-	0.5	10	nA
I_{OZ}	OFF-state output current	V_O = 0 V; $V_O = V_{DD}$; on-chip pull-up/down resistors disabled		-	0.5	10	nA

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Table 9. Static characteristics *...continued*

T_{amb} = −40 °C to +105 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
V_I	input voltage	$V_{DD} \geq 1.8$ V	[11] [12]	0	-	5.0	V
		V_{DD} = 0 V		0	-	3.6	V
V_O	output voltage	output active		0	-	V_{DD}	V
V_{IH}	HIGH-level input voltage			$0.7V_{DD}$	-	-	V
V_{IL}	LOW-level input voltage			-	-	$0.3V_{DD}$	V
V_{hys}	hysteresis voltage			0.4	-	-	V
V_{OH}	HIGH-level output voltage	2.5 V ≤ V_{DD} ≤ 3.6 V; I_{OH} = 20 mA		V_{DD} − 0.4	-	-	V
		1.8 V ≤ V_{DD} < 2.5 V; I_{OH} = 12 mA		V_{DD} − 0.4	-	-	V
V_{OL}	LOW-level output voltage	2.5 V ≤ V_{DD} ≤ 3.6 V; I_{OL} = 4 mA		-	-	0.4	V
		1.8 V ≤ V_{DD} < 2.5 V; I_{OL} = 3 mA		-	-	0.4	V
I_{OH}	HIGH-level output current	V_{OH} = V_{DD} − 0.4 V; 2.5 V ≤ V_{DD} ≤ 3.6 V		20	-	-	mA
		1.8 V ≤ V_{DD} < 2.5 V		12	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V 2.5 V ≤ V_{DD} ≤ 3.6 V		4	-	-	mA
		1.8 V ≤ V_{DD} < 2.5 V		3	-	-	mA
I_{OLS}	LOW-level short-circuit output current	V_{OL} = V_{DD}	[13]	-	-	50	mA
I_{pd}	pull-down current	V_I = 5 V	[14]	10	50	150	µA
I_{pu}	pull-up current	V_I = 0 V 2.0 V ≤ V_{DD} ≤ 3.6 V	[14]	15	50	85	µA
		1.8 V ≤ V_{DD} < 2.0 V		10	50	85	µA
		V_{DD} < V_I < 5 V		0	0	0	µA
I^2C-bus pins (PIO0_10 and PIO0_11); see Figure 13							
V_{IH}	HIGH-level input voltage			$0.7V_{DD}$	-	-	V
V_{IL}	LOW-level input voltage			-	-	$0.3V_{DD}$	V
V_{hys}	hysteresis voltage			-	$0.05V_{DD}$	-	V
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; I^2C-bus pins configured as standard mode pins 2.5 V ≤ V_{DD} ≤ 3.6 V		3.5	-	-	mA
		1.8 V ≤ V_{DD} < 2.5 V		3	-	-	
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; I^2C-bus pins configured as Fast-mode Plus pins 2.5 V ≤ V_{DD} ≤ 3.6 V		20	-	-	mA
		1.8 V ≤ V_{DD} < 2.5 V		16	-	-	
I_{LI}	input leakage current	V_I = V_{DD}	[15]	-	2	4	µA
		V_I = 5 V		-	10	22	µA

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Table 9. Static characteristics *…continued*

T_{amb} = −40 °C to +105 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
Oscillator input pins (PIO0_8 and PIO0_9)							
$V_{i(xtal)}$	crystal input voltage			−0.5	1.8	1.95	V
$V_{o(xtal)}$	crystal output voltage			−0.5	1.8	1.95	V

[1] Typical ratings are not guaranteed. The values listed are for room temperature (25 °C), nominal supply voltages.

[2] I_{DD} measurements were performed with all pins configured as GPIO outputs driven LOW and pull-up resistors disabled.

[3] IRC enabled; system oscillator disabled; system PLL disabled.

[4] BOD disabled.

[5] All peripherals disabled in the SYSAHBCLKCTRL register. Peripheral clocks to USART, CLKOUT, and IOCON disabled in system configuration block.

[6] Low-current mode PWR_LOW_CURRENT selected when running the set_power routine in the power profiles.

[7] IRC enabled; system oscillator disabled; system PLL enabled.

[8] IRC disabled; system oscillator enabled; system PLL enabled.

[9] All oscillators and analog blocks turned off in the PDSLEEPCFG register; PDSLEEPCFG = 0x0000 18FF.

[10] WAKEUP pin pulled HIGH externally.

[11] Including voltage on outputs in tri-state mode.

[12] 3-state outputs go into tri-state mode in Deep power-down mode.

[13] Allowed as long as the current limit does not exceed the maximum current allowed by the device.

[14] Pull-up and pull-down currents are measured across the weak internal pull-up/pull-down resistors. See Figure 8.

[15] To V_{SS}.

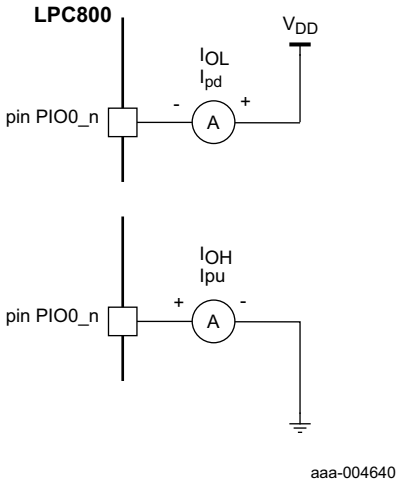

Fig 13. Pin input/output current measurement

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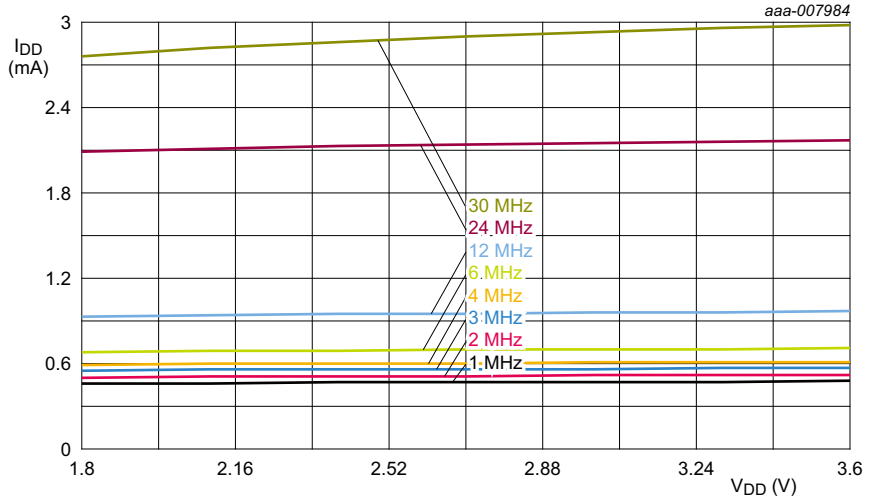
11.1 Power consumption

Power measurements in Active, Sleep, Deep-sleep,and Power-down modes were performed under the following conditions:

- Configure all pins as GPIO with pull-up resistor disabled in the IOCON block.
- Configure GPIO pins as outputs using the GPIO DIR register.
- Write 1 to the GPIO CLR register to drive the outputs LOW.



Conditions: T_{amb} = 25 °C; active mode entered executing code `while(1){}` from flash; all peripherals disabled in the SYSAHBCLKCTRL register (SYSAHBCLKCTRL =0x1F); all peripheral clocks disabled; internal pull-up resistors disabled; BOD disabled; low-current mode.

1 MHz - 6 MHz: IRC enabled; PLL disabled.

12 MHz: IRC enabled; PLL disabled.

24 MHz: IRC enabled; PLL enabled.

30 MHz: IRC disabled; SYSOSC enabled; PLL enabled.

Fig 14. Active mode: Typical supply current I_{DD} versus supply voltage V_{DD}

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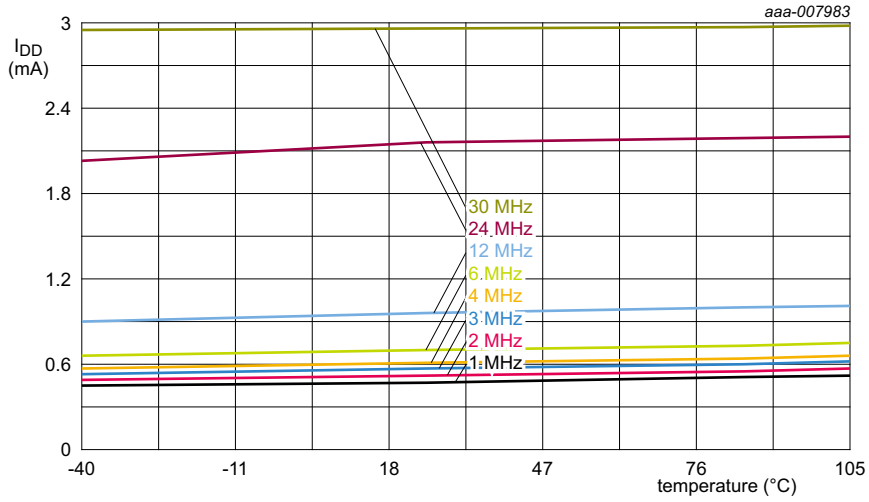

Conditions: V_{DD} = 3.3 V; active mode entered executing code `while(1){}` from flash; all peripherals disabled in the SYSAHBCLKCTRL register (SYSAHBCLKCTRL = 0x1F); all peripheral clocks disabled; internal pull-up resistors disabled; BOD disabled; low-current mode.

1 MHz - 6 MHz: IRC enabled; PLL disabled.

12 MHz: IRC enabled; PLL disabled.

24 MHz: IRC enabled; PLL enabled.

30 MHz: IRC disabled; SYSOSC enabled; PLL enabled.

Fig 15. Active mode: Typical supply current I_{DD} versus temperature

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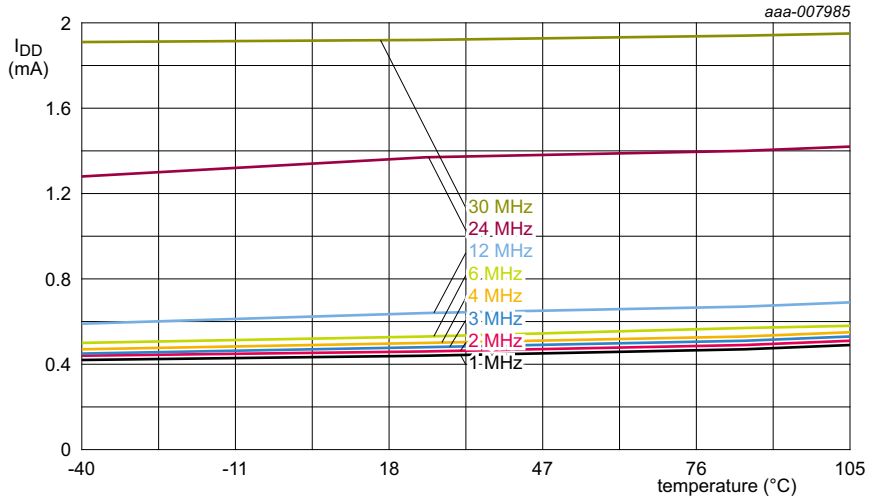


Conditions: V_{DD} = 3.3 V; sleep mode entered from flash; all peripherals disabled in the SYSAHBCLKCTRL register (SYSAHBCLKCTRL = 0x1F); all peripheral clocks disabled; internal pull-up resistors disabled; BOD disabled; low-current mode.

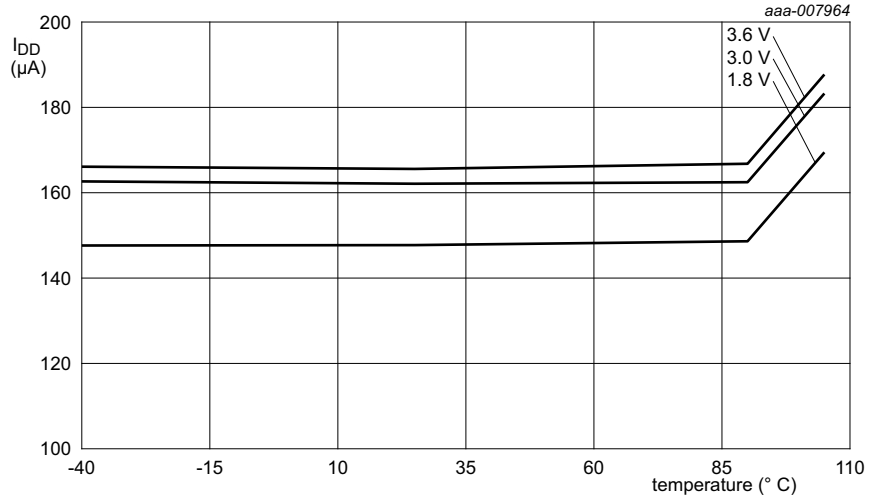
1 MHz - 6 MHz: IRC enabled; PLL disabled.

12 MHz: IRC enabled; PLL disabled.

24 MHz: IRC enabled; PLL enabled.

30 MHz: IRC disabled; SYSOSC enabled; PLL enabled.

Fig 16. Sleep mode: Typical supply current I_{DD} versus temperature for different system clock frequencies



Conditions: BOD disabled; all oscillators and analog blocks disabled in the PDSLEEPCFG register (PDSLEEPCFG = 0x0000 18FF).

Fig 17. Deep-sleep mode: Typical supply current I_{DD} versus temperature for different supply voltages V_{DD}

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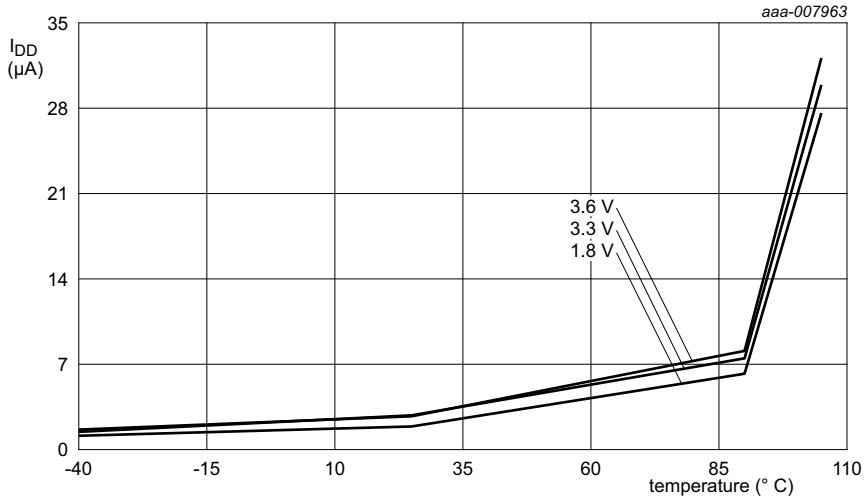
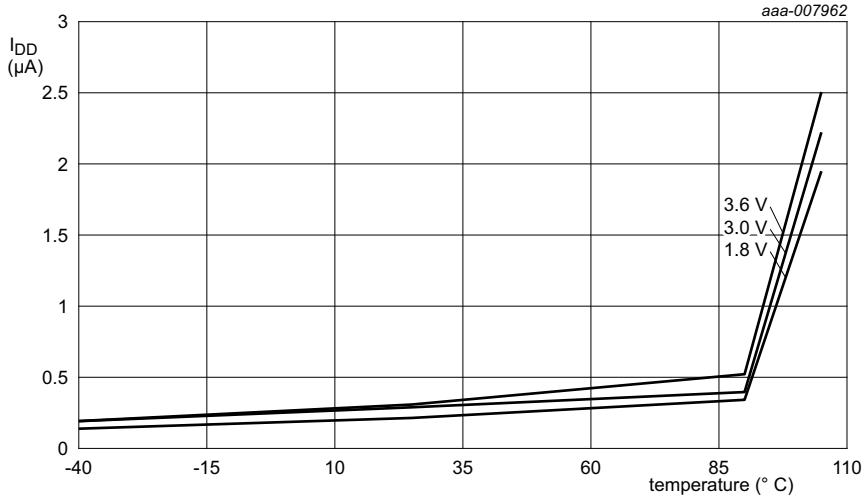


Conditions: BOD disabled; all oscillators and analog blocks disabled in the PDSLEEPCFG register (PDSLEEPCFG = 0x0000 18FF).

Fig 18. Power-down mode: Typical supply current I_{DD} versus temperature for different supply voltages V_{DD}



WKT not running.

Fig 19. Deep power-down mode: Typical supply current I_{DD} versus temperature for different supply voltages V_{DD}

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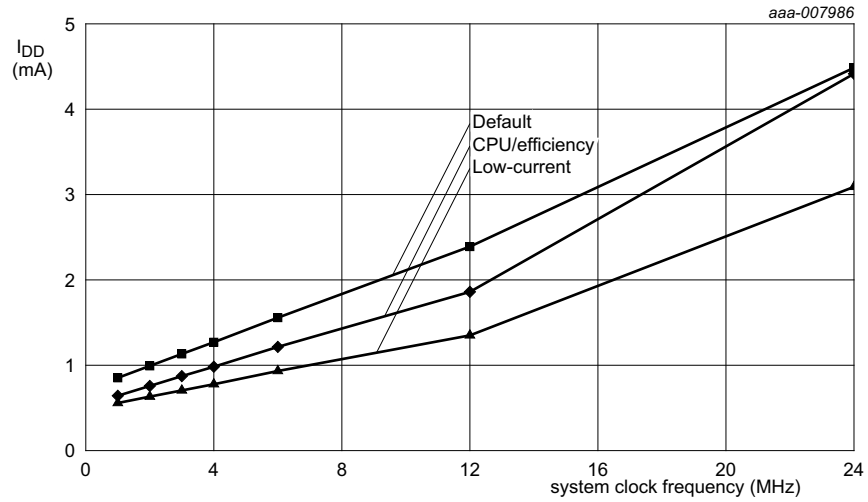
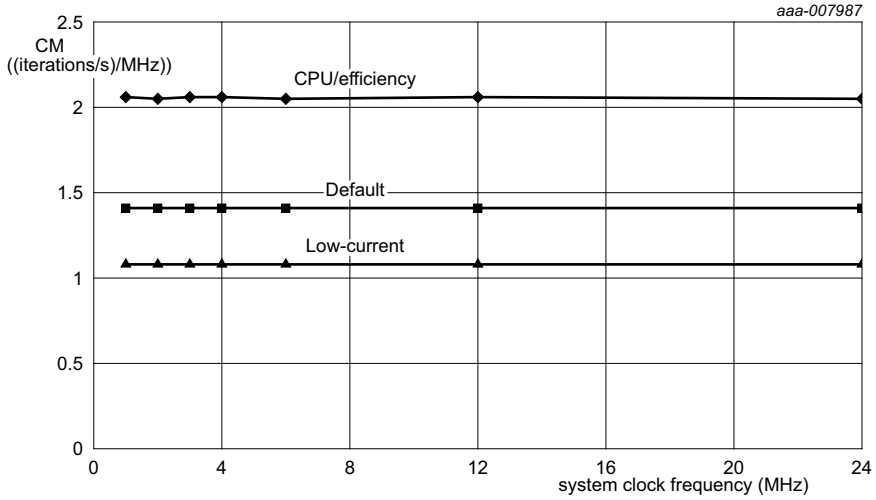
11.2 CoreMark data



Conditions: V_{DD} = 3.3 V; T_{amb} = 25 °C; active mode; all peripherals except one UART and the SCT disabled in the SYSAHBCLKCTRL register; system clock derived from the IRC; system oscillator disabled; internal pull-up resistors enabled; BOD disabled. Measured with Keil uVision v.4.7.

Fig 20. Active mode: CoreMark power consumption I_{DD}



Conditions: V_{DD} = 3.3 V; active mode; all peripherals except one UART and the SCT disabled in the SYSAHBCLKCTRL register; internal pull-up resistors enabled; BOD disabled. Measured with Keil uVision v.4.7.

Fig 21. CoreMark score

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11.3 Peripheral power consumption

The supply current per peripheral is measured as the difference in supply current between the peripheral block enabled and the peripheral block disabled in the SYSAHBCLKCFG and PDRUNCFG (for analog blocks) registers. All other blocks are disabled in both registers and no code is executed. Measured on a typical sample at T_{amb} = 25 °C. Unless noted otherwise, the system oscillator and PLL are running in both measurements.

The supply currents are shown for system clock frequencies of 12 MHz and 30 MHz.

Table 10. Power consumption for individual analog and digital blocks

Peripheral	Typical supply current in mA			Notes
	n/a	12 MHz	30 MHz	
IRC	0.21	-	-	System oscillator running; PLL off; independent of main clock frequency.
System oscillator at 12 MHz	0.28	-	-	IRC running; PLL off; independent of main clock frequency.
Watchdog oscillator at 500 kHz/2	0.002	-	-	System oscillator running; PLL off; independent of main clock frequency.
BOD	0.05	-	-	Independent of main clock frequency.
Main PLL	-	0.31	-	-
CLKOUT	-	0.06	0.09	Main clock divided by 4 in the CLKOUTDIV register.
ROM	-	0.08	0.19	-
I2C	-	0.06	0.15	-
GPIO + pin interrupt/pattern match	-	0.09	0.23	GPIO pins configured as outputs and set to LOW. Direction and pin state are maintained if the GPIO is disabled in the SYSAHBCLKCFG register.
SWM	-	0.03	0.07	-
SCT	-	0.17	0.42	-
WKT	-	0.01	0.03	-
MRT	-	0.09	0.21	-
SPI0	-	0.05	0.13	-
SPI1	-	0.06	0.14	-
CRC	-	0.03	0.07	-
USART0	-	0.04	0.10	-
USART1	-	0.04	0.11	-
USART2	-	0.04	0.10	-
WWDT	-	0.04	0.10	Main clock selected as clock source for the WDT.
IOCON	-	0.03	0.08	-
Comparator	-	0.04	0.09	-

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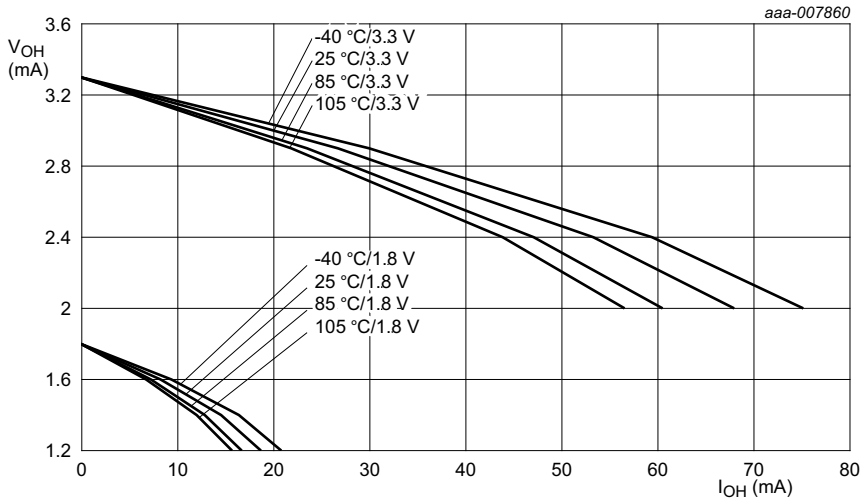
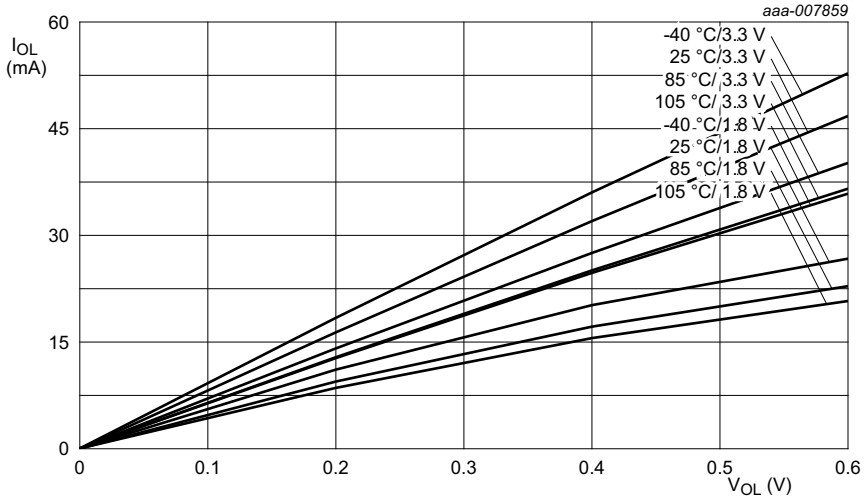
11.4 Electrical pin characteristics



Conditions: V_{DD} = 3.3 V and V_{DD} = 1.8 V; on pins PIO0_2, PIO0_3, PIO0_7, PIO0_12, PIO0_13.

Fig 22. High-drive output: Typical HIGH-level output voltage V_{OH} versus HIGH-level output current I_{OH}



Conditions: V_{DD} = 3.3 V and V_{DD} = 1.8 V; on pins PIO0_10 and PIO0_11.

Fig 23. I^2C-bus pins (high current sink): Typical LOW-level output current I_{OL} versus LOW-level output voltage V_{OL}

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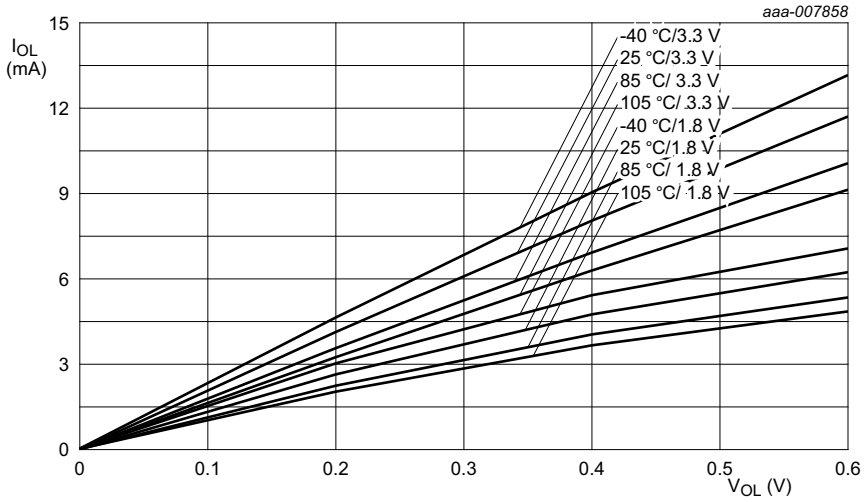
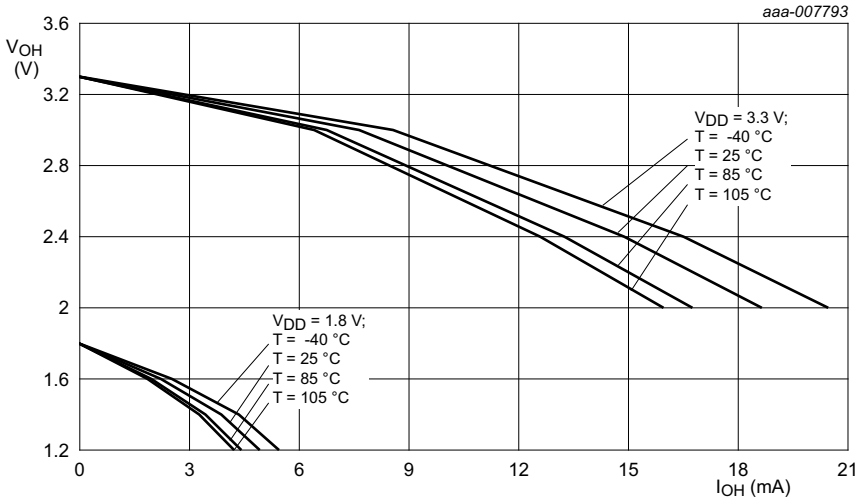


Conditions: V_{DD} = 3.3 V and V_{DD} = 1.8 V; standard port pins and high-drive pins PIO0_2, PIO0_3, PIO0_7, PIO0_12, PIO0_13.

Fig 24. Typical LOW-level output current I_{OL} versus LOW-level output voltage V_{OL}



Conditions: V_{DD} = 3.3 V and V_{DD} = 1.8 V; standard port pins.

Fig 25. Typical HIGH-level output voltage V_{OH} versus HIGH-level output source current I_{OH}

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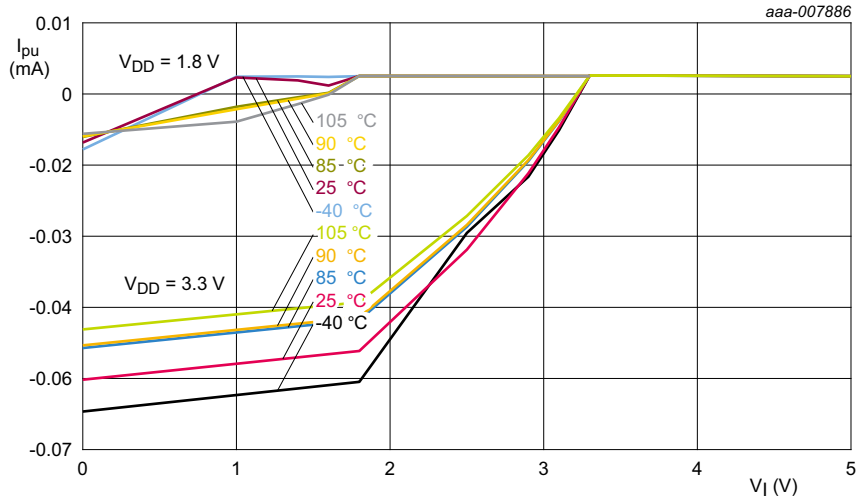
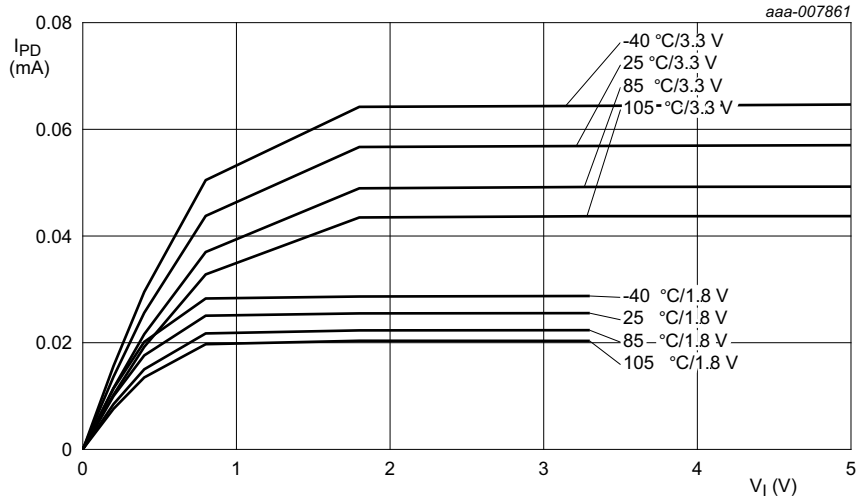


Conditions: V_{DD} = 3.3 V and V_{DD} = 1.8 V; standard port pins.

Fig 26. Typical pull-up current I_{pu} versus input voltage V_I



Conditions: V_{DD} = 3.3 V and V_{DD} = 1.8 V; standard port pins.

Fig 27. Typical pull-down current I_{pd} versus input voltage V_I

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12. Dynamic characteristics

12.1 Power-up ramp conditions

Table 11. Power-up characteristics

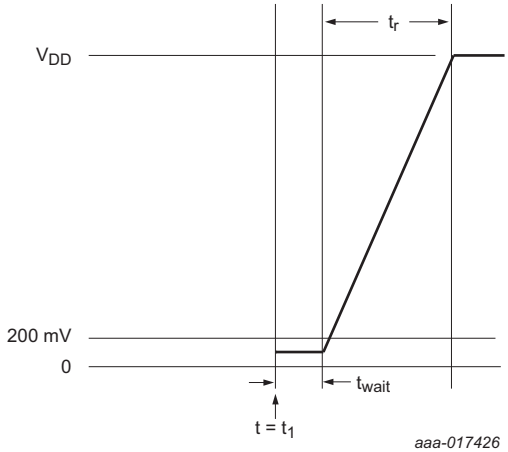
T_{amb} = −40 °C to +105 °C; 1.8 V ≤ V_{DD} ≤ 3.6 V

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_r	rise time	$V_I \leq 200$ mV	[1][3]	0	-	500	ms
t_{wait}	wait time		[1][2][3]	12	-	-	µs
V_I	input voltage	at t = t_1 on pin V_{DD}	[3]	0	-	200	mV

[1] See Figure 28.

[2] The wait time specifies the time the power supply must be at levels below 200 mV before ramping up. See the LPC81x errata sheet.

[3] Based on characterization, not tested in production.



Condition: 0 < $V_I \leq 200$ mV at start of power-up (t = t_1)

Fig 28. Power-up ramp

12.2 Flash memory

Table 12. Flash characteristics

T_{amb} = −40 °C to +105 °C. Based on JEDEC NVM qualification. Failure rate < 10 ppm for parts as specified below.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
N_{endu}	endurance		[1]	10000	100000	-	cycles

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Table 12. Flash characteristics

T_{amb} = −40 °C to +105 °C. Based on JEDEC NVM qualification. Failure rate < 10 ppm for parts as specified below.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{ret}	retention time	powered		10	20	-	years
		unpowered		20	40	-	years
t_{er}	erase time	page or multiple consecutive pages, sector or multiple consecutive sectors		95	100	105	ms
t_{prog}	programming time		[2]	0.95	1	1.05	ms

[1] Number of program/erase cycles.

[2] Programming times are given for writing 64 bytes to the flash. $T_{amb} \leq +85$ °C. Flash programming with IAP calls (see *LPC800 user manual*).

12.3 External clock for the oscillator in slave mode

Remark: The input voltage on the XTAL1/2 pins must be ≤ 1.95 V (see Table 9). For connecting the oscillator to the XTAL pins, also see Section 14.2.

Table 13. Dynamic characteristic: external clock (XTALIN inputs)

T_{amb} = −40 °C to +105 °C; V_{DD} over specified ranges.[1]

Symbol	Parameter	Conditions		Min	Typ[2]	Max	Unit
f_{osc}	oscillator frequency			1	-	25	MHz
$T_{cy(clk)}$	clock cycle time			40	-	1000	ns
t_{CHCX}	clock HIGH time			$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCX}	clock LOW time			$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCH}	clock rise time			-	-	5	ns
t_{CHCL}	clock fall time			-	-	5	ns

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are for room temperature (25 °C), nominal supply voltages.

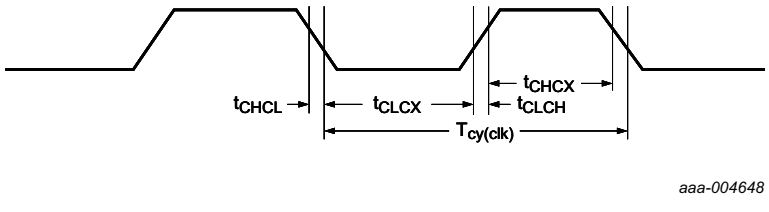

Fig 29. External clock timing (with an amplitude of at least $V_{i(RMS)}$ = 200 mV)

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12.4 Internal oscillators

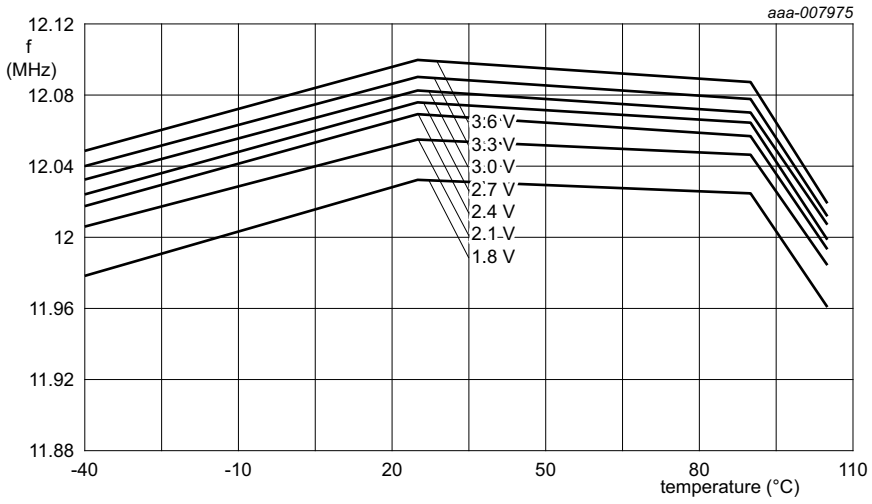
Table 14. Dynamic characteristics: IRC

T_{amb} = −40 °C to +105 °C; 2.7 V ≤ V_{DD} ≤ 3.6 V[1].

Symbol	Parameter	Conditions	Min	Typ[2]	Max	Unit
$f_{osc(RC)}$	internal RC oscillator frequency	T_{amb} = −40 °C to +105 °C	11.82	12	12.18	MHz

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are for room temperature (25 °C), nominal supply voltages.



Conditions: Frequency values are typical values. 12 MHz ± 1.5 % accuracy is guaranteed for 2.7 V ≤ V_{DD} ≤ 3.6 V and T_{amb} = −40 °C to +105 °C. Variations between parts may cause the IRC to fall outside the 12 MHz ± 1.5 % accuracy specification for voltages below 2.7 V.

Fig 30. Typical Internal RC oscillator frequency versus temperature

Table 15. Dynamic characteristics: Watchdog oscillator

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
$f_{osc(int)}$	internal oscillator frequency	DIVSEL = 0x1F, FREQSEL = 0x1 in the WDTOSCCTRL register;	[2][3]	-	9.4	-	kHz
		DIVSEL = 0x00, FREQSEL = 0xF in the WDTOSCCTRL register	[2][3]	-	2300	-	kHz

[1] Typical ratings are not guaranteed. The values listed are at nominal supply voltages.

[2] The typical frequency spread over processing and temperature (T_{amb} = −40 °C to +105 °C) is ±40 %.

[3] See the LPC81xM *user manual.*

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12.5 I/O pins

Table 16. Dynamic characteristics: I/O pins[1]

T_{amb} = −40 °C to +105 °C; 3.0 V ≤ V_{DD} ≤ 3.6 V.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_r	rise time	pin configured as output		3.0	-	5.0	ns
t_f	fall time	pin configured as output		2.5	-	5.0	ns

[1] Applies to standard port pins and $\overline{\text{RESET}}$ pin.

12.6 I²C-bus

Table 17. Dynamic characteristic: I²C-bus pins[1]

T_{amb} = −40 °C to +105 °C.[2]

Symbol	Parameter		Conditions	Min	Max	Unit
f_{SCL}	SCL clock frequency		Standard-mode	0	100	kHz
			Fast-mode	0	400	kHz
			Fast-mode Plus; on pins PIO0_10 and PIO0_11	0	1	MHz
t_f	fall time	[4][5][6][7]	of both SDA and SCL signals Standard-mode	-	300	ns
			Fast-mode	20 + 0.1 × C_b	300	ns
			Fast-mode Plus; on pins PIO0_10 and PIO0_11	-	120	ns
t_{LOW}	LOW period of the SCL clock		Standard-mode	4.7	-	µs
			Fast-mode	1.3	-	µs
			Fast-mode Plus; on pins PIO0_10 and PIO0_11	0.5	-	µs
t_{HIGH}	HIGH period of the SCL clock		Standard-mode	4.0	-	µs
			Fast-mode	0.6	-	µs
			Fast-mode Plus; on pins PIO0_10 and PIO0_11	0.26	-	µs
$t_{HD;DAT}$	data hold time	[3][4][8]	Standard-mode	0	-	µs
			Fast-mode	0	-	µs
			Fast-mode Plus; on pins PIO0_10 and PIO0_11	0	-	µs
$t_{SU;DAT}$	data set-up time	[9][10]	Standard-mode	250	-	ns
			Fast-mode	100	-	ns
			Fast-mode Plus; on pins PIO0_10 and PIO0_11	50	-	ns

[1] See the I²C-bus specification *UM10204* for details.

[2] Parameters are valid over operating temperature range unless otherwise specified.

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[3] $t_{HD;DAT}$ is the data hold time that is measured from the falling edge of SCL; applies to data in transmission and the acknowledge.

[4] A device must internally provide a hold time of at least 300 ns for the SDA signal (with respect to the V_{IH}(min) of the SCL signal) to bridge the undefined region of the falling edge of SCL.

[5] C_b = total capacitance of one bus line in pF.

[6] The maximum t_f for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time for the SDA output stage t_f is specified at 250 ns. This allows series protection resistors to be connected in between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_f.

[7] In Fast-mode Plus, fall time is specified the same for both output stage and bus timing. If series resistors are used, designers should allow for this when considering bus timing.

[8] The maximum $t_{HD;DAT}$ could be 3.45 µs and 0.9 µs for Standard-mode and Fast-mode but must be less than the maximum of $t_{VD;DAT}$ or $t_{VD;ACK}$ by a transition time (see *UM10204*). This maximum must only be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal. If the clock stretches the SCL, the data must be valid by the set-up time before it releases the clock.

[9] $t_{SU;DAT}$ is the data set-up time that is measured with respect to the rising edge of SCL; applies to data in transmission and the acknowledge.

[10] A Fast-mode I^2C-bus device can be used in a Standard-mode I^2C-bus system but the requirement $t_{SU;DAT}$ = 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{r(max)} + t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the Standard-mode I^2C-bus specification) before the SCL line is released. Also the acknowledge timing must meet this set-up time.

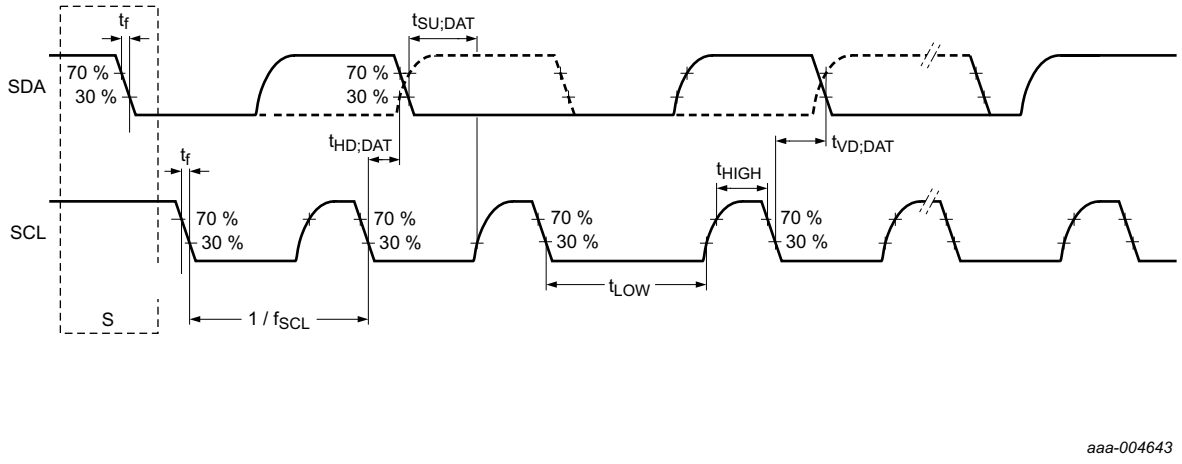

Fig 31. I^2C-bus pins clock timing

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12.7 SPI interfaces

The maximum data bit rate is 30 Mbit/s in master mode and 25 Mbit/s in slave mode.

Remark: SPI functions can be assigned to all digital pins. The characteristics are valid for all digital pins except the open-drain pins PIO0_10 and PIO0_11.

Table 18. SPI dynamic characteristics

T_{amb} = −40 °C to 105 °C; 1.8 V ≤ V_{DD} ≤ 3.6 V. Simulated parameters sampled at the 50 % level of the rising or falling edge; values guaranteed by design.

Symbol	Parameter	Conditions		Min	Max	Unit
SPI master[1]						
$T_{cy(clk)}$	clock cycle time		[2]	33	-	ns
t_{DS}	data set-up time			0	-	ns
t_{DH}	data hold time			16	-	ns
$t_{v(Q)}$	data output valid time	C_L = 10 pF		-	0.5	ns
$t_{h(Q)}$	data output hold time	C_L = 10 pF		0.5	-	ns
SPI slave						
$T_{cy(clk)}$				40		ns
t_{DS}	data set-up time			0	-	ns
t_{DH}	data hold time			16	-	ns
$t_{v(Q)}$	data output valid time	C_L = 10 pF		-	10	ns
$t_{h(Q)}$	data output hold time	C_L = 10 pF		10	-	ns

[1] Capacitance on pin SPIn_SCK C_{SCK} < 5 pF.

[2] $T_{cy(clk)}$ = DIVVAL/CCLK with CCLK = system clock frequency. DIVVAL is the SPI clock divider. See the *LPC800 User manual UM10601*.

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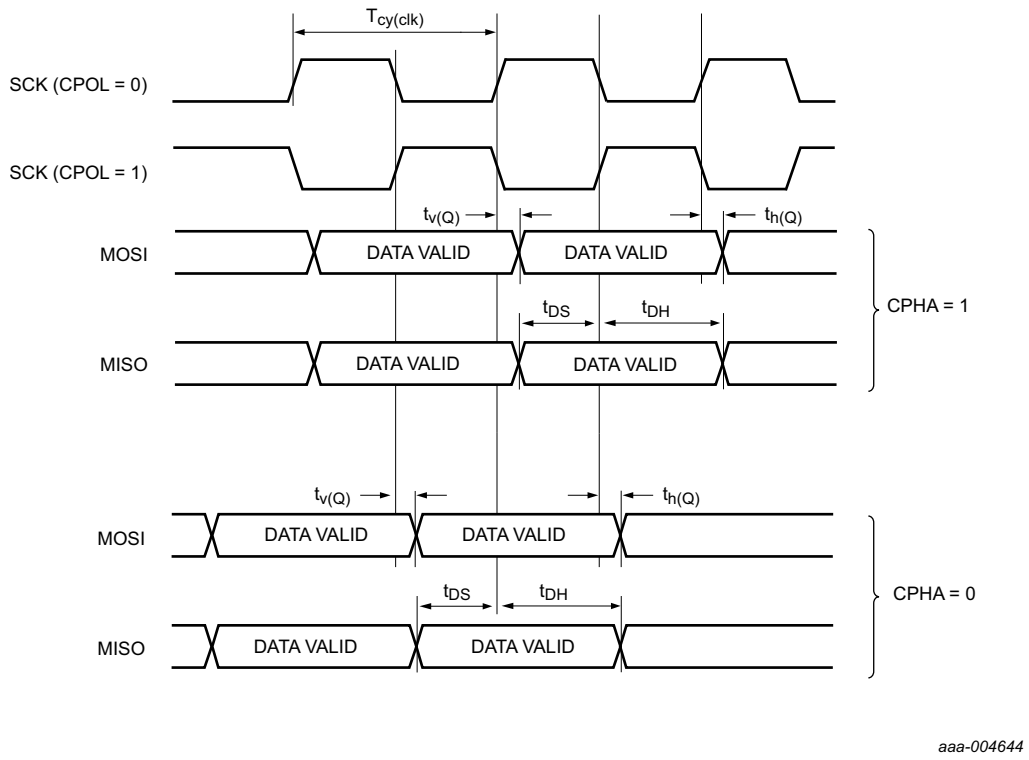

Pin names SCK, MISO, and MOSI refer to pins for both SPI peripherals, SPI0 and SPI1.

Fig 32. SPI master timing

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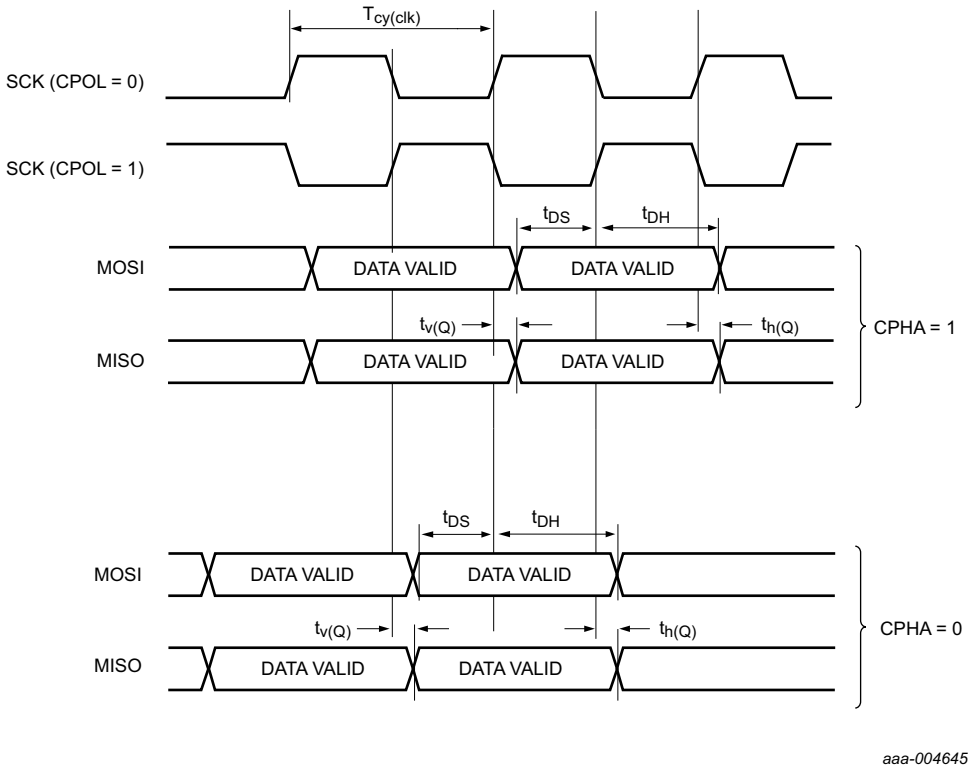

Pin names SCK, MISO, and MOSI refer to pins for both SPI peripherals, SPI0 and SPI1.

Fig 33. SPI slave timing

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12.8 USART interface

The maximum USART bit rate is 1.875 Mbit/s in asynchronous mode and 10 Mbit/s in synchronous mode slave and master mode.

Remark: USART functions can be assigned to all digital pins. The characteristics are valid for all digital pins except the open-drain pins PIO0_10 and PIO0_11.

Table 19. USART dynamic characteristics

T_{amb} = −40 °C to 105 °C; 1.8 V ≤ V_{DD} ≤ 3.6 V. Simulated parameters sampled at the 50 % level of the falling or rising edge; values guaranteed by design.

Symbol	Parameter	Conditions		Min	Max	Unit
$T_{cy(clk)}$	clock cycle time		[2]	100	-	ns
USART master (in synchronous mode)[3]						
$t_{su(D)}$	data input set-up time			44	-	ns
$t_{h(D)}$	data input hold time			0	-	ns
$t_{v(Q)}$	data output valid time			-	-8	ns
$t_{h(Q)}$	data output hold time			-8	-	ns
USART slave (in synchronous mode)						
$t_{su(D)}$	data input set-up time			5	-	ns
$t_{h(D)}$	data input hold time			0	-	ns
$t_{v(Q)}$	data output valid time	C_L = 10 pF		-	40	ns
$t_{h(Q)}$	data output hold time	C_L = 10 pF		40	-	ns

[1] Typical ratings are not guaranteed. The values listed are for room temperature (25 °C), V_{DD} = 3.3 V, typical samples.

[2] $T_{cy(clk)}$ = U_PCLK/BRGVAL. See the *LPC800 User manual UM10601*.

[3] Capacitance on pin Un_SCLK C_{SCLK} < 5 pF.

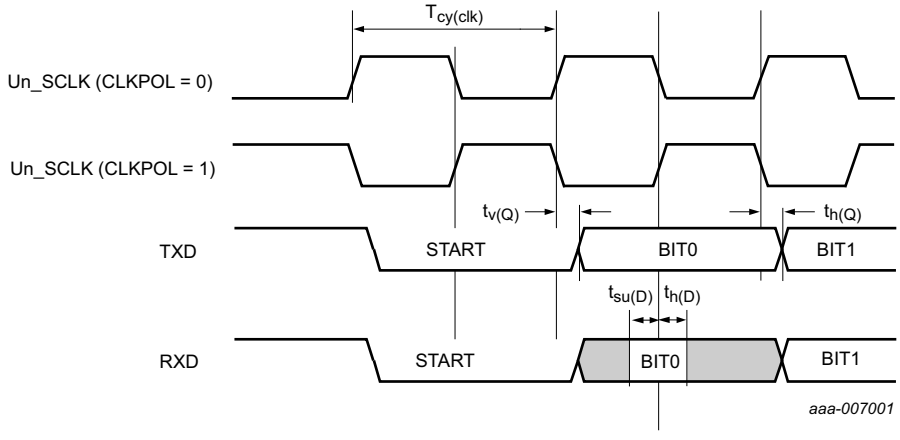

Fig 34. USART timing

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13. Analog characteristics

13.1 BOD

Table 20. BOD static characteristics[1]

T_{amb} = −40 °C to +105 °C.

Symbol	Parameter	Conditions	Typ[2]	Unit
V_{th}	threshold voltage	interrupt level 1		
		assertion	2.3	V
		de-assertion	2.4	V
		interrupt level 2		
		assertion	2.6	V
		de-assertion	2.7	V
		interrupt level 3		
		assertion	2.8	V
		de-assertion	2.9	V
		reset level 1		
		assertion	2.1	V
		de-assertion	2.2	V
		reset level 2		
		assertion	2.4	V
		de-assertion	2.5	V
		reset level 3		
		assertion	2.6	V
		de-assertion	2.8	V

[1] Interrupt levels are selected by writing the level value to the BOD control register BODCTRL.

[2] Typical ratings are not guaranteed. The values listed are for room temperature (25 °C), V_{DD} = 3.3 V, typical samples.

13.2 Internal voltage reference

Table 21. Internal voltage reference static and dynamic characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_O	output voltage	T_{amb} = −40 °C to +105 °C	[1]	0.855	0.900	0.945	V
		T_{amb} = 70 °C to 105 °C	[2]	-	0.906	-	V
		T_{amb} = 50 °C	[2]	-	0.905	-	V
		T_{amb} = 25 °C	[4]	0.893	0.903	0.913	V
		T_{amb} = 0 °C	[2]	-	0.902	-	V
		T_{amb} = −20 °C	[2]	-	0.899	-	V
		T_{amb} = −40 °C	[2]	-	0.896	-	V
$t_{s(pu)}$	power-up settling time	to 99% of V_O	[3]	-	155	195	µs

[1] Characterized through simulation.

[2] Characterized on a typical silicon sample.

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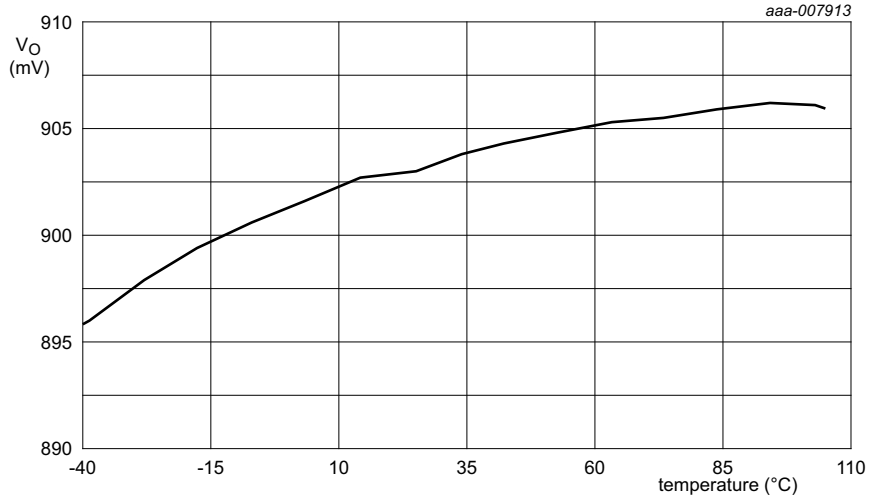
[3] Typical values are derived from nominal simulation (V_{DD} = 3.3 V; T_{amb} = 27 °C; nominal process models). Maximum values are derived from worst case simulation (V_{DD} = 2.6 V; T_{amb} = 105 °C; slow process models).

[4] Maximum and minimum values are measured on samples from the corners of the process matrix lot.



V_{DD} = 3.3 V

Fig 35. Typical internal voltage reference output voltage

13.3 Comparator

Table 22. Comparator characteristics

V_{DD} = 3.0 V and T_{amb} = 27 °C unless noted otherwise.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
$V_{ref(cmp)}$	comparator reference voltage	pin PIO0_6/VDDCMP configured for function VDDCMP		1.5	-	3.6	V
I_{DD}	supply current			-	55	-	µA
V_{IC}	common-mode input voltage			0	-	V_{DD}	V
DV_O	output voltage variation			0	-	V_{DD}	V
V_{offset}	offset voltage	V_{IC} = 0.1 V		-	1.9	-	mV
		V_{IC} = 1.5 V		-	2.1	-	mV
		V_{IC} = 2.8 V		-	2.0		mV
Dynamic characteristics							
$t_{startup}$	start-up time	nominal process		-	4	-	µs

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Table 22. Comparator characteristics *…continued*

V_{DD} = 3.0 V and T_{amb} = 27 °C unless noted otherwise.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{PD}	propagation delay	HIGH to LOW; V_{DD} = 3.0 V; V_{IC} = 0.1 V; 50 mV overdrive input	[1]	-	109	121	ns
		V_{IC} = 0.1 V; rail-to-rail input	[1]	-	155	164	ns
		V_{IC} = 1.5 V; 50 mV overdrive input	[1]	-	95	105	ns
		V_{IC} = 1.5 V; rail-to-rail input	[1]	-	101	108	ns
		V_{IC} = 2.9 V; 50 mV overdrive input	[1]	-	122	129	ns
		V_{IC} = 2.9 V; rail-to-rail input	[1]	-	74	82	ns
t_{PD}	propagation delay	LOW to HIGH; V_{DD} = 3.0 V; V_{IC} = 0.1 V; 50 mV overdrive input	[1]	-	246	260	ns
		V_{IC} = 0.1 V; rail-to-rail input	[1]	-	57	59	ns
		V_{IC} = 1.5 V; 50 mV overdrive input	[1]	-	218		ns
		V_{IC} = 1.5 V; rail-to-rail input	[1]	-	146	155	ns
		V_{IC} = 2.9 V; 50 mV overdrive input	[1]	-	184	206	ns
		V_{IC} = 2.9 V; rail-to-rail input	[1]	-	250	286	ns
V_{hys}	hysteresis voltage	positive hysteresis; V_{DD} = 3.0 V; V_{IC} = 1.5 V	[2]	-	6, 11, 21	-	mV
V_{hys}	hysteresis voltage	negative hysteresis; V_{DD} = 3.0 V; V_{IC} = 1.5 V	[2][2]	-	4, 9, 19	-	mV
R_{lad}	ladder resistance	-		-	1.034	-	MΩ

[1] C_L = 10 pF; results from measurements on silicon samples over process corners and over the full temperature range T_{amb} = −40 °C to +105 °C. Typical data are for T_{amb} = 27 °C.

[2] Input hysteresis is relative to the reference input channel and is software programmable to three levels.

Table 23. Comparator voltage ladder dynamic characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$t_{s(pu)}$	power-up settling time	to 99% of voltage ladder output value	[1]	-	-	30	µs
$t_{s(sw)}$	switching settling time	to 99% of voltage ladder output value	[1] [2]	-	-	15	µs

[1] Maximum values are derived from worst case simulation (V_{DD} = 2.6 V; T_{amb} = 105 °C; slow process models).

[2] Settling time applies to switching between comparator channels.

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Table 24. Comparator voltage ladder reference static characteristics

V_{DD} = 3.3 V; T_{amb} = −40 °C to + 105 °C.

Symbol	Parameter	Conditions		Min	Typ	Max[1]	Unit
$E_{V(O)}$	output voltage error	Internal V_{DD} supply decimal code = 00	[2]	-	0	0	%
		decimal code = 08		-	0	±0.4	%
		decimal code = 16		-	−0.2	±0.2	%
		decimal code = 24		-	−0.2	±0.2	%
		decimal code = 30		-	−0.1	±0.1	%
		decimal code = 31		-	−0.1	±0.1	%
$E_{V(O)}$	output voltage error	External VDDCMP supply decimal code = 00		-	0	0	%
		decimal code = 08		-	−0.1	±0.5	%
		decimal code = 16		-	−0.2	±0.4	%
		decimal code = 24		-	−0.2	±0.3	%
		decimal code = 30		-	−0.2	±0.2	%
		decimal code = 31		-	−0.1	±0.1	%

[1] Measured over a polyresistor matrix lot with a 2 kHz input signal and overdrive < 100 μV.

[2] All peripherals except comparator and IRC turned off.

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14. Application information

14.1 Typical wake-up times

Table 25. Typical wake-up times (3.3 V, Temp = 25 °C)

Power modes	V_{DD} current	Wake-up time
Sleep mode (12 MHz)[1][2]	0.7 mA	2.6 µs
Deep-sleep mode[1][3]	150 µA	4 µs
Power-down mode[1][3]	0.9 µA	50 µs
Deep Power-down mode[4]	170 nA	215 µs

[1] The wake-up time measured is the time between when a GPIO input pin is triggered to wake the device up from the low power modes and from when a GPIO output pin is set in the interrupt service routine (ISR) wake-up handler.

[2] IRC enabled, all peripherals off.

[3] Watchdog oscillator disabled, Brown-Out Detect (BOD) disabled.

[4] Self wakeup-timer disabled. Wake-up from deep power-down causes the LPC800 to go through entire reset process. The wake-up time measured is the time between when a wake-up pin is triggered to wake the device up from the low power modes and from when a GPIO output pin is set in the reset handler.

14.2 XTAL input

The input voltage to the on-chip oscillators is limited to 1.8 V. If the oscillator is driven by a clock in slave mode, it is recommended that the input be coupled through a capacitor with C_i = 100 pF. To limit the input voltage to the specified range, choose an additional capacitor to ground C_g which attenuates the input voltage by a factor $C_i/(C_i + C_g)$. In slave mode, a minimum of 200 mV(RMS) is needed.

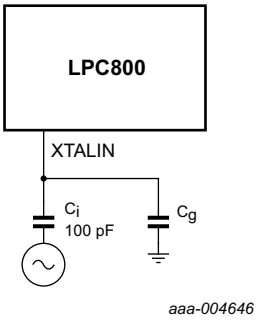

Fig 36. Slave mode operation of the on-chip oscillator

In slave mode the input clock signal should be coupled by means of a capacitor of 100 pF (Figure 36), with an amplitude between 200 mV (RMS) and 1000 mV (RMS). This corresponds to a square wave signal with a signal swing of between 280 mV and 1.4 V. The XTALOUT pin in this configuration can be left unconnected.

External components and models used in oscillation mode are shown in Figure 37 and in Table 26 and Table 27. Since the feedback resistance is integrated on chip, only a crystal and the capacitances C_{X1} and C_{X2} need to be connected externally in case of fundamental mode oscillation (the fundamental frequency is represented by L, C_L and

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R_S). Capacitance C_P in Figure 37 represents the parallel package capacitance and should not be larger than 7 pF. Parameters F_{OSC}, C_L, R_S and C_P are supplied by the crystal manufacturer (see Table 26).

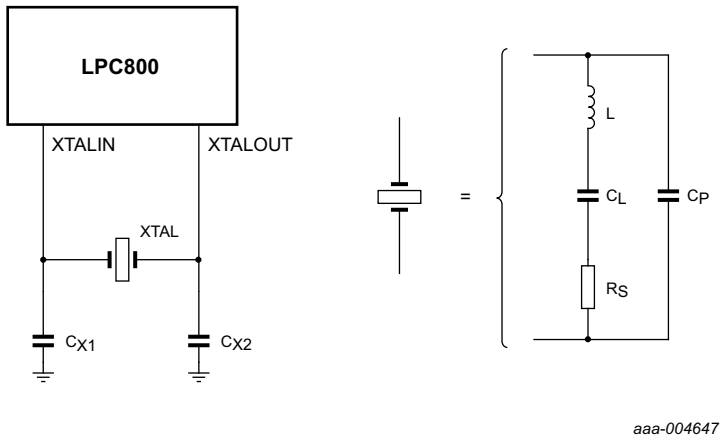

Fig 37. Oscillator modes and models: oscillation mode of operation and external crystal model used for C_{X1}/C_{X2} evaluation

Table 26. Recommended values for C_{X1}/C_{X2} in oscillation mode (crystal and external components parameters) low frequency mode

Fundamental oscillation frequency F_{OSC}	Crystal load capacitance C_L	Maximum crystal series resistance R_S	External load capacitors C_{X1}, C_{X2}
1 MHz to 5 MHz	10 pF	< 300 Ω	18 pF, 18 pF
	20 pF	< 300 Ω	39 pF, 39 pF
	30 pF	< 300 Ω	57 pF, 57 pF
5 MHz to 10 MHz	10 pF	< 300 Ω	18 pF, 18 pF
	20 pF	< 200 Ω	39 pF, 39 pF
	30 pF	< 100 Ω	57 pF, 57 pF
10 MHz to 15 MHz	10 pF	< 160 Ω	18 pF, 18 pF
	20 pF	< 60 Ω	39 pF, 39 pF
15 MHz to 20 MHz	10 pF	< 80 Ω	18 pF, 18 pF

Table 27. Recommended values for C_{X1}/C_{X2} in oscillation mode (crystal and external components parameters) high frequency mode

Fundamental oscillation frequency F_{OSC}	Crystal load capacitance C_L	Maximum crystal series resistance R_S	External load capacitors C_{X1}, C_{X2}
15 MHz to 20 MHz	10 pF	< 180 Ω	18 pF, 18 pF
	20 pF	< 100 Ω	39 pF, 39 pF
20 MHz to 25 MHz	10 pF	< 160 Ω	18 pF, 18 pF
	20 pF	< 80 Ω	39 pF, 39 pF

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14.3 XTAL Printed Circuit Board (PCB) layout guidelines

The crystal should be connected on the PCB as close as possible to the oscillator input and output pins of the chip. Take care that the load capacitors C_{x1},C_{x2}, and C_{x3} in case of third overtone crystal usage have a common ground plane. The external components must also be connected to the ground plain. Loops must be made as small as possible in order to keep the noise coupled in via the PCB as small as possible. Also parasitics should stay as small as possible. Values of C_{x1} and C_{x2} should be chosen smaller accordingly to the increase in parasitics of the PCB layout.

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14.4 ElectroMagnetic Compatibility (EMC)

Radiated emission measurements according to the IEC61967-2 standard using the TEM-cell method are shown for part LPC812M101FDH20.

Table 28. ElectroMagnetic Compatibility (EMC) for part LPC812M101 (TEM-cell method)
V_{DD} = 3.3 V; T_{amb} = 25 °C.

Parameter	Frequency band	System clock =			Unit
		12 MHz	24 MHz	30 MHz	
Input clock: IRC (12 MHz)					
maximum peak level	1 MHz to 30 MHz	–6	–5	–5	dBµV
	30 MHz to 150 MHz	-2	-1	-2	dBµV
	150 MHz to 1 GHz	–1	-1	-1	dBµV
IEC level[1]	-	O	O	O	-
Input clock: crystal oscillator (12 MHz)					
maximum peak level	1 MHz to 30 MHz	–5	–6	–6	dBµV
	30 MHz to 150 MHz	–2	-1	-2	dBµV
	150 MHz to 1 GHz	–1	-2	-1	dBµV
IEC level[1]	-	O	O	N	-

[1] IEC levels refer to Appendix D in the IEC61967-2 Specification.

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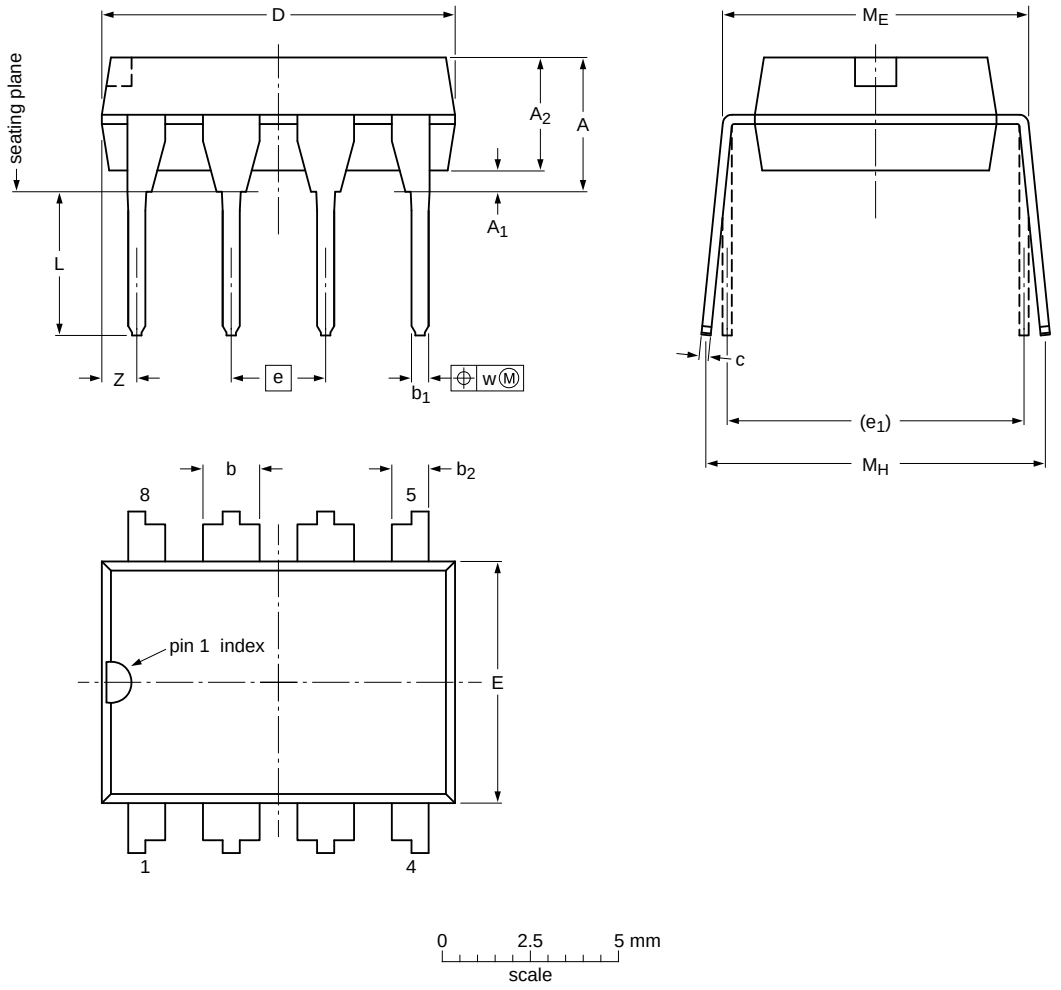
15. Package outline

DIP8: plastic dual in-line package; 8 leads (300 mil) **SOT97-2**



Dimensions (inch dimensions are derived from the original dimensions)

Unit[1]		A	A_1	A_2	b	b_1	b_2	c	D[1]	E[1]	e	e_1	L	M_E	M_H	w	Z[1]
mm	max	4.2		3.43	1.73	0.53	1.07	0.38	9.8	6.48			3.60	7.88	9.40		1.15
	nom										2.54	7.62				0.254	
	min		0.51		1.14	0.38	0.89	0.20	9.2	6.20			3.05	7.62	7.88		
inches	max	0.17		0.14	0.068	0.021	0.042	0.015	0.39	0.26			0.14	0.31	0.37		0.045
	nom										0.1					0.01	
	min		0.02		0.045	0.015	0.035	0.008	0.36	0.24		0.3	0.12	0.30	0.31		

Note
1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included

sot097-2_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT97-2	- - -	MO-001	- - -			~~10-10-15~~ 10-10-18

Fig 38. Package outline SOT097-2 (DIP8)

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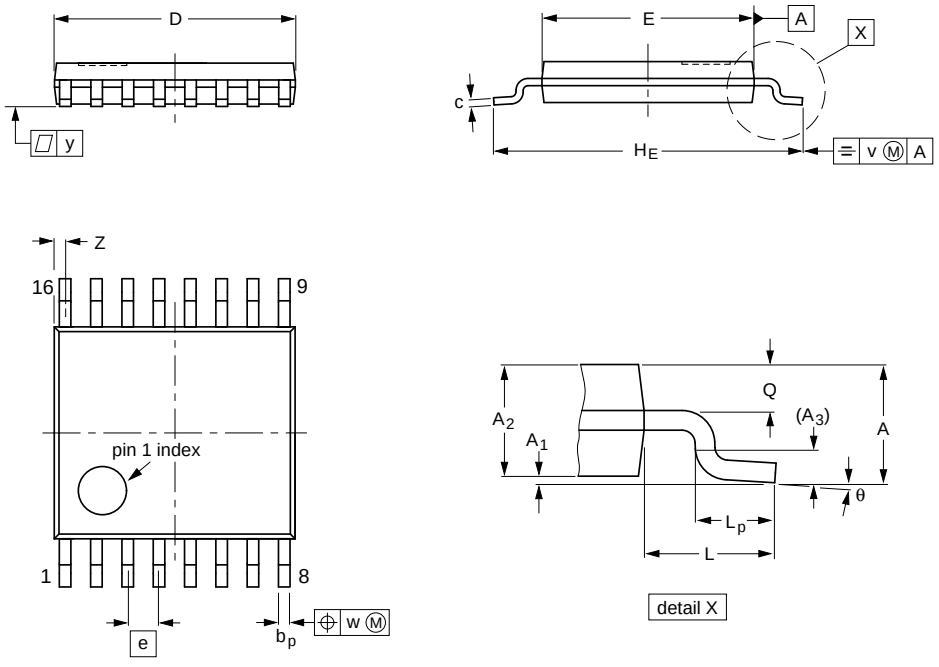
TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				~~99-12-27~~ 03-02-18

Fig 39. Package outline SOT403-1 (TSSOP16)

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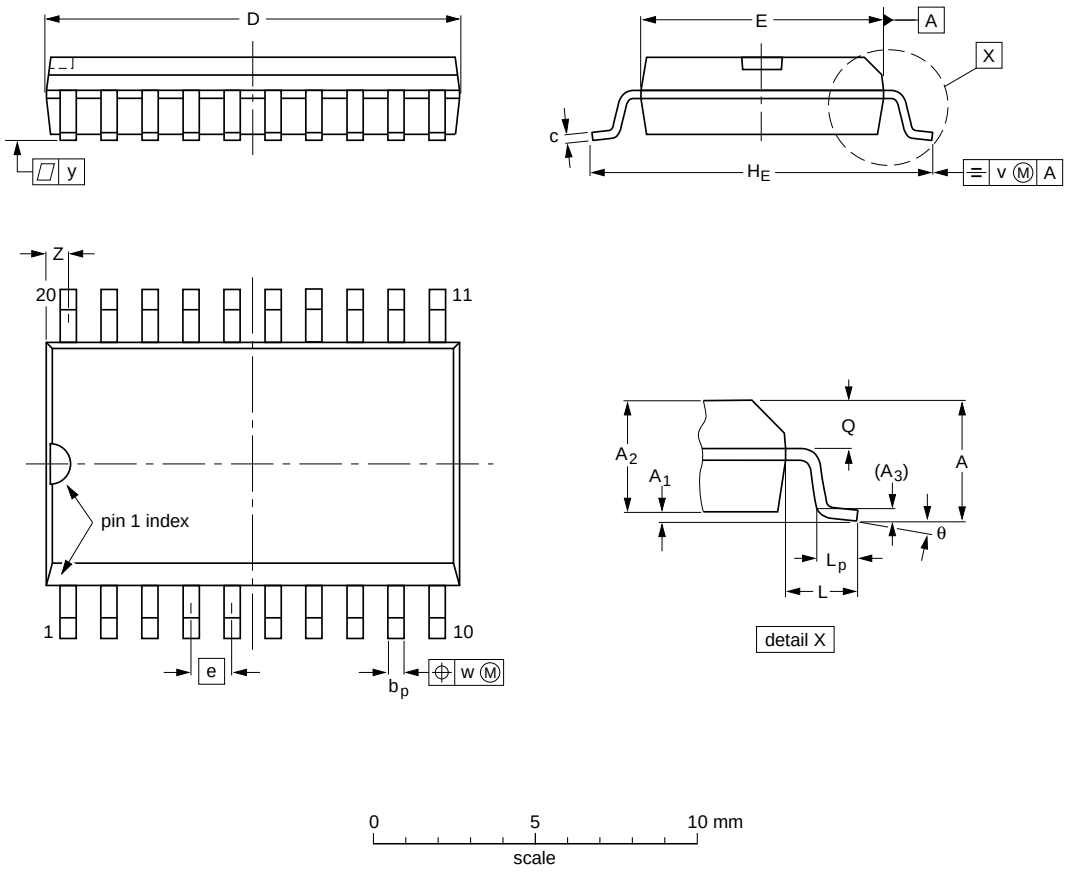
SO20: plastic small outline package; 20 leads; body width 7.5 mm **SOT163-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT163-1	075E04	MS-013				~~99-12-27~~ 03-02-19

Fig 40. Package outline SOT163-1 (SO20)

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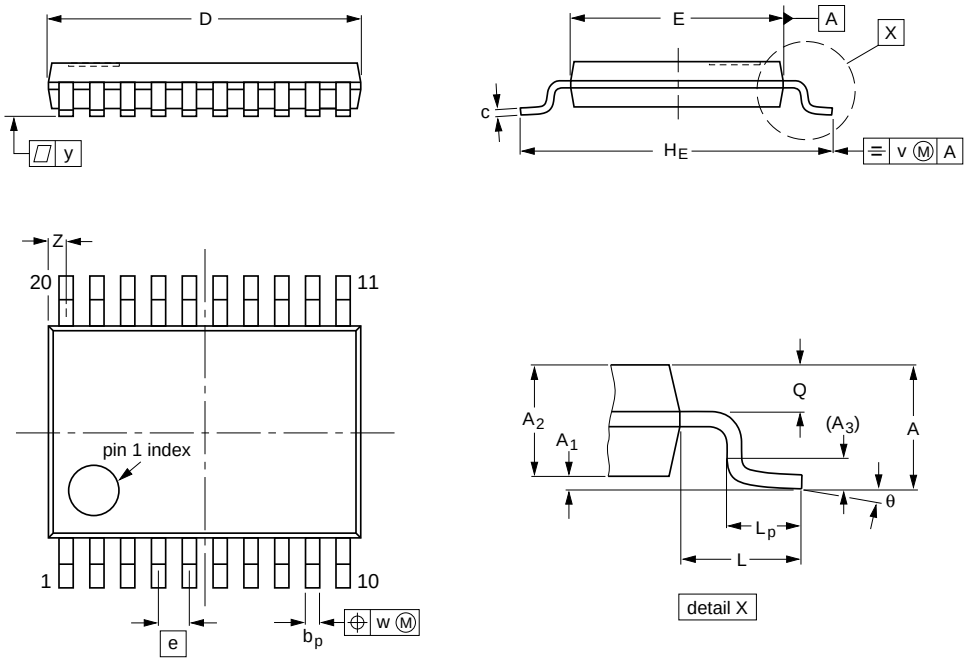
TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm **SOT360-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT360-1		MO-153				~~99-12-27~~ 03-02-19

Fig 41. Package outline SOT360-1 (TSSOP20)

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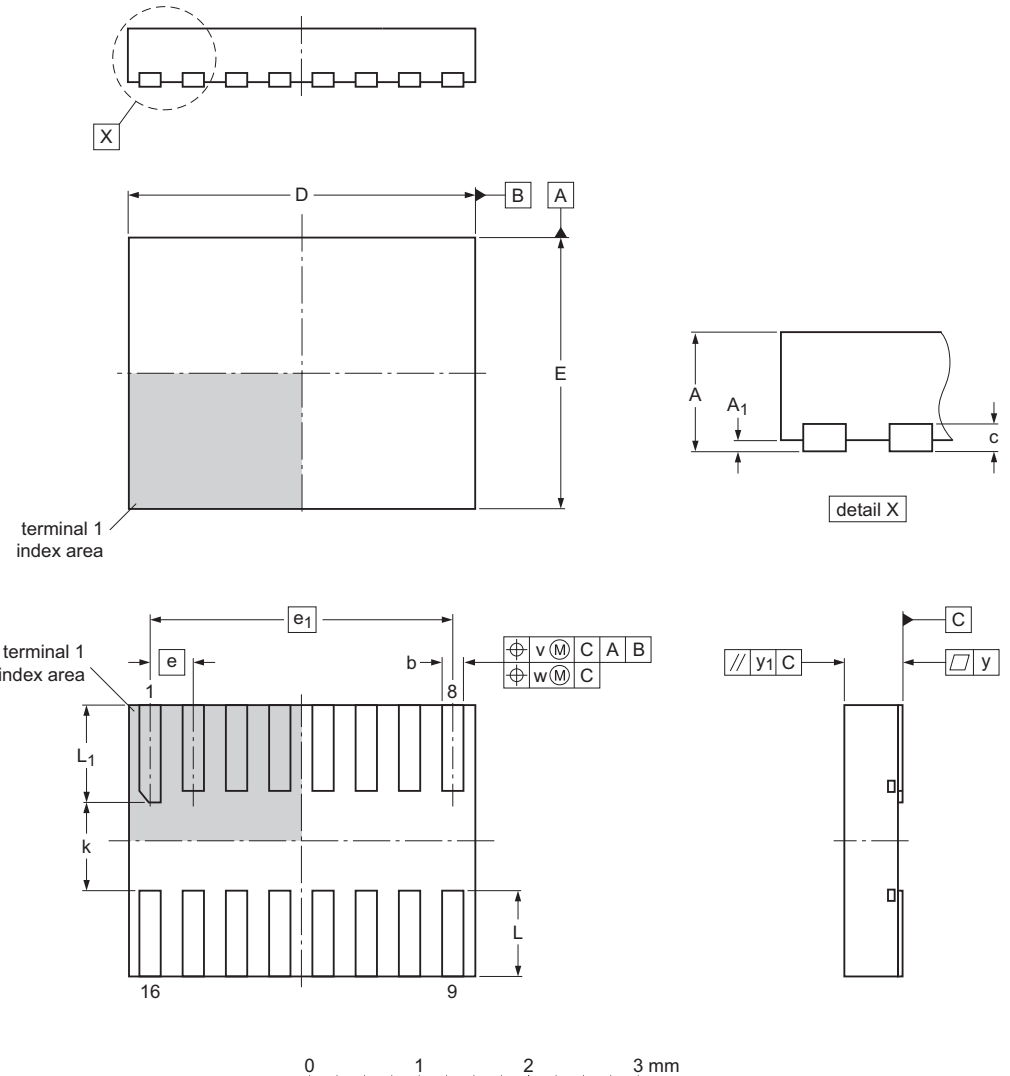
XSON16: plastic extremely thin small outline package; no leads; 16 terminals; body 2.5 x 3.2 x 0.5 mm **SOT1341-1**



Dimensions (mm are the original dimensions)

Unit[1]		A	A_1	b	c	D	E	e	e_1	k	L	L_1	v	w	y	y_1
mm	max	0.5	0.05	0.25	0.152	3.3	2.6				0.9	1.0				
	nom			0.20		3.2	2.5	0.4	2.8		0.8	0.9	0.1	0.05	0.05	0.05
	min		0.00	0.15	0.050	3.1	2.4			0.2	0.7	0.8				

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot1341-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1341-1	- - -	MO-252	- - -			~~12-09-05~~ 13-02-13

Fig 42. Package outline SOT1341-1 (XSON16)

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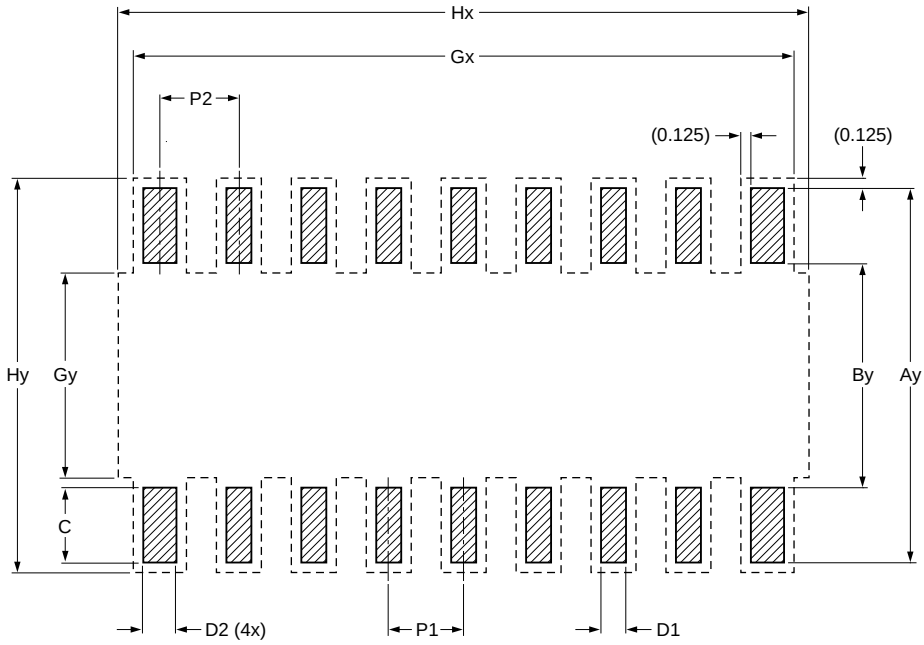
16. Soldering

Footprint information for reflow soldering of TSSOP16 package **SOT403-1**



Generic footprint pattern

Refer to the package outline drawing for actual layout

solder land

occupied area

DIMENSIONS in mm

P1	P2	Ay	By	C	D1	D2	Gx	Gy	Hx	Hy
0.650	0.750	7.200	4.500	1.350	0.400	0.600	5.600	5.300	5.800	7.450

sot403-1_fr

Fig 43. Reflow soldering of the TSSOP16 package

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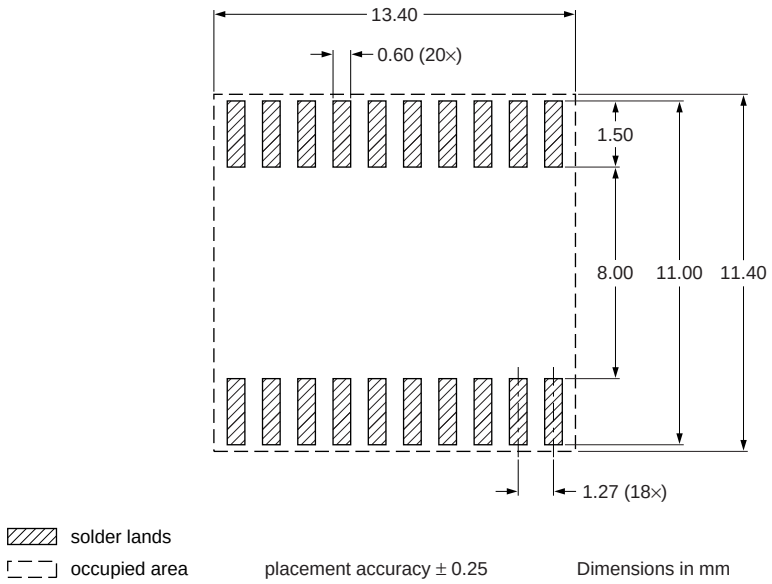

Fig 44. Reflow soldering of the SO20 package

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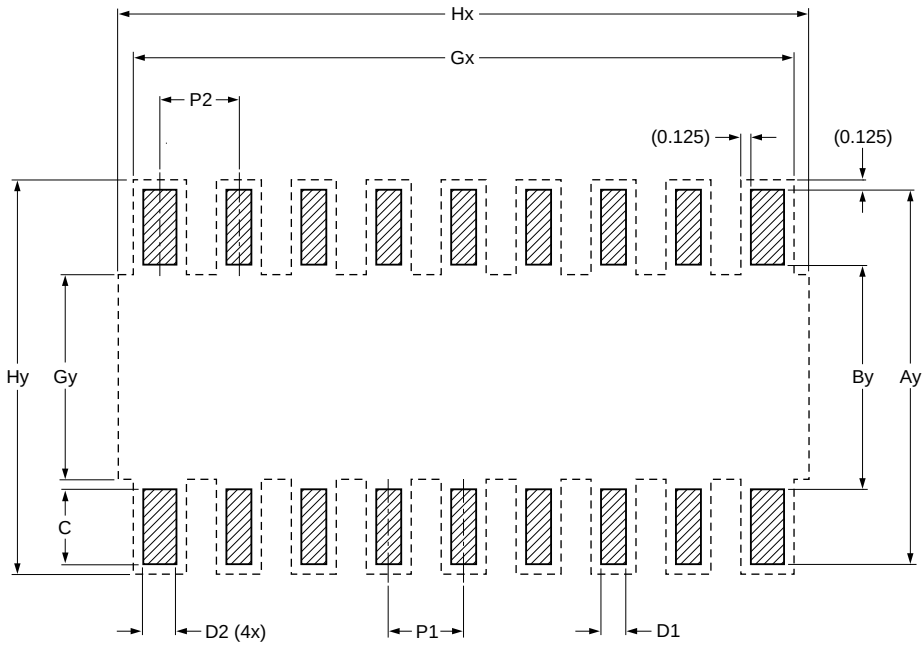
Footprint information for reflow soldering of TSSOP20 package **SOT360-1**



Generic footprint pattern

Refer to the package outline drawing for actual layout

solder land

occupied area

DIMENSIONS in mm

P1	P2	Ay	By	C	D1	D2	Gx	Gy	Hx	Hy
0.650	0.750	7.200	4.500	1.350	0.400	0.600	6.900	5.300	7.300	7.450

sot360-1_fr

Fig 45. Reflow soldering of the TSSOP20 package

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Footprint information for reflow soldering of XSON16 package **SOT1341-1**

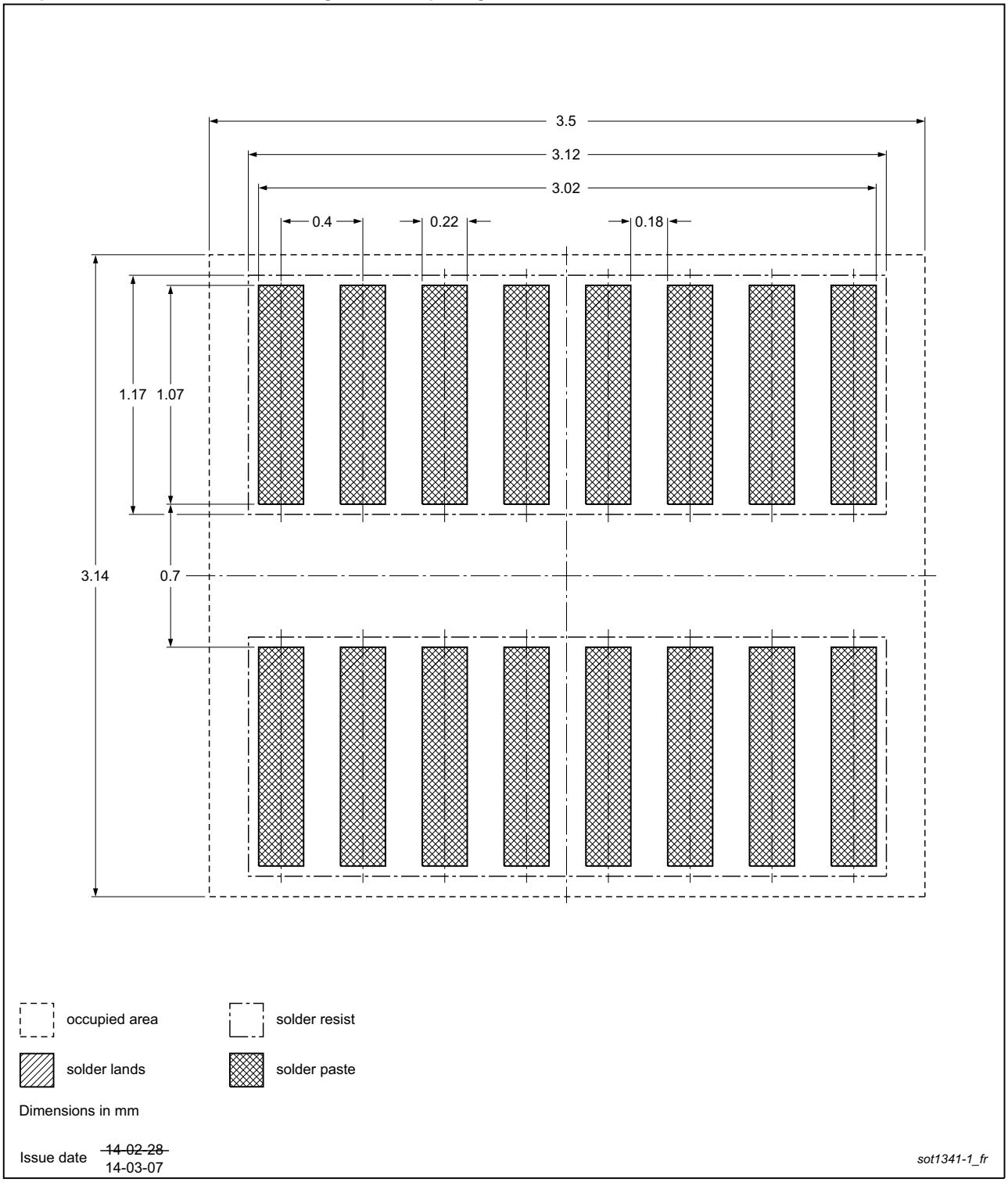

Fig 46. Reflow soldering of the XSON16 package

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17. Abbreviations

Table 29. Abbreviations

Acronym	Description
AHB	Advanced High-performance Bus
APB	Advanced Peripheral Bus
BOD	BrownOut Detection
GPIO	General-Purpose Input/Output
PLL	Phase-Locked Loop
RC	Resistor-Capacitor
SPI	Serial Peripheral Interface
SMBus	System Management Bus
TEM	Transverse ElectroMagnetic
UART	Universal Asynchronous Receiver/Transmitter

18. References

[1] I2C-bus specification *UM10204*.

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19. Revision history

Table 30. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC81XM v.4.7	20210319	Product data sheet	-	LPC81XM v.4.6
	• Updated Table 11 “Power-up characteristics” , Table 7 “Limiting values”, and Table 9 “Static characteristics”.			
LPC81XM v.4.6	20180404	Product data sheet	201804004I	LPC81XM v.4.5
Modifications:	• Updated table note 2 of Section 12.1 “Power-up ramp conditions”.			
LPC81XM v.4.5	20160603	Product data sheet	-	LPC81XM v.4.4
Modifications:	• Added Section 12.1 “Power-up ramp conditions”. • Updated Figure 4 “Pin configuration SO20 package (LPC812M101JD20)”: Corrected function of pin 12 to ACMP_I2. • Updated the remark in Section 8.12 “USART0/1/2” to: USART2 is available on parts LPC812M101JTB16, LPC812M101JDH16, and LPC812M101JDH20 only.			
LPC81XM v.4.4	20150619	Product data sheet	-	LPC81XM v.4.3
Modifications:	• Section 14.4 “ElectroMagnetic Compatibility (EMC)” added.			
LPC81XM v.4.3	20140422	Product data sheet	-	LPC81XM v.4.2
Modifications:	• Section 8.20.2 “Clock input” updated for clarity. • CLKIN signal removed from Table 13 “Dynamic characteristic: external clock (XTALIN inputs)”. • Name “SCT” changed to “SCTimer/PWM” for clarity. • Remove slew rate control from GPIO features for clarity. • MRT bus stall mode added. • WWDT clock source corrected in Section 8.17.1. • Pin description table updated for clarification (I2C-bus pins, WAKEUP, $\overline{\text{RESET}}$). • Added reflow solder diagram and thermal resistance numbers for XSON16 (SOT1341-1). • Table 22: Added $V_{ref(cmp)}$ spec for PIO0_6/VDDCMP..			
LPC81XM v.4.2	20131210	Product data sheet	-	LPC81XM v.4.1
Modifications:	Corrected vertical axis marker in Figure 21 “CoreMark score”.			
LPC81XM v.4.1	20131112	Product data sheet	-	LPC81XM v.4
Modifications:	• Corrected XSON16 pin information in Figure 6 and Table 4.			
LPC81XM v.4	20131025	Product data sheet	-	LPC81XM v.3.1
Modifications:	• Added Section 14.1 “Typical wake-up times”. • Added LPC812M101JTB16 and XSON16 package.			
LPC81XM v.3.1	20130916	Product data sheet	-	LPC81XM v.3
Modifications:	• Correct the pin interrupt features: Pin interrupts can wake up the part from Sleep mode, Deep-sleep mode, and Power-down mode. See Section 8.11.1. • Table 9 “Static characteristics”: Updated power numbers for Deep-sleep, Power-down, and Deep power-down. • Added 30 MHz data to Figure 13 “Active mode: Typical supply current IDD versus supply voltage VDD”, Figure 14 “Active mode: Typical supply current IDD versus temperature”, and Figure 15 “Sleep mode: Typical supply current IDD versus temperature for different system clock frequencies”.			

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Table 30. Revision history *...continued*

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC81XM v.3	20130729	Product data sheet	-	LPC81XM v.2.1
	• Operating temperature range changed to −40 °C to 105 °C. • Type numbers updated to reflect the new operating temperature range. See Table 1 “Ordering information” and Table 2 “Ordering options”. • ISP entry pin moved from PIO0_1 to PIO0_12 for TSSOP, and SSOP packages. See Table 4 and Table 6. • Propagation delay values updated in Table 21 “Comparator characteristics”. • SPI characteristics updated. See Section 12.6. • IRC characteristics updated. See Section 12.3. • CoreMark data updated. See Figure 19 and Figure 20. • IRC frequency changed to 12 MHz +/- 1.5 %. See Table 13. • Data sheet status updated to Product data sheet.			
LPC81XM v.2.1	20130325	Preliminary data sheet	-	LPC81XM v.2
	• Editorial updates (temperature sensor removed). • CoreMark data added. See Figure 19 “Active mode: CoreMark power consumption IDD” and Figure 20 “CoreMark score”. • I_{DD} in Deep power-down mode added for condition Low-power oscillator on/WKT wake-up enabled. See Table 10. • Table note 3 updated for Table 4 “Pin description table (fixed pins)”. • Conditions for t_{er} and t_{prog} updated in Table 12 “Flash characteristics”. • Section 13.3 “Internal voltage reference” added. • Typical timing data added for SPI. See Section 12.6. • Typical timing data added for USART in synchronous mode. See Section 12.7. • BOD characterization added. See Section 13.1. • IRC characterization added. See Section 12.3. • Internal voltage reference characteristics added. See Section 13.3. • Data sheet status changed to Preliminary data sheet.			
LPC81XM v.2	20130128	Objective data sheet	-	LPC81XM v.1
Modifications:	• MTB memory space changed to 1 kB in Figure 6. • Electrical pin characteristics added in Table 10. • Figure 11 “Connecting the SWD pins to a standard SWD connector” added. • Peripheral power consumption added in Table 11. • Table 7 updated. • MRT implementation changed to 31-bit timer. • Power consumption data in active and sleep mode with IRC added. See Figure 13 to Figure 15. • Power consumption (parameter I_{DD}) in active and sleep mode for low-power mode at 12 MHz corrected in Table 10. • Power consumption (parameter I_{DD}) in active and sleep mode at 24 MHz added in Table 10. • Maximum USART speed in synchronous mode changed to 10 Mbit/s. • Section 5 “Marking” added.			
LPC81XM v.1	20121112	Objective data sheet	-	-

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