THE DATASHEET OF

ICM-30630

ICM-30630 Product Specification

Revision 1.0

GENERAL DESCRIPTION

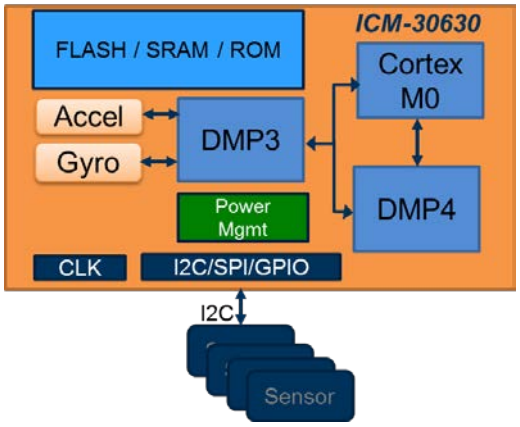
The single-chip ICM-30630 is the world's first tri-core 6-axis motion tracking solution with integrated sensor-hub framework software. It combines industry leading gyroscope and accelerometer sensors with tri-core processors (an ARM Cortex-M0 CPU, a DMP3 and a DMP4 Digital Motion Processor™) in a small 3x3x1mm LGA package.

The ICM-30630 serves as a sensor hub that supports the collection and processing of data from internal and external sensors. The multi-cores are designed to offload processing from the Application Processor, thereby saving system power and improving performance.

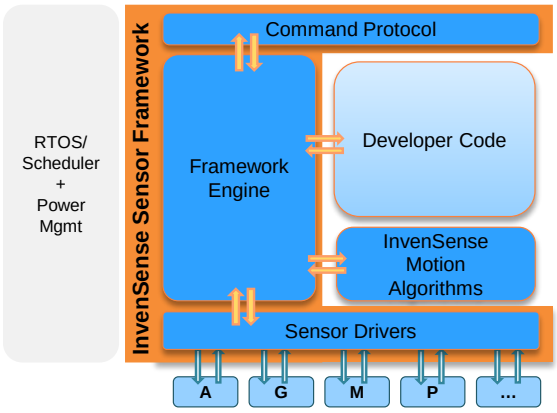
The ARM Cortex-M0 CPU provides a low-power programmable platform for software development. The DMP3 offloads Android L processing from the CPU and provides ready-to-use physical and virtual Android sensors. The DMP4 is optimized for fixed point processing and FFT generation and complements the CPU by offloading math intensive operations.

The integrated InvenSense Sensor Framework provides an open and powerful platform for creating cutting-edge always-on applications for mobile platforms. Developers can use the built-in framework components to rapidly develop and launch new features. The command protocol is designed for seamless porting to new systems, allowing software reuse and thus maximizing returns on software investment.

BLOCK DIAGRAM



SENSOR FRAMEWORK SOFTWARE



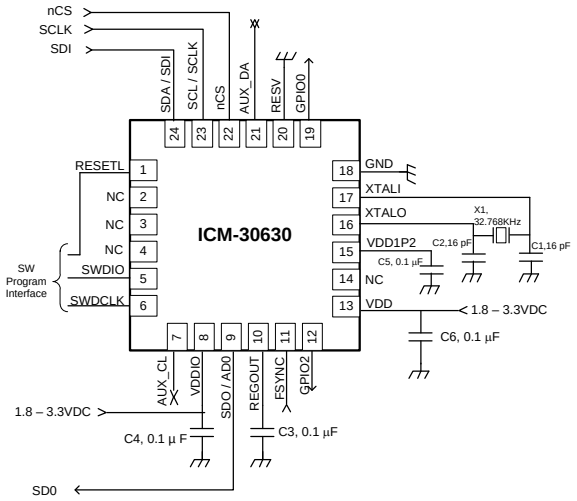
APPLICATIONS

- Smartphones and Tablets
- Wearables

FEATURES

- Tri-core sensor hub with integrated 6-Axis in a 24-Pin LGA: 3mm x 3mm x 1mm package
- Built-in sensor framework for fast time-to-market
- Low Power 6-Axis Device:
  - 2.25mW 6-Axis Power (Gyro+Accel 102.3Hz ODR)
- Android L Support
- On-Chip Runtime Calibration
- Auxiliary I^2C interface to support additional sensors, enabling multi-sensor MotionFusion operation
- 3-Axis Gyroscope with Programmable FSR of ±250, ±500, ±1000, and ±2000dps
- 3-Axis Accelerometer with Programmable FSR of ±2g, ±4g, ±8g and ±16g
- ARM Cortex-M0 CPU & DMP3 and DMP4
- Flash 64Kbytes
- SRAM 64Kbytes (shared by Cortex-M0, DMPs, FIFO)
- DMA Controller
- 4 timers that can be used for timestamp, watchdog, and general purpose timer functions
- Serial Wire Data Port for Cortex-M0 debug/trace
- 3 on-chip oscillators for system clock, accurate time stamping, and periodic wakeup
- 3 GPIO bidirectional pins configurable as general purpose input/output, or interrupt input/output
- I^2C up to 2.7MHz; SPI up to 6.4MHz

TYPICAL OPERATING CIRCUIT



ORDERING INFORMATION

PART	TEMP RANGE	PACKAGE
ICM-30630†	−40°C to +85°C	24-Pin LGA

†Denotes RoHS and Green-Compliant Package

TABLE OF CONTENTS

TABLE OF FIGURES

TABLE OF TABLES

1.1 PURPOSE AND SCOPE

This document is a preliminary product specification, providing a description, specifications, and design related information on the ICM-30630 MotionTracking device.

Specifications are subject to change without notice. Final specifications will be updated based upon characterization of production silicon.

1.2 PRODUCT OVERVIEW

The ICM-30630 is a MotionTracking device that combines a 3-axis gyroscope, 3-axis accelerometer, and tri-core processors (an ARM Cortex-M0 CPU, and a DMP3 and a DMP4 Digital Motion Processor™) all in a small 3x3x1mm LGA package. The device supports the following features:

- ARM Cortex-M0 based open platform optimized for motion applications with dual-DMP based motion accelerators
- Support for Android L and beyond
- Memory (DMP + FIFO): Variable size FIFO based on DMP feature-set
- Runtime Calibration

The ICM-30630 serves as a sensor hub, supporting the collection and processing of data from internal and external sensors. It can offload processing from the Application Processor in a system, thereby helping to save system power and improve performance. The device includes a primary serial interface (I^2C and 4-wire SPI) for communication from the host processor.

ICM-30630 devices, with their 6-axis integration, ARM Cortex-M0 CPU, DMPs, and run-time calibration firmware, enable manufacturers to eliminate the costly and complex selection, qualification, and system level integration of discrete devices, guaranteeing optimal motion performance for consumers.

The gyroscope has a programmable full-scale range of ±250, ±500, ±1000, and ±2000 degrees/sec. The accelerometer has a user-programmable accelerometer full-scale range of ±2*g*, ±4*g*, ±8*g*, and ±16*g*. Factory-calibrated initial sensitivity of both sensors reduces production-line calibration requirements.

Other key features include on-chip 16-bit ADCs, programmable digital filters, an embedded temperature sensor, and programmable interrupts. The device features I^2C and SPI serial interfaces, a VDD operating range of 1.71 to 3.6V, and a separate digital IO supply, VDDIO from 1.71V to 3.6V. The device supports the following interface speeds: I^2C up to 2.7MHz or SPI up to 6.4MHz.

By leveraging its patented and volume-proven CMOS-MEMS fabrication platform, which integrates MEMS wafers with companion CMOS electronics through wafer-level bonding, InvenSense has driven the package size down to a footprint and thickness of 3x3x1mm (24-pin LGA), to provide a very small yet high performance low cost package. The device provides high robustness by supporting 10,000*g* shock reliability.

1.3 APPLICATIONS

- Smart Phones and Tablets
- Wearables

2 FEATURES

2.1 GYROSCOPE FEATURES

- Digital-output X-, Y-, and Z-axis angular rate sensors (gyroscopes) with a user-programmable full-scale range of ±250, ±500, ±1000, and ±2000°/sec and integrated 16-bit ADCs
- User-selectable ODR
- User-selectable low pass filters
- Self-test

2.2 ACCELEROMETER FEATURES

- Digital-output X-, Y-, and Z-axis accelerometer with a programmable full scale range of ±2*g*, ±4*g*, ±8*g* and ±16*g* and integrated 16-bit ADCs
- User-selectable ODR
- User-selectable low pass filters
- Wake-on-motion interrupt for low power operation of applications processor
- Self-test

2.3 ARM CORTEX-M0 FEATURES

- 32-bit microprocessor
- Maximum speed 64MHz
- Serial Wire Data Port for ARM Cortex-M0 user debug
    - Pin 5 (SWDIO) for data signal and pin 6 (SWDCLK) for clock signal

2.4 DMP FEATURES

- DMP3 and DMP4
- Advanced MotionProcessing and low power functions such as gesture recognition using programmable interrupts
- Optimized for Android L support and beyond
- Offloads computation of motion processing algorithms from the host processor. The DMPs can be used to minimize power, simplify timing, simplify the software architecture, and save valuable MIPS on the host processor for use in applications.
- The DMP3 enables ultra-low power run-time and background calibration of the accelerometer, gyroscope, and external sensors, maintaining optimal performance of the sensor data for both physical and virtual sensors generated through sensor fusion. This enables the best user experience for all sensor enabled applications for the lifetime of the device. DMP3 is closely integrated with the MEMS to enable ultra-low power performance.
- The DMP4 is optimized for fixed point processing and FFT generation and complements the CPU by offloading math intensive operations.
- DMP features simplify the software architecture resulting in a more robust overall solution.
- DMP features are OS, Platform, and Architecture independent, supporting virtually any AP, MCU, or other embedded architecture.

2.5 ON-CHIP MEMORY

- 64KB Flash (provides user access for on-chip reprogrammable nonvolatile memory)
- 64KB SRAM (accessible by Cortex-M0, DMPs, FIFO)
- Configurable FIFO with multiple modes of operation and multiple watermark interrupts

2.6 CLOCK GENERATION UNIT

- High frequency RC oscillator for system clock
- Low frequency RC oscillator for periodic wake up
- 32.768kHz crystal oscillator for accurate time stamping
    - This oscillator also requires an external 32.768kHz input (pin 17 XTALI)
    - Oscillator output pin (pin 16 XTALO)

2.7 SERIAL INTERFACES

- One I^2C slave controller for communication with application processors, operating at up to 2.7MHz in High-Speed Mode, or up to 0.8MHz in Fast-Mode Plus, or up to 320kHz in Fast-Mode, or up to 80kHz in Standard-Mode
- One I^2C master controller for interfacing to external sensors (e.g. compass or barometer), operating at up to 2.7MHz in High-Speed Mode, or up to 0.8MHz in Fast-Mode Plus, or up to 320kHz in Fast-Mode, or up to 80kHz in Standard-Mode
- One 4-wire SPI slave controller operating at speeds of up to 6.4MHz for communication with application processor
- I^2C slave controller and SPI slave controller are multiplexed together, only one or the other may be used

2.8 DIGITAL PERIPHERALS

- 3 GPIO bidirectional pins that can be configured as general purpose input, general purpose output, interrupt input, or interrupt output
- Four timers used for watchdog, timestamp, and general purpose timer functions

2.9 POWER MANAGEMENT

- Single 1.8V (1.71V to 3.6V) power supply with on-chip internal voltage regulator for the multiple voltage islands and always on domain
- Single 1.8V (1.71V to 3.6V) IO power supply
- External 1.2 volts supply pin
    - The device can be configured to use external 1.2 volts supply or on-chip regulators
- Power modes for different levels of power savings: Sleep, Deep-Sleep, Power-Down
- Wake up from Sleep, and Deep-Sleep power modes via external interrupts or interrupts generated by always on blocks
- On-chip Power-On Reset and dedicated reset input pin
    - Reset input can be used to wake up the device from sleep

3 ELECTRICAL CHARACTERISTICS

3.1 GYROSCOPE SPECIFICATIONS

Typical Operating Circuit of section 4.2, VDD = 1.8V, VDDIO = 1.8V, T_A=25°C, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
GYROSCOPE SENSITIVITY						
Full-Scale Range			±250		°/s	1
			±500		°/s	1
			±1000		°/s	1
			±2000		°/s	1
Gyroscope ADC Word Length			16		bits	1
Sensitivity Scale Factor	Full-Scale Range = ±250°/s		131		LSB/(°s)	1
	Full-Scale Range = ±500°/s		65.5		LSB/(°s)	1
	Full-Scale Range = ±1000°/s		32.8		LSB/(°s)	1
	Full-Scale Range = ±2000°/s		16.4		LSB/(°s)	1
Sensitivity Scale Factor Tolerance	25°C		±3		%	2
Sensitivity Scale Factor Variation Over Temperature	-40°C to +85°C		±4		%	2
Nonlinearity	Best fit straight line; 25°C		±0.2		%	2, 3
Cross-Axis Sensitivity			±2		%	2, 3
ZERO-RATE OUTPUT (ZRO)						
Initial ZRO Tolerance	25°C		±20		°/s	2
ZRO Variation Over Temperature	-40°C to +85°C		±0.24		°/s/°C	2
GYROSCOPE NOISE PERFORMANCE (GYRO_FS_SEL=0)						
Total RMS Noise	Noise Bandwidth = 154Hz Calculated from Noise Spectral Density		0.20		°/s-rms	2, 3
Noise Spectral Density	Based on Noise Bandwidth = 10Hz		0.016		°/s/√Hz	2
GYROSCOPE MECHANICAL FREQUENCIES		25	27	29	kHz	2
LOW PASS FILTER RESPONSE	Programmable Range	5.7		197	Hz	1, 3
GYROSCOPE START-UP TIME	From Full-Chip Sleep mode		35		ms	2, 3
OUTPUT DATA RATE	Standard (duty-cycled) Mode	4.4		562.5	Hz	1
	Low-Noise Mode	4.4		1.125k (additional 9kHz option)	Hz	

Table 1. Gyroscope Specifications

Notes:

1. Guaranteed by design
2. Derived from validation or characterization of parts, not guaranteed in production
3. Low-noise mode specification

3.2 ACCELEROMETER SPECIFICATIONS

Typical Operating Circuit of section 4.2, VDD = 1.8V, VDDIO = 1.8V, T_A=25°C, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS	NOTES
ACCELEROMETER SENSITIVITY							
Full-Scale Range				±2		*g*	1
				±4		*g*	1
				±8		*g*	1
				±16		*g*	1
ADC Word Length	Output in two's complement format			16		bits	1
Sensitivity Scale Factor	Full-Scale Range = ±2g			16,384		LSB/*g*	1
	Full-Scale Range = ±4g			8,192		LSB/*g*	1
	Full-Scale Range = ±8g			4,096		LSB/*g*	1
	Full-Scale Range = ±16g			2,048		LSB/*g*	1
Initial Tolerance	Component-level			±3		%	2
Sensitivity Change vs. Temperature	-40°C to +85°C			±0.026		%/°C	2
Nonlinearity	Best Fit Straight Line			±0.5		%	2, 3
Cross-Axis Sensitivity				±2		%	2, 3
ZERO-G OUTPUT							
Initial Tolerance	Component-level, all axes			±80		m*g*	2
Zero-G Level Change vs. Temperature	-40°C to +85°C	X and Y axes		±0.64		mg/°C	2
		Z axis		±2		mg/°C	2
ACCELEROMETER NOISE PERFORMANCE							
Total RMS Noise	Noise Bandwidth = 136Hz Calculated from Noise Spectral Density			2.92		mg-rms	2, 3
Noise Spectral Density	Based on Noise Bandwidth = 10Hz			250		µg/√Hz	2
LOW PASS FILTER RESPONSE	Programmable Range		5.7		246	Hz	1, 3
INTELLIGENCE FUNCTION INCREMENT				32		mg/LSB	1
ACCELEROMETER STARTUP TIME	From Sleep mode			20		ms	2, 3
	From Cold Start, 1ms V_{DD} ramp			30		ms	2, 3
OUTPUT DATA RATE	Standard (duty-cycled) Mode		0.27		563	Hz	1
	Low-Noise Mode		4.5		1.125k (additional 4.5kHz option)	Hz	

Table 2. Accelerometer Specifications

Notes:

1. Guaranteed by design
2. Derived from validation or characterization of parts, not guaranteed in production
3. Low-noise mode specification

3.3 ELECTRICAL SPECIFICATIONS

3.3.1 D.C. Electrical Characteristics

Typical Operating Circuit of section 4.2, VDD = 1.8V, VDDIO = 1.8V, T_A=25°C, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
SUPPLY VOLTAGES						
VDD		1.71	1.8	3.6	V	1
VDDIO		1.71	1.8	3.6	V	1
SUPPLY CURRENTS						
Gyroscope Only (DMP & Accelerometer disabled)	102.3Hz update rate, 1x averaging filter		1.21		mA	2, 3
Accelerometer Only (DMP & Gyroscope disabled)	102.3Hz update rate, 1x averaging filter		66		µA	2. 3
Gyroscope + Accelerometer (DMP disabled)	102.3Hz update rate, 1x averaging filter		1.25		mA	2, 3
Deep Sleep Mode			32		µA	2
Power Down Mode			10		µA	2
TEMPERATURE RANGE						
Specified Temperature Range	Performance parameters are not applicable beyond Specified Temperature Range	-40		+85	°C	1

Table 3. D.C. Electrical Characteristics

Notes:

1. Guaranteed by design
2. Derived from validation or characterization of parts, not guaranteed in production
3. The 102.3Hz ODR value shown here is an example, other ODRs may also be used

3.3.2 A.C. Electrical Characteristics

Typical Operating Circuit of section 4.2, VDD = 1.8V, VDDIO = 1.8V, T_A=25°C, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
SUPPLIES						
Supply Ramp Time (T_{RAMP})	Monotonic ramp. Ramp rate is 10% to 90% of the final value.	0.4	20	100	ms	1
TEMPERATURE SENSOR						
Operating Range	Ambient	-40		85	°C	1
Sensitivity	Untrimmed		333.87		LSB/°C	
Room Temp Offset	21°C		0		LSB	
Power-On RESET						
Supply Ramp Time (T_{RAMP})	Valid power-on RESET	0.01	20	100	ms	1
Start-up time for register read/write	From power-up		11	100	ms	1
I^2C SLAVE ADDRESS	AD0 = 0 AD0 = 1		1101010 (0x6A) 1101011 (0x6B)			
DIGITAL INPUTS (FSYNC, AD0, SCLK, SDI, CS)						
V_{IH}, High Level Input Voltage		0.7*VDDIO			V	1
V_{IL}, Low Level Input Voltage				0.3*VDDIO	V	
C_I, Input Capacitance			< 10		pF	
DIGITAL OUTPUT (SDO, GPIOs)						
V_{OH}, High Level Output Voltage	R_{LOAD}=1MΩ;	0.9*VDDIO			V	1
V_{OL1}, LOW-Level Output Voltage	R_{LOAD}=1MΩ;			0.1*VDDIO	V	
$V_{OL.INT1}$, INT Low-Level Output Voltage	OPEN=1, 0.3mA sink Current			0.1	V	
Output Leakage Current	OPEN=1		100		nA	
t_{INT}, INT Pulse Width	LATCH_INT_EN=0	1		16	µs	
I2C I/O (SCL, SDA)						
V_{IL}, LOW Level Input Voltage		-0.5V		0.3*VDDIO	V	1
V_{IH}, HIGH-Level Input Voltage		0.7*VDDIO		VDDIO + 0.5V	V	
V_{hys}, Hysteresis			0.1*VDDIO		V	
V_{OL}, LOW-Level Output Voltage	3mA sink current	0		0.4	V	
I_{OL}, LOW-Level Output Current	V_{OL}=0.4V V_{OL}=0.6V		3 6		mA mA	
Output Leakage Current			100		nA	
t_{of}, Output Fall Time from V_{IHmax} to V_{ILmax}	C_b bus capacitance in pf	20+0.1C_b		250	ns	
AUXILLIARY I/O (AUX_CL, AUX_DA)						
V_{IL}, LOW-Level Input Voltage		-0.5V		0.3*VDDIO	V	1
V_{IH}, HIGH-Level Input Voltage		0.7* VDDIO		VDDIO + 0.5V	V	
V_{hys}, Hysteresis			0.1* VDDIO		V	
V_{OL1}, LOW-Level Output Voltage	VDDIO > 2V; 1mA sink current	0		0.4	V	
V_{OL3}, LOW-Level Output Voltage	VDDIO < 2V; 1mA sink current	0		0.2* VDDIO	V	
I_{OL}, LOW-Level Output Current	V_{OL} = 0.4V V_{OL} = 0.6V		3 6		mA mA	
Output Leakage Current			100		nA	
t_{of}, Output Fall Time from V_{IHmax} to V_{ILmax}	C_b bus capacitance in pF	20+0.1C_b		250	ns	
INTERNAL CLOCK SOURCE						
RC Oscillator	Maximum Frequency			64	MHz	1
	Variation over operating range	-10		+10	%	1
Wakeup Oscillator	Target Frequency		8		kHz	1
	Variation over operating range	-20		+20	%	1

EXTERNAL CLOCK SOURCE						
Crystal Oscillator	Frequency		32.768		kHz	1
	Crystal Q	4250				1
	Duty Cycle	30		70	%	1
	Crystal Load Capacitance		9		pF	1
	Device Startup Time			200	ms	1

Table 4. A.C. Electrical Characteristics

Notes:

1. Derived from validation or characterization of parts, not guaranteed in production.

3.4 I2C TIMING CHARACTERIZATION

Typical Operating Circuit of section 4.2, VDD = 1.8V, VDDIO = 1.8V, T_A=25°C, unless otherwise noted.

PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
I^2C TIMING	**I^2C HIGH-SPEED MODE**					
f_{SCL}, SCL Clock Frequency				2.7	MHz	
$t_{HD.STA}$, (Repeated) START Condition Hold Time		160			ns	
t_{LOW}, SCL Low Period		320			ns	
t_{HIGH}, SCL High Period		120			ns	
$t_{SU.STA}$, Repeated START Condition Setup Time		160			ns	
$t_{HD.DAT}$, SDA Data Hold Time		0		150	ns	
$t_{SU.DAT}$, SDA Data Setup Time		10			ns	
t_r, SDA and SCL Rise Time		20		160	ns	
t_f, SDA and SCL Fall Time		20		160	ns	
$t_{SU.STO}$, STOP Condition Setup Time		160			ns	
C_b, Capacitive Load for each Bus Line			< 400		pF	

Table 5. I^2C Timing Characteristics

Notes:

1. Timing Characteristics apply to both Primary and Auxiliary I2C Bus

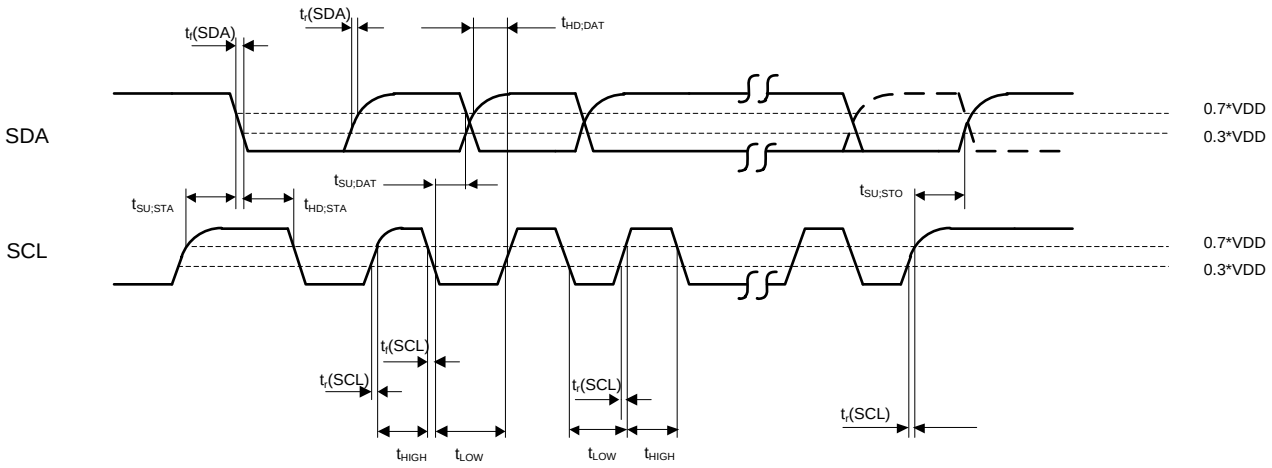


Figure 1.I2C Bus Timing Diagram

3.5 SPI TIMING CHARACTERIZATION

Typical Operating Circuit of section 4.2, VDD = 1.8V, VDDIO = 1.8V, T_A=25°C, unless otherwise noted.

PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
SPI TIMING						
f_{SCLK}, SCLK Clock Frequency				6.4	MHz	
t_{LOW}, SCLK Low Period		50			ns	
t_{HIGH}, SCLK High Period		50			ns	
$t_{SU.CS}$, CS Setup Time		0			ns	
$t_{HD.CS}$, CS Hold Time		20			ns	
$t_{SU.SDI}$, SDI Setup Time		0			ns	
$t_{HD.SDI}$, SDI Hold Time		75			ns	
$t_{VD.SDO}$, SDO Valid Time				12	ns	
$t_{HD.SDO}$, SDO Hold Time		15			ns	
$t_{DIS.SDO}$, SDO Output Disable Time				62	ns	

Table 6. SPI Timing Characteristics

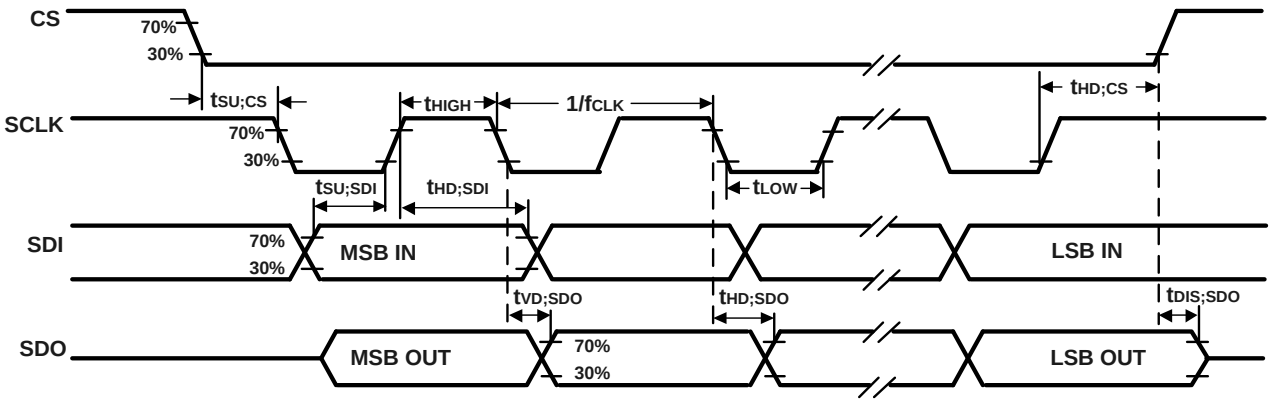


Figure 2. SPI Bus Timing Diagram

3.6 ABSOLUTE MAXIMUM RATINGS

Stress above those listed as “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to the absolute maximum ratings conditions for extended periods may affect device reliability.

PARAMETER	RATING
Supply Voltage, VDD	-0.5V to +4V
Supply Voltage, VDDIO	-0.5V to +4V
REGOUT	-0.5V to 2V
Input Voltage Level (AUX_DA, AD0, FSYNC, INT, SCL, SDA)	-0.5V to VDDIO + 0.5V
Acceleration (Any Axis, unpowered)	10,000g for 0.2ms
Operating Temperature Range	-40°C to +105°C
Storage Temperature Range	-40°C to +125°C
Electrostatic Discharge (ESD) Protection	2kV (HBM); 200V (MM)
Latch-up	JEDEC Class II (2),125°C ±100mA

Table 7. Absolute Maximum Ratings

4 APPLICATIONS INFORMATION

4.1 PIN OUT DIAGRAM AND SIGNAL DESCRIPTION

PIN NUMBER	PIN NAME	PIN DESCRIPTION
1	RESETL	External reset input
2	RESV	Reserved
3	RESV	Reserved
4	RESV	Reserved
5	SWDIO	Serial Wire Debug Port – Data Signal
6	SWDCLK	Serial Wire Debug Port – Clock Signal
7	AUX_CL	I^2C master serial clock, for connection to external sensors
8	VDDIO	Digital I/O supply voltage
9	SDO/AD0	SPI slave serial data port output (SPI host interface mode); I^2C slave address LSB (I^2C host interface mode)
10	REGOUT	Regulator filter capacitor connection
11	FSYNC/GPIO1	Frame synchronization digital input, connect to GND if unused; GPIO/Interrupt
12	GPIO2	GPIO/Interrupt
13	VDD	Power supply voltage
14	RESV	Reserved
15	VDD1P2	External 1.2V supply. NC if not used.
16	XTALO	32kHz crystal output
17	XTALI	32kHz crystal input
18	GND	Power supply ground
19	GPIO0	GPIO/Interrupt
20	RESV	Reserved. Do not connect.
21	AUX_DA	I^2C master serial data, for connection to external sensors
22	nCS/RESV	SPI slave chip select (SPI host interface mode); Tie High (I^2C host interface mode)
23	SCLK/SCL	SPI slave serial clock (SPI host interface mode); I^2C slave serial clock (I^2C host interface mode)
24	SDI/SDA	SPI slave serial data input (SPI host interface mode); I^2C slave serial data (I^2C host interface mode)

Table 8. Signal Descriptions

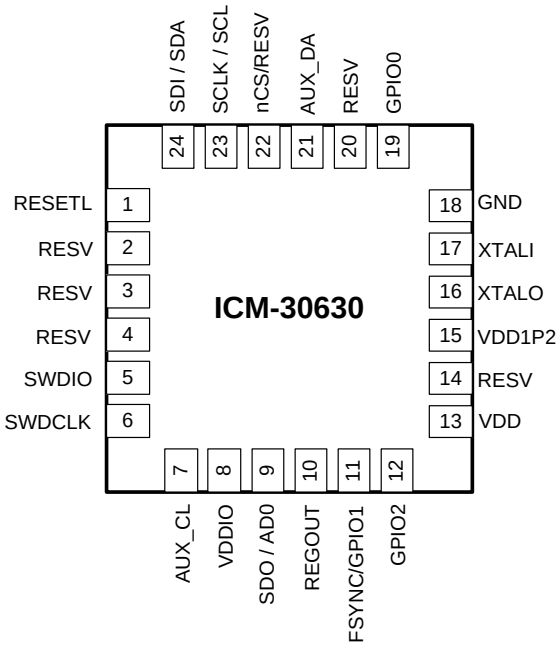


Figure 3. Pin out Diagram for ICM-30630 3x3x1mm LGA

4.2 TYPICAL OPERATING CIRCUIT

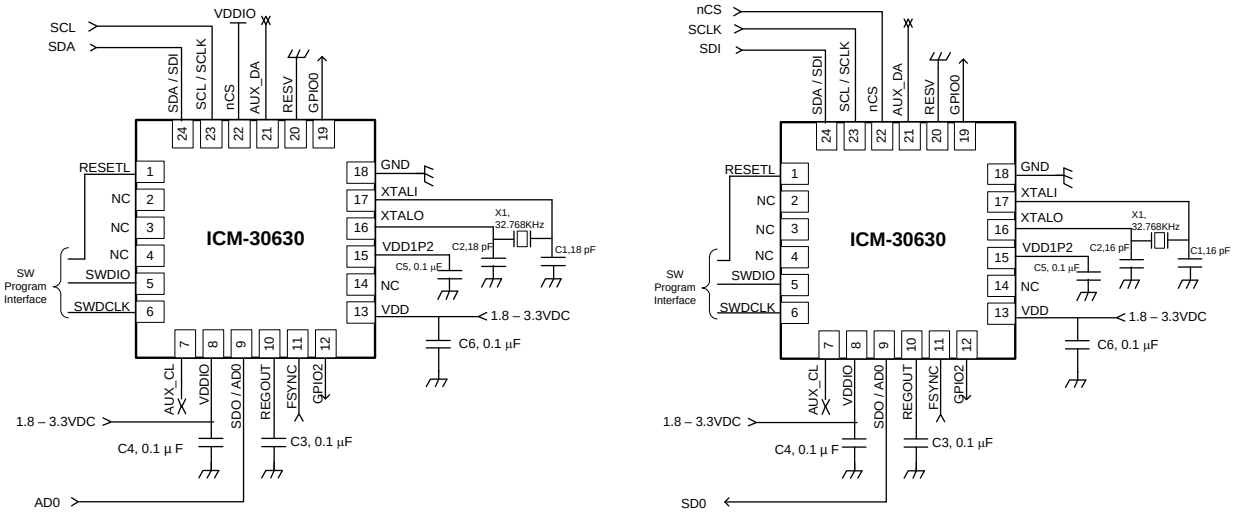


Figure 4. ICM-30630 Application Schematic (a) I2C operation (b) SPI operation

4.3 BILL OF MATERIALS FOR EXTERNAL COMPONENTS

COMPONENT	LABEL	SPECIFICATION	QUANTITY
Decoupling Capacitor	C3, C4, C5, C6	Ceramic, X7R, 0.1µF ±10%, 10V	4
Crystal Resonator Load Capacitor[1]	C1, C2	Ceramic, X7R, 18pF ±5%, 10V	2
Crystal Resonator	X1	Xtal, AH-32.768KDZF-T, or equiv	1

Table 9. Bill of Materials

Note 1:

Crystal Resonator Load Capacitor = 2 x ($C_{crystal}$ – 3.15pF - C_{pcb})

4.4 ICM-30630 BLOCK DIAGRAM

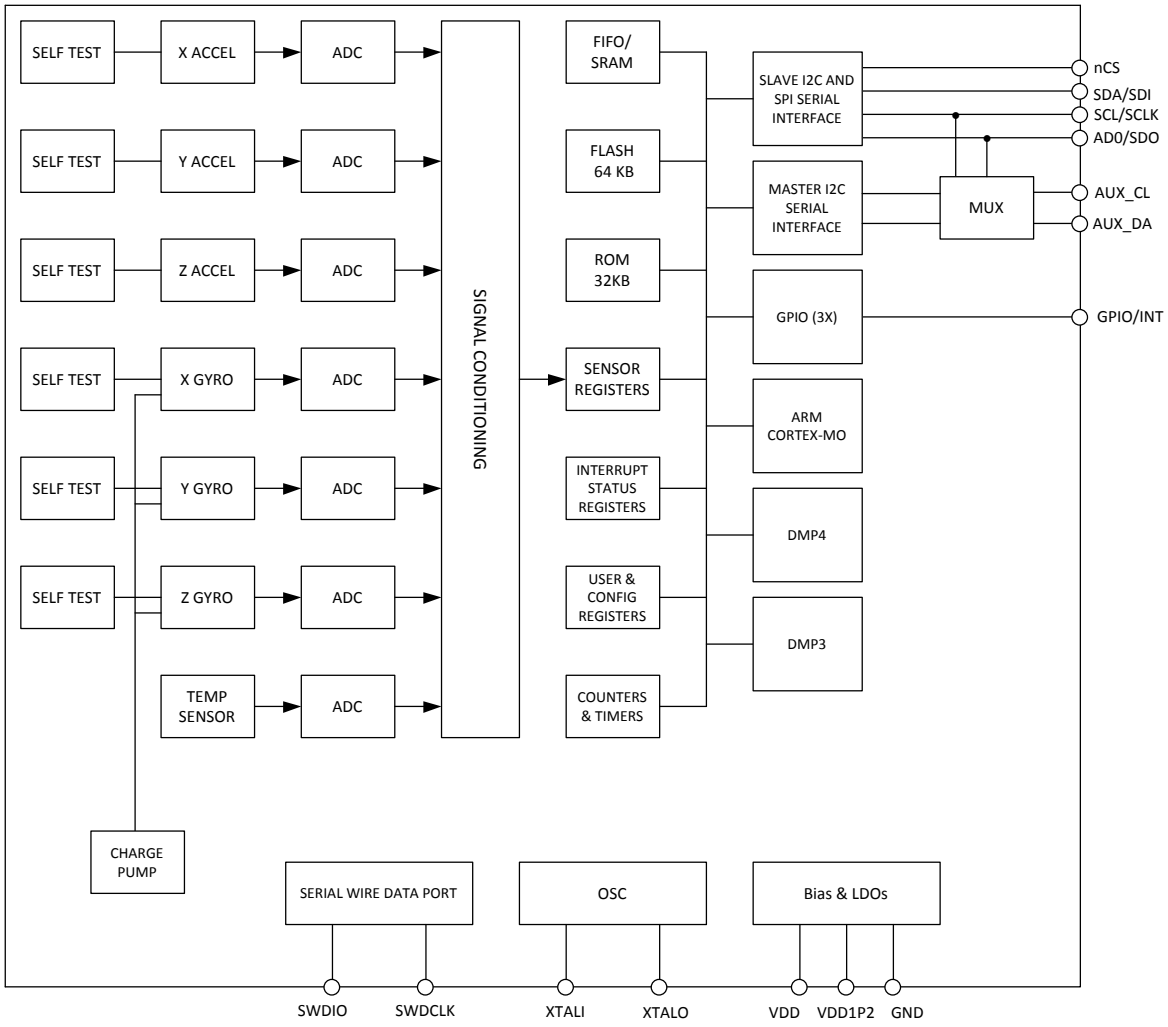


Figure 5. ICM-30630 Block Diagram

4.5 OVERVIEW

The ICM-30630 serves as a hub for collecting sensor data from sensors located on the ICM-30630 as wellas external 3rd party sensors. The device consists of the following key blocks and functions:

- Three-axis MEMS rate gyroscope sensor with 16-bit ADCs and signal conditioning
- Three-axis MEMS accelerometer sensor with 16-bit ADCs and signal conditioning
- ARM Cortex-M0 CPU
- Two Digital Motion Processor (DMP) engines
- Flash
- ROM
- SRAM
- FIFO
- 3 GPIOs
- DMA Controller
- Primary slave I^2C or slave SPI serial communications interfaces
- Auxiliary I^2C serial interface
- 4 Timers
- Serial Wire Data Port
- Self-Test
- Clocking
- Interrupts
- On-Chip Oscillators
- On-Chip Regulators
- Charge Pump
- Power Modes

4.6 THREE-AXIS MEMS GYROSCOPE WITH 16-BIT ADCS AND SIGNAL CONDITIONING

The ICM-30630 consists of three independent vibratory MEMS rate gyroscopes, which detect rotation about the X-, Y-, and Z- Axes. When the gyros are rotated about any of the sense axes, the Coriolis Effect causes a vibration that is detected by a capacitive pickoff. The resulting signal is amplified, demodulated, and filtered to produce a voltage that is proportional to the angular rate. This voltage is digitized using individual on-chip 16-bit Analog-to-Digital Converters (ADCs) to sample each axis. The full-scale range of the gyro sensors may be digitally programmed to ±250, ±500, ±1000, or ±2000 degrees per second (dps).

4.7 THREE-AXIS MEMS ACCELEROMETER WITH 16-BIT ADCS AND SIGNAL CONDITIONING

The ICM-30630's 3-Axis accelerometer uses separate proof masses for each axis. Acceleration along a particular axis induces displacement on the corresponding proof mass, and capacitive sensors detect the displacement differentially. The ICM-30630's architecture reduces the accelerometers' susceptibility to fabrication variations as well as to thermal drift. When the device is placed on a flat surface, it will measure 0*g* on the X- and Y-axes and +1*g* on the Z-axis. The accelerometers' scale factor is calibrated at the factory and is nominally independent of supply voltage. Each sensor has a dedicated sigma-delta ADC for providing digital outputs. The full scale range of the digital output can be adjusted to ±2*g*, ±4*g*, ±8*g*, or ±16*g*.

4.8 ARM CORTEX-M0 CPU

The ICM-30630 includes an ARM Cortex-M0 CPU. The CPU is a general purpose, 32-bit microprocessor that offers high performance at very low power consumption. It can operate at up to a maximum speed of 64MHz. The CPU uses Thumb-2® technology, providing a blend of 16/32-bit instructions that deliver a small code size. Due to its embedded ARM core, the ICM-30630 is compatible with ARM tools and software.

The CPU can be used to collect and process data from sensors that are included in the ICM-30630 as well as external sensors, so that the ICM-30630 can be used as a Sensor Hub. It enables the ICM-30630 to function as a sensor hub which is an open platform where developers can add their differentiated features.

4.9 DIGITAL MOTION PROCESSORS

The ICM-30630 includes 2 Digital Motion Processors (DMPs), a DMP3 and a DMP4. The DMPs together with the ARM Cortex-M0 CPU can offload computation of motion processing algorithms from the host processor. DMP3 is utilized for proven track record and quick deployment, benefiting from the existing code base. DMP4 is a higher functioning processor with specialties in fixed point processing and FFT generation. It is register based for power and flexibility.

4.10 FLASH

Flash Memory is partitioned into two memory blocks:

- A main memory block of 64K bytes that is available for user program.
- A second memory block is reserved for InvenSense use. It is programmed by InvenSense during device production. It contains information for optimizing device performance.

At startup, the ICM-30630 boots from the reserved section that was programmed by InvenSense. At the end of this step, the system boots from the main Flash that contains the user program.

4.11 SRAM

The ICM-30630 includes SRAM whose total size is 64K bytes. This SRAM space is shared among storage for ARM Cortex-M0, DMPs, and FIFO.

4.12 FIFO

The ICM-30630 contains a FIFO that is accessible via the SPI/I2C interfaces. The FIFO is used to keep a history of most recent sensors output, DMP or Cortex M0 results. The FIFO can be configured as a single FIFO or multiple FIFOs. The FIFO uses part of the SRAM, while the remainder of the SRAM is used by the M0, DMP, and as shared SRAM. FIFO size is variable depending on software configuration.

The FIFO can be written to by DMA, DMP, ARM Cortex-M0 and by the user through serial interface. It can be read through serial interface, DMP or ARM Cortex-M0. In multiple FIFO mode, up to 4 FIFOs are available and any number, ranging from 0-3 can be configured. There is no association of a FIFO to a particular sensor type, the DMP or the M0. DMP and M0 can read and write to all 4 FIFOs.

In multiple FIFO mode, each sensor output can be read from a separate FIFO. Separate sensors can control their FIFOs based on individual ODRs. Slower sensors (compass, barometer) do not need to update the FIFO at the same rate as faster sensors. This provides ease of use and more efficient use of FIFO space.

4.13 GPIO

The ICM-30630 supports 3 GPIO bidirectional pins that can be configured as general purpose input, general purpose output, interrupt input, or interrupt output.

4.14 DMA CONTROLLER

The DMA controller allows various types of data transfers without processor intervention.

4.15 PRIMARY SLAVE I2C OR SLAVE SPI SERIAL COMMUNICATIONS INTERFACES

The ICM-30630 communicates to a host application processor through either an I^2C or an SPI serial interface. The ICM-30630 always acts as a slave when communicating to the application processor. The I^2C and SPI slave interface can be used by the application processor to program the ICM-30630 or to read its on-chip memories. The following interface modes are supported:

- I2C Standard-Mode: Up to 80kHz
- I2C Fast-Mode: Up to 320kHz
- I2C Fast-Mode Plus: Up to 0.8MHz
- I2C High-Speed Mode: Up to 2.7MHz
- SPI Interface: Up to 6.4MHz

4.15.1 ICM-30630 Solution Using I2C Interface

In the figure below, the system processor is an I^2C master to the ICM-30630. In addition, the ICM-30630 is an I^2C master to the optional external compass sensor.

The ARM Cortex-M0 processor on ICM-30630 can be used to manage the initial configuration of any auxiliary sensors. Alternatively, the system processor can be used for initial configuration of auxiliary sensors. The ICM-30630 has an interface bypass multiplexer, which connects the system processor I^2C bus pins 23 and 24 (SDA and SCL) directly to the auxiliary sensor I^2C bus pins 6 and 7 (AUX_DA and AUX_CL). Once the auxiliary sensors have been configured by the system processor, the interface bypass multiplexer should be disabled so that the ICM-30630 auxiliary I^2C master can take control of the sensor I^2C bus and gather data from the auxiliary sensors.

For further information regarding I^2C master control, please refer to section 5.

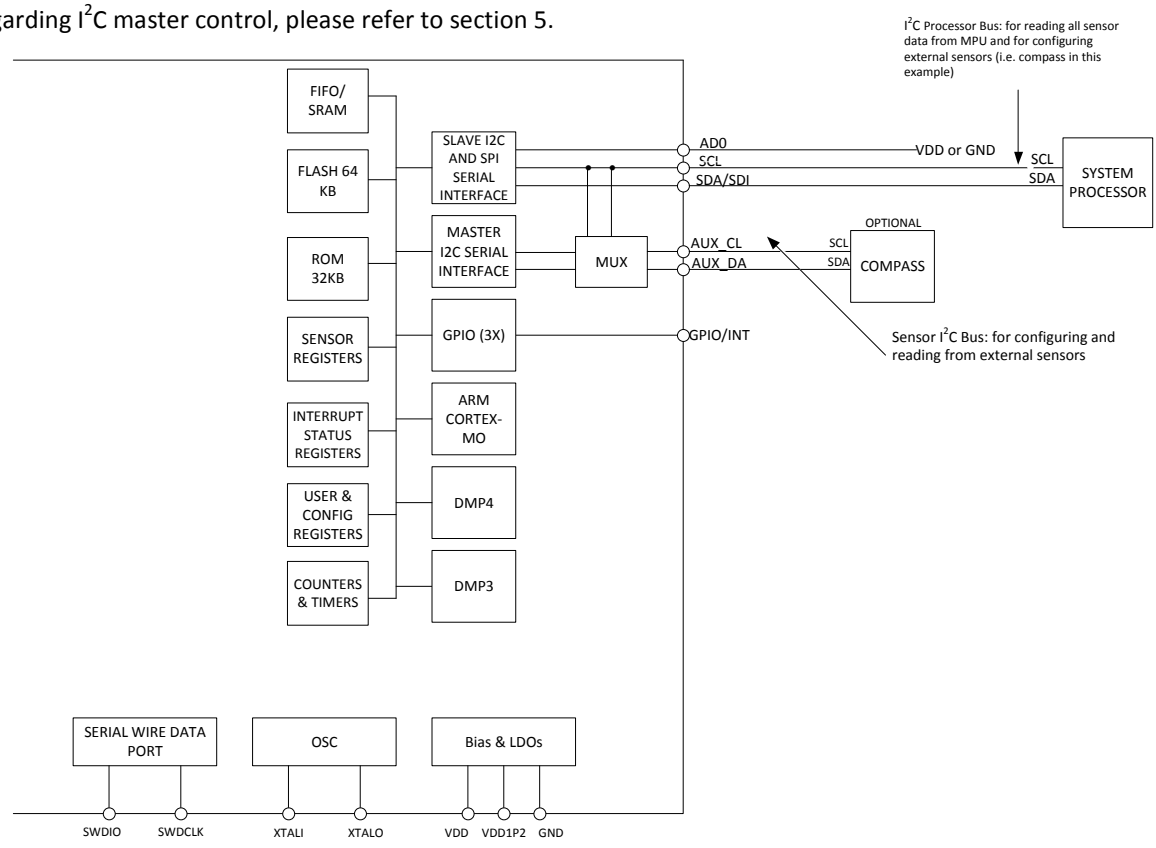


Figure 6 ICM-30630 Solution Using I^2C Interface

4.15.2 ICM-30630 Solution Using SPI Interface

In the figure below, the system processor is an SPI master to the ICM-30630. Pins 8, 9, 23, and 24 are used to support the CS, SDO, SCLK, and SDI signals for SPI communications. Because these SPI pins are shared with the I^{2}C slave pins, the system processor cannot access the auxiliary I^{2}C bus through the interface bypass multiplexer, which connects the processor I^{2}C interface pins to the sensor I^{2}C interface pins. The ARM Cortex-M0 can be used to manage the initial configuration of any auxiliary sensors. The alternative approach described in the previous section, of using the system processor to manage initial configuration of auxiliary sensors, cannot be used in this case.

Once the external sensors have been configured, the ICM-30630 can perform single or multi-byte reads using the sensor I^{2}C bus.

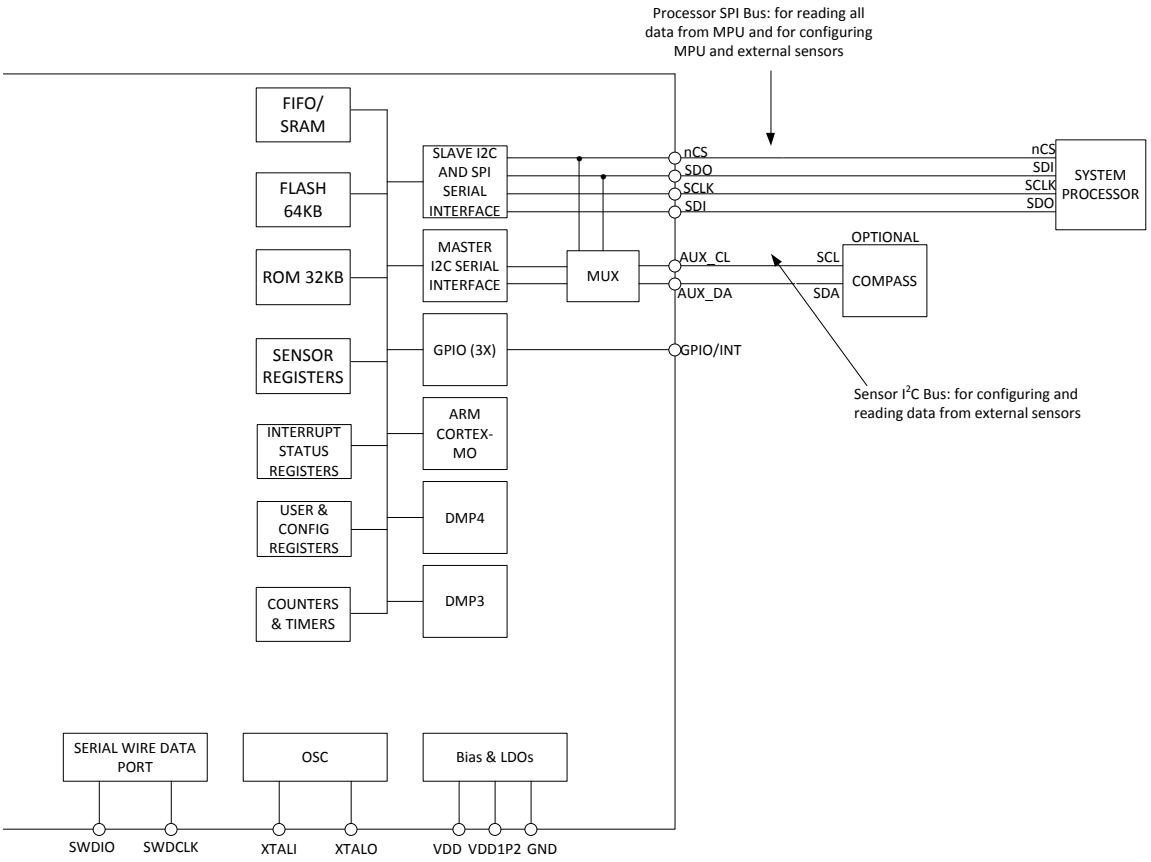


Figure 7. ICM-30630 Solution Using SPI Interface

4.16 AUXILIARY I2C SERIAL INTERFACE

The ICM-30630 has an auxiliary I^{2}C bus for communicating to an off-chip 3-Axis digital output magnetometer or other sensors. This bus has two operating modes:

- I^{2}C Master Mode: The ICM-30630 acts as a master to any external sensors connected to the auxiliary I^{2}C bus
- Pass-Through Mode: The ICM-30630 directly connects the primary and auxiliary I^{2}C buses together, allowing the system processor to directly communicate with any external sensors.

Auxiliary I^2C Bus Modes of Operation:

- I^2C Master Mode: Allows the ICM-30630 to directly access the data registers of external digital sensors, such as a magnetometer. In this mode, the ICM-30630 directly obtains data from auxiliary sensors without intervention from the system applications processor.

  For example, in I^2C Master mode, the ICM-30630 can be configured to perform burst reads, returning the following data from a magnetometer:
  - X magnetometer data (2 bytes)
  - Y magnetometer data (2 bytes)
  - Z magnetometer data (2 bytes)

- Pass-Through Mode: Allows an external system processor to act as master and directly communicate to the external sensors connected to the auxiliary I^2C bus pins (AUX_DA and AUX_CL). In this mode, the auxiliary I^2C bus control logic (3rd party sensor interface block) of the ICM-30630 is disabled, and the auxiliary I^2C pins AUX_DA and AUX_CL (Pins 6 and 7) are connected to the main I^2C bus through analog switches internally. Pass-Through mode is useful for configuring the external sensors.

4.17 TIMERS

The ICM-30630 includes four timers that can be used for timestamp, watchdog, and general purpose timer functions.

- **Timestamp Timer:** A 32-bit free running counter is used for time stamping. This timer runs on a 32kHz crystal.
- **Watchdog Timer:** This is a 32-bit timer that can be used as a watchdog timer for either the ARM Cortex-M0 or DMP4.
- **General Purpose Timers:** These are two general purpose 32-bit countdown timers used to generate interrupts.

4.18 SERIAL WIRE DATA PORT

The ICM-30630 includes a reduced pin-count debug interface, known as the Serial Wire Data Port. It provides the ability to debug and trace functionality on the ARM-M0 processor on the ICM-30630. The port consists of two pins:

- SWDIO: Serial Wire Debug Port – Data Signal
- SWDCLK: Serial Wire Debug Port – Clock Signal

4.19 INTERRUPTS

The ICM-30630 has a programmable interrupt system which can generate an interrupt signal on the 3 interrupt pins that are shared with GPIO. Status flags indicate the source of an interrupt. Interrupt sources may be enabled and disabled individually.
The following events can cause an interrupt:

- DMP or ARM Cortex M0 signals a Motion Detection interrupt to the application processor
- FIFO data ready interrupt
- FIFO watermark interrupt
- FIFO overflow
- Sensor data ready
- External FSYNC
- I2C slave interrupt
- I2C slave NACK or I2C master lost arbitration

External slaves can interrupt ICM-30630 through GPIOs configured as interrupt inputs. These are usually the I2CMST interrupt pins.

4.20 ON-CHIP OSCILLATORS

The ICM-30630 includes 3 on-chip oscillators:

- High frequency RC oscillator for system clock
- Low frequency RC oscillator for periodic wake up
- 32.768 KHz crystal oscillator for accurate time stamping functions
    - This oscillator also allows an external 32 KHz input

4.21 ON-CHIP REGULATORS

On-Chip Regulators generate the internal supply and the reference voltages and currents required by the ICM-30630. An external 1.2 volts supply pin is also provided and ICM-30630 can be configured through Flash to always use external 1.2 volts or on–chip regulators. ICM-30630 supports multiple power modes for different levels of power savings vs. startup time. In all modes the ICM-30630 can respond to the AP, gracefully suspend current state, and perform the AP's request.

4.22 CHARGE PUMP

An on-chip charge pump generates the high voltage required for the MEMS oscillators.

4.23 STANDARD POWER MODES

The ICM-30630 supports the following power modes:

- **Power Down Mode:** All digital circuitry is off, but analog POR is on and listening to external input to wake up the system on an interrupt. There is no data retention in this mode except for Flash.
- **Deep Sleep Mode:** ROM and Flash are powered off but the rest of the digital circuitry is on for data retention. RC oscillator is powered off.
- **Sleep Mode:** All digital circuitry is powered on and idle. RC oscillator is powered off.

In addition, the ICM-30630 supports active power modes with the following functionalities: 6-axis, Accelerometer only, Gyroscope only, ARM-M0 only, DMP4 only, DMP3 only.

In active power state the sensors and CPUs are either off or duty cycling. The chip can transition from active mode to any of the sleep modes, but not from one sleep mode to another.

The following table summarizes the state of the main elements of ICM-30630 in various power modes:

Note: The standard mode of gyroscope and accelerometer operation is duty-cycled

Mode	ARM-M0	DMP4	DMP3	Gyroscope	Accelerometer
Power Down	Off	Off	Off	Off	Off
Deep Sleep	Off	Off	Off	Off	Off
Sleep	Off	Off	Off	Off	Off
6-Axis	On or Duty-Cycled or Off	On or Duty-Cycled or Off	On or Duty-Cycled or Off	Low-Noise or Duty-Cycled	Low-Noise or Duty-Cycled
Accelerometer	On or Duty-Cycled or Off	On or Duty-Cycled or Off	On or Duty-Cycled or Off	Off	Low-Noise or Duty-Cycled
Gyroscope	On or Duty-Cycled or Off	On or Duty-Cycled or Off	On or Duty-Cycled or Off	Low-Noise or Duty-Cycled	Off
ARM-M0 Only	On	Off	Off	Off	Off
DMP4 Only	Off	On	Off	Off	Off
DMP3 Only	Off	Off	On	Off	Off

5 DIGITAL INTERFACE

5.1 I2C AND SPI SERIAL INTERFACES

The ICM-30630 can be accessed using either I^2C at up to 2.7MHz or SPI at up to 6.4MHz. SPI operates in four-wire mode.

PIN NUMBER	PIN NAME	PIN DESCRIPTION
9	SDO/AD0	I^2C Slave Address LSB (AD0); SPI serial data output (SDO)
22	nCS/RESV	SPI slave chip select (SPI host interface mode); Tie High (I^2C host interface mode)
23	SCLK/SCL	I^2C serial clock (SCL); SPI serial clock (SCLK)
24	SDI/SDA	I^2C serial data (SDA); SPI serial data input (SDI)

Table 10. Serial Interface

5.2 I2C INTERFACE

I^2C is a two-wire interface comprised of the signals serial data (SDA) and serial clock (SCL). In general, the lines are open-drain and bi-directional. In a generalized I^2C interface implementation, attached devices can be a master or a slave. The master device puts the slave address on the bus, and the slave device with the matching address acknowledges the master.

The ICM-30630 always operates as a slave device when communicating to the system processor, which thus acts as the master. SDA and SCL lines typically need pull-up resistors to VDDIO.

The slave address of the ICM-30630 is b110100X which is 7 bits long. The LSB bit of the 7 bit address is determined by the logic level on pin AD0. This allows two ICM-30630s to be connected to the same I^2C bus. When used in this configuration, the address of the one of the devices should be b1101010 (pin AD0 is logic low) and the address of the other should be b1101011 (pin AD0 is logic high).

5.3 I2C COMMUNICATIONS PROTOCOL

START (S) and STOP (P) Conditions

Communication on the I^2C bus starts when the master puts the START condition (S) on the bus, which is defined as a HIGH-to-LOW transition of the SDA line while SCL line is HIGH (see figure below). The bus is considered to be busy until the master puts a STOP condition (P) on the bus, which is defined as a LOW to HIGH transition on the SDA line while SCL is HIGH (see figure below). Additionally, the bus remains busy if a repeated START (Sr) is generated instead of a STOP condition.

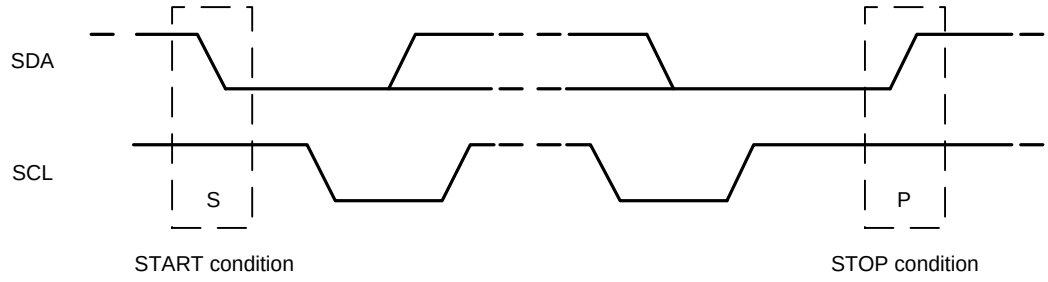


Figure 8. START and STOP Conditions

Data Format / Acknowledge

I^2C data bytes are defined to be 8-bits long. There is no restriction to the number of bytes transmitted per data transfer. Each byte transferred must be followed by an acknowledge (ACK) signal. The clock for the acknowledge signal is generated by the master, while the receiver generates the actual acknowledge signal by pulling down SDA and holding it low during the HIGH portion of the acknowledge clock pulse.

If a slave is busy and cannot transmit or receive another byte of data until some other task has been performed, it can hold SCL LOW, thus forcing the master into a wait state. Normal data transfer resumes when the slave is ready, and releases the clock line (refer to the following figure).

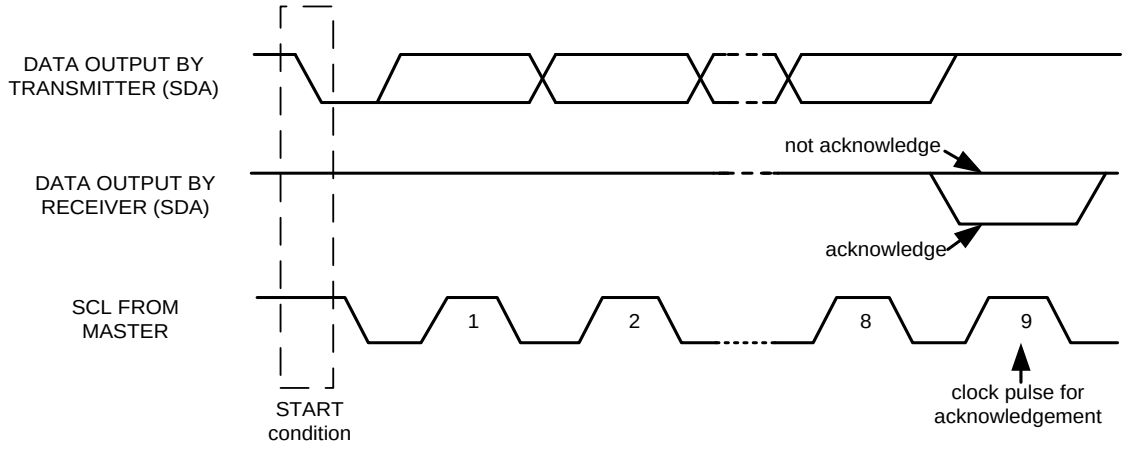


Figure 9. Acknowledge on the I^2C Bus

Communications

After beginning communications with the START condition (S), the master sends a 7-bit slave address followed by an 8th bit, the read/write bit. The read/write bit indicates whether the master is receiving data from or is writing to the slave device. Then, the master releases the SDA line and waits for the acknowledge signal (ACK) from the slave device. Each byte transferred must be followed by an acknowledge bit. To acknowledge, the slave device pulls the SDA line LOW and keeps it LOW for the high period of the SCL line. Data transmission is always terminated by the master with a STOP condition (P), thus freeing the communications line. However, the master can generate a repeated START condition (Sr), and address another slave without first generating a STOP condition (P). A LOW to HIGH transition on the SDA line while SCL is HIGH defines the stop condition. All SDA changes should take place when SCL is low, with the exception of start and stop conditions.

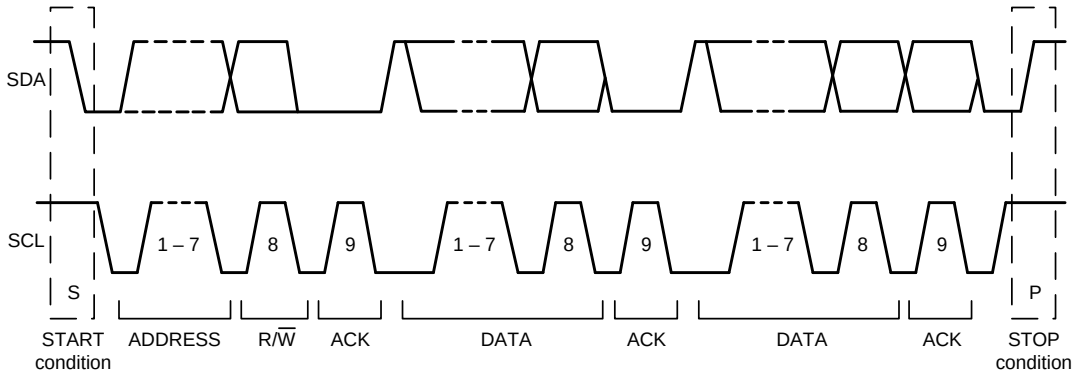


Figure 10. Complete I²C Data Transfer

5.4 I²C TERMS

SIGNAL	DESCRIPTION
S	Start Condition: SDA goes from high to low while SCL is high
AD	Slave I²C address
W	Write bit (0)
R	Read bit (1)
ACK	Acknowledge: SDA line is low while the SCL line is high at the 9th clock cycle
NACK	Not-Acknowledge: SDA line stays high at the 9th clock cycle
DATA	Transmit or received data
P	Stop condition: SDA going from low to high while SCL is high

Table 11 I²C Terms

5.5 SPI INTERFACE

SPI is a 4-wire synchronous serial interface that uses two control lines and two data lines. The ICM-30630 always operates as a Slave device during standard Master-Slave SPI operation.

With respect to the Master, the Serial Clock output (SCLK), the Serial Data Output (SDO) and the Serial Data Input (SDI) are shared among the Slave devices. Each SPI slave device requires its own Chip Select (CS) line from the master.
CS goes low (active) at the start of transmission and goes back high (inactive) at the end. Only one CS line is active at a time, ensuring that only one slave is selected at any given time. The CS lines of the non-selected slave devices are held high, causing their SDO lines to remain in a high-impedance (high-z) state so that they do not interfere with any active devices.

SPI Operational Features

1. Data is delivered MSB first and LSB last
2. Data is latched on the rising edge of SCLK
3. Data should be transitioned on the falling edge of SCLK
4. The maximum frequency of SCLK is 6.4MHz
5. SPI read and write operations are completed in 16 or more clock cycles (two or more bytes). The first byte contains the SPI Address, and the following byte(s) contain(s) the SPI data. The first bit of the first byte contains the Read/Write bit and indicates the Read (1) or Write (0) operation. The following 7 bits contain the Register Address. In cases of multiple-byte Read/Writes, data is two or more bytes:

SPI Address format

MSB							**LSB**
R/W	A6	A5	A4	A3	A2	A1	A0

SPI Data format

MSB							**LSB**
D7	D6	D5	D4	D3	D2	D1	D0

6. Supports Single or Burst Read/Writes.

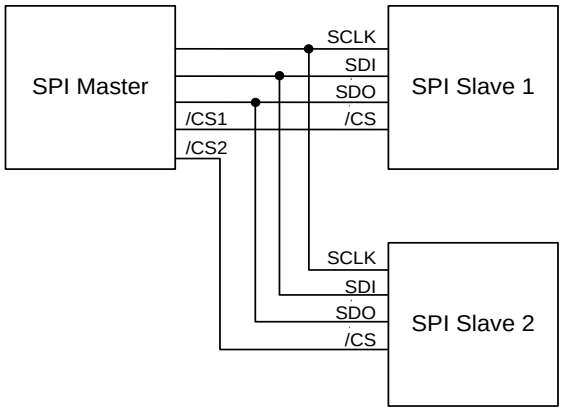


Figure 11. Typical SPI Master / Slave Configuration

6 SERIAL INTERFACE CONSIDERATIONS

6.1 ICM-30630 SUPPORTED INTERFACES

The ICM-30630 supports I^2C communications on both its primary (microprocessor) serial interface and its auxiliary interface..
The ICM-30630's I/O logic levels are set to be VDDIO.

The figure below depicts a sample circuit of ICM-30630 with a third party magnetometer attached to the auxiliary I^2C bus. It shows the relevant logic levels and voltage connections.

Note: Actual configuration will depend on the auxiliary sensors used.

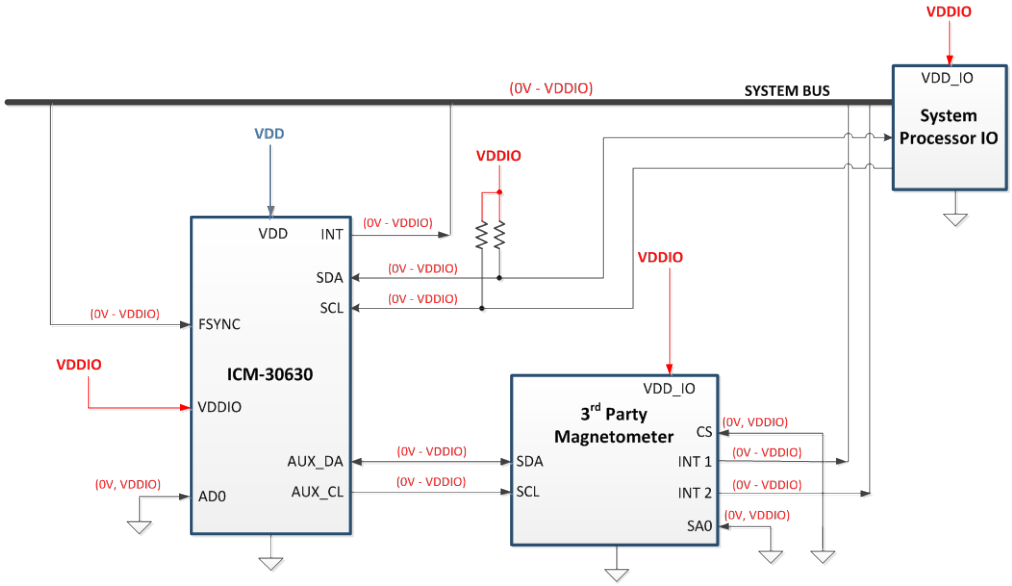


Figure 12. I/O Levels and Connections

7 USE NOTES

7.1 I2C PROGRAM LENGTH

I2C programs should be restricted to MAX 30 bytes length.

8 ORIENTATION OF AXES

The diagram below shows the orientation of the axes of sensitivity and the polarity of rotation. Note the pin 1 identifier (•) in the figure.

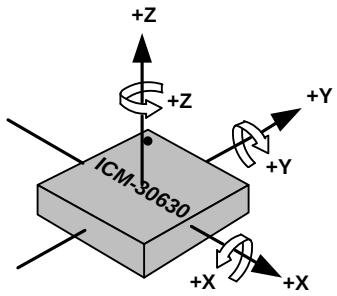
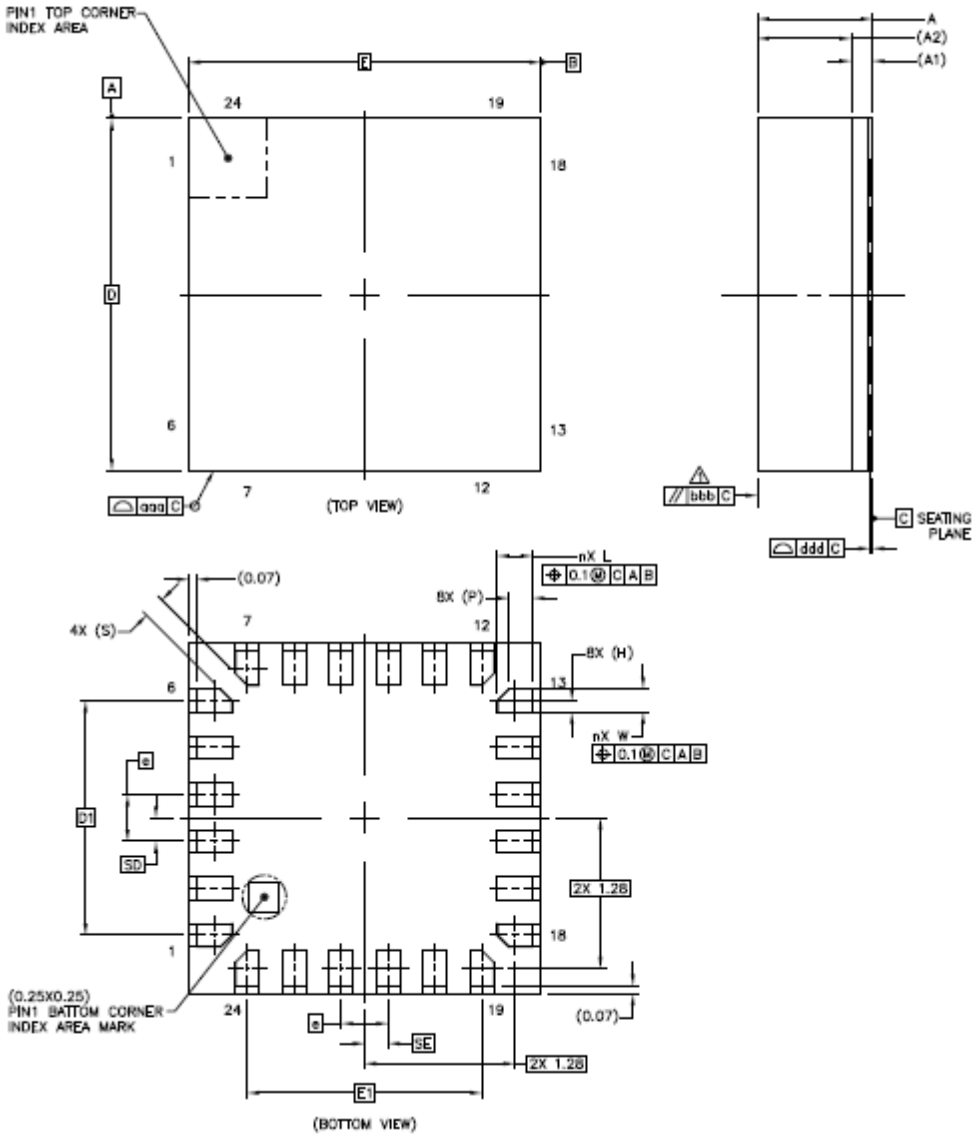


Figure 13 Orientation of Axes of Sensitivity and Polarity of Rotation

9 PACKAGE DIMENSIONS

This section provides package dimensions for the ICM-30630.

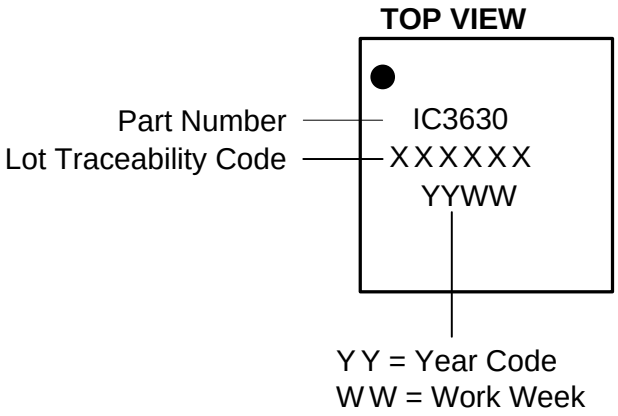


	Symbol	Common Dimensions		
		MIN.	NOM.	MAX.
Total Thickness	A	0.91	0.98	1.05
Substrate Thickness	A1		0.18	REF
Mold Thickness	A2		0.8	REF
Body Size	D	2.9	3	3.1
	E	2.9	3	3.1
Lead Width	W	0.15	0.2	0.25
Lead Length	L	0.25	0.3	0.35
Lead Pitch	e		0.4	BSC
Lead Count	n		24	
Edge Ball Center to Center	D1		2	BSC
	E1		2	BSC
Body Center to Contact Ball	SD		0.2	BSC
	SE		0.2	BSC
Ball Width	b	---	---	---
Ball Diameter			---	
Ball Opening			---	
Ball Pitch	e1		---	
Ball Count	n1		---	
Pre-Solder		---	---	---
Package Edge Tolerance	aaa		0.1	
Mold Flatness	bbb		0.2	
Coplanarity	ddd		0.08	
Ball Offset (Package)	eee		---	
Ball Offset (Ball)	fff		---	
Corner Lead Width	H		0.1	REF
Corner Lead Length	P		0.2	REF
Corner Lead to Lead Space	S		0.184	REF

10 PART NUMBER PART MARKINGS

The part number part markings for ICM-30630 devices are summarized below:

PART NUMBER	PART NUMBER PART MARKING
ICM-30630	IC3630



11 RELIABILITY

11.1 QUALIFICATION TEST POLICY

InvenSense's products complete a Qualification Test Plan before being released to production. The Qualification Test Plan for the ICM-30630 followed the JESD47I Standards, "Stress-Test-Driven Qualification of Integrated Circuits," with the individual tests described below.

11.2 QUALIFICATION TEST PLAN

Accelerated Life Tests

TEST	Method/Condition	Lot Quantity	Sample / Lot	Acc / Reject Criteria
(HTOL/LFR) High Temperature Operating Life	JEDEC JESD22-A108D, Dynamic, 3.63V biased, Tj>125°C [read-points 168, 500, 1000 hours]	3	77	(0/1)
(HAST) Highly Accelerated Stress Test (1)	JEDEC JESD22-A118A Condition A, 130°C, 85%RH, 33.3 psia., unbiased, [read-point 96 hours]	3	77	(0/1)
(HTS) High Temperature Storage Life	JEDEC JESD22-A103D, Cond. A, 125°C Non-Bias Bake [read-points 168, 500, 1000 hours]	3	77	(0/1)

Device Component Level Tests

TEST	Method/Condition	Lot Quantity	Sample / Lot	Acc / Reject Criteria
(ESD-HBM) ESD-Human Body Model	JEDEC JS-001-2012, (2.0 KV)	1	3	(0/1)
(ESD-MM) ESD-Machine Model	JEDEC JESD22-A115C, (250V)	1	3	(0/1)
(LU) Latch Up	JEDEC JESD-78D Class II (2), 125°C; ±100mA	1	6	(0/1)
(MS) Mechanical Shock	JEDEC JESD22-B104C, Mil-Std-883, Method 2002.5, Cond. E, 10,000*g's*, 0.2ms, ±X, Y, Z – 6 directions, 5 times/direction	3	5	(0/1)
(VIB) Vibration	JEDEC JESD22-B103B, Variable Frequency (random), Cond. B, 5-500Hz, X, Y, Z – 4 times/direction	3	5	(0/1)
(TC) Temperature Cycling (1)	JEDEC JESD22-A104D Condition G [-40°C to +125°C], Soak Mode 2 [5'], 1000 cycles	3	77	(0/1)

(1) Tests are preceded by MSL3 Preconditioning in accordance with JEDEC JESD22-A113F

12 REFERENCES

Please refer to “InvenSense MEMS Handling Application Note (AN-IVS-0002A-00)” for the following information:

- Manufacturing Recommendations
  - Assembly Guidelines and Recommendations
  - PCB Design Guidelines and Recommendations
  - MEMS Handling Instructions
  - ESD Considerations
  - Reflow Specification
  - Storage Specifications
  - Package Marking Specification
  - Tape & Reel Specification
  - Reel & Pizza Box Label
  - Packaging
  - Representative Shipping Carton Label
- Compliance
  - Environmental Compliance
  - DRC Compliance
  - Compliance Declaration Disclaimer

13 DOCUMENT INFORMATION

13.1 REVISION HISTORY

REVISION DATE	REV NUMBER	DESCRIPTION
11/19/2014	1.0	Initial Release

COMPLIANCE DECLARATION DISCLAIMER

InvenSense believes the environmental and other compliance information given in this document to be correct but cannot guarantee accuracy or completeness. Conformity documents substantiating the specifications and component characteristics are on file. InvenSense subcontracts manufacturing and the information contained herein is based on data received from vendors and suppliers, which has not been validated by InvenSense.

InvenSense

©2014 InvenSense, Inc. All rights reserved.

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

- View ICM-30630 on WIN SOURCE
- TDK InvenSense Information

Optimize Your Supply Chain with WIN SOURCE Solutions

- Global Sourcing Solution
- Obsolete Management
- Cost Control Management
- Shortage Management
- Alternative Solution
- Excess Inventory Management