THE DATASHEET OF

MP5515GU-Z

MP5515

Wide Input 2.7 - 18V, 5A, High-Efficiency Bidirectional, Power Back-Up Manager with Integrated Hot-Swap, I²C, ADC, and Cap Health Test

The Future of Analog IC Technology

DESCRIPTION

The MP5515 is an input power conditioning PMIC targeting enterprise solid-state drives, NVDIMM, and other applications with back-up system requirements. The MP5515 consists of input current limiting, input reverse current blocking, and an MPS-patented, high-efficiency, bidirectional, boost-buck converter with only one inductor for energy storage and system back-up power when there is an input power failure. The MP5515 also provides I²C interface and ADC. By using the I²C, users can set the input current limit, slew rate, and perform cap health tests. The MP5515 can also monitor system status, such as input voltage, input current, storage voltage, temperature, and provide interrupt options for these features.

The internal input current-limit block prevents inrush current during system start-up while the reverse-current block prevents backup energy from flowing to the failing VIN port. MPS's patented energy storage and release management control circuit minimizes the storage capacitor requirement. It pumps the input voltage to a higher backup voltage and releases the energy over a hold-up time to the system bus voltage in case of an input outage.

The MP5515 requires a minimal number of standard, external components and is available in a 30-pin QFN (5mmx5mm) package.

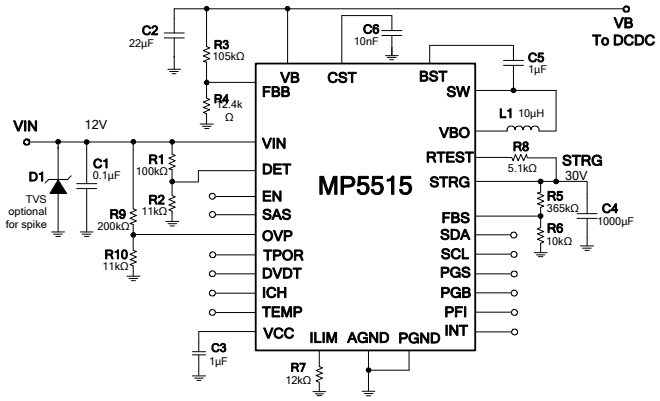
FEATURES

- Wide 2.7V-to-18V Operating Input Range
- Up to 32V Programmable Storage Voltage
- Up to 6A Programmable Input Current Limit
- 5A Buck Load Capability
- Adjustable Slew Rate for VB Voltage Rising
- Input Current Limiter with Integrated 14mΩ MOSFET
- Input Over-Voltage Protection (OVP)
- Reverse-Current Protection (RCP)
- Input Power Failure Indicator
- Backup Capacitor Health Test
- Comprehensive Voltage, Current, Temperature Sensor ADC Conversion
- Thermal Protection
- Available in a QFN-30 (5mmx5mm) Package

APPLICATIONS

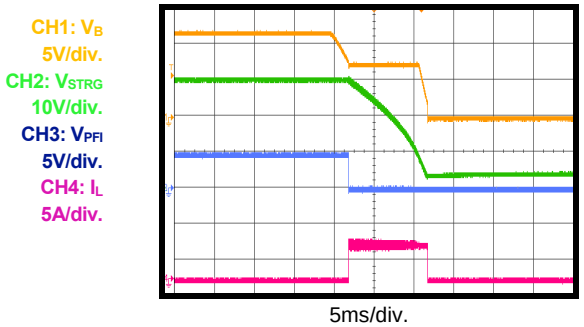
- Solid-State Drives (SSD)
- NVDIMMs
- Hard-Disk Drives
- Power Back-Up Systems

TYPICAL APPLICATION



V_{STRG} Release

V_{IN} = 12V, V_B = 7.5V, VB load = 5A



ORDERING INFORMATION

Part Number	Package	Top Marking
MP5515GU*	QFN-30 (5mmx5mm)	*See Below*
EVKT-5515	Evaluation Kit	

* For Tape & Reel, add suffix –Z (e.g. MP5515GU–Z)

TOP MARKING

MPSYYWW
MP5515
LLLLLLL

MPS: MPS prefix
YY: Year code
WW: Week code
MP5515: Product code of MP5515GU
LLLLLLL: Lot number

EVALUATION KIT EVKT-5515

EVKT-5515 Kit contents: (Items can be ordered separately).

#	Part Number	Item	Quantity
1	EV5515-U-00A	MP5515GU evaluation board	1
2	EVKT-USBI2C-02	Includes one USB to I2C dongle, one USB cable, and one ribbon cable	1
3	Tdrive-5515	USB flash drive that stores the GUI installation file and supplement documents	1

Order direct from MonolithicPower.com or our distributors.

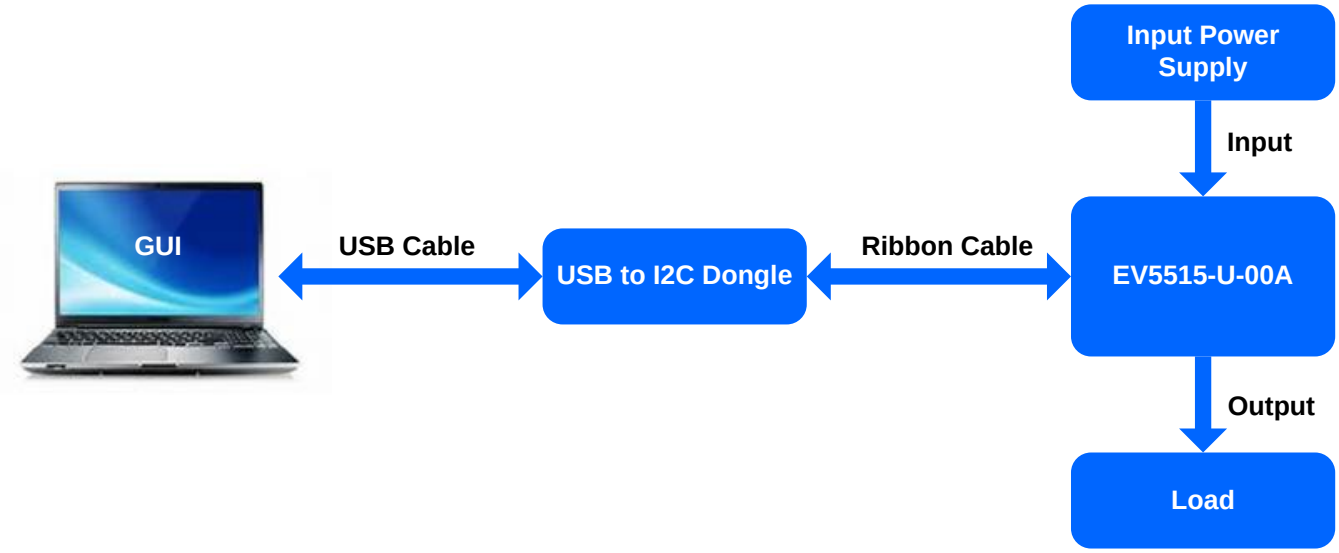
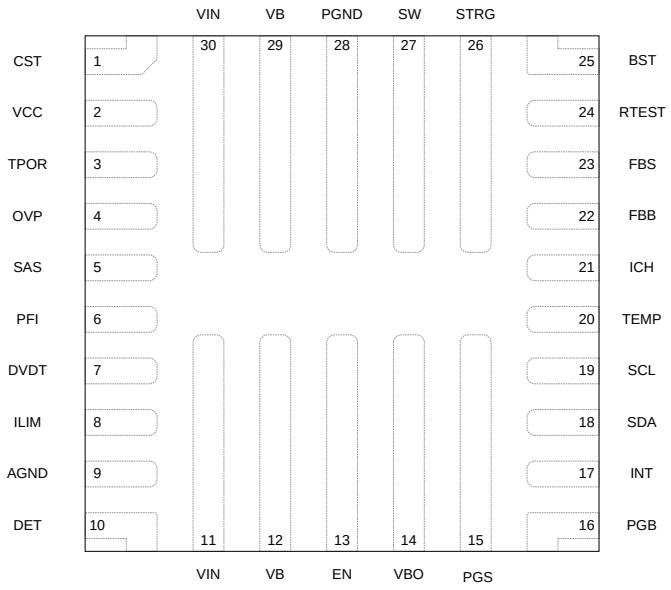


Figure 1: EVKT-5515 Evaluation Kit Set-Up

PACKAGE REFERENCE

TOP VIEW



QFN-30 (5mmx5mm)

ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN}) 21V
V_B, V_{BO} .....-0.3V to 21V
V_{STRG}, V_{RTEST} .....-0.3V to 36V
V_{SW}.....-0.3V (-6V for <10ns) to V_{STRG} + 0.3V
V_{BST} .....-0.3V to V_{STRG} + 6V
V_{CST} .....-0.3V to 28V
All other pins .....-0.3V to 6V
EN current.....1mA (2)
PFI, PGB, PGS, INT current 5mA (3)
RTEST current.....500mA (3)
Continuous power dissipation (T_A =+25°C) (4) (7)
..... 3.57W
Junction temperature .....150°C
Lead temperature .....260°C
Storage temperature..... -65°C to +150°C

Recommended Operating Conditions (5)

Supply voltage (V_{IN}) ..... 2.7V (6) to 18V
Bus voltage (V_B).....2.6V to 16V
Storage voltage (V_{STRG}).....V_{IN_MAX} + 3V to 32V
Max input current 6A
Max buck-release current 5A
EN current.....0.5mA (2)
Operating junction temp. (T_J)... -40°C to +125°C

Thermal Resistance θ_{JA} θ_{JC}

QFN-30 (5mmx5mm)			
EV5515-U-00A (7)	35	6.5	°C/W
JESD51-7 (8)	36	8	°C/W

NOTES:

1) Exceeding these ratings may damage the device.
2) For more detail, refer to the Enable Control section on page 22.
3) When these pins are pulled up to the power source, the current should be limited below the maximum value.
4) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
5) The device is not guaranteed to function outside of its operating conditions.
6) Guaranteed for temperature conditions 25°C or higher. If the temperature is lower than 25°C, one Schottky diode from VIN to VCC is recommended to help start-up from a 2.7V input.
7) Measured on EV5515-U-00A, 2-layer 63mmx63mm PCB.
8) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, V_{EN} = 2V, T_J = -40°C to 125°C (9), typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Power Supply						
Supply current (shutdown)	I_S	EN = 0V, then power on VIN, T_J = 25°C		2.5	5	μA
Supply current (quiescent)	I_Q	SAS = 2V, EN = 2V, $V_{FBB/FBS/DET}$ = 1.1V		1.5		mA
		SAS = 0V, EN = 2V, $V_{FBB/FBS/DET}$ = 1.1V		2.5	3	mA
VCC regulator	V_{CC}	VIN or VB = 6V, Ivcc = 1mA	4.75	5	5.25	V
VIN under-voltage lockout threshold rising (10)	$INUV_R$	VCC floating, T_J = 25°C		2.5	2.68	V
VIN under-voltage lockout threshold hysteresis	$INUV_{HYS}$			0.1		V
VIN to VB current limit MOSFET on resistance	R_{DSON}			14		mΩ
VIN to VB continuous current limit	I_{LIM}	R_{ILIM} = 36.5kΩ, T_J = 25°C	1.92	2	2.08	A
		R_{ILIM} = 36.5kΩ, T_J = -40°C to 125°C	1.88	2	2.12	A
Off state leakage current	I_{LEAK}	V_{IN} = 12V, V_B = 0V or V_B = 12V, V_{IN} = 0V, T_J = 25°C		2	3	μA
VB clamping voltage	V_{CLAMP}	V_{IN} = 18V	15.2	16	16.8	V
VB rise time (DVDT) control (11)	T_{DVDT}	DVDT floating, VIN = 12V, DVDT bits = 00, test VB rise time		1.6		ms
	I_{DVDT}	Connect capacitor to DVDT, test DVDT charge current		3		μA
Internal reset delay-time control	T_{DLY}	TPOR floating, test reset delay time		1.5		ms
	I_{TPOR}	Connect capacitor to TPOR, test TPOR charge current		1		μA
Energy Storage and Release						
Storage pre-charge current	I_{CH-PRE}		250	350	450	mA
Boost disconnect switch R_{ON}	R_{dison}			30		mΩ
Switching peak current @ boost mode	I_{CH}	ICH floating, L = 10μH		2		A
		R_{ICH} = 200kΩ, L = 10μH		0.65		A
Energy management HS R_{ON}	R_{Hon}			80		mΩ
Energy management LS R_{ON}	R_{Lon}			40		mΩ
Feedback voltage	$V_{FBB-REF}$, $V_{FBS-REF}$, $V_{DET-REF}$	T_J = 25°C	0.792	0.8	0.808	V
		T_J = -40°C to 125°C	0.786		0.812	
Feedback current	I_{FBB}, I_{FBS}, I_{DET}	V_{FBB} = V_{FBS} = V_{DET} = 0.85V		10	50	nA

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{EN} = 2V, T_J = -40°C to 125°C (9), typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
VIN over-voltage threshold	V_{OVP}	OVP pin voltage rising		0.81		V
VIN over-voltage hysteresis	$V_{OVP-HYS}$	OVP pin voltage hysteresis		45		mV
Vs over-voltage threshold	V_{S-OVP}			1.1		$V_{FBS-REF}$
VIN to VB ISOFET turn-on voltage		VIN - VB, VB = 5V, then start VIN		0.2		V
VIN to VB ISOFET shut-down current	$I_{IN-VB-OFF}$	PFI = low		-250	0	mA
PFI high threshold	PFI_H			1.02		$V_{DET-REF}$
PFI low threshold	PFI_L			0.99		$V_{DET-REF}$
PFI falling delay	PFI_{D-L}			0.5		µs
PFI rising delay	PFI_{D-H}			200		µs
PFI sink current capability	V_{PFI}	Sink 4mA			0.3	V
PGB high threshold	PG_{H-VB}			0.95		$V_{FBB-REF}$
PGB low threshold	PG_{L-VB}			0.9		$V_{FBB-REF}$
PGB delay	PG_{D-VB}	Rising and falling edge		5		µs
PGB sink-current capability	V_{PG-VB}	Sink 4mA			0.3	V
PGS high threshold	PG_{H-S}	PGS threshold bits = 1111		0.97		$V_{FBS-REF}$
PGS low threshold	PG_{L-S}	PGS threshold bits = 1111		0.95		$V_{FBS-REF}$
PGS delay	PGS_{D-S}	Rising and falling edge		25		µs
PGS sink-current capability	V_{PG-S}	Sink 4mA			0.3	V
Buck-mode dumping valley current limit	$I_{DUMP-VALLEY}$		5	6.5		A
Release-buck switching frequency	f_{s-RLS}	V_{STRG} from 32V to 10V, buck_Fsw bits = 100	380	480	580	kHz
VB under-voltage lockout threshold rising (10)	$INUVB_R$		2.2	2.35	2.5	V
VB under-voltage lockout threshold hysteresis (10)	$INUVB_{HYS}$			0.1		V
ADC						
Voltage range			0		1.28	V
ADC resolution (12)				10		bits
ADC conversion time (12)		ADC conversion for one data		45		µs

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{EN} = 2V, T_J = -40°C to 125°C (9), typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Logic Interface (SDA, SCL, INT, SAS, EN)						
High-level input voltage	V_{IH}	SDA, SCL, SAS, EN	1.2			V
Low-level input voltage	V_{IL}	SDA, SCL, SAS, EN			0.4	V
Low-level output voltage	V_{OL}	Sink 4mA, SDA, INT			0.3	V
Input leakage current	I_{LKG}	Connected to 6V, SCL		10		nA
High level output leakage		Open drain, connected to 6V, SDA		10		nA
Protection						
Thermal shutdown, forced backup (12)	T_{SD}			150		°C
Thermal shutdown, forced backup hysteresis (12)	T_{HYS}			25		°C
Thermal warning (12)	T_{WRN}			120		°C

NOTES:

9) Guaranteed by over-temperature correlation, not tested in production.
10) VIN UVLO controls the IC start-up voltage threshold. VB UVLO controls energy storage and release circuitry. The internal VCC is powered from both VIN and VB. If either VIN or VB is higher than UVLO, the IC will not shut down.
11) Refer to the “Power-On Reset Delay and VB Rising Control” section on page 19 for detailed calculations.
12) Guaranteed by characterization, not tested in production.

I²C PORT SIGNAL CHARACTERISTICS

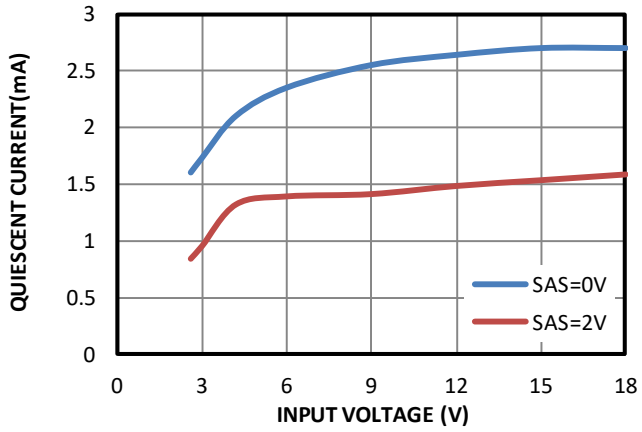
Parameter	Symbol	Condition	Cb = 100pF		Cb = 400pF		Units
			Min	Max	Min	Max	
SCLH and SCL clock frequency	f_{SCHL}		0	3.4	0	0.4	MHz
Set-up time for a repeated start condition	$T_{SU;STA}$		160	-	600	-	ns
Hold-time (repeated) start condition	$T_{HD;STA}$		160	-	600	-	ns
Low period of the SCL clock	T_{LOW}		160	-	1300	-	ns
High period of the SCL clock	t_{HIGH}		60	-	600	-	ns
Data set-up time	$T_{SU:DAT}$		10	-	100	-	ns
Data hold time	$T_{HD;DAT}$		0	70	0	-	ns
Rise time of SCLH signal	T_{rCL}		10	40	20*0.1Cb	300	ns
Rise time of SCLH signal after a repeated start condition and after an acknowledge bit	T_{fCL1}		10	80	20*0.1Cb	300	ns
Fall time of SCLH signal	T_{fCL}		10	40	20*0.1Cb	300	ns
Rise time of SDAH signal	T_{rDA}		10	80	20*0.1Cb	300	ns
Fall time of SDAH signal	T_{fDA}		10	80	20*0.1Cb	300	ns
Set-up time for stop condition	$T_{SU;STO}$		160	-	600	-	ns
Bus free time between a stop and start condition	T_{BUF}		160	-	1300	-	ns
Data valid time	$T_{VD;DAT}$		-	16	-	90	ns
Data valid acknowledge time	$T_{VD;ACK}$		-	160	-	900	ns
Pulse width of spikes that must be suppressed by the input filter	t_{SP}		0	10	0	50	ns
Capacitive load for each bus line	C_b	SDAH and SCLH line	-	100	-	400	pF
		SDAH + SDA line and SCLH + SCL line	-	400	-	400	pF

TYPICAL CHARACTERISTICS

V_{IN} = 12V, VB_{RLS} = 7.5V, L = 10µH, T_A = 25°C, unless otherwise noted.

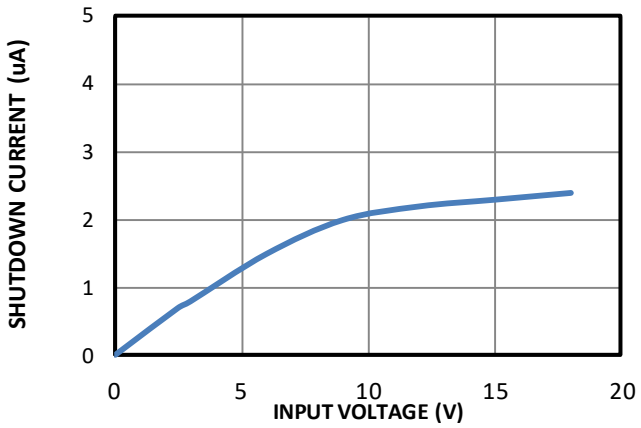
Quiescent Current vs. Input Voltage

EN=high,V_{FBB}=V_{DET}=V_{FBS}=1V

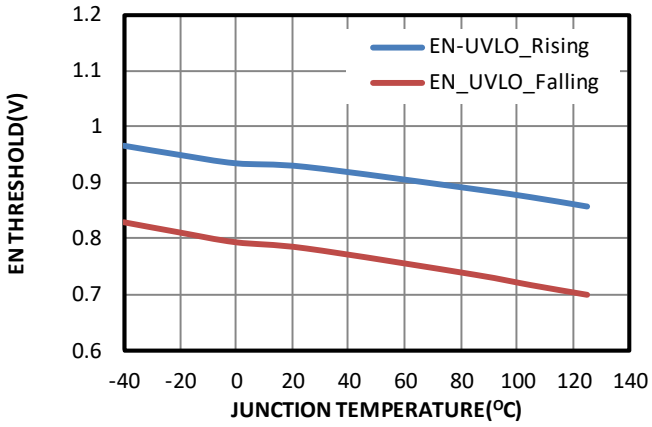


Shutdown Current vs. Input Voltage

EN=0V

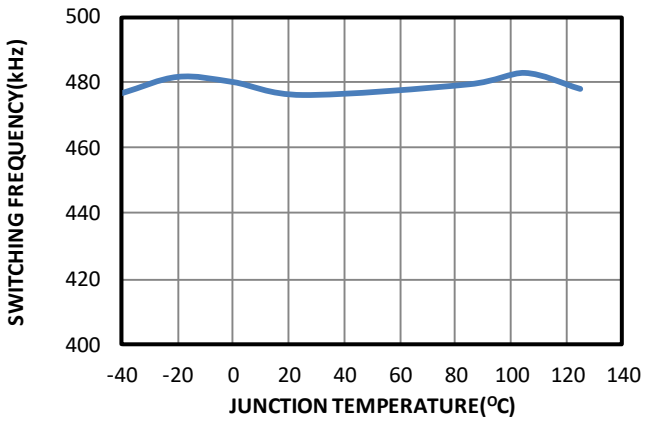


EN UVLO Threshold vs. Temperature

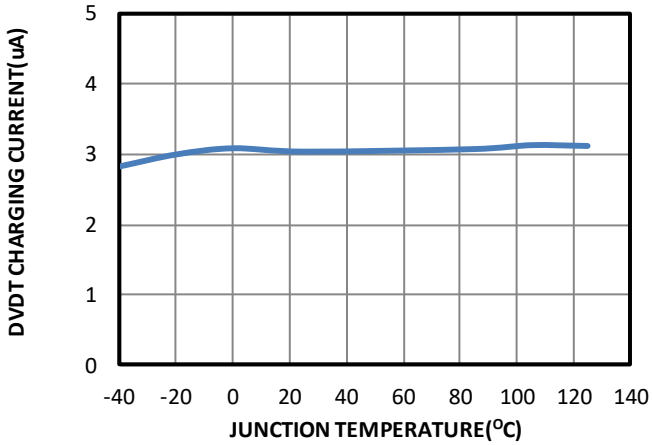


Buck Switching Frequency vs. Temperature

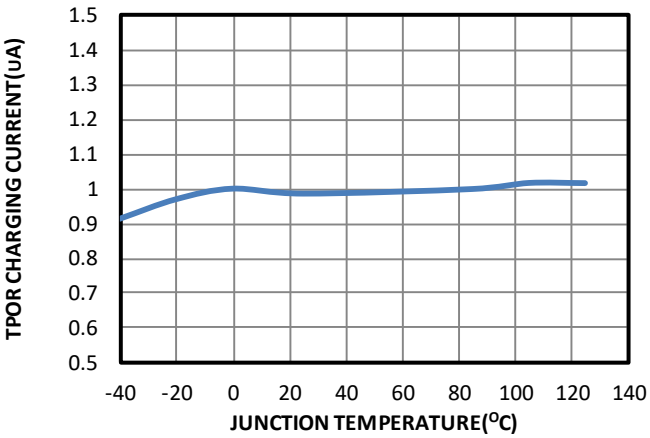
STRG=24V



DVDT Charge Current vs. Temperature



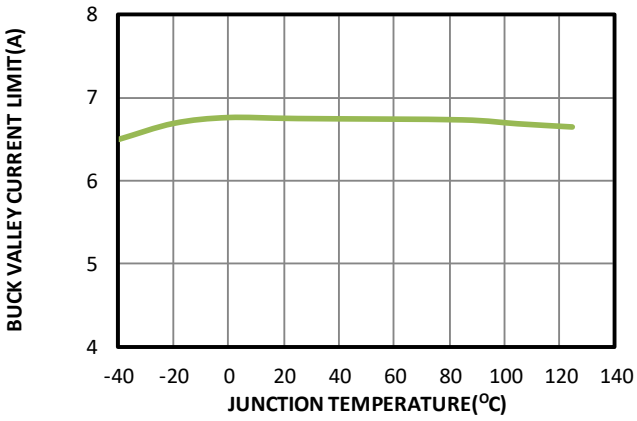
TPOR Charge Current vs. Temperature



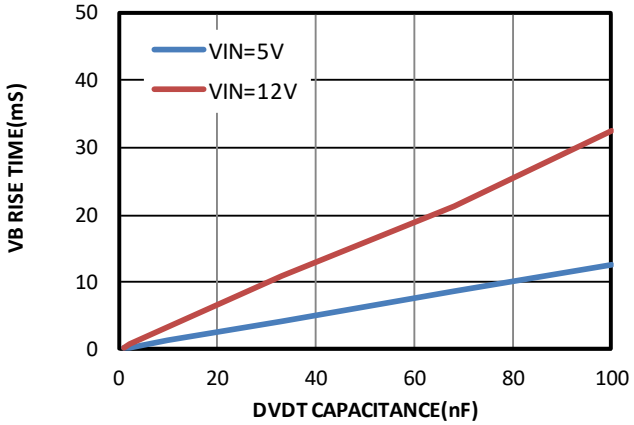
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, VB_{RLS} = 7.5V, L = 10µH, T_A = 25°C, unless otherwise noted.

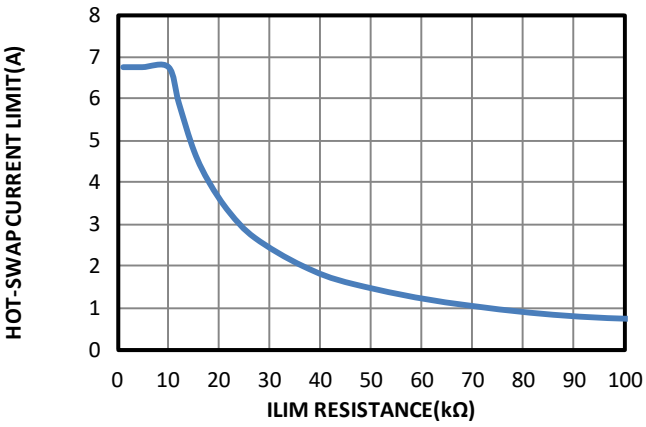
Buck Valley Current Limit vs. Temperature



VB Rising Time vs. DVDT Capacitance

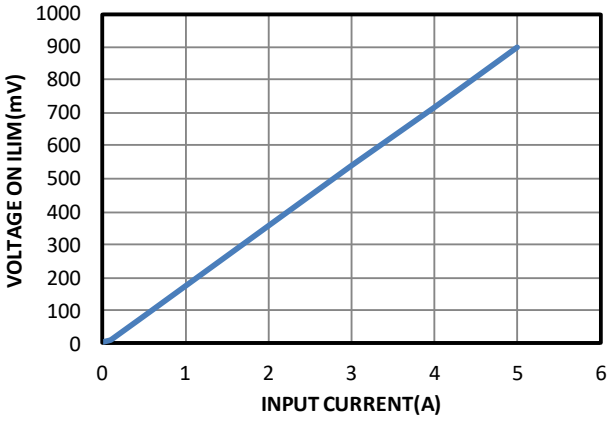


Hot-swap Current Limit vs. ILIM Resistor

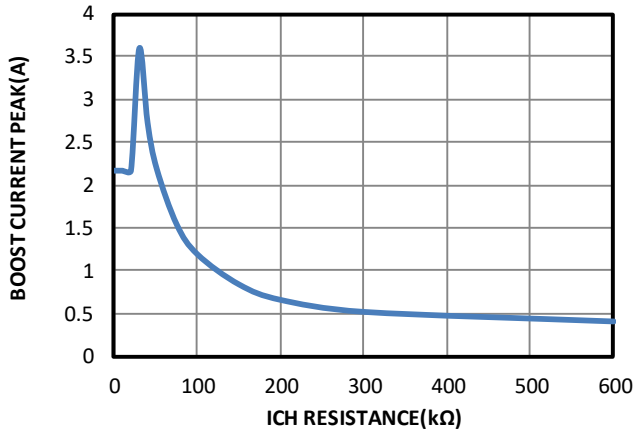


ILIM Monitor Voltage vs. Input Current

R_{ILIM}=12kΩ

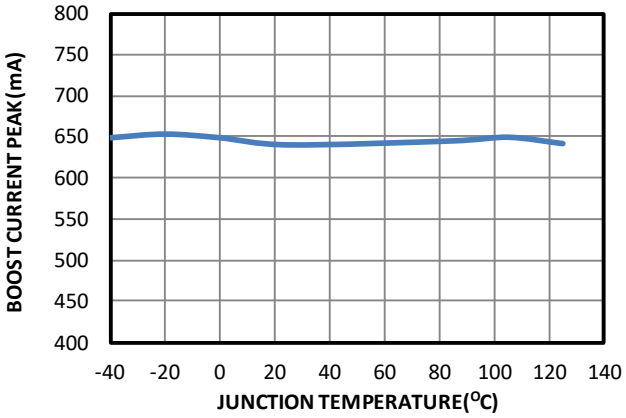


Boost switching Peak Current vs. ICH Resistor



Boost switching Peak Current vs. Temperature

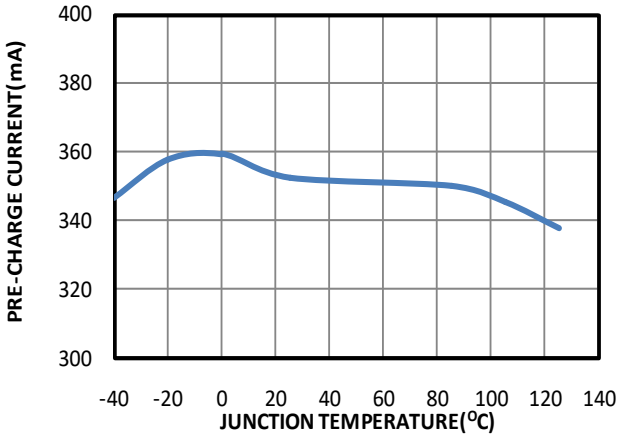
R_{ICH}=200kΩ



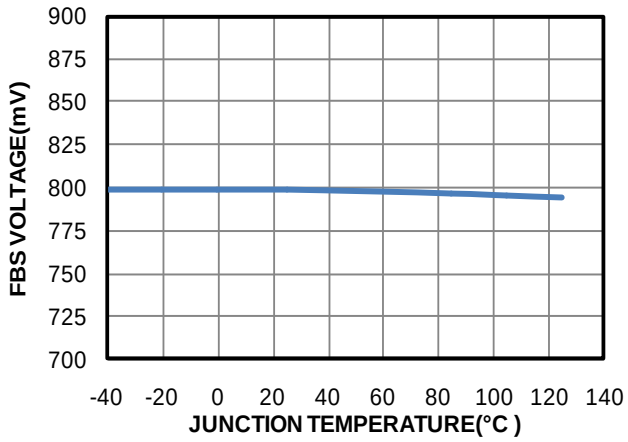
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, VB_{RLS} = 7.5V, L = 10µH, T_A = 25°C, unless otherwise noted.

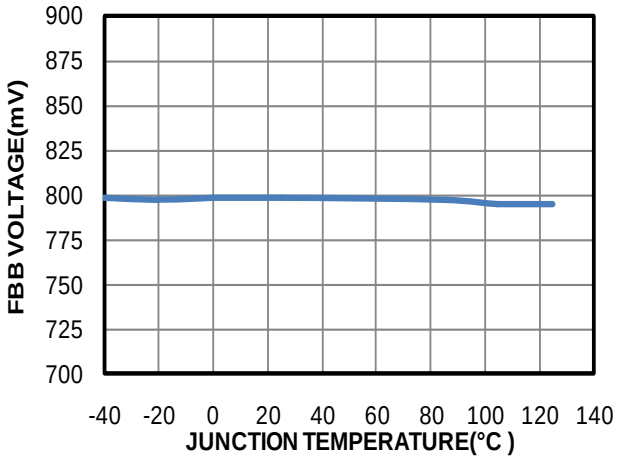
Boost Pre-Charge Current vs. Temperature



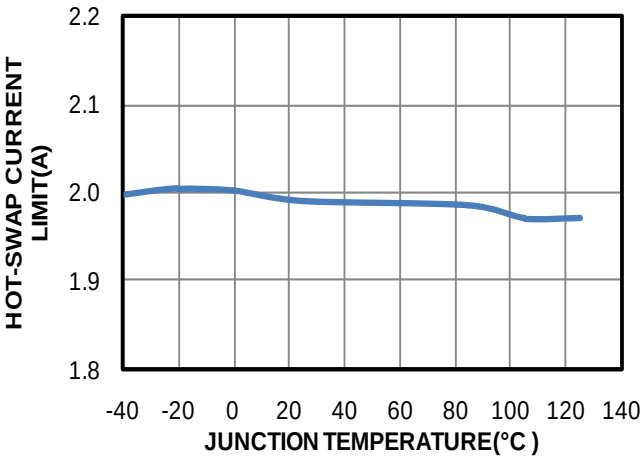
FBS vs. Temperature



FBB vs. Temperature



Hot-Swap Current Limit vs. Temperature

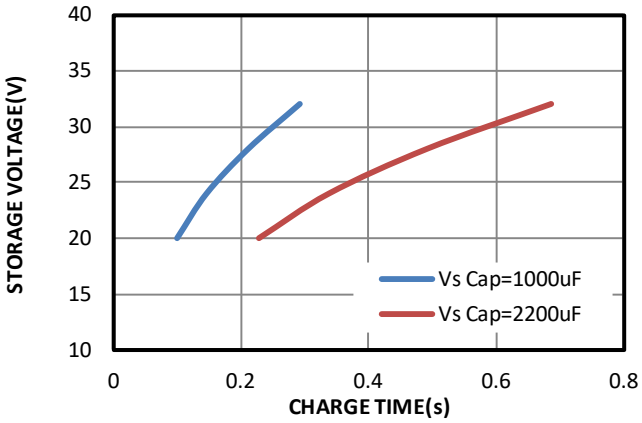


TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{STRG} = 30V, V_{PFI} = 8V, VB_{RLS} = 7.5V, L = 10µH, I_{LOAD} = 5A, T_A = 25°C, unless otherwise noted.

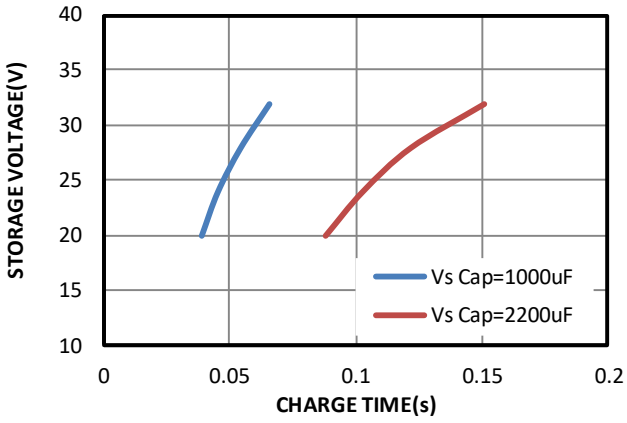
Storage Voltage vs. Charge Time

R_{ICH}=200kΩ

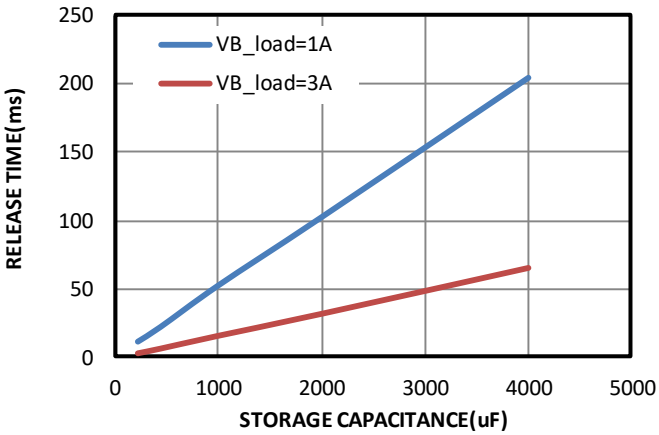


Storage Voltage vs. Charge Time

R_{ICH}=Float

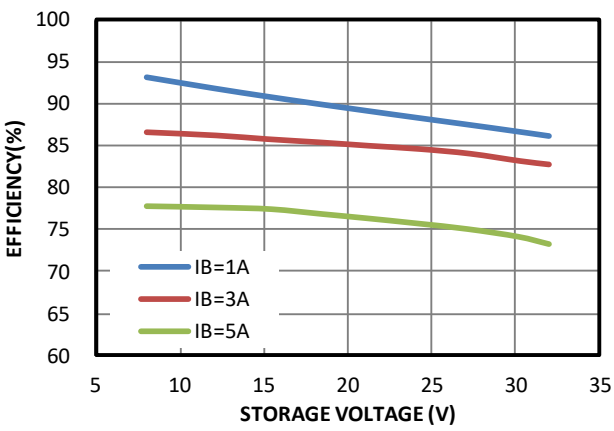


Rlelease Time vs. STRG Capacitance



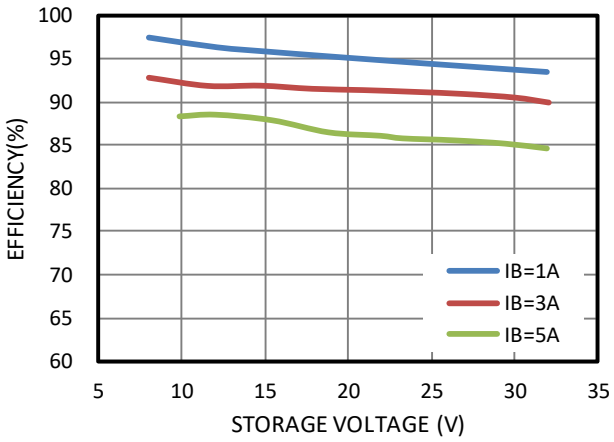
Buck Efficiency

V_B=2.9V, L=4.7uH



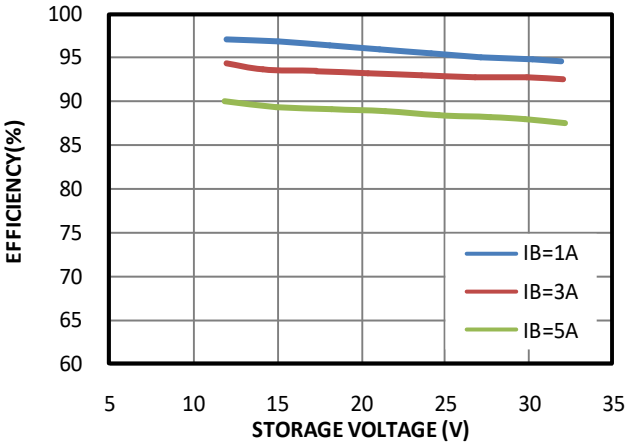
Buck Efficiency

V_B=7.5V, L=10uH



Buck Efficiency

V_B=10V, L=10uH

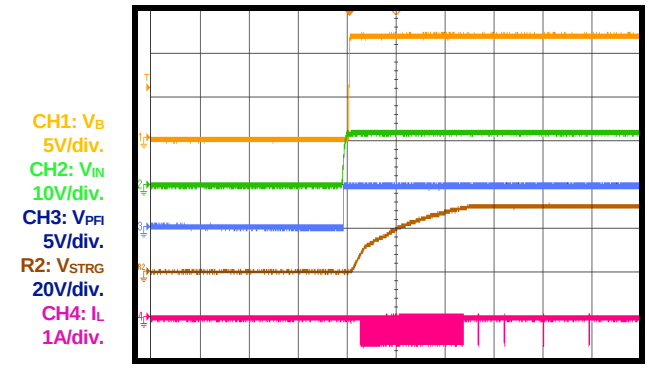


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{STRG} = 30V, V_{PFI} = 8V, VB_{RLS} = 7.5V, L = 10µH, I_{LOAD} = 5A, T_A = 25°C, unless otherwise noted.

Input Power-On

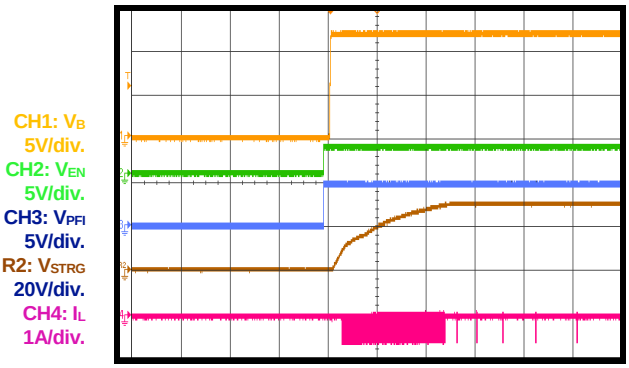
VB load = 5A



100ms/div.

EN Turn-On

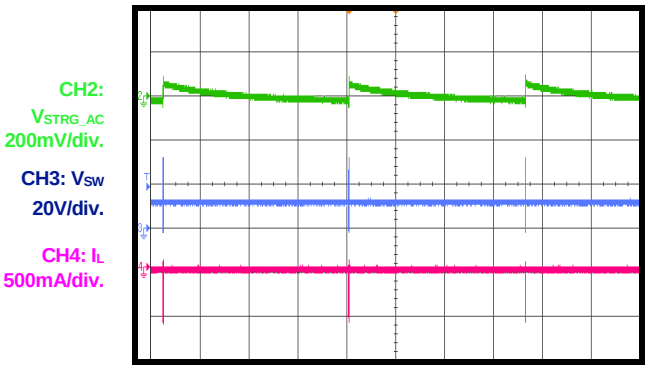
VB load = 5A



100ms/div.

Boost Steady State

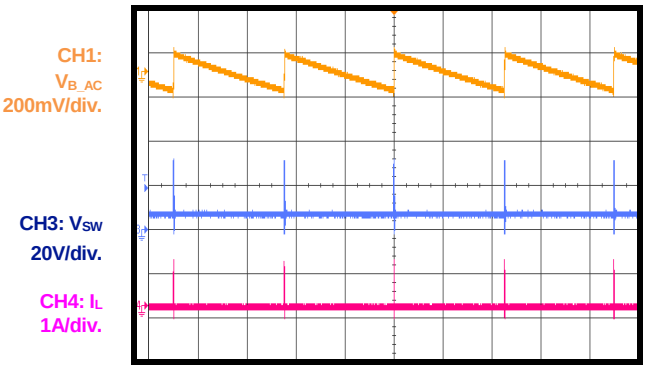
R_{ICH} = 200kΩ



100ms/div.

Buck Steady State

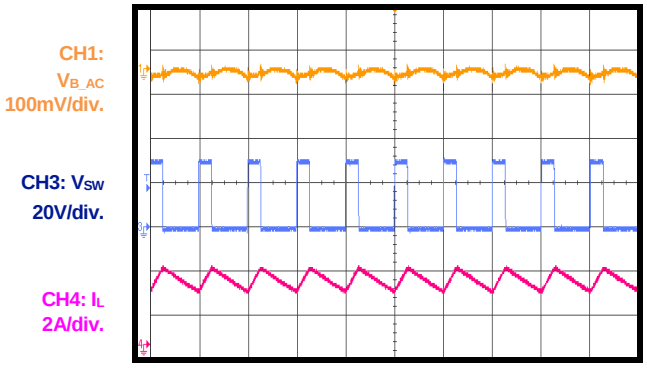
VB load = 0A, 22µF ceramic cap on VB



500ms/div.

Buck Steady State

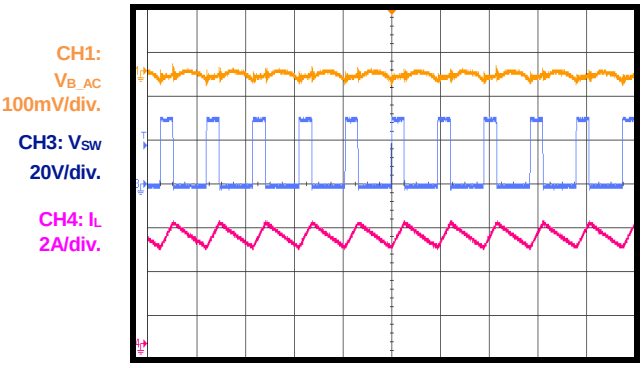
VB load = 3A, 22µF ceramic cap on VB



2µs/div.

Buck Steady State

VB load = 5A, 22µF ceramic cap on VB

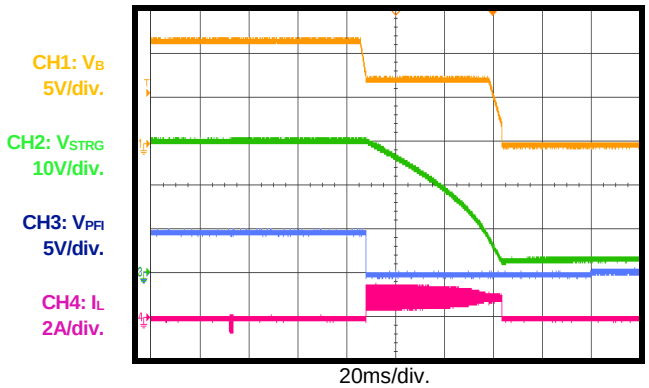


2µs/div.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

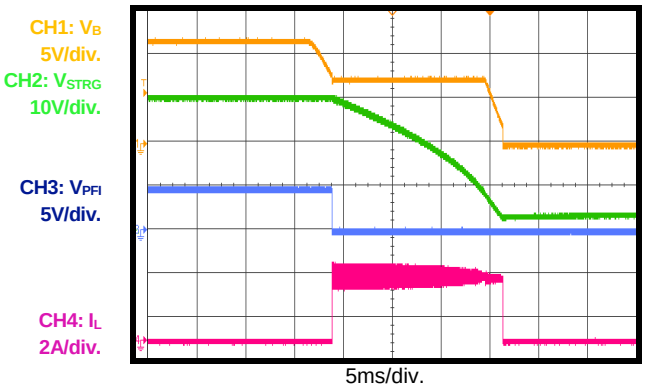
V_{IN} = 12V, V_{STRG} = 30V, V_{PFI} = 8V, VB_{RLS} = 7.5V, L = 10µH, I_{LOAD} = 5A, T_A = 25°C, unless otherwise noted.

V_{STRG} Release
VB load = 1A



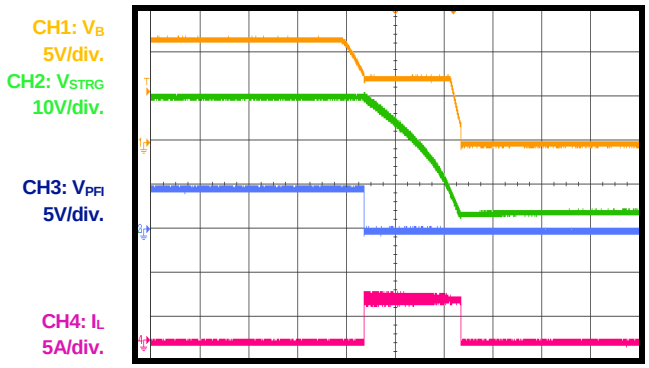
20ms/div.

V_{STRG} Release
VB load = 3A



5ms/div.

V_{STRG} Release
VB load = 5A



5ms/div.

PIN FUNCTIONS

QFN-30 Pin #	Name	Description
1	CST	**Storage capacitor for the internal charge pump.** A 10nF capacitor is required between CST and AGND to drive the input current-limit MOSFET and disconnection MOSFET. Do not connect CST to a capacitor over 47nF.
2	VCC	**Internal LDO output.** VCC provides power for the internal circuits. Decouple VCC with a minimum 1μF ceramic capacitor placed as close to VCC as possible. Do not add an external load to VCC.
3	TPOR	**Power-on reset delay.** Connect a capacitor 1nF or higher between TPOR and AGND to determine the power-on reset delay time. Leave TPOR floating for the 1.5ms default power-on reset delay time
4	OVP	**Over-voltage detection.** A resistor divider from VIN to OVP can program the input over-voltage threshold. If the OVP voltage is higher than 0.81V, the MP5515 is forced into buck mode and recovers when the OVP voltage drops to 0.765V and VB triggers VB_UVLO with a new TPOR time as the first power-on in default. Connect OVP to AGND if the OVP function is not needed.
5	SAS	**Configured as SAS function.** When applying a high-level voltage on SAS, the input current limit switch turns off, and backup mode begins operating. When VB and V_{STRG} are discharged to UVLO, buck_release shuts down, but VCC continues working. SAS is pulled down internally through a 4MΩ resistor.
6	PFI	**Power failure indicator.** PFI is an open-drain output. To indicate a signal, PFI should be pulled up to a power source through a resistor. PFI goes high if the DET voltage exceeds 1.02 x $V_{DET-REF}$. PFI goes low if the DET voltage drops below 0.99 x $V_{DET-REF}$. Once PFI is pulled low, a 200μs blanking time keeps PFI low. PFI is pulled down if SAS, OTP, or EN is off. If PFI is pulled up to another external DC source, PFI can still be pulled low when EN is low. If both VIN and VCC are not available, PFI is pulled low to about 0.85V.
7	DVDT	**Bus voltage start-up slew rate control.** Connect a capacitor 1nF or higher from DVDT to AGND to program different VB charge-up slew rates. The DVDT time can be controlled by the I^2C if DVDT is floating.
8	ILIM	**DC input current limit.** Connect a resistor between ILIM and AGND to adjust the DC current limit from VIN to VB. Apply a voltage higher than 1.5V on ILIM to trigger OCP and disable the ISOFET from VIN to VB.
9	AGND	**IC signal ground.**
10	DET	**Input voltage detection sense.** DET sets the buck release start voltage when VIN drops.
11, 30	VIN	**Input supply voltage.** Place a 0.1μF ceramic capacitor as close to VIN as possible. A TVS diode at the input is necessary if the VIN power line is long and the VIN voltage spike is high in the system. Otherwise, the TVS can be ignored. Refer to the Selecting the Input Capacitor and TVS section on page 37 for more detail.
12, 29	VB	**Bus voltage.** A 22μF to 47μF ceramic capacitor is required as close to VB as possible.
13	EN	**On/off control.** EN enables or disables the internal circuits. When EN is low, the MP5515 is forced to buck mode until V_{STRG} is discharged. The IC shuts down after VB drops, and EN is pulled down internally through a 4MΩ resistor. There is more sink current on EN if a voltage 2V or higher is forced on EN.
14	VBO	**Source of the internal disconnect MOSFET.** Connect an inductor between SW and VBO for backup boost charge and buck release operation.

PIN FUNCTIONS *(continued)*

QFN-30 Pin #	Name	Description
15	PGS	**Storage voltage power good indicator.** By default with the PGS threshold bits = 1111, PGS goes high if the FBS voltage exceeds 0.97 x $V_{FBS-REF}$. PGS goes low if the FBS voltage drops below 0.95 x $V_{FBS-REF}$. PGS can be programmed by the PGS threshold bits. PGS is driven by an internal circuit, which does not require an external pull-up. PGS is low even if the IC is disabled, but if both VIN and VCC power are not available, PGS is pulled low to about 1.3V.
16	PGB	**Bus voltage power-good indicator.** PGB goes high if the FBB voltage exceeds 0.95 x $V_{FBB-REF}$. PGB goes low if the FBB voltage drops below 0.9 x $V_{FBB-REF}$. PGB is driven by an internal circuit, which does not require an external pull-up. PGB is low even if the IC is disabled, but if both VIN and VCC power are not available, PGB is pulled low to about 1.3V.
17	INT	**Interrupt output from the MP5515.** INT is an open-drain output. Even if INT is pulled up to external DC source, INT is pulled low when EN is low and the IC is not in buck switching mode. If both VIN and VCC are not available, INT is pulled low only to about 0.85V.
18	SDA	**I^2C serial data.**
19	SCL	**I^2C serial clock.**
20	TEMP	**Temperature sensor input from thermistor to ADC.**
21	ICH	**Boost-mode charge switching peak current programmable.** Float ICH to set the boost switching peak current at 2A.
22	FBB	**Bus voltage feedback sense.** FBB regulates the bus voltage in buck mode.
23	FBS	**Storage voltage feedback sense.** FBS sets the storage voltage in boost mode.
24	RTEST	**Resistor connect for capacitor health test.** In backup capacitor health test mode, RTEST is pulled to GND internally. One resistor from STRG to RTEST can discharge the backup capacitor. The discharge current through RTEST must be limited below 500mA.
25	BST	**Bootstrap.** A bootstrap capacitor is required from BST to SW to supply the high-side switch driver.
26	STRG	**Backup energy storage.** Connect a backup capacitor to STRG for energy storage and release operation.
27	SW	**Switch output.** SW is used for the energy storage and release circuitry. Connect an inductor between SW and VBO.
28	PGND	**Power ground.**

BLOCK DIAGRAM

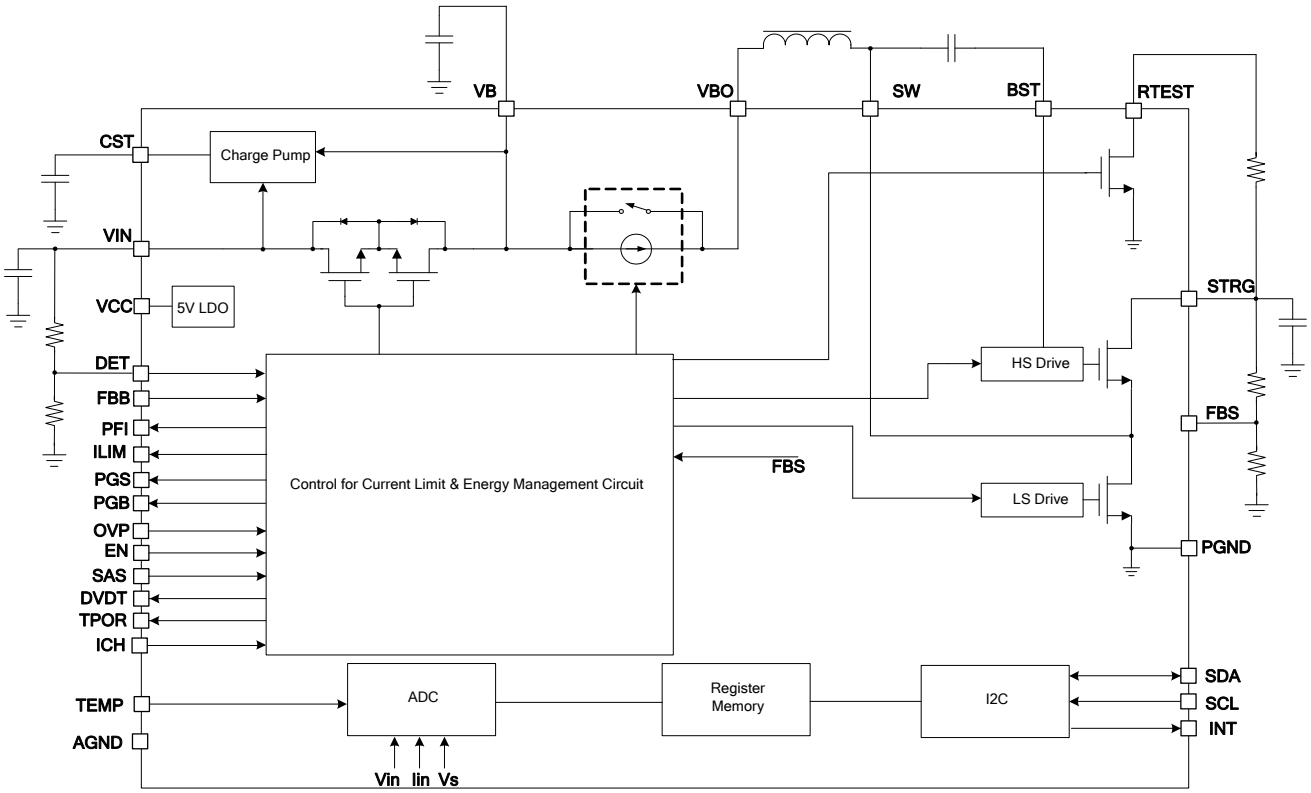


Figure 2: Functional Block Diagram

OPERATION

The MP5515 is an energy backup and management unit in a QFN-30 (5mmx5mm) package. The MP5515 provides a very compact and efficient energy management solution for typical solid-state drive or hard disk drive applications. MPS's patented lossless energy storage and release management circuits use a bidirectional buck-boost converter to achieve optimal energy transfer and provide the most cost-effective energy storage solution.

The integrated boost converter raises the energy backup voltage level. The backup feedback resistor divider sets the backup voltage. If the input shuts down suddenly, the internal buck converter transfers the energy from the backup capacitor to the bus and holds the bus voltage when the system consumes the energy from the backup capacitor.

The MP5515 also features an I²C interface. This interface can be used to write the control command and the monitor system status. One integrated ADC converter converts the voltage, current, and temperature sensor signals.

Start-Up

When the VIN power is higher than its under-voltage lockout (UVLO) threshold, the VCC and I²C interface is enabled. After the power-on reset delay time, if VCC is ready and VIN is 0.2V higher than VB, the isolation MOSFET (ISOFET) from VIN to VB is turned on, and the bus capacitor is charged from 0V to VIN controlled by the DVDT slew rate.

When the DVDT voltage is saturated, the backup boost converter is unlocked and can be enabled by the register bits. There is a timer for ~1.2ms of delay time before starting the boost converter to ensure that the ISOFET is fully turned on.

The backup boost converter is enabled by default. The storage voltage is charged up with about 350mA of trickle current during the pre-charge period. Once the storage voltage is close to VB, the boost switching circuit initiates, and the storage voltage is boosted and regulated to the target voltage (see Figure 3).

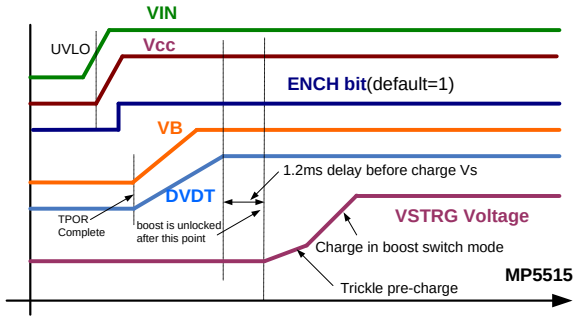


Figure 3: System Power-Up Sequence

Back-Up Voltage

After the start-up period, the internal boost converter regulates the backup voltage to the set value automatically. The MP5515 uses burst mode to minimize the converter's power loss. When the storage voltage drops below the set voltage, burst mode initiates and charges the storage capacitor.

During the boost period, the boost switching current limit and the low-side MOSFET (LS-FET) control the boost. When the LS-FET turns on, the inductor current increases until it reaches its peak current level set by ICH. After reaching the peak current level, the LS-FET turns off for the set minimum off time. At the end of this minimum off time, if the feedback voltage remains below the 0.8V internal reference, the LS-FET turns on again. Otherwise, the MP5515 waits until the voltage drops below the reference before turning on the LS-FET. In boost mode, the high-side MOSFET (HS-FET) does not turn on, and the inductor current conducts through the body diode of the HS-FET.

The boost-current limit is programmed by the ICH resistor. The programmed boost-switching current limit can be estimated with Equation (1):

$$I_{CH}(A) = \frac{88}{R_{ICH}(k\Omega)} + \frac{V_{IN}}{L(H)\times 10^{7}} + 0.1 \quad (1)$$

Where R_{ICH} is the resistor connected to ICH, and L is the boost inductor.

The boost switching current limit is programmed by the ICH resistor (0.5A to 2A recommended for normal application). By floating ICH, the boost switching peak current is set at 2A by default with ICH bits = 11 (for typical 12V input and 10µH inductor application conditions).

Refer to the ICH bits register description on page 31 for other boost peak settings with ICH floating.

The MP5515 applies an over-voltage protection (OVP) function for V_{STRG}. If the feedback voltage of V_{STRG} on FBS is over 1.1 x $V_{FBS-REF}$, the MP5515 shuts down the LS-FET of the boost converter until V_{STRG} drops to the regulating voltage. It is not necessary to add an external power to STRG with a voltage higher than the V_{STRG} regulation voltage.

Power-Down Release

After the first start-up period and the boost starts switching, the MP5515 registers and enables the release function. Once the input power drops and DET drops to 0.99 x $V_{DET-REF}$, the storage boost converter stops charging and works in buck-release mode. At the same time, the ISOFET shuts down to prevent a negative current from VB to VIN.

In buck mode, the MP5515 transfers energy from the high-voltage storage capacitor to the low-voltage bus capacitor. The regulated bus voltage is determined by $V_{FBB-REF}$ and the resistor divider from VB to FBB.

Figure 4 shows the detailed system shutdown process. Buck mode has a max current limit function to limit the release current. In each buck mode switching cycle, the high-side switch does not turn on until the inductor current drops to a 6.5A valley current, typically.

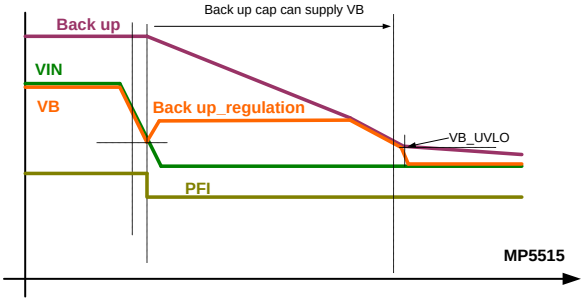


Figure 4: VIN Shutdown Sequence

Input Recovery Start-Up

If the input power fails and is restored, the MP5515 remains in buck release mode. When STRG is discharged and VB drops to VB_UVLO, the MP5515 restarts from the recovered VIN power, which is a new input power start-up cycle with TPOR delay.

Input Current Limit

The input current limit controls the input inrush current of the ISOFET carefully to prevent an inrush current from VIN to VB. The internal DVDT bits or external DVDT cap can set the soft-start time. In addition to the soft-start process, ILIM can limit the steady-state current by connecting a resistor between ILIM and AGND to set the current limit. The current limit can be estimated with Equation (2):

$$I_{LIM} = \frac{70.04}{R_{ILIM}(k\Omega)} + 0.08 \quad (2)$$

Where R_{ILIM} is the current-limit setting resistor from ILIM to AGND.

The voltage on ILIM can also monitor and indicate the current in the ISOFET. The relationship between the input current and ILIM voltage can be estimated with Equation (3):

$$I_{IN} = \frac{V_{ILIM} * 64.26}{R_{ILIM}(k\Omega)} + 0.08 \quad (3)$$

Where V_{ILIM} is the ILIM voltage. V_{ILIM} can be read through an ADC converter.

The voltage on ILIM is lower than 1.09V in normal applications. If a voltage greater than 1.5V is applied on ILIM externally, the ISOFET is shut down, and the MP5515 enters a buck-up process.

When the VB load is close to the ILIM threshold, during every boost refresh cycle, the input current may easily trigger the current limit as well as the system interrupt. To avoid continuously triggering ILIM interrupt in this condition, during every boost-up refresh cycle, the input over current-interrupt is masked automatically. The mask time depends on the boost-up switching time.

Once the input over-current threshold is triggered and FBB drops to $V_{FBB-REF}$, the backup buck converter starts working to maintain VB. Once FBB is charged back to 105% of $V_{FBB-REF}$, the buck is disabled again in this condition. During the boost refresh cycle, the buck converter is not enabled, even if the over-current threshold is triggered.

Power-On Reset Delay and VB Rising Control

TPOR controls the power-on reset function for hot swapping. By floating TPOR, the TPOR time is about 1.5ms by default. If an external capacitor is connected to TPOR, an internal 1μA current charges the capacitor and determines the TPOR time (charge TOPR cap from 0V to 1V). The power-reset-delay time can be estimated with Equation (4):

$$T_D = \frac{C_{TPOR} \times 1V}{1\mu A} \quad (4)$$

After the TPOR time, one capacitor across DVDT programs the VB soft-start (SS) time. During the SS period, the relationship between VB and DVDT can be estimated with Equation (5):

$$VB = 13 \times V_{DVDT} \quad (5)$$

Where V_{DVDT} is the DVDT capacitor voltage charged by a 3μA current. The V_{DVDT} charge is saturated to about 1.23V.

The VB soft-start time from 0V to VIN can be estimated with Equation (6):

$$T_R = \frac{VB \times C_{DVDT}}{13 \times 3\mu A} \quad (6)$$

By floating DVDT, the VB rising time can be programmed by the internal DVDT register bits. By default, the DVDT bit is set to 00, and the VB slew rate is about 7.5V/ms. VB from 0V to 12V is 1.6ms by default, typically, if DVDT is floating. Refer to the DVDT register description on page 33 for other DVDT bit settings.

Reverse-Current Protection (RCP)

The VIN to VB MOSFET turns on when the input voltage exceeds the VIN UVLO threshold and VIN becomes greater than VB + 0.2V. This MOSFET turns off when the DET voltage falls, causing the MP5515 to enter buck-release mode and does not turn on again until buck mode finishes.

The ISOFET circuit applies reverse-current protection (RCP) when energy is released from the storage capacitors to VB. Typically, a 250mA reverse current from VB to VIN shuts down the ISOFET.

Start-Up Sequence

After the IC is enabled, MP5515 starts to work with the TPOR reset time and DVDT soft-start time. During the VB rising time, an internal charge pump charges the CST capacitor. This provides a driver source for the hot-swap MOSFET. Too short of a DVDT time may trigger the input current-limit threshold. Too large of a CST capacitor may affect the charge-pump slew rate. A 10nF CST capacitor is recommended. During the DVDT soft start, the VB capacitor is charged, and the STRG capacitor is not charged.

Once VB is charged, the DVDT voltage charges to about 1.23V and is held at this saturated voltage. If PFI is high and DVDT saturates, the charge function is enabled and the storage capacitor charges to the target voltage.

Backup Capacitance Test

The MP5515 features a back-up capacitor test by discharging the backup capacitor through one external resistor from STRG to RTEST. Figure 5 shows the discharge block. The MOSFET is about 4.5Ω, and the peak discharge current must be limited below 500mA by an external resistor, even it is discharged in a short time.

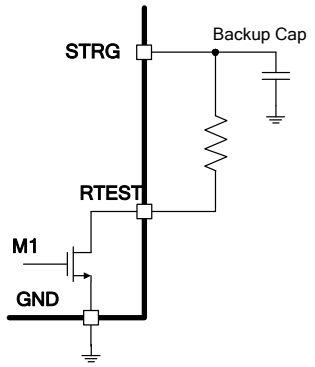


Figure 5: Backup Capacitance Test Circuit

When the Start Cap Test register bit is set, the MP5515 disables the boost charge switching, and RTEST is connected to GND through the internal MOSFET (M1) for energy discharging. The MP5515 enables the V_{STRG} ADC conversion when FBS drops to the $V_{FBS-REF}$ threshold (SOC can read the STRG voltage

through the I²C). Simultaneously, an internal counter is enabled to measure the discharge time. The counter continues until the cap voltage drops below the PGS threshold voltage. When V_{STRG} drops to the PGS threshold, the ADC reads V_{STRG} again, and the Cap Test Done register is set to indicate that cap test is complete. Cap Test Done produces one interrupt to inform the SOC that the test has been completed. The SOC can read the backup voltage and the counter timer registers. With the initial voltage and end voltage reading, the discharge time can be determined as acceptable or not.

At the first ADC conversion, the MP5515 reads V_{STRG} and stores this in the register ADC Backup Voltage Data2. At the end of the capacitor discharge ADC records the end voltage in the register 'ADC Backup Voltage Data1. The counter result is stored in the register Cap Test Timer.

After the cap test is done, the Cap Test Start bit is reset automatically, and the recharge function is enabled automatically. Figure 6 shows the work flow of performing the capacitance test.

SOC capacitance test function follows the following operations:

1. Write register 04h bit[2] and bit[6] to code 1 (mask PGS Not Ok and ADC Done interrupt).
2. Write register 06h to code 00h or another value (set PGS Threshold at 80% or another ratio of regulation).
3. If VIN is lower than 3.8V, write register 1Bh bit[1] to code 1. This turns on the internal V_{STRG} to the VCC LDO. If VIN is higher than 3.8V, ignore this step.
4. Write register 01h bit[3] to code 1 (request Start Cap Test).

   The MP5515 disables the V_{STRG} charge function automatically after V_{STRG} is charged higher than the FBS-set voltage. Register 01h bit[0] does not change.

   The MP5515 starts discharging the STRG cap through an external resistor after V_{STRG} is fully charged.

   The MP5515 starts the ADC only when V_{FBS} drops to the $V_{REF-FBS}$ threshold. ADC reads V_{STRG} and stores data in ADC Backup Voltage Data2.
   The internal timer starts when V_{FBS} drops to the $V_{REF-FBS}$ threshold.
5. Wait for the interrupt from the MP5515 (afterward, if register 02h bit[7] is 1, the cap test is complete).

   When V_{STRG} discharges to the PGS threshold, the discharge stops, and the timer value is written to register Cap Test Timer.

   When PGS Threshold falling is triggered, the MP5515 starts ADC a second time and stores data in ADC Backup Voltage Data1.

   After ADC conversion, the MP5515 sets the Cap Test Done interrupt.

   The MP5515 resets register 01h bit[3] to code 0 automatically to clear Cap Test Start.

   The MP5515 re-enables the boost charge function automatically.
6. Read registers 12h bit[7:0], 13h bit[1:0] and store as V_{FINAL}, total 10 bits (12h is the high byte, 13h is the low byte).

   Read registers 14h bit[7:0], 15h bit[1:0] and store as $V_{INITIAL}$, total 10 bits (14h is the high byte, 15h is the low byte)

   Read registers 16h bit[7:0], 17h bit[7:0] and store as Time, total 16 bits (16h is the low byte, 17h is the high byte).
7. Write register 02h bit[7] to code 1 to reset the cap test interrupt event. Write both register 04h bit[2] and bit[6] to code 1 to re-enable PGS Not OK and ADC Done interrupt. Write register 1Bh bit[1] to code 0 if it was set to 1 in step 3.
8. Calculate ADC results with Equation (7):

$$C_{STRG} = \frac{Time}{R_{DISCH} \times \ln\left(\frac{V_{INITIAL} + R_{DISCH} \times I_{LDO}}{V_{FINAL} + R_{DISCH} \times I_{LDO}}\right)} \quad (7)$$

Where $V_{INITIAL}$ is V_{STRG} before the discharge timer starts stored in ADC Backup Voltage Data2 (in V), V_{FINAL} is V_{STRG} after discharge completes and stored in ADC Backup Voltage

Data1 register (in V), and R_{DISCH} is the resistor between STRG and RTEST (in kΩ).

When VIN is less than 5V and register 1Bh bit[1] = 1, I_{LDO} is typically 2mA, which is the VCC LDO current from V_{STRG}. Otherwise, I_{LDO} is 0mA. It is recommended to reset the LDO_EN bit after the capacitance test finishes to save operation current (use the mA unit for the LDO in the cap test).

Time is recorded in the counter register Cap Test Timer (unit in 1ms).

Refer to the ADC Results register on page 32 for cap test time and voltage calculation.

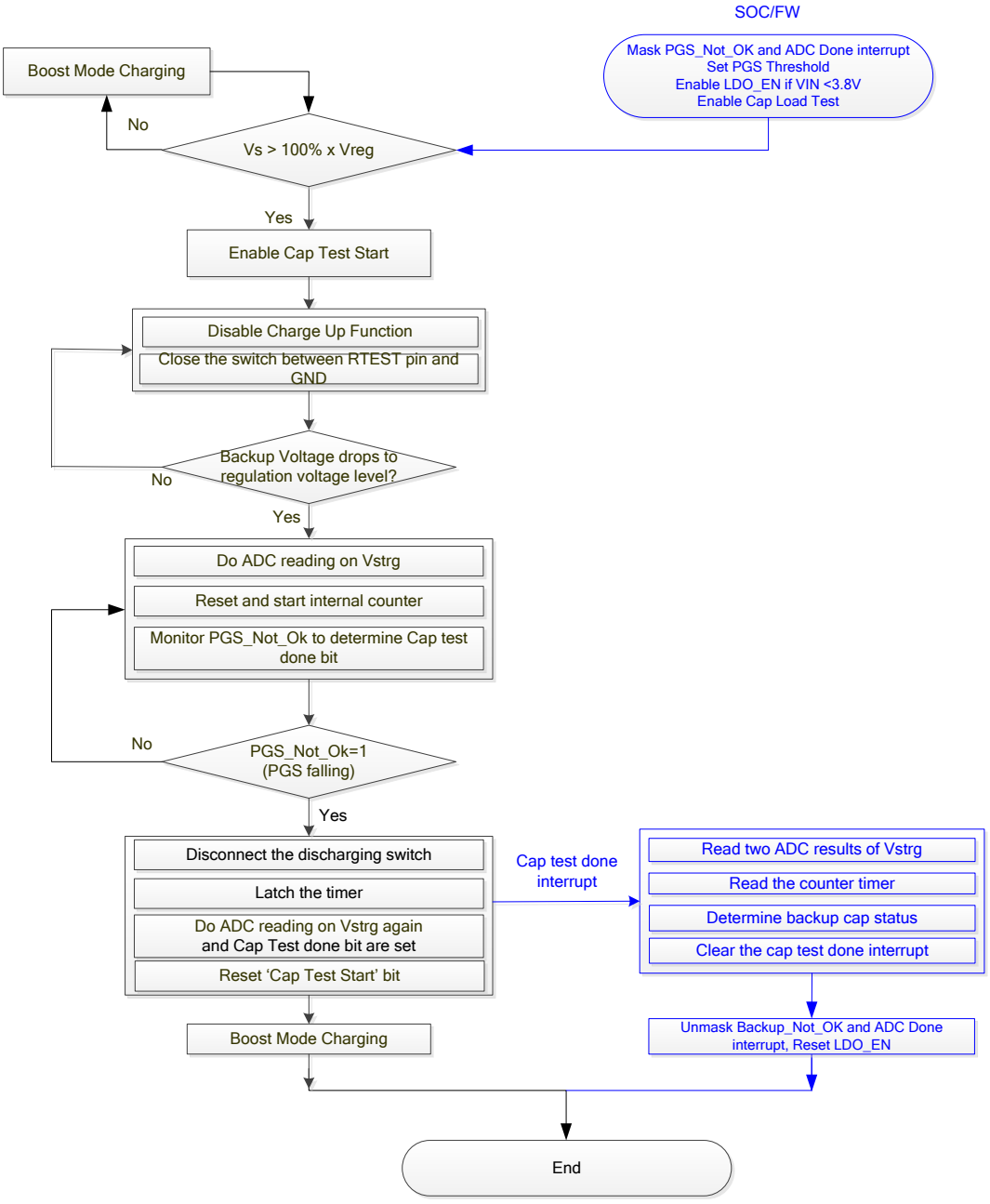


Figure 6: Backup Capacitance Test Work Flow

The MP5515 enters buck mode if VIN fails during the cap test. The cap test cannot be done in buck mode. For more information on the cap health test, refer to the application note AN125, "MP5515 Capacitor Health Measurement Accuracy and Recommended Method."

VCC Power Management

The MP5515 internal circuits are powered by the VCC capacitor. VCC is supplied by VIN, VB, or V_{STRG} under different conditions (see Table 1).

Table 1: VCC Power Sources

Operation Mode	LDO_EN Bit	Power Sources
Boost charge	0 (default)	VCC is supplied by the higher value of either VIN or VB.
Buck discharge		VCC is supplied by the higher value of either VIN or VB when it is above 4.5V (typical value). If VCC is lower than 4.5V, the LDO from V_{STRG} to VCC is enabled and regulates the VCC at about 4.5V.
Boost charge	1	
Buck discharge		

The LDO_EN (0x1Bh bit[1]) is useful for ADC conversion, including the cap test when VIN and VB are low. It is recommended to enable the LDO_EN bit before ADC operation when VIN and VB are low. Refer to the 10-Bit ADC section on page 23 for more details.

A capacitor no less than 1µF is required on VCC. When starting up from 3V or a lower VIN, VCC is low due to the VIN-to-VCC voltage drop. Any external current on VCC (i.e.: a PFI pull-up resistor) pulls VCC lower and makes the MP5515 difficult to start up. Typically, a 100kΩ pull-up resistor for PFI and INT is suggested, but these pins can also be pulled up to VB if the VB voltage is lower than 5V.

The MP5515 can start up from a 2.7V low input power at 25°C or a higher temperature. If the temperature is lower than 25°C, the UVLO rises slightly. One external Schottky diode from VIN to VCC is suggested if the IC needs to start up with 2.7V under low-temperature conditions. This diode is recommended even if VIN is 3V under -40°C.

Enable Control (EN)

The EN pin of the MP5515 works together with the EN bit to enable the internal circuit. The MP5515 is enabled after both the EN pin and EN bit are high. During application, the EN pin cannot be connected to a voltage higher than 6.5V. For resistor pull-up condition, an internal Zener diode clamps the voltage at the EN pin. The maximum pull-up current (assuming the worst case, 6V) for the internal Zener clamp should be less than 1mA. When pulled up to VIN and VB, 100kΩ pull-up resistors to both VIN and VB are recommended.

SAS Function

The MP5515 provides a forced backup mode for energy discharge. When SAS or the Force Buck Release bit is high, the ISOFET turns off, operates in buck release mode, and PFI drops low to indicate the power status. If VB drops to UVLO before SAS resets, the buck shuts down, and the VCC power continues working. The MP5515 works with a new start cycle when SAS resets. If VB is still higher than UVLO after SAS resets to 0, PFI is pulled high, and the ISOFET works as the VIN power recovery after VB triggers VB_UVLO.

Input Power Failure Indicator (PFI)

If DET drops below 0.99 x $V_{DET-REF}$, the MP5515 pulls PFI low internally to indicate a power failure. Simultaneously, the MP5515 exits boost mode. If the DET voltage rises to 1.02 x $V_{DET-REF}$, PFI is set to high again (if pulled up by a resistor externally), but the MP5515 does not exit buck mode, even if PFI is high, until the V_{STRG} energy is discharged to UVLO or the IC resets.

Bus Voltage Power Good Indicator (PGB)

When the voltage on the FBB (VB feedback) drops below 0.9 x $V_{FBB-REF}$, the MP5515 pulls PGB low internally. When the FBB voltage is above 0.95 x $V_{FBB-REF}$, PGB goes high.

STRG Voltage Power Good Indicator (PGS)

The storage power good threshold can be programmed by the PGS Threshold bits. By default, the PGS falling threshold is 95% of the reference voltage. When the voltage on FBS (V_{STRG} feedback) drops below 0.95 x $V_{FBS-REF}$, the MP5515 pulls PGS low internally.

When the FBB voltage is above 0.97 x $V_{FBS-REF}$, PGS goes high.

Input Over-Voltage Protection (OVP)

A resistor divider from the VIN power to OVP can set input over-voltage protection (OVP). Once the OVP pin voltage rises to 0.81V, the MP5515 is forced into buck backup mode. After the OVP pin voltage drops to 0.765V and the buck stops (VB triggers VB_UVLO), the MP5515 restarts automatically as a new power-on cycle with a TPOR process. One Input Over-Voltage register bit records the OVP event and generates an interrupt signal on INT if it is unmasked.

10-Bit ADC

The MP5515 integrates a 10-bit A/D converter to measure the input voltage, input current, backup voltage, and TEMP pin temperature sensor voltage. The register Start ADC can enable A/D conversion. ADC Done is set if one ADC conversion completes. An interrupt request to the controller can be set if the ADC Done bit is set. Figure 7 shows the ADC setting work flow. Refer to the ADC Results register on page 32 for details on ADC converting results calculation.

When VIN is lower than 3.8V, set register 0x1Bh bit[1] to 1 by the host chip before enabling the ADC or capacitance test functions. Setting this bit enables the LDO from V_{STRG} to VCC, provides more margins for the internal ADC reference, and insures ADC accuracy. The LDO from V_{STRG} to VCC draws about 2mA of current from STRG. It is recommended to disable the LDO after ADC or the capacitance test completes. By default, the LDO_EN bit is 0.

Interrupt Control

The MP5515 pulls INT high if any fault condition in the interrupt register occurs when the fault bits are not masked. This interrupt signal is asserted to inform the SOC that certain fault conditions have occurred. When there is an existing interrupt event, and a second interrupt event occurs before SOC resets INT where the INT voltage is still high, the MP5515 keeps INT high until SOC resets all interrupt event sources (see Figure 8).

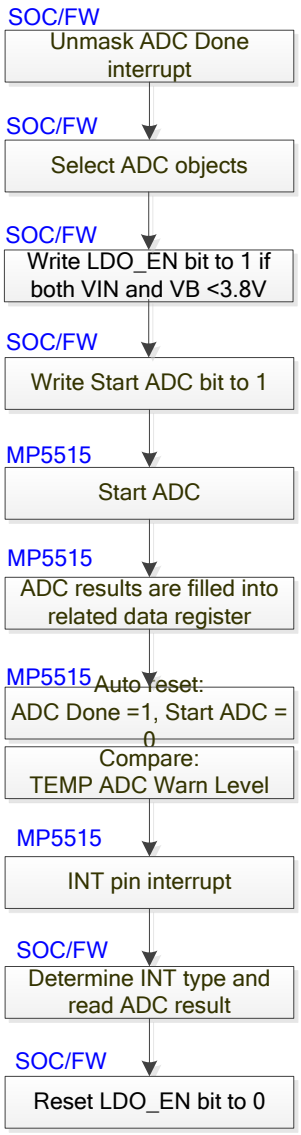


Figure 7: ADC Converter Work Flow

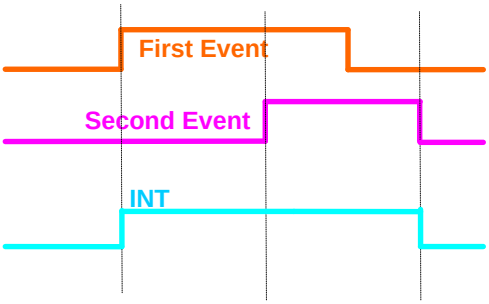


Figure 8: Interrupt Sequence

After the fault event occurs, the MP5515 generates an interrupt and other actions (see Table 2).

Thermal Shutdown

Thermal shutdown is implemented to prevent the chip from running away thermally. When the silicon die temperature is higher than 120°C, the T_J warn bit is set to 1 and sends an interrupt to SOC. Write 1 to the TJ Warn bit to reset the interrupt after T_J drops below 100°C.

If the silicon die temperature is higher than 150°C, the MP5515 is forced into backup mode and discharges energy from V_{STRG} to VB. In this condition, the ISOFET is off and PFI is low. The buck is released until the energy is fully discharged. When the junction temperature is lower than 125°C, the MP5515 is re-powered from VIN and works as the VIN power recovery. There is an interrupt for 150°C over-temperature. It can be reset by writing 1 to the TJ Warn bit.

If the silicon die temperature rises to 165°C, the MP5515 turns off all circuits.

Register Default Value Program

The MP5515 has many control register bits, and all have a fixed default value after a power reset. After power-up, all bits can be programmed by writing the I^2C. Registers 0x06h, 0x07h, 0x21h, and the device I^2C address default value can be programmed, so providing different default values can match different system requirements after power-on.

Table 2: Fault Event Response Table

Event	Status Bit	Status/INT Reset Condition	PFI	INT	MP5515 Power Action
Input over-current	Input Over-Current	POR, write 1 to the bit	No action	Yes (high)	Limit input current. Enter buck if VB drops to FBB regulation.
Input power fail	N/A	N/A	Yes (low)	No action	ISOFET off, IC switches to buck release mode.
OVP pin over-voltage	Input Over-Voltage	POR, write 1 to the bit	Yes (low)	Yes (high)	ISOFET off, IC switches to buck release mode.
VSTRG triggers PGS falling	PGS Not Ok	POR, write 1 to the bit	No action	Yes (high)	No action.
TEMP pin warn	TEMP Warn	POR, write 1 to the bit	No action	Yes (high)	No action.
Die temp high warning	IC T_J Warn	POR, write 1 to the bit	No action	Yes (high)	No action.
Die over-temp to forced buck	IC T_J Shutdown	POR, write 1 to the bit	Yes (low)	Yes (high)	ISOFET is off, IC switches to buck release mode, then shuts down after power is discharged.
SAS disable supply	SAS DIS	POR, write 1 to the bit	Yes (low)	Yes (high)	ISOFET off, IC switches to buck release mode.
ADC complete	ADC Done	POR, write 1 to the bit	No action	Yes (high)	No action.
Cap test complete	Cap Test Done	POR, write 1 to the bit	No action	Yes (high)	Refer to cap test state diagram.

It is suggested to use the default register value of registers 0x06h, 0x07h, 0x21h, and device I²C address for application. If different default values are needed for these registers, please contact MPS for a program solution.

I²C Interface

The I²C is a two-wire, bidirectional, serial interface consisting of a data line (SDA) and a clock line (SCL). The lines are pulled to a bus voltage externally when they are idle. When connecting to the line, a master device generates the SCL signal and device address and arranges the communication sequence. The MP5515 interface is an I²C slave. The I²C interface adds flexibility to the SSD power system control by different register configurations.

The MP5515 7-bit device address is defined as 33h (011 0011). When the master sends an 8-bit address value, the 7-bit I²C address should be followed by a 0 or 1 to indicate a write or read operation, respectively.

I²C Data Validity

One clock pulse is generated for each data bit transferred. The data on the SDA line must be stable during the high period of the clock. A high or low state of the data line can change only when the clock signal on the SCL line is low as shown in Figure 9.

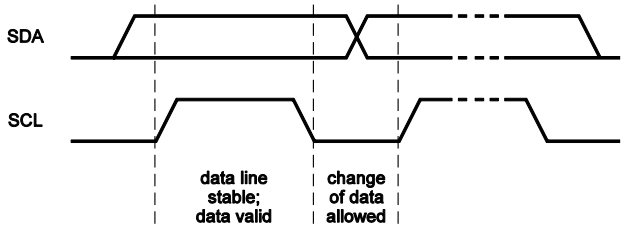


Figure 9: Bit Transfer on the I²C Bus

The start and stop are signaled by the master device, which signifies the beginning and the end of the I²C transfer. The start condition is defined as the SDA signal transitioning from high to low while the SCL is high. The stop condition is defined as the SDA signal transitioning from low to high while the SCL is high (see Figure 10).

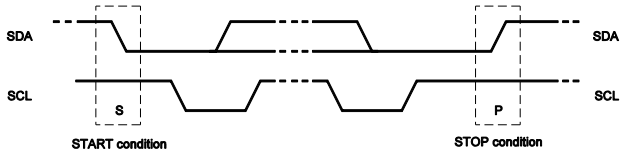


Figure 10: Start and Stop Conditions

Start and stop conditions are always generated by the master. The bus is considered to be busy after the start condition. The bus is considered to be free again after a minimum of 4.7µs after the stop condition. The bus stays busy if a repeated start (Sr) is generated instead of a stop condition. The start (S) and repeated start (Sr) conditions are identical functionally.

I²C Transfer Data

Every byte put on the SDA line must be eight bits long. Each byte must be followed by an acknowledge bit. The acknowledge-related clock pulse is generated by the master. The transmitter releases the SDA line (high) during the acknowledge clock pulse. The receiver must pull down the SDA line during the acknowledge clock pulse so it remains stable low during the high period of this clock pulse.

Data transfers follow the format shown in Figure 11. After the start condition (S), a slave address is sent. This address is seven bits long followed by an eighth bit, which is a data direction bit (r/w). A zero (0) indicates a transmission (write), and a one (1) indicates a request for data (read). A data transfer is always terminated by a stop condition (P) generated by the master. However, if a master still wishes to communicate on the bus, it can generate a repeated start condition (Sr) and address another slave without first generating a stop condition.

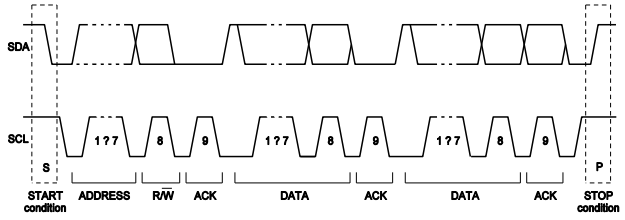
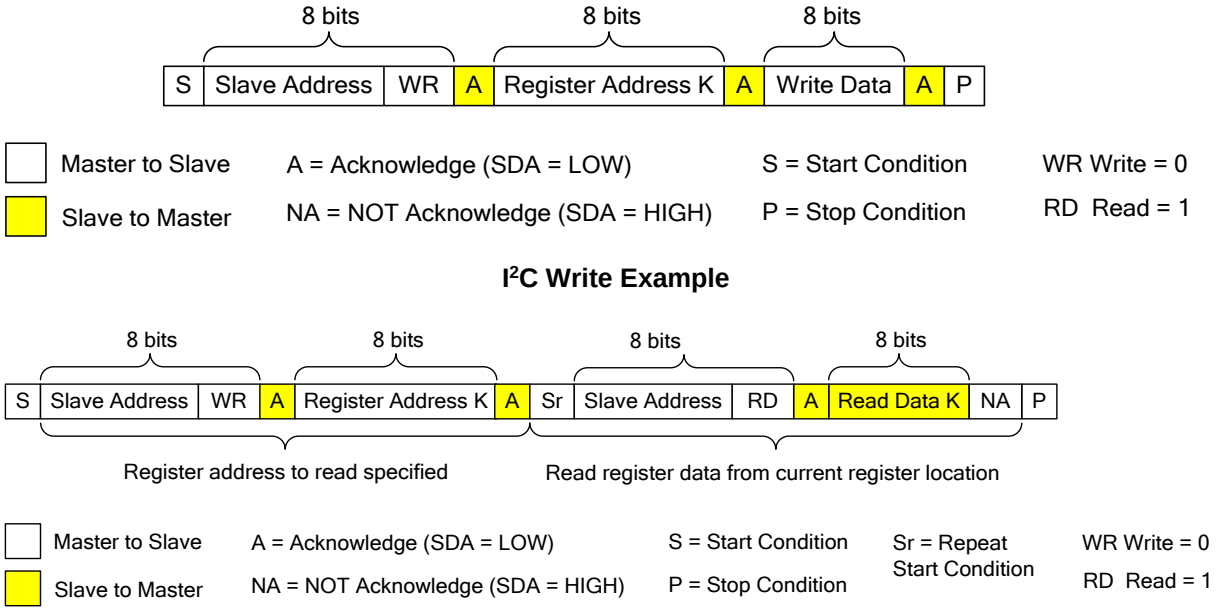


Figure 11: Complete Data Transfer

The MP5515 includes a full I²C slave controller. The I²C slave fully complies with the I²C specification requirements and requires a start condition, a valid I²C address, a register address byte, and a data byte for a single data update. After receiving each byte, the MP5515 acknowledges by pulling the SDA line low during the high period of a single clock pulse. A valid I²C address selects the MP5515. The MP5515 performs an update on the falling edge of the LSB byte.

Figure 12 shows an example of an I²C read and write command.



I²C Write Example

I²C Read Example

Figure 12: I²C Read and Write

REGISTER DESCRIPTION

Register Map

Addr	Register	Type	D7	D6	D5	D4	D3	D2	D1	D0	Reset State
0x00h	Vendor ID	r	Fab		Major Rev		Minor Rev		Vendor ID		0000 0000
0x01h	Sys Control 1	r/w	-	-	-	-	Start Cap Test	Start ADC	-	ENCH	0000 0001
0x02h	Interrupt1 Status	r/w	Cap Test Done	ADC Done	-	Input Over-Current	Input Over-Voltage	PGS Not Ok	-	TEMP Warn	0000 0100
0x03h	Interrupt2 Status	r/w	-	SAS DIS	ISOFET Off	IC TJ Shut-down	IC TJ Warn	-	-	-	0010 0000
0x04h	Interrupt1 Mask Control	r/w	Cap Test Done Mask	ADC Done Mask	-	Input Over-Current Mask	Input Over-Voltage Mask	PGS Not Ok Mask	-	TEMP Warn Mask	0010 0100
0x05h	Interrupt2 Mask Control	r/w	-	SAS DIS Mask	ISOFET Off Mask	IC TJ Shut-down Mask	IC TJ Warn Mask	-	-	-	0010 0101
0x06h	Backup Cap Threshold	r/w	-	-	ICH		PGS Threshold				0011 1111
0x07h	TEMP Warn Threshold	r/w	-	-	-	Temp ADC Warn Level					0001 1111
0x08h	-	-	-	-	-	-	-	-	-	-	0001 1111
0x09h	ADC Source Select	r/w	-	-	-	Backup Voltage	-	Temp Pin	Input Current	Input Voltage	0000 0000
0x0Ah	ADC Input Voltage Data	r	VIN High Byte								0000 0000
0x0Bh		r	-	-	-	-	-	-	VIN Low Byte		0000 0000
0x0Ch	ADC Input Current Data	r	I_IN High Byte								0000 0000
0x0Dh		r	-	-	-	-	-	-	I_IN Low Byte		0000 0000
0x0Eh	ADC TEMP Voltage Data	r	TEMP High Byte								0000 0000
0x0Fh		r	-	-	-	-	-	-	TEMP Low Byte		0000 0000
0x12h	ADC Backup Voltage Data1	r	VSTRG1 High Byte								0000 0000
0x13h		r	-	-	-	-	-	-	VSTRG1 Low Byte		0000 0000
0x14h	ADC Backup Voltage Data2	r	VSTRG2 High Byte								0000 0000
0x15h		r	-	-	-	-	-	-	VSTRG2 Low Byte		0000 0000
0x16h	Cap Test Timer	r	Cap Test Timer Low Byte								0000 0000
0x17h		r	Cap Test Timer High Byte								0000 0000
0x1Bh	VIN Recover Control	r/w							LDO_EN	VIN Recover mode	0000 0000
0x1Fh	Reserve	r	-	Reserve (13)							0011 0011

Register Map *(continued)*

Addr	Register	Type	D7	D6	D5	D4	D3	D2	D1	D0	Reset State
0x20h	Sys Control 2	r/w	Reserve (13)	Input ILIMT Set	Reserve (13)	Reserve (13)	Buck Fsw			Force Buck Release	1000 1000
0x21h	Sys Control 3	r/w	Internal ILIM Threshold			DVDT		TPOR		EN	0000 0001
0x22h	Sys Control 4	r/w	-	-	-	-	ILIM_EN	ILIM_Tune			0000 0000

NOTE:
13) Reserved bits. DO NOT write different values to these bits in application.

Register Name: Vendor ID, 00h (read only)

Name	Bits	Default Value	Description
Fab	D[7:6]	00	Fab location.
Major Rev	D[5:4]	00	Major revision.
Minor Rev	D[3:2]	00	Minor revision.
Vendor ID	D[1:0]	00	Vendor ID.

Register Name: System Control 1, 01h (read/write)

Name	Bits	Default Value	Description
Start Cap Test	D[3]	0	Cap test start enable bit. 1: starts the capacitance test on the backup capacitors. Resets to 0 after the cap test completes automatically. 0: cap test function is disabled. The LDO_EN bit is recommended to be set to 1 before the capacitance test if VIN is lower than 3.8V. The LDO_EN bit is recommended to be disabled after the cap test is completed.
Start ADC	D[2]	0	ADC converting enable bit. 1: starts ADC conversion. Resets to 0 after the cap test completes automatically. 0: no ADC converting event. The LDO_EN bit is recommended to be set to 1 before starting ADC if both VIN and VB are lower than 3.8V. Disable the LDO_EN bit after ADC is completed.
ENCH	D[0]	1	Backup boost enable bit, not writable in buck mode. 1: enable boost charge function. 0: disable boost charge function. This bit will not affect the buck release after V_{STRG} is charged high even if ENCH is set to 0.

Register Name: Interrupt1 Status, 02h (read/write)

Name	Bits	Default Value	Description
Cap Test Done	D[7]	0	Cap test complete indicating bit. 1: capacitance test completes and the discharge time is stored in the Cap Test Timer registers. Generates an interrupt on INT if unmasked. Write 1 to this bit to reset it to 0 and reset the interrupt event. 0: no cap test event occurs.
ADC Done	D[6]	0	ADC converting complete indicating bit. 1: ADC conversion completes. Generates an interrupt on INT if unmasked. Write 1 to this bit to reset it to 0 and reset the interrupt event. 0: no ADC event occurs.
Input Over Current	D[4]	0	Trigger VIN to the VB current limit indicating bit. 1: input current triggers the current limit. Generates an interrupt on INT if unmasked. After the input current limit event disappears, write 1 to this bit to reset it to 0 and reset the interrupt event. 0: no input current limit event occurs.
Input Over Voltage	D[3]	0	Over-voltage on OVP indicating bit. 1: OVP voltage is above the OVP threshold. Generates an interrupt on INT if unmasked. After the over-voltage event disappears, write 1 to this bit to reset it to 0 and reset the interrupt event. 0: no over-voltage event occurs.
PGS Not OK	D[2]	1	Storage voltage power not good indicating bit. 1: V_{STRG} is below the PGS threshold, reflects to PGS and generates an interrupt on INT if unmasked. After V_{STRG} rises again, write 1 to this bit to reset it to 0 and reset the interrupt event. PGS resets to high automatically after V_{STRG} rises again. 0: the V_{STRG} power does not drop below the PGS threshold.
TEMP Warn	D[0]	0	TEMP temperature sensor voltage-high warn indication bit. 1: external temperature sensor on TEMP is higher than Temp ADC Warn Level (must be higher than, not equal to, this warn level). Generates interrupt on INT if unmasked. If new ADC result from TEMP is lower than this threshold, write 1 to this bit to reset it to 0 and reset the interrupt event. 0: no TEMP ADC result, or TEMP ADC result is lower than Temp ADC Warn Level.

Register Name: Interrupt2 Status, 03h (read/write)

Name	Bits	Default Value	Description
SAS DIS	D[6]	0	SAS-forced buck mode indicating bit. 1: IC is disabled by the SAS signal and forced into buck mode. This bit generates an interrupt on INT if unmasked. After SAS resets to low, write 1 to this bit to reset it to 0 and reset the interrupt event. 0: no SAS force buck event occurs.
ISOFET Off	D[5]	1	VIN to VB MOSFET off indicating bit. 1: input ISOFET is off, generates an interrupt on INT if unmasked. After the ISOFET turns on again, write 1 to this bit to reset it to 0 and reset the interrupt event. 0: ISOFET is always on.
IC TJ Shut down	D[4]	0	Over-temperature protection indicating bit. 1: IC junction temperature is above 150°C, generates an interrupt on INT if unmasked. After the temperature drops below 125℃°C, write 1 to this bit to reset it to 0 and reset the interrupt event. The MP5515 resumes working when the temperature drops, even if the interrupt signal is not cleared. 0: no OTP occurs.
IC TJ Warn	D[3]	0	High temperature warning bit. 1: IC junction temperature is above 125°C, generates an interrupt on INT if unmasked. After the temperature drops below 100℃°C, write 1 to this bit to reset it to 0 and reset the interrupt event. 0: no 125°C, high junction temperature occurs.

Register Name: Interrupt1 Mask Control, 04h (read/write)

Name	Bits	Default Value	Description
Cap Test Done_Mask	D[7]	0	Mask cap test complete interrupt. 1: mask cap test done interrupt. Cap Test Done status bit is set after the event, but this bit suppresses the interrupt signal on INT. 0: Cap Test Done interrupt can work.
ADC Done_Mask	D[6]	0	Mask ADC complete interrupt. 1: mask ADC conversion complete interrupt. ADC Done status bit sets after the event, but this bit suppresses the interrupt signal on INT. 0: ADC Done interrupt can work.
Input Over Current_Mask	D[4]	0	Mask VIN to VB current limit interrupt. 1: mask input current limit event interrupt. Input Over-Current status bit sets after the event, but this bit suppresses the interrupt signal on INT. 0: Input Over-Current event interrupt can work.
Input Over Voltage_Mask	D[3]	0	Mask OVP interrupt. 1: mask OVP pin over-voltage interrupt event. This bit sets after the event, but suppresses the interrupt signal on INT. 0: OVP interrupt can work.
PGS Not OK_Mask	D[2]	1	Mask PGS power not good interrupt. 1: mask PGS power not good interrupt. PSG Not OK status bit sets after the event, but this bit suppresses the interrupt signal on INT. 0: PGS interrupt can work.

TEMP Warn_Mask	D[0]	0	Mask TEMP pin temperature sensor warning interrupt. 1: mask external temperature warn interrupt. TEMP Warn status bit sets after the event, but this bit suppresses the interrupt signal on INT. 0: TEMP ADC warn interrupt can work.

Register Name: Interrupt2 Mask Control, 05h (read/write)

Name	Bits	Default Value	Description
SAS DIS_Mask	D[6]	0	Mask interrupt of SAS force buck event. 1: mask interrupt of SAS forced buck event. SAS DIS status bit sets after the event, but this bit suppresses the interrupt signal on INT. 0: SAS forced buck event can generate interrupt.
ISOFET Off_Mask	D[5]	1	Mask interrupt of ISOFET off event. 1: mask interrupt of ISOFET off event. ISOFET Off status bit sets after the event, but this bit suppresses the interrupt signal on INT. 0: ISOFET Off interrupt can work.
IC TJ Shutdown_Mask	D[4]	0	Mask OTP interrupt. 1: mask OTP interrupt. IC TJ Shutdown status bit sets after the event, but this bit suppresses the interrupt signal on INT. 0: OTP interrupt can work.
IC TJ Warn_Mask	D[3]	0	Mask interrupt of high temperature warning. 1: mask IC junction temperature warning interrupt. IC TJ Warn status bit sets after the event, but this bit suppresses the interrupt signal on INT. 0: high junction temperature warning interrupt can work.

Register Name: Backup Cap Threshold, 06h (read/write)

Name	Bits	Default Value	Description
ICH	D[5:4]	11	Set boost switching peak current limit when ICH is floating. 00: 0.5A 01: 1A 10: 1.5A 11: 2A
PGS Threshold	D[3:0]	1111	Programmable PGS falling threshold from 80% (0000) to 95% (1111) with 1% step size.

Register Name: Temp Warn Threshold, 07h (read/write)

Name	Bits	Default Value	Description
TEMP ADC Warn Level	D[4:0]	1 1111	Sets the warning level for TEMP pin voltage ADC results (from external sensor). High bits of TEMP ADC results are compared with this warn level.

Register Name: ADC Source Select, 09h (read/write)

Name	Bits	Default Value	Description
Backup Voltage	D[4]	0	1: selects ADC conversion of the backup voltage. 0: disables ADC conversion of the backup voltage.
TEMP Pin	D[2]	0	1: selects ADC conversion of TEMP sensor voltage. 0: disables ADC conversion of TEMP sensor voltage.
Input Current	D[1]	0	1: selects ADC conversion of the input current signal. 0: disables ADC conversion of the input current signal. The input current is monitored through ILIM. When the current triggers the input current limit, the ILIM voltage signal is 1.09V. Calculate the current based on the R_{ILIM} setting.
Input Voltage	D[0]	0	1: selects ADC conversion of the input voltage. 0: disables the ADC conversion of the input voltage.

Register Name: ADC Results, 0Ah, 0Bh, 0Ch, 0Dh, 0Eh, 0Fh, 12h, 13h, 14h, 15h (read only)

Name	Bits	Default Value	Description
ADC Input Voltage Data	0Ah D[7:0]	0000 0000	High bits of VIN ADC results.
	0Bh D[1:0]	00	Low bits of VIN ADC results. LSB = 18.4V/1023 (V)
ADC Input Current Data	0Ch D[7:0]	0000 0000	High bits of input current ADC results.
	0Dh D[1:0]	00	Low bits of input current ADC results. V_LSB = 1.28/1023 (V) IN = V_LSB x BIN2DEC(D[9:0]) x 64.26/R_{ILIM} + 0.241/R_{ILIM} + 0.08 (A) Where R_{ILIM} is in kΩ.
ADC TEMP Voltage Data	0Eh D[7:0]	0000 0000	High bits of TEMP voltage ADC results.
	0Fh D[1:0]	00	Low bits of TEMP voltage ADC results. LSB = 1.28/1023 (V)
ADC Backup Voltage Data1	12h D[7:0]	0000 0000	High bits of backup storage voltage ADC1 results.
	13h D[1:0]	00	Low bits of backup storage voltage ADC1 results. LSB = 40.1/1023 (V)
ADC Backup Voltage Data2	14h D[7:0]	0000 0000	High bits of backup storage voltage ADC2 results.
	15h D[1:0]	00	Low bits of backup storage voltage ADC2 results. LSB = 40.1/1023 (V)

Register Name: Cap Test Timer, 16h, 17h (read only)

Name	Bits	Default Value	Description
Cap Test Timer	14h D[7:0]	0000 0000	Low bits of cap test timer results, LSB = 1ms.
	15h D[7:0]	0000 0000	High bits of cap test timer results.

Register Name: VIN Recover Control, 1Bh (read/write)

Name	Bits	Default Value	Description
LDO_EN	D[1]	0	0: disables the LDO from STRG to VCC. 1: enable the LDO from STRG to VCC. It is recommended to only enable this LDO during the ADC or cap test if both VIN and VB are lower than 3.8V. Disable the LDO_EN bit after the ADC or cap test is completed.
VIN Recover Mode	D[0]	0	0: works in buck mode until VB_UVLO is triggered after VIN recovers. 1: exits buck mode and charges Vs again once VIN recovers during the buck condition.

Register Name: System Control2, 20h (read/write)

Name	Bits	Default Value	Description
Input ILIM Set	D[6]	0	1: input current limit is set by internal circuit. 0: input current limit is set by external ILIM pin resistor.
Buck Fsw	D[3:1]	100	Program buck switching frequency. 000: 270kHz 001: 300kHz 010: 360kHz 011: 420kHz 100: 480kHz 101: 570kHz 110: 860kHz 111: 1.25MHz
Force Buck Release	D[0]	0	1: force IC into buck mode. After resetting this bit to 0, the MP5515 continues in buck mode until VB_UVLO is triggered.

Register Name: System Control3, 21h (read/write)

Name	Bits	Default Value	Description
Internal ILIM Threshold	D[7:5]	000	Internal input current limit option. 000: 6.6A 001: 5.6A 010, 011, 100: 2.3A 101: 1.3A 110: 4.7A 111: 3.4A
DVDT	D[4:3]	00	VB ramp up slew rate control bits. 00: 7.5V/ms 01:1.5V/ms 10: 1V/ms 11: 0.67V/ms
TPOR	D[2:1]		TPOR delay time program bits when TPOR floats. 00: 1.6ms 01: 8ms 10: 32ms 11: 64ms
EN	D[0]	1	Enable control bit. This bit is not writable during buck release mode unless VB_UVLO is triggered. 1: enable MP5515. 0: disable MP5515.

Register Name: System Control4, 22h (read/write)

Name	Bits	Default Value	Description
ILIM_EN	D[3]	0	1: disables ISOFET current limit function. The current limit function can be disabled, but the input over-current limit status bit is still set. 0: enables ISOFET current limit function.
ILIM_Tune	D[2:0]	000	Tune input current limit threshold. 000: keep 100% of the ILIM set current limit. 001: decrease 2% of the ILIM set current limit. 010: increase 2% of the ILIM set current limit. 011: decrease 4% of the ILIM set current limit. 100: increase 4% of the ILIM set current limit.

APPLICATION INFORMATION

Setting the Storage Voltage

Set the storage voltage by choosing the external feedback resistors R5 and R6 (see Figure 13).

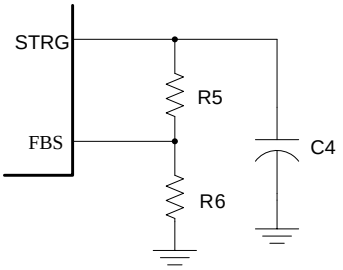


Figure 13: Storage Feedback Circuit

The storage voltage is determined by Equation (8):

$$V_{STORAGE} = (1+\frac{R5}{R6}) \times V_{FBS-REF} \quad (8)$$

Where $V_{FBS-REF}$ is 0.8V, typically. R5 and R6 are not critical for normal operation. Select an R6 value higher than 10kΩ to reduce the bleed current. Select an R6 value lower than 50kΩ to enhance noise immunity. For example, if R6 is 10kΩ, R5 can be calculated with Equation (9):

$$R5 = \frac{10k\Omega \times (V_{STORAGE} - V_{FBS-REF})}{V_{FBS-REF}} \quad (9)$$

For a 30V storage voltage, R5 is 365kΩ.

Table 3 lists recommended feedback resistance for different storage voltages.

Table 3: Resistor Pairs for $V_{STORAGE}$

$V_{STORAGE}$ (V)	R5 (kΩ)	R6 (kΩ)
12	140	10
20	240	10
30	365	10

Setting VIN Power Failure Threshold Voltage and VB Release Regulation Voltage

Set the release-trigger voltage by choosing the external feedback resistors R1 and R2 (see Figure 14). The release trigger voltage is determined by 0.99 x $V_{DET-REF}$, which is 0.792V.

The input power-failure release threshold can be calculated with Equation (10):

$$V_{PFI} = (1+\frac{R1}{R2}) \times 0.792V \quad (10)$$

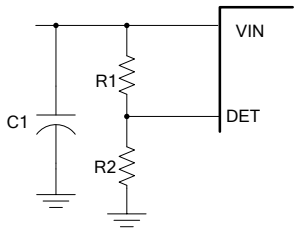


Figure 14: Release-Feedback Circuit

V_{DET} determines the release-trigger voltage, and V_{FBB} determines the VB release-regulation voltage (see Figure 15).

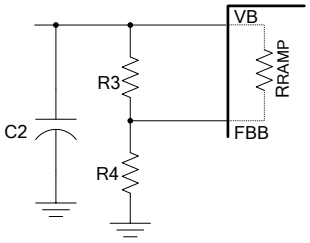


Figure 15: VB Regulation Feedback Circuit

The bus-regulation voltage can be calculated with Equation (11):

$$VB_{RLS} = (1+\frac{R3 // R_{RAMP}}{R4}) \times V_{FBB-REF} \quad (11)$$

Where $V_{FBS-REF}$ is 0.8V, typically, and R_{RAMP} is an equivalent resistor for stabilizing the circuit internally (typically 9MΩ).

R3 and R4 are related to buck-release stability. Since the release-buck mode works in constant-on-time (COT) mode, avoid using small resistor values that can affect the internal voltage ramp. Generally, choose R3 parallel to R4 ≥ 10kΩ for stable performance with C_B = 22~44μF.

Selecting the Storage Capacitor

The storage capacitor stores energy during normal operation and releases this energy to VB when VIN loses input power. Use a general-purpose electrolytic capacitor or low-profile POS capacitor for most applications. Select a storage capacitor with a voltage margin 20% higher than the targeted storage voltage. When choosing the capacitors, consider the capacitance reduction with the DC voltage offset. Different capacitors have different

capacitance de-rating performances. Choose a capacitor with a voltage rating high enough to guarantee enough capacitance.

The required capacitance depends on the length of the dying gasp for a typical application. Assume the bus release current is $I_{RELEASE}$ when the bus voltage is regulated at VB_{RLS} for the DC/DC converter. The storage is V_{STRG}, and the required dying gasp time is τ_{DASP}. The required storage capacitance can be calculated with Equation (12):

$$C_{STRG} = \frac{2 \times VB_{RLS} \times I_{RELEASE} \times \tau_{DASP}}{(V_{STRG}^2 - VB_{RLS}^2) \times Eff} \quad (12)$$

Where Eff is the energy-release efficiency in the buck converter (refer to the efficiency curve on page 11 for more detail). Select the proper storage capacitance to ensure enough capacitance for buck-power loss. If $I_{RELEASE}$ is 3A, τ_{DASP} is 20ms, $V_{STORAGE}$ is 28V, VB_{RLS} is 7.5V, and the efficiency is 90%, then the required storage capacitance is 1374μF.

Setting the Input Hot-Swap Current Limit

Connect a resistor from ILIM to AGND to set the current-limit value. For example, a 36.5kΩ resistor on ILIM sets the current limit to about 2A. Refer to the Input Current Limit section on page 18 for the current-limit calculation.

The MP5515 also supports an internal ILIM program function by setting the Input ILIM Set and Internal ILIM Threshold register bits through the I²C interface. Refer to register map description on page 33 for more detail.

Setting the Boost Peak-Current Limit

Connect a resistor from ICH to AGND to set the boost peak-inductor current. Refer to the Back-Up Voltage section on page 17 for the boost-peak current-limit setting calculation.

If ICH is floating, the boost peak-current limit can be programmed by the ICH register bits. The boost peak current is about 2A with a default ICH bits value of 11 (in typical 12V input and 10μH inductor conditions).

Selecting the Inductor

An inductor is necessary for supplying constant current to the load. Since boost mode and buck mode share the same inductor (and generally the buck-mode current is higher), an inductor supporting the buck-mode releasing current is recommended.

Select the inductor based on the buck-releasing mode. If the storage voltage is V_{STRG}, the bus-regulation voltage is VB_{RLS} with the buck running at a fixed 480kHz frequency. The inductance value can be calculated with Equation (13):

$$L = \frac{VB_{RLS}}{\Delta I_L \times F_{SW}} \times (1 - \frac{VB_{RLS}}{V_{STRG}}) \quad (13)$$

Where ΔI_L is the peak-to-peak inductor ripple current, which can be set at 20 - 40% of the full-releasing current. The inductor should not saturate under the maximum inductor peak current.

Setting the Power-On Reset Delay Time

Connect a capacitor 1nF or higher to TPOR to set the power-on-reset delay time. Leave this capacitor floating for the default delay time of around 1.5ms. Table 4 lists recommended capacitors for different delay times.

Table 4: Reset Delay vs. Capacitor Value

T_D (ms)	C_{TPOR} (nF)
10	10
100	100
500	500

Setting the Bus Voltage Rise Time

Connect a capacitor 1nF or higher to DVDT to set the bus voltage start-up slew rate and soft-start time. Leave this capacitor floating for the default soft-start slew rate (around 7.5V/ms and 1.6ms from 0V to 12V). Table 5 lists the recommended capacitors for different soft-start slew rates.

Table 5: Soft Start vs. Capacitor Value

Slew Rate (V/ms)	$C_{dv/dt}$ (nF)
3.9	10
0.39	100

VCC Power Supply

VCC is powered from VIN during start-up. An external load on VCC is not permitted. When VIN is lower than 3V, if PFI and INT signals are pulled up to VCC, use 100kΩ resistors to lower the sink current from VCC during start-up.

The MP5515 can start up from a 2.7V low-input power under temperatures 25°C or higher. If the temperature is lower than 25°C, the UVLO rises slightly. An external Schottky diode from VIN to VCC is suggested if the IC needs to start up with 2.7V under a low-temperature condition. This diode is suggested even if VIN is 3V at -40°C).

Selecting BST and CST Capacitance

The BST capacitor supplies power to the buck converter HS-FET. A 0.1~1μF ceramic capacitor is recommended for BST decoupling. The CST capacitor supplies power for the input hot-swap MOSFET and the VBO disconnecting MOSFET. The CST capacitor is charged by an internal charge pump. A 10nF ceramic capacitor is recommended. A CST capacitor with more than 47nF capacitance is not recommended since it affects the voltage charge-up slew rate.

STRG Capacitor Test Resistor

The MP5515 discharges the back-up capacitor through one external resistor from STRG to RTEST. The MOSFET from RTEST to GND is about 4.5Ω, and the discharge peak current must be limited below 500mA by an external resistor. Consider the 4.5Ω resistance if the selected RTEST resistor is close to it. Normally, a 1k~10kΩ discharge resistor is recommended for reducing the resistor size. Other resistor values should also be sufficient.

Selecting the Input Capacitor and TVS

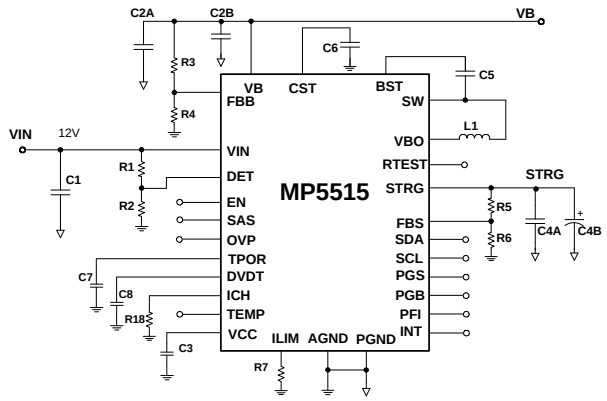
Capacitors at VIN are recommended to absorb possible voltage spikes during the input power turn-on, input switch hard-off (during power-off), or other special conditions. The application determines the capacitor. For example, if the input power trace is too long (with a higher parasitic inductance), during the input-switch hard-off period, more energy pumps into the input. This means more input capacitors are needed for the input voltage spike to stay in a safe range. A capacitor 0.1μF or larger is recommended.

Consider the inrush current requirements when selecting an input capacitor. Typically, more input capacitors result in a higher input-inrush current during hot-plugging. A smaller input capacitor is needed for a smaller inrush current. The MP5515 can work normally with a very small input capacitor or without an input capacitor. However, this leads to a possible high-voltage spike. An efficient solution is to add a TVS diode at the input to absorb the possible input voltage spike. Simultaneously, keep the inrush current small during hot-plugging. A typical TVS diode, like SMA6J13A, is recommended.

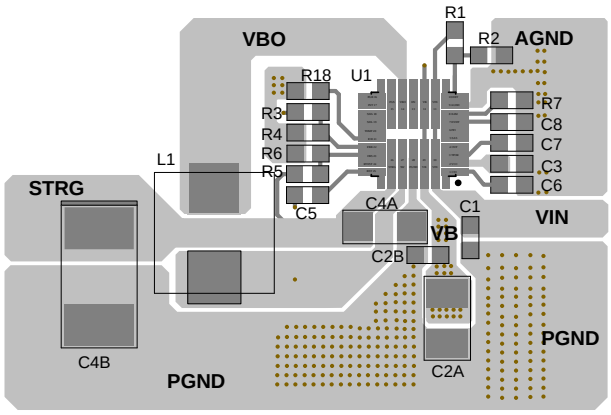
PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For best results, refer to Figure 16 and follow the guidelines below.

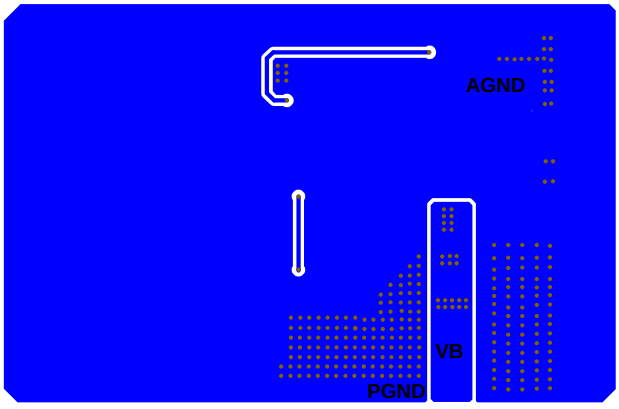
1. Connect the high-current paths (VIN, VB, VBO, SW, STRG, and PGND) with short, wide, and direct traces.
2. Keep the SW trace as short as possible while VBO is far from SW.
3. Place the decoupling capacitor across VB and PGND (as close as possible).
4. Place the decoupling capacitor across STRG and PGND (as close as possible).
   When using a large volume capacitor, a small ≥1μF ceramic capacitor is required. Place it as close to STRG and PGND as possible.
5. Place the decoupling capacitor across VCC and AGND (as close as possible).
6. Keep the switching node SW short and away from the feedback network.
7. The external feedback resistors should be placed next to FBB/FBS/DET.
8. Keep the BST voltage path (BST, C5 and SW) as short as possible.
9. Connect all signal grounds together and connected to PGND with a one-point connection.



Schematic for Layout



Top Layer



Bottom Layer

Figure 16: Recommended Layout

Design Example

Table 6 is a design example following the application guidelines for the following specifications.

Table 6: Design Example

Parameter	Symbol	Value	Units
Input voltage	V_{IN}	12	V
Storage voltage	V_{STRG}	30	V
Input P_{FAIL} threshold	V_{PFI}	8	V
Bus backup voltage	VB_{RLS}	7.5	V
Bus backup max load	$I_{RELEASE}$	5	A

See Figure 17 for a detailed application schematic. The waveforms are shown in the Typical Performance section. For more detailed device applications, please refer to the related evaluation board datasheet.

TYPICAL APPLICATION CIRCUIT

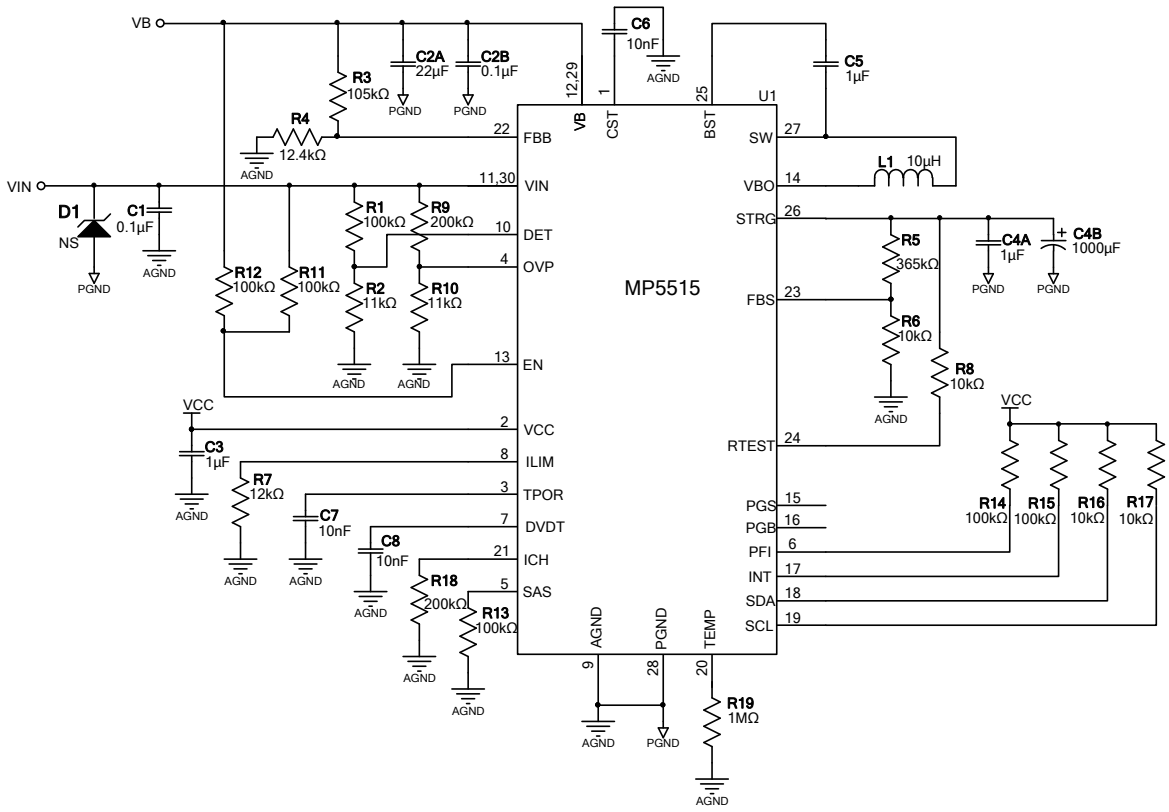
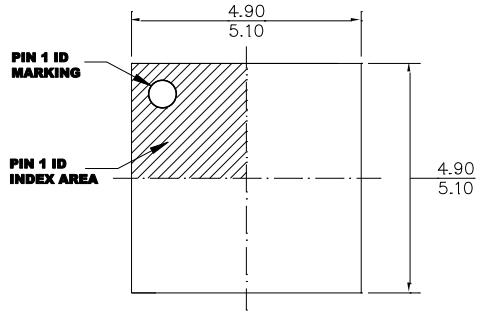


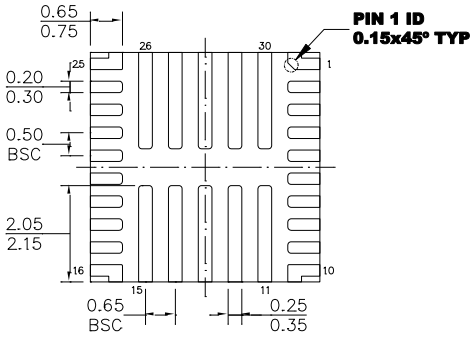
Figure 17: 12V Input, 30V Storage Typical Application Circuit

PACKAGE INFORMATION

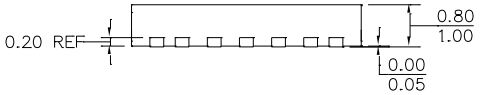
QFN-30 (5mmx5mm)



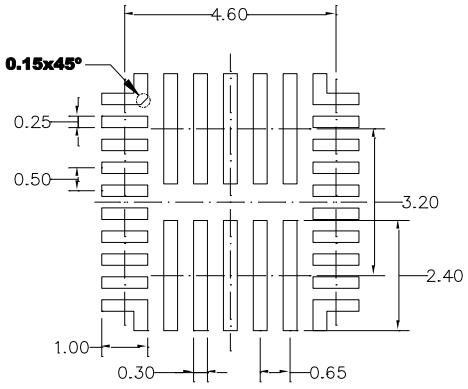
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
4) REFERENCEIS MO-220.
5) DRAWING IS NOT TO SCALE.

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