



# THE DATASHEET OF NUC100RC1AN



## Cortex™-M0

### 32-bit Microcontroller

#### 1 GENERAL DESCRIPTION

The NUC100 series are 32-bit microcontrollers with embedded ARM® Cortex™-M0 core for industrial control and applications need **high-speed serial interfaces**. The Cortex™-M0 is the newest ARM embedded processor with 32-bit performance and at a cost equivalent traditional 8-bit microcontroller.

The NUC100 series embeds Cortex™-M0 core running up to 50MHz with 32K/64K/128K-byte embedded flash and 4K/8K/16K-byte embedded SRAM. It also equips with plenty of peripheral devices, such as Timers, Watchdog Timer, RTC, PDMA, UART, SPI/SSP, I<sup>2</sup>C, I<sup>2</sup>S, PWM Timer, GPIO, 12-bit ADC, Analog Comparator, Low Voltage Detector and Brown-out detector.

#### 2 FEATURES

- Core
  - ARM® Cortex™-M0 core runs up to 50MHz.
  - One 24-bit system timer.
  - Low power sleep mode supports.
  - Single-cycle 32-bit hardware multiplier.
  - NVIC for the 32 interrupt inputs, each with 4-levels of priority.
  - Serial Wire Debug supports with 2 watchpoints/4 breakpoints.
- Widely operating voltage range from 2.5V to 5.5V
- Flash EPROM Memory
  - 32K/64K/128K bytes Flash EPROM for program code.
  - 4kB flash for ISP loader
  - Support ISP/IAP program code update
  - 512 byte page erase for flash
  - Configurable data flash address and size for 128kB system, fixed 4kB data flash for the 32kB and 64kB system.
  - Support 2 wire ICP update from ICE interface
  - Support fast parallel programming mode by external programmer.
- SRAM Memory
  - 4K/8K/16k bytes embedded SRAM.
  - Support PDMA mode





- PDMA (Peripheral DMA)
  - Support 9 channels PDMA for automatic data transfer between SRAM and peripherals.
- Clock Control
  - Flexible selection for different applications.
  - Build-in 22MHz OSC (Trimmed to 1%) for system operation, and low power 10KHz OSC for watchdog and wakeup sleep operation.
  - Support one PLL, up to 50MHz, for high performance system operation.
  - External 12MHz crystal input for USB and precise timing operating mode.
  - External 32 kHz crystal input for RTC function and low power system operation.
- GPIO
  - Four I/O modes:
    - ◆ Quasi bi-direction
    - ◆ Push-Pull output
    - ◆ Open-Drain output
    - ◆ Input only with high impedance
  - TTL/Schmitt trigger input selectable.
  - I/O pin can be configured as interrupt source with edge/level setting.
  - High driver and high sink IO mode support.
- Timers
  - 4 sets of 24-bit timer with 8-bit pre-scaler.
  - Counter auto reload.
- Watch Dog Timer
  - Default ON/OFF by configuration setting
  - Multiple clock sources
  - 8 selectable time out period from 6ms ~ 3.0sec (depends on clock source)
  - WDT can wake up power down/sleep.
  - Interrupt or reset selectable on watchdog time-out.
- RTC
  - Support software compensation by setting frequency compensate register (FCR)
  - Support RTC counter (second, minute, hour) and calendar counter (day, month, year)
  - Support Alarm registers (second, minute, hour, day, month, year)
  - Switchable 12-hour or 24-hour mode
  - Automatic leap year recognition
  - Support time tick interrupt
  - Support wake up function.
- PWM/Capture
  - Built-in up to four 16-bit PWM generators provide eight PWM outputs or four complementary paired PWM outputs.
  - Each PWM generator equipped with one clock source selector, one clock divider, one 8-bit pre-scaler and one Dead-Zone generator for complementary paired PWM.
  - PWM interrupt synchronous to PWM period.
  - Up to eight 16-bit digital Capture timers(shared with PWM timers) provide eight rising/falling capture inputs.
  - Support Capture interrupt



- UART
  - Up to three compatible 16550 UART devices.
  - UART ports with flow control (TX, RX, CTS and RTS)
  - UART0 with 64-byte FIFO is for high speed
  - UART1/2(optional) with 16-byte FIFO for standard device
  - Support IrDA(SIR) function
  - Programmable baud-rate generator up to 1/16 system clock
  - Support PDMA mode
- SPI
  - Up to four sets of SPI device.
  - Master up to 16 Mbps / Slave up to 10 Mbps.
  - Support MICROWIRE/SPI master/slave mode (SSP)
  - Full duplex synchronous serial data transfer
  - Variable length of transfer data from 1 to 32 bits
  - MSB or LSB first data transfer
  - Rx and Tx on both rising or falling edge of serial clock independently
  - 2 slave/device select lines when it is as the master, and 1 slave/device select line when it is as the slave
  - Byte Sleeping mode in 32-bit transmission
  - Support PDMA mode
- I<sup>2</sup>C
  - Two sets of I<sup>2</sup>C device.
  - Master/Slave up to 1Mbit/s ( Fast-mode Plus )
  - Bidirectional data transfer between masters and slaves
  - Multi-master bus (no central master).
  - Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
  - Serial clock synchronization allows devices with different bit rates to communicate via one serial bus.
  - Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer.
  - Programmable clocks allow versatile rate control.
  - I<sup>2</sup>C-bus controllers support multiple address recognition ( two slave address with mask option)
- I<sup>2</sup>S
  - Interface with external audio CODEC
  - Operate as either master or slave mode
  - Capable of handling 8, 16, and 32 bit word sizes
  - Mono and stereo audio data supported
  - I<sup>2</sup>S and MSB justified data format supported
  - Two 8 word FIFO data buffers are provided, one for transmit and one for receive
  - Generates interrupt requests when buffer levels cross a programmable boundary
  - Support two DMA requests, one for transmit and one for receive

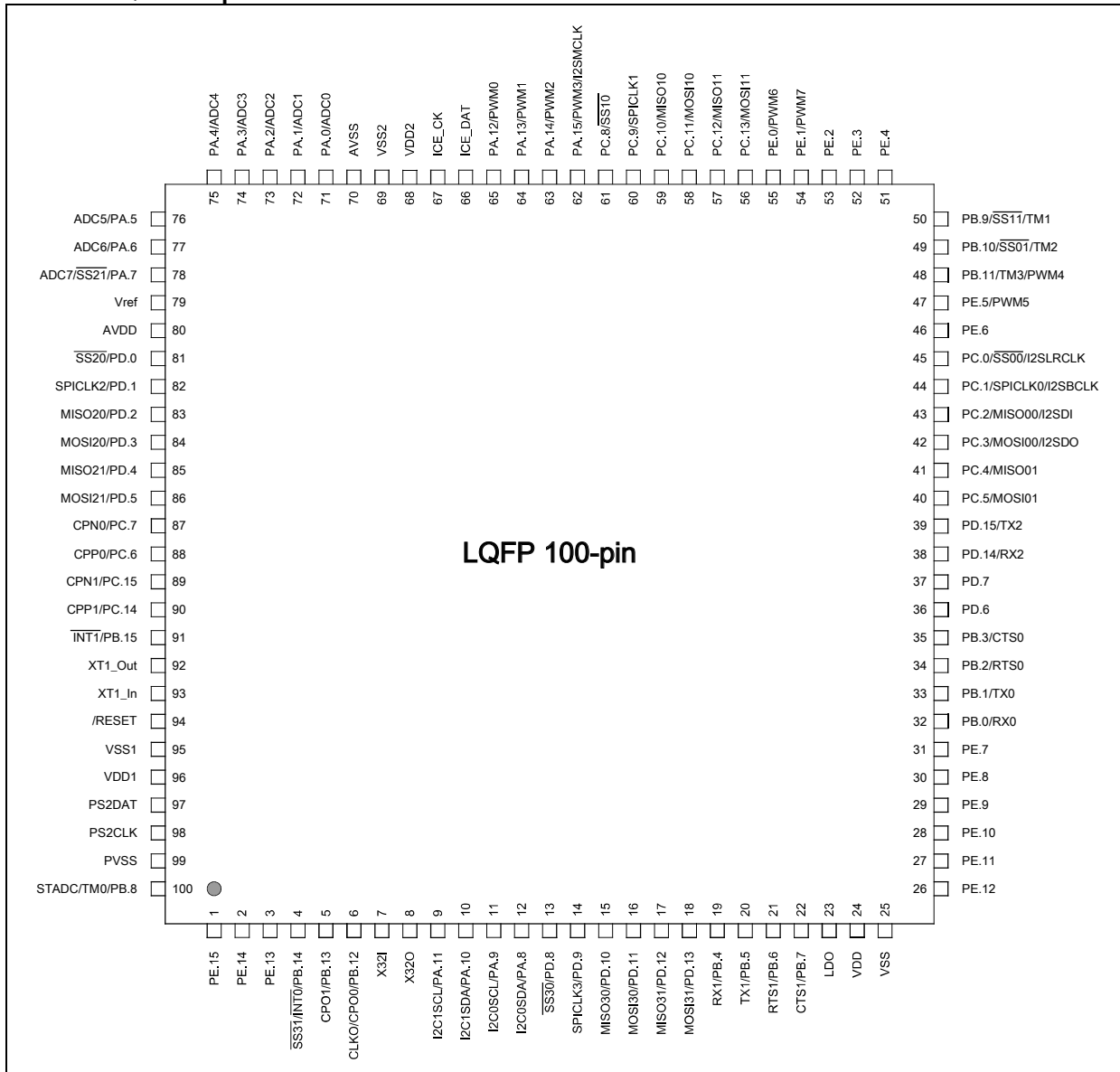


- ADC
  - 12-bit SAR ADC with 800ksps
  - Up to 8-ch single-end mode or 4-ch differential-end mode
  - Single scan/single cycle scan/continuous scan
  - Each channel with individual result register
  - Scan on enabled channels
  - Threshold voltage detection
  - Conversion start by S/W, external pins
- Analog Comparator
  - Up to 2 comparator analog modules
  - External input or internal banggap voltage selectable at negative node
  - Interrupt when compare result change
  - Power down wake up
- Temperature sensor
  - One temperature sensor built-in with 1°C resolution.
- Brown-out detector
  - with 4 levels: 4.5V/3.8V/2.7V/2.4V
  - Support Brownout Interrupt and Reset option
- LDO
  - One LDO is built-in.
- Low Voltage Reset
- Operating Temperature: -40°C~85°C
- Packages:
  - All Green package (RoHS)
    - ◆ LQFP 100-pin / 64-pin / 48-pin



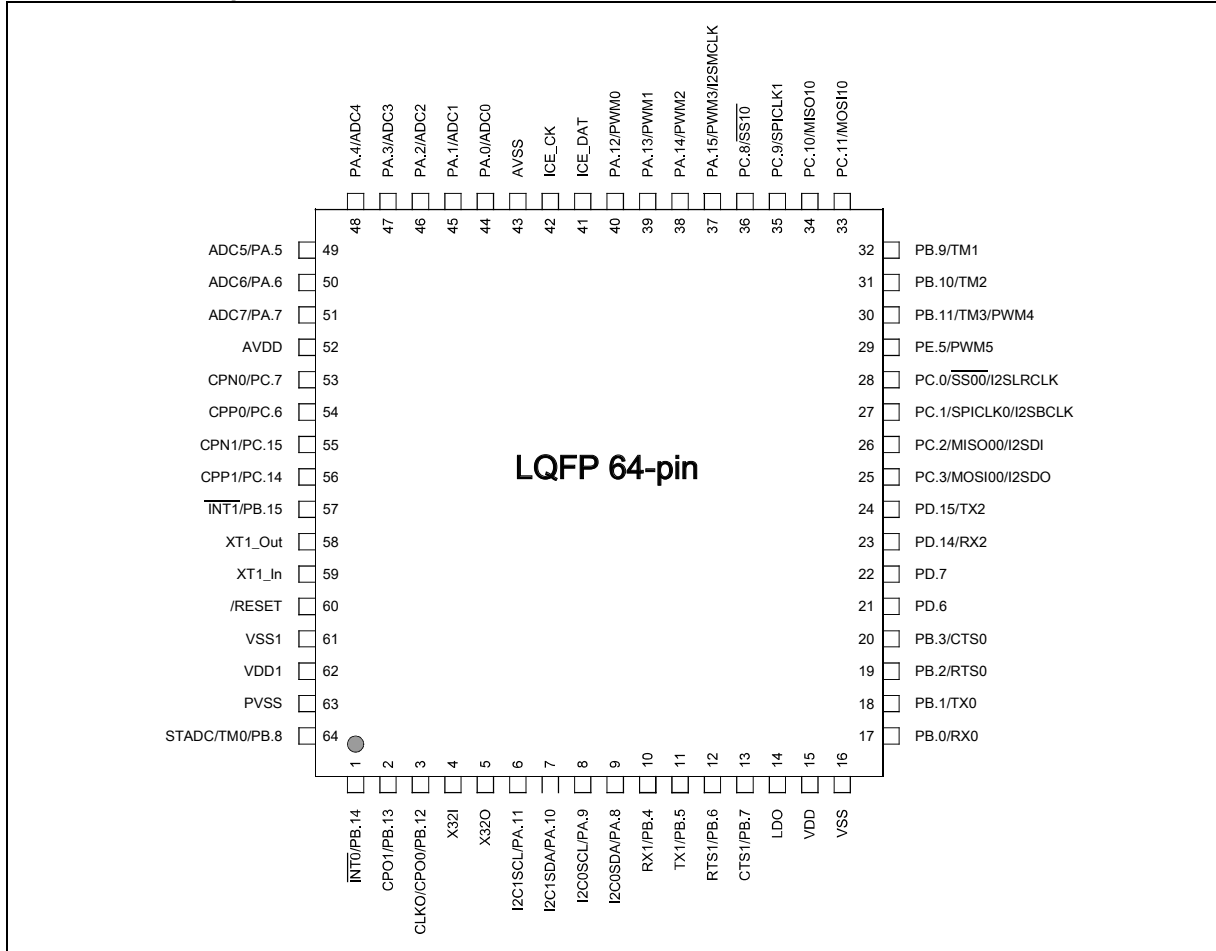
### 3 PIN DIAGRAM

- LQFP 100 pin



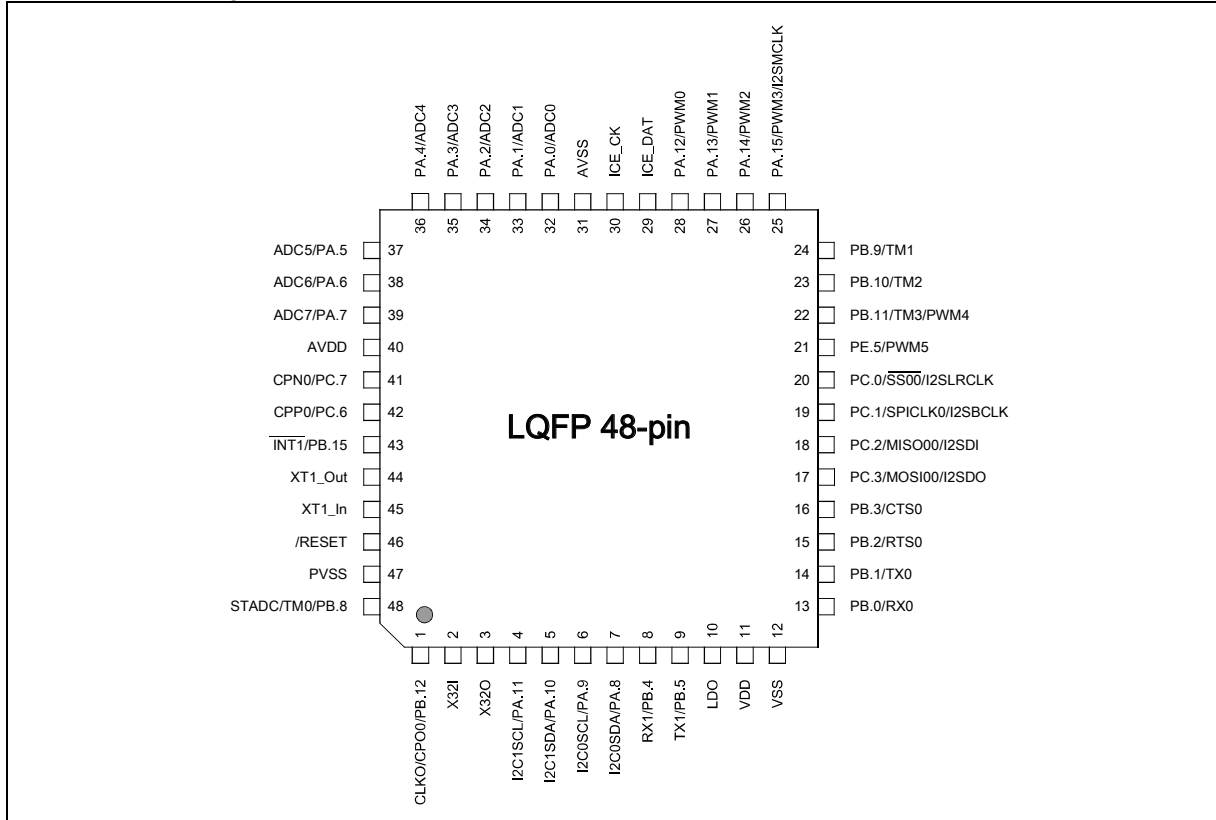


- LQFP 64 pin



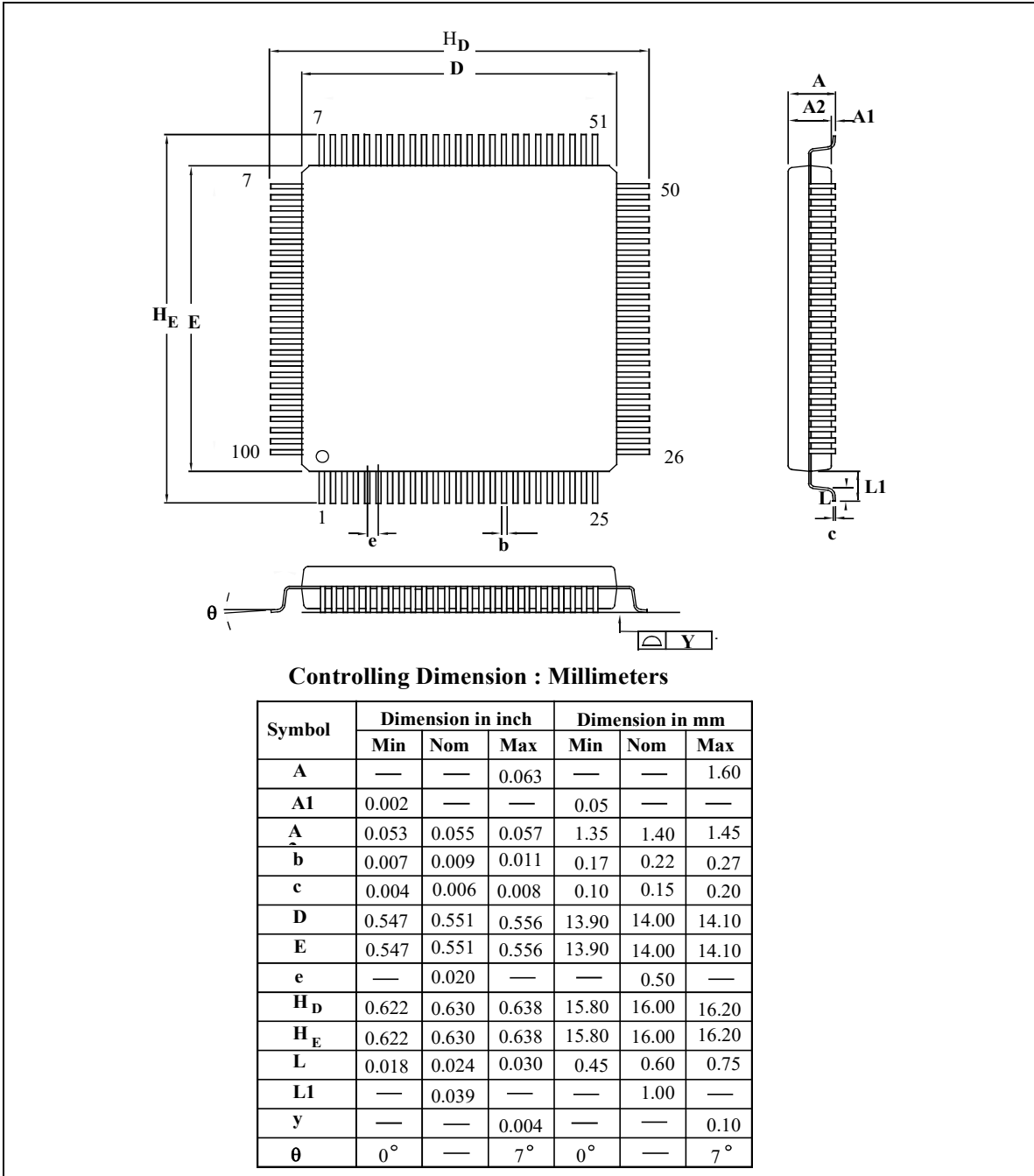


- LQFP 48 pin

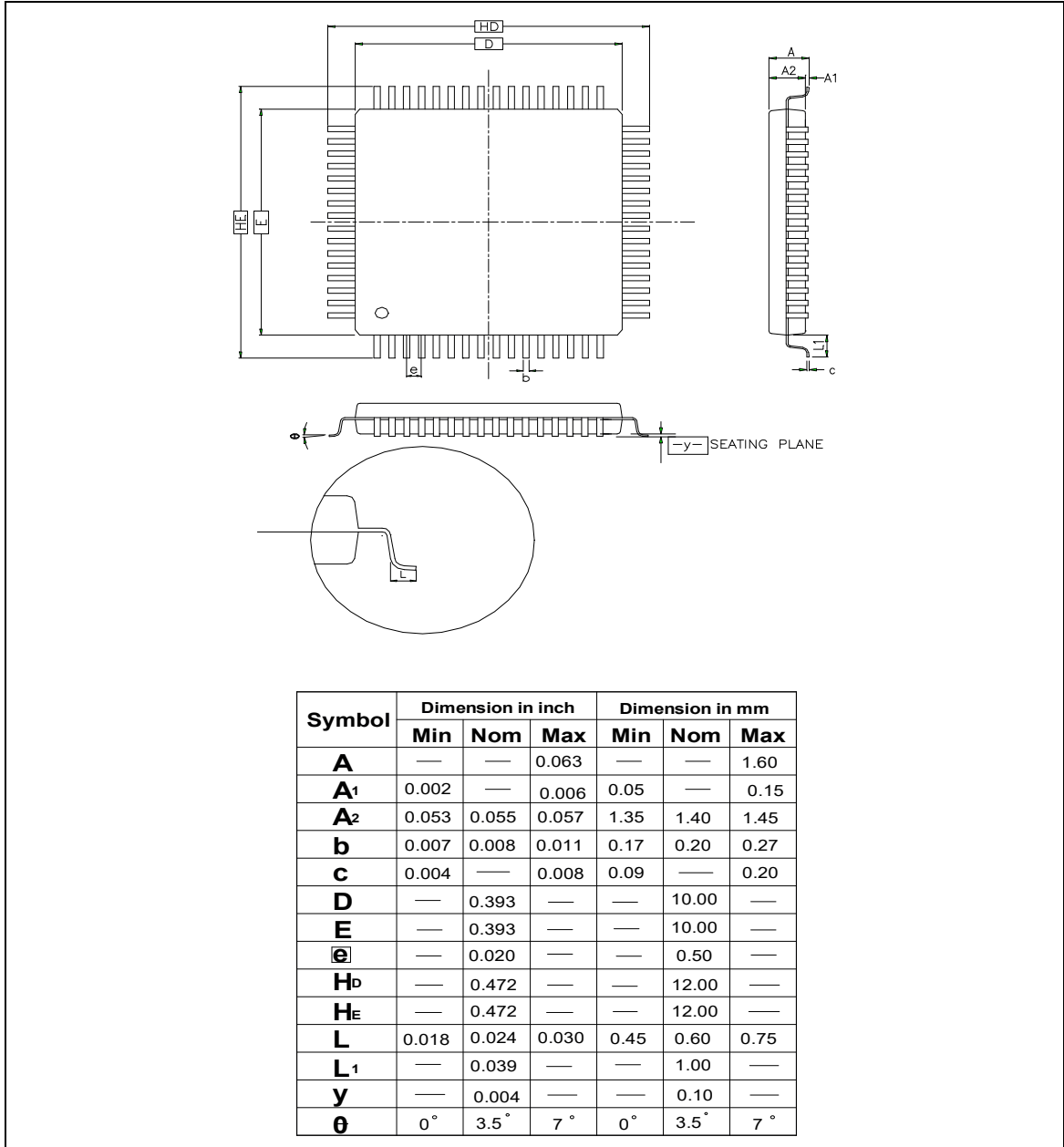


#### 4 PACKAGE DIMENSIONS

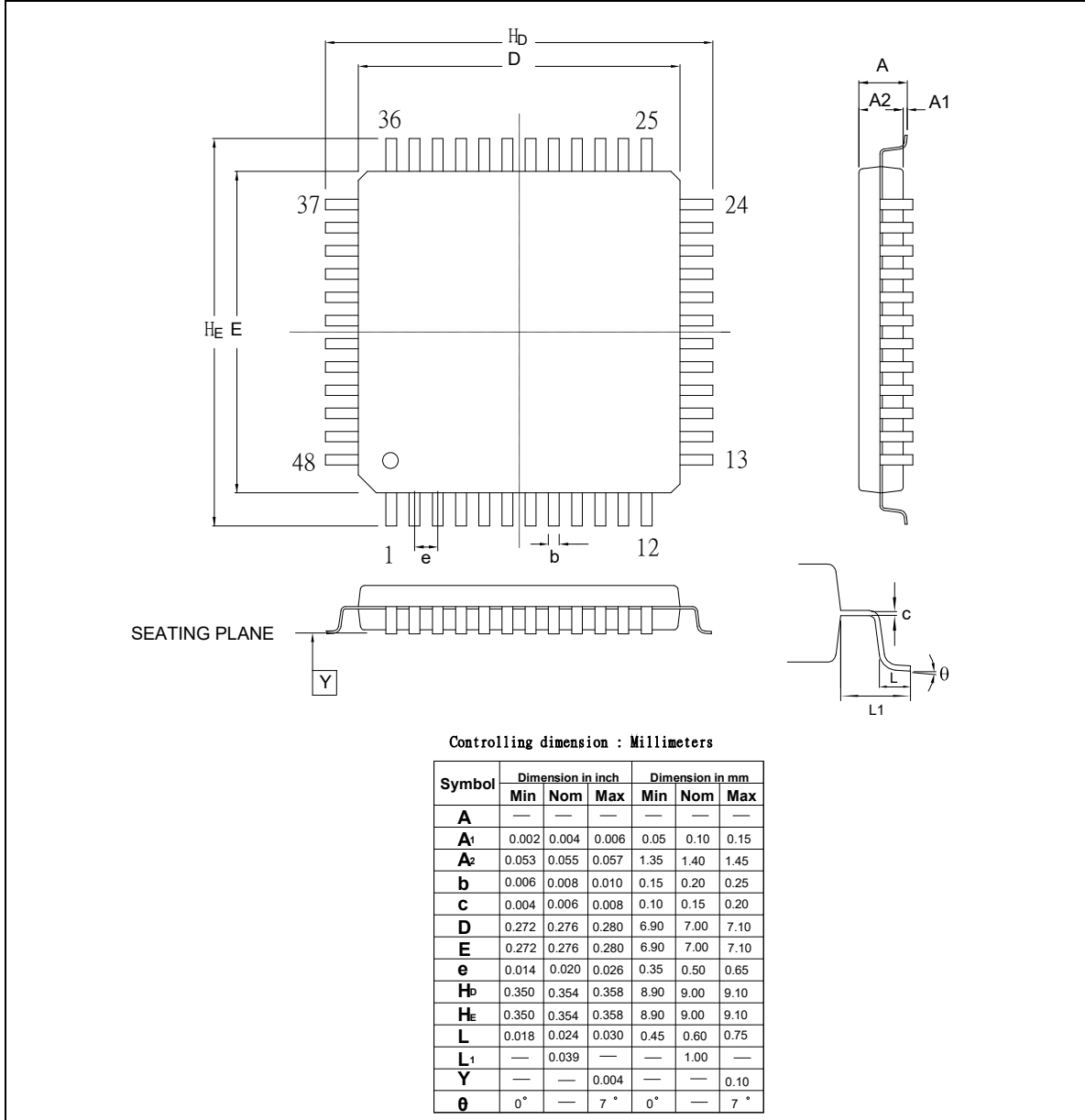
##### 4.1 100L LQFP (14x14x1.4mm footprint 2.0mm)



4.2 64L LQFP (10x10x1.4mm footprint 2.0mm)



4.3 48L LQFP (7x7x1.4mm footprint 2.0mm)





## 5 ELECTRICAL CHARACTERISTICS

### 5.1 DC Characteristics

(VDD-VSS=3.3V, TA = 25°C, F<sub>OSC</sub> = 50Mhz unless otherwise specified.)

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Operation voltage	V <sub>DD</sub>	2.5		5.5	V	V <sub>DD</sub> = 2.5V ~ 5.5V up to 50MHz
Power Ground	V <sub>SS</sub> AV <sub>SS</sub>	-0.3			V	
LDO Output Voltage (bypass = 0)	V <sub>LDO</sub>	-10%	2.45	+10%	V	
LDO Output Voltage (bypass = 0)	V <sub>LDO</sub>	-10%	V <sub>DD</sub>	+10%	V	V <sub>DD</sub> < 2.7V
Analog Operating Voltage	AV <sub>DD</sub>	0		V <sub>DD</sub>	V	
Analog Reference Voltage	V <sub>ref</sub>	0		AV <sub>DD</sub>	V	
Operating Current	I <sub>DD1</sub>		42		mA	Normal run, all peripherals on
	I <sub>DD2</sub>		26		mA	Normal run, all peripherals off
	I <sub>DD3</sub>		10		uA	Deep sleep mode, all peripherals off
Input Current PA~PE	I <sub>IN1</sub>	-60	-	+15	μA	V <sub>DD</sub> = 5.5V, V <sub>IN</sub> = 0V or V <sub>IN</sub> =V <sub>DD</sub>
Input Current at /RESET <sup>[1]</sup>	I <sub>IN2</sub>	-55	-45	-30	μA	V <sub>DD</sub> = 5.5V, V <sub>IN</sub> = 0.45V
Input Leakage Current PA~PE	I <sub>LK</sub>	-2	-	+2	μA	V <sub>DD</sub> = 5.5V, 0 < V <sub>IN</sub> < V <sub>DD</sub>
Logic 1 to 0 Transition Current PA~PE (Quasi-bidiretional mode)	I <sub>TL</sub> <sup>[*3]</sup>	-650	-	-200	μA	V <sub>DD</sub> = 5.5V, V <sub>IN</sub> < 2.0V
Input Low Voltage P0, P1, P2, P3, P4 (TTL input)	V <sub>IL1</sub>	-0.3	-	1.0	V	V <sub>DD</sub> = 4.5V
		-0.3	-	0.6		V <sub>DD</sub> = 2.5V
Input High Voltage P0, P1, P2, P3, P4 (TTL input)	V <sub>IH1</sub>	2.2	-	V <sub>DD</sub> + 0.2	V	V <sub>DD</sub> = 5.5V
		1.5	-	V <sub>DD</sub> + 0.2		V <sub>DD</sub> = 3.0V
Input Low Voltage XT1 <sup>[*2]</sup>	V <sub>IL3</sub>	0	-	0.8	V	V <sub>DD</sub> = 4.5V
		0	-	0.4		V <sub>DD</sub> = 3.0V
Input High Voltage XT1 <sup>[*2]</sup>	V <sub>IH3</sub>	3.5	-	V <sub>DD</sub> + 0.2	V	V <sub>DD</sub> = 5.5V
		2.4	-	V <sub>DD</sub> + 0.2		V <sub>DD</sub> = 3.0V

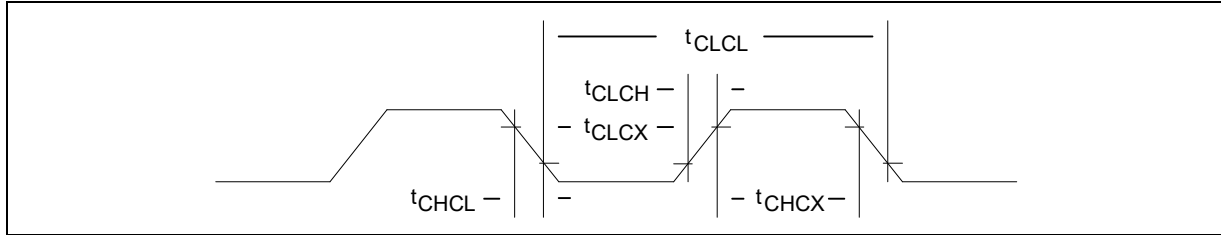


Input Low Voltage X32I <sup>[*2]</sup>	V <sub>IL4</sub>	0	-	0.8		
		0	-	0.4		
Input High Voltage X32O <sup>[*2]</sup>	V <sub>IH4</sub>	3.5	-	V <sub>DD</sub> +0.2		
		2.4	-	V <sub>DD</sub> +0.2		
Negative going threshold (Schmitt input), /RST	V <sub>ILS</sub>	-0.5	-	0.3V <sub>DD</sub>	V	
Positive going threshold (Schmitt input), /RST	V <sub>IHS</sub>	0.7V <sub>DD</sub>	-	V <sub>DD</sub> +0.5	V	
Internal /RST pin pull up resistor	R <sub>RST</sub>	50		100	KΩ	
Hysteresis voltage	V <sub>HY</sub>				V	
Source Current PA~PE (Quasi-bidirectional Mode)	I <sub>SR11</sub>	-300	-370	-450	μA	V <sub>DD</sub> = 4.5V, V <sub>S</sub> = 2.4V
	I <sub>SR12</sub>	-50	-70	-90	μA	V <sub>DD</sub> = 2.7V, V <sub>S</sub> = 2.2V
	I <sub>SR12</sub>	-40	-60	-80	μA	V <sub>DD</sub> = 2.5V, V <sub>S</sub> = 2.0V
Source Current PA~PE (Push-pull Mode)	I <sub>SR21</sub>	-20	-24	-28	mA	V <sub>DD</sub> = 4.5V, V <sub>S</sub> = 3.0V
	I <sub>SR22</sub>	-4	-6	-8	mA	V <sub>DD</sub> = 2.7V, V <sub>S</sub> = 2.2V
	I <sub>SR22</sub>	-3	-5	-7	mA	V <sub>DD</sub> = 2.5V, V <sub>S</sub> = 2.0V
Sink Current PA~PE (Quasi-bidirectional and Push-pull Mode)	I <sub>SK1</sub>	10	16	20	mA	V <sub>DD</sub> = 4.5V, V <sub>S</sub> = 0.45V
	I <sub>SK1</sub>	7	10	13	mA	V <sub>DD</sub> = 2.7V, V <sub>S</sub> = 0.45V
	I <sub>SK1</sub>	6	9	12	mA	V <sub>DD</sub> = 2.5V, V <sub>S</sub> = 0.45V
Brownout voltage with BOV_VL [1:0] =00b	V <sub>BO2.2</sub>	2.1	2.2	2.3	V	
Brownout voltage with BOV_VL [1:0] =01b	V <sub>BO2.7</sub>	2.6	2.7	2.8	V	
Brownout voltage with BOV_VL [1:0] =10b	V <sub>BO3.8</sub>	3.7	3.8	3.9	V	
Brownout voltage with BOV_VL [1:0] =11b	V <sub>BO4.5</sub>	4.4	4.5	4.6	V	
Hysteresis range of BOD voltage	V <sub>Bh</sub>	30	-	150	mV	V <sub>DD</sub> = 2.4V~5.5V

**Notes:**

1. /RST pin is a Schmitt trigger input.
2. XTAL1 is a CMOS input.
3. Pins of P0, P1, P2, P3 and P4 can source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when Vin approximates to 2V.

## 5.2 AC Characteristics



Note: Duty cycle is 50%.

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	CONDITION
Clock High Time	$t_{CHCX}$	20	-	-	nS	
Clock Low Time	$t_{CLCX}$	20	-	-	nS	
Clock Rise Time	$t_{CLCH}$	-	-	10	nS	
Clock Fall Time	$t_{CHCL}$	-	-	10	nS	

### 5.2.1 External XTAL1 Oscillator

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Input clock frequency	External crystal	4	12	24	MHz
Temperature	-	-40	-	85	°C
$V_{DD}$	-	2.5	5	5.5	V
Operating current	12MHz@ $V_{DD} = 5V$	-	5	-	mA

#### 5.2.1.1 Typical Crystal Application Circuits

CRYSTAL	C1	C2	R
4MHz ~ 24 MHz	without	without	without

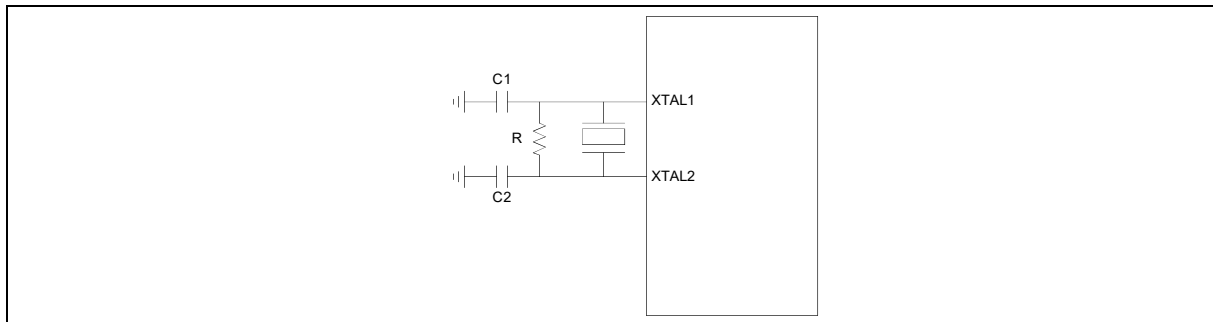


Figure 7-1 Typical Crystal Application Circuit



**5.2.2 External 32KHz XTAL Oscillator**

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Input clock frequency	External crystal	-	32	-	KHz
Temperature	-	-40	-	85	°C
V <sub>DD</sub>	-	2.5	-	5.5	V
Operating current	V <sub>DD</sub> = 5V	-	5	-	uA

**5.2.3 Internal 22.1184MHz RC Oscillator**

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Supply voltage <sup>[1]</sup>	-	2.5	-	5.5	V
Center Frequency	-	-	22.1184	-	MHz
Calibrated Internal Oscillator Frequency	+25°C; V <sub>DD</sub> =5V	-1	-	+1	%
	-40°C~+85°C; V <sub>DD</sub> =2.5V~5.5V	-3	-	+3	%
Accuracy of Un-calibrated Internal Oscillator Frequency	-40°C~+85°C; V <sub>DD</sub> =2.5V~5.5V	-25	-	+25	%
Operating current	V <sub>DD</sub> =5V	-	500	-	uA

**5.2.4 Internal 10KHz RC Oscillator**

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Supply voltage <sup>[1]</sup>	-	2.5	-	5.5	V
Center Frequency	-	-	10	-	KHz
Calibrated Internal Oscillator Frequency	+25°C; V <sub>DD</sub> =5V	-30	-	+30	%
	-40°C~+85°C; V <sub>DD</sub> =2.5V~5.5V	-50	-	+50	%
Operating current	V <sub>DD</sub> =5V	-	5	-	uA

**Notes:**

1. Internal operation voltage comes from LDO.



### 5.3 Analog Characteristics

#### 5.3.1 Specification of 1-MS/s 12-bit SARADC

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT
Resolution	-	-	-	12	Bit
Differential nonlinearity error	DNL	-	±3	-	LSB
Integral nonlinearity error	INL	-	±4	-	LSB
Offset error	EO	-	±1	10	LSB
Gain error (Transfer gain)	EG	-	1	1.005	-
Monotonic	-	Guaranteed			-
ADC clock frequency	FADC	-	-	20	MHz
Calibration time	TCAL	-	127	-	Clock
Sample time	TS	-	7	-	Clock
Conversion time	TADC	-	13	-	Clock
Sample rate	FS	-	-	800	Ksps
Supply voltage	V <sub>LDO</sub>	-	2.5	-	V
	V <sub>ADD</sub>	3	-	5.5	V
Supply current (Avg.)	I <sub>DD</sub>	-	0.5	-	mA
	I <sub>DDA</sub>	-	1.5	-	mA
Reference voltage	V <sub>REFP</sub>	-	V <sub>DDA</sub>	-	V
Reference current (Avg.)	I <sub>REFP</sub>	-	1	-	mA
Input voltage range	V <sub>IN</sub>	0	-	V <sub>REFP</sub>	V
Capacitance	C <sub>IN</sub>	-	5	-	pF

### 5.3.2 Specification of LDO & Power management

PARAMETER	MIN	TYP	MAX	UNIT	NOTE
Input Voltage	2.7	5	5.5	V	V <sub>DD</sub> input voltage
Output Voltage (bypass=0)	-10%	2.45	+10%	V	LDO output voltage
Output Voltage (bypass=1)	-10%	Input Voltage	+10%	V	Input Voltage < 2.7V
Temperature	-40	25	85	oC	
Quiescent Current (PD=0, bypass=0)	-	100	-	uA	
Quiescent Current (PD=1, bypass=0)	-	5	-	uA	
Quiescent Current (PD=1, bypass=1)	-	5	-	uA	
Iload (PD=0)	-	-	100	mA	
Iload (PD=1)	-	-	100	uA	
Cbp	-	1u	-	F	Resr=1ohm
Cload	-	250p	-	F	

Note:

1. It is recommended that a 10uF or higher capacitor and a 100nF bypass capacitor are connected between VDD and the closest VSS pin of the device.
2. For ensuring power stability, a 4.7uF or higher capacitor must be connected between LDO pin and the closest VSS pin of the device. Also a 100nF bypass capacitor between LDO and VSS help suppressing output noise.



**5.3.3 Specification of Low Voltage Reset**

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Operation voltage	-	1.7	-	5.5	V
Quiescent current	VDD5V=5.5V	-	-	5	uA
Temperature	-	-40	25	85	°C
Threshold voltage	Temperature=25°	1.7	2.0	2.3	V
	Temperature=-40°	-	2.4	-	V
	Temperature=85°	-	1.6	-	V
Hysteresis	-	0	0	0	V

**5.3.4 Specification of Brownout Detector**

Parameter	Condition	Min.	Typ.	Max.	Unit
Operation voltage	-	2.5	-	5.5	V
Quiescent current	AVDD=5.5V	-	-	125	μA
Temperature	-	-40	25	85	°C
Brown-out voltage	BOV_VL[1:0]=11	4.4	4.5	4.6	V
	BOV_VL [1:0]=10	3.7	3.8	3.9	V
	BOV_VL [1:0]=01	2.6	2.7	2.8	V
	BOV_VL [1:0]=00	2.1	2.2	2.3	V
Hysteresis	-	30m	-	150m	V

**5.3.5 Specification of Power-On Reset (5V)**

Parameter	Condition	Min.	Typ.	Max.	Unit
Temperature	-	-40	25	85	°C
Reset voltage	V+	-	2	-	V
Quiescent current	Vin>reset voltage	-	1	-	nA



**5.3.6 Specification of Temperature Sensor**

PARAMETER	MIN	TYP	MAX	UNIT	Conditions
Supply voltage <sup>[1]</sup>	2.5	-	5.5	V	
Temperature	-40	-	125	°C	
Current consumption	6.4	-	10.5	uA	
Gain	-1.95	-2	-2.05	mV/°C	
Offset	688	708	730	mV	Temp=0 °C

**Notes:**

1. Internal operation voltage comes from LDO.

**5.3.7 Specification of Comparator**

PARAMETER	MIN.	TYP.	MAX.	Condition
Temperature	-40°C	25 °C	85°C	-
VDD	2.4	3	5.5	-
VDD current	-	20uA	40uA	20uA@VDD=3V
Input offset voltage	-	5mV	15mV	-
Output swing	0.1	-	VDD-0.1	-
Input common mode range	0.1	-	VDD-1.2	-
DC gain	-	70dB	-	-
Propagation delay	-	200ns	-	@VCM=1.2V & VDIFF=0.1V
Comparison voltage	10mV	20mV	-	20mV@VCM=1V 50mV@VCM=0.1V 50mV@VCM=VDD-1.2 @10mV for non-hysteresis
Hysteresis	-	±10mV	-	One bit control W/O & W. hysteresis @VCM=0.4V ~ VDD-1.2V
Wake up time	-	-	2us	@CINP=1.3V CINN=1.2V



## 6 NUC100 PRODUCTS SELECTION GUIDE

NUC100 series Advance Line Selection Guide (Medium density)

Part number	Flash	SRAM	Connectivity			I <sup>2</sup> S	PWM	Comp.	ADC	Timer	RTC	ISP ICP	I/O	Package
			UART	SPI/SSI	I <sup>2</sup> C									
NUC100LE3AN	128 KB	16 KB	2	1	2	1	6	1	8x12-bit	4x24-bit	v	v	up to 35	LQFP48
NUC100LD3AN	64 KB	16 KB	2	1	2	1	6	1	8x12-bit	4x24-bit	v	v	up to 35	LQFP48
NUC100RE3AN	128 KB	16 KB	3	2	2	1	6	2	8x12-bit	4x24-bit	v	v	up to 49	LQFP64
NUC100RD3AN	64 KB	16 KB	3	2	2	1	6	2	8x12-bit	4x24-bit	v	v	up to 49	LQFP64
NUC100VE3AN	128 KB	16 KB	3	4	2	1	8	2	8x12-bit	4x24-bit	v	v	up to 80	LQFP100
NUC100VD3AN	64 KB	16 KB	3	4	2	1	8	2	8x12-bit	4x24-bit	v	v	up to 80	LQFP100
NUC100VD2AN	64 KB	8 KB	3	4	2	1	8	2	8x12-bit	4x24-bit	v	v	up to 80	LQFP100

NUC100 series Advance Line Selection Guide (Low density)

※ The followings are without PDMA

Part number	Flash	SRAM	Connectivity			I <sup>2</sup> S	PWM	Comp.	ADC	Timer	RTC	ISP ICP	I/O	Package
			UART	SPI/SSI	I <sup>2</sup> C									
NUC100LD2AN	64 KB	8 KB	2	1	2	1	4	1	8x12-bit	4x24-bit	v	v	up to 35	LQFP48
NUC100LD1AN	64 KB	4 KB	2	1	2	1	4	1	8X12-Bit	4x24-bit	v	v	up to 35	LQFP48
NUC100LC1AN	32 KB	4 KB	2	1	2	1	4	1	8X12-Bit	4x24-bit	v	v	up to 35	LQFP48
NUC100RD2AN	64 KB	8 KB	3	2	2	1	4	2	8x12-bit	4x24-bit	v	v	up to 49	LQFP64
NUC100RD1AN	64 KB	4 KB	3	2	2	1	4	2	8X12-Bit	4x24-bit	v	v	up to 49	LQFP64
NUC100RC1AN	32 KB	4 KB	3	2	2	1	4	2	8X12-Bit	4x24-bit	v	v	up to 49	LQFP64





## 7 REVISION HISTORY

VERSION	DATE	PAGE/ CHAP.	DESCRIPTION
V1.0	-	-	Initial Issued
V1.4	November 19, 2009		1 · Revise Pin-Assignment diagram 2 · Revise Selection Guide
V1.6	December 23, 2009		Revise Selection Guide for low density series
V1.7	January 08, 2010		Add electrical characteristics spec
V1.8	January 22, 2010		Add I <sup>2</sup> S feature and update pin diagram
V1.9	January 27, 2010		Add package dimension information
V1.10	February 10, 2010		1 · Fix "SELECTION TABLE" typo 2 · Modify ADC specification

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