



# THE DATASHEET OF PSMN040-100MSEX





# PSMN040-100MSE

N-channel 100 V 36.6 mΩ standard level MOSFET in LFAK33 designed specifically for high power PoE applications

26 March 2013

Product data sheet

## 1. General description

New standards and proprietary approaches are enabling Power-over-Ethernet (PoE) systems capable of delivering up to 90W to each powered device (PD). Such solutions place increased demands on the power sourcing equipment (PSE) in terms of “soft-start”, thermal management and power density requirements.

## 2. Features and benefits

- Enhanced forward biased safe operating area for superior linear mode operation
- Low  $R_{DS(on)}$  for low conduction losses
- Ultra reliable LFAK33 package for superior thermal and ruggedness performance
- Very low  $I_{DSS}$

## 3. Applications

- High power PoE applications (60W and higher)
- IEEE802.3at and proprietary solutions

## 4. Quick reference data

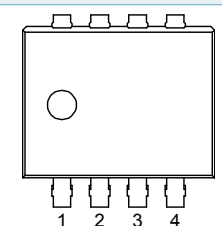
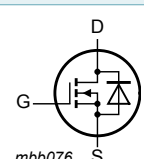
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}; T_j \leq 175\text{ °C}$	-	-	100	V
$I_D$	drain current	$T_j = 25\text{ °C}; V_{GS} = 10\text{ V};$ <a href="#">Fig. 1</a>	-	-	30	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C};$ <a href="#">Fig. 2</a>	-	-	91	W
<b>Static characteristics</b>						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 10\text{ A}; T_j = 25\text{ °C};$ <a href="#">Fig. 13</a>	-	29.4	36.6	mΩ
<b>Dynamic characteristics</b>						
$Q_{GD}$	gate-drain charge	$V_{GS} = 10\text{ V}; I_D = 10\text{ A}; V_{DS} = 50\text{ V};$	-	10.7	-	nC
$Q_{G(tot)}$	total gate charge	$T_j = 25\text{ °C};$ <a href="#">Fig. 14</a> ; <a href="#">Fig. 15</a>	-	30	-	nC
<b>Avalanche Ruggedness</b>						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10\text{ V}; T_{j(init)} = 25\text{ °C}; I_D = 30\text{ A};$ $V_{sup} \leq 100\text{ V}; R_{GS} = 50\text{ Ω};$ unclamped; <a href="#">Fig. 3</a>	-	-	54	mJ

N-channel 100 V 36.6 m $\Omega$  standard level MOSFET in LFAK33  
designed specifically for high power PoE applications

## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 <p>LFAK33 (SOT1210)</p>	 <p>mbb076</p>
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

## 6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN040-100MSE	LFAK33	Plastic single ended surface mounted package (LFAK33); 4 leads	SOT1210

## 7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN040-100MSE	M40E10

## 8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ }^\circ\text{C}$ ; $T_j \leq 175\text{ }^\circ\text{C}$	-	100	V
$V_{DGR}$	drain-gate voltage	$T_j \geq 25\text{ }^\circ\text{C}$ ; $T_j \leq 175\text{ }^\circ\text{C}$ ; $R_{GS} = 20\text{ k}\Omega$	-	100	V
$V_{GS}$	gate-source voltage		-20	20	V
$I_D$	drain current	$V_{GS} = 10\text{ V}$ ; $T_j = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 1</a>	-	30	A
		$V_{GS} = 10\text{ V}$ ; $T_{mb} = 100\text{ }^\circ\text{C}$ ; <a href="#">Fig. 1</a>	-	21	A
$I_{DM}$	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; $T_{mb} = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 4</a>	-	121	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 2</a>	-	91	W
$T_{stg}$	storage temperature		-55	175	$^\circ\text{C}$

N-channel 100 V 36.6 mΩ standard level MOSFET in LFPAK33 designed specifically for high power PoE applications

Symbol	Parameter	Conditions		Min	Max	Unit
$T_j$	junction temperature			-55	175	°C
$T_{sld(M)}$	peak soldering temperature			-	260	°C
<b>Source-drain diode</b>						
$I_S$	source current	$T_{mb} = 25\text{ °C}$	[1]	-	70	A
$I_{SM}$	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; $T_{mb} = 25\text{ °C}$		-	121	A
<b>Avalanche Ruggedness</b>						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10\text{ V}$ ; $T_{j(\text{init})} = 25\text{ °C}$ ; $I_D = 30\text{ A}$ ; $V_{sup} \leq 100\text{ V}$ ; $R_{GS} = 50\text{ }\Omega$ ; unclamped; <a href="#">Fig. 3</a>		-	54	mJ

[1] Continuous current is limited by package.

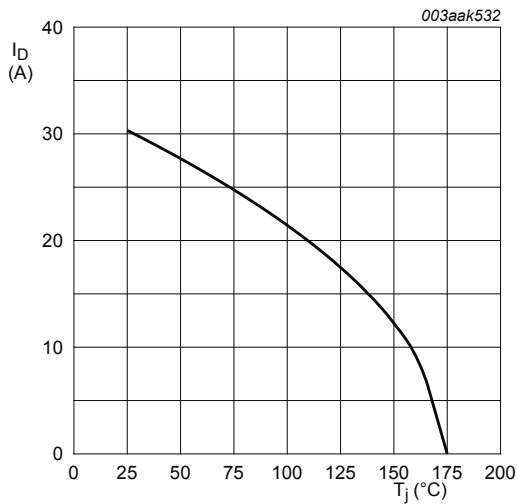


Fig. 1. Continuous drain current as a function of mounting base temperature

$$V_{GS} \geq 10V$$

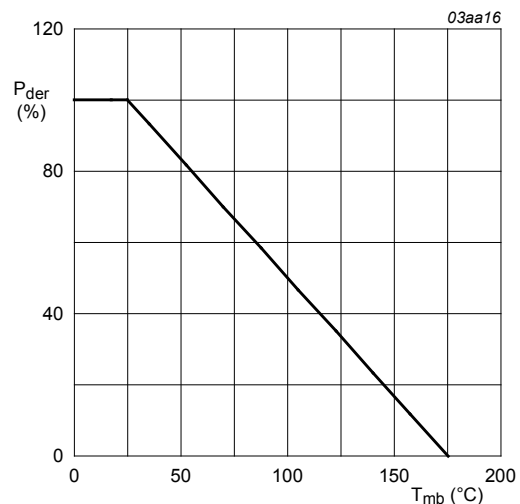


Fig. 2. Normalized total power dissipation as a function of mounting base temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ\text{C})}} \times 100\%$$

N-channel 100 V 36.6 mΩ standard level MOSFET in LFPAK33 designed specifically for high power PoE applications

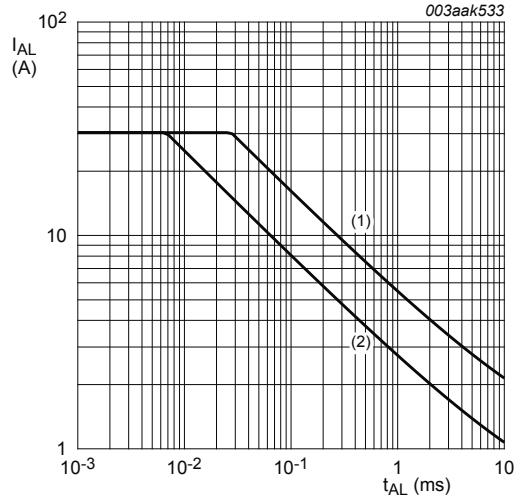


Fig. 3. Single pulse avalanche rating; avalanche current as a function of avalanche time

(1)  $T_{j (init)} = 25^{\circ}C$ ; (2)  $T_{j (init)} = 100^{\circ}C$

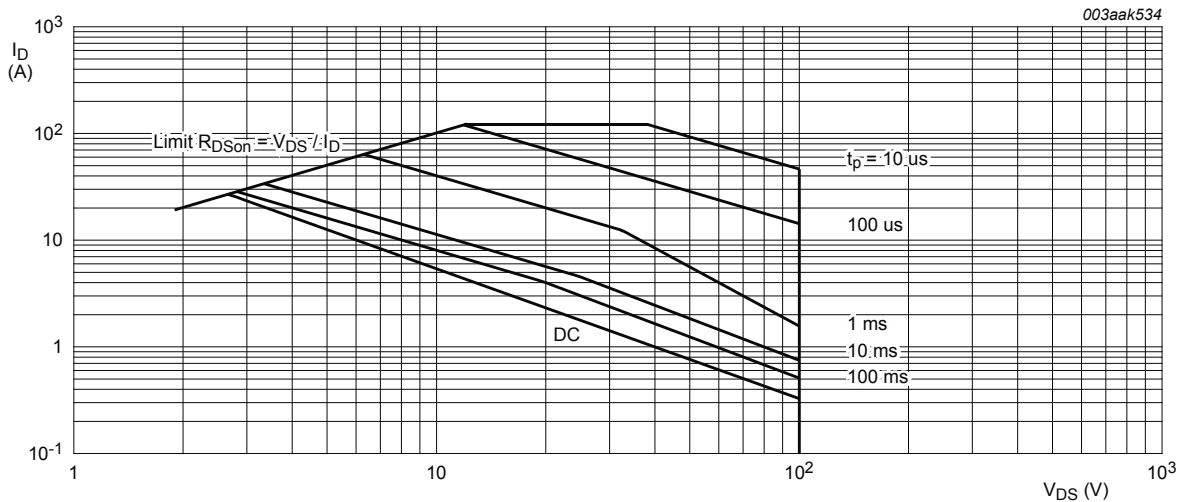


Fig. 4. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

$T_{mb} = 25^{\circ}C$ ;  $I_{DM}$  is a single pulse

## 9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	<a href="#">Fig. 5</a>	-	1.44	1.65	K/W

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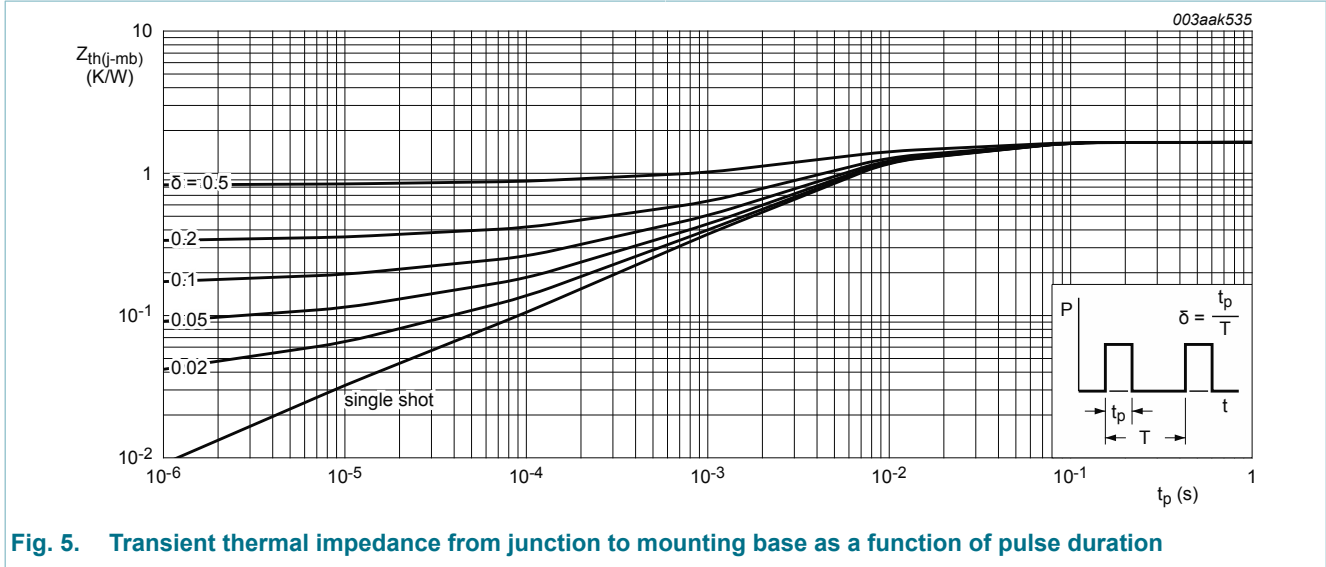


Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

## 10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	100	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$	90	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ C;$ <a href="#">Fig. 10; Fig. 11</a>	2.3	3.3	4	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ C;$ <a href="#">Fig. 10</a>	-	-	4.6	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ }^\circ C;$ <a href="#">Fig. 10</a>	1	-	-	V
$I_{DSS}$	drain leakage current	$V_{DS} = 100 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	0.05	1	$\mu A$
		$V_{DS} = 100 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 175 \text{ }^\circ C$	-	-	500	$\mu A$
$I_{GSS}$	gate leakage current	$V_{GS} = -20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	10	100	nA
		$V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	10	100	nA
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 10 \text{ A}; T_j = 100 \text{ }^\circ C;$ <a href="#">Fig. 12; Fig. 13</a>	-	-	66	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 10 \text{ A}; T_j = 175 \text{ }^\circ C;$ <a href="#">Fig. 12; Fig. 13</a>	-	-	99	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 10 \text{ A}; T_j = 25 \text{ }^\circ C;$ <a href="#">Fig. 13</a>	-	29.4	36.6	mΩ
$R_G$	gate resistance	$f = 10 \text{ MHz}$	-	1.65	-	Ω

N-channel 100 V 36.6 mΩ standard level MOSFET in LFPK33  
designed specifically for high power PoE applications

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Dynamic characteristics</b>						
Q <sub>G(tot)</sub>	total gate charge	I <sub>D</sub> = 10 A; V <sub>DS</sub> = 50 V; V <sub>GS</sub> = 10 V; T <sub>j</sub> = 25 °C; <a href="#">Fig. 14</a> ; <a href="#">Fig. 15</a>	-	30	-	nC
		I <sub>D</sub> = 0 A; V <sub>DS</sub> = 0 V; V <sub>GS</sub> = 10 V; T <sub>j</sub> = 25 °C	-	24	-	nC
Q <sub>GS</sub>	gate-source charge	I <sub>D</sub> = 10 A; V <sub>DS</sub> = 50 V; V <sub>GS</sub> = 10 V; T <sub>j</sub> = 25 °C; <a href="#">Fig. 14</a> ; <a href="#">Fig. 15</a>	-	7.6	-	nC
Q <sub>GS(th)</sub>	pre-threshold gate-source charge		-	4.5	-	nC
Q <sub>GS(th-pl)</sub>	post-threshold gate-source charge		-	3.1	-	nC
Q <sub>GD</sub>	gate-drain charge		-	10.7	-	nC
V <sub>GS(pl)</sub>	gate-source plateau voltage	I <sub>D</sub> = 10 A; V <sub>DS</sub> = 50 V; T <sub>j</sub> = 25 °C; <a href="#">Fig. 14</a> ; <a href="#">Fig. 15</a>	-	5.6	-	V
C <sub>iss</sub>	input capacitance	V <sub>DS</sub> = 50 V; V <sub>GS</sub> = 0 V; f = 1 MHz; T <sub>j</sub> = 25 °C; <a href="#">Fig. 16</a>	-	1470	-	pF
C <sub>oss</sub>	output capacitance		-	110	-	pF
C <sub>rss</sub>	reverse transfer capacitance		-	80	-	pF
t <sub>d(on)</sub>	turn-on delay time	V <sub>DS</sub> = 50 V; R <sub>L</sub> = 5 Ω; V <sub>GS</sub> = 10 V; R <sub>G(ext)</sub> = 5 Ω; T <sub>j</sub> = 25 °C	-	8.3	-	ns
t <sub>r</sub>	rise time		-	14.1	-	ns
t <sub>d(off)</sub>	turn-off delay time		-	18.7	-	ns
t <sub>f</sub>	fall time		-	13	-	ns
<b>Source-drain diode</b>						
V <sub>SD</sub>	source-drain voltage	I <sub>S</sub> = 20 A; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C; <a href="#">Fig. 17</a>	-	0.82	1.2	V
t <sub>rr</sub>	reverse recovery time	I <sub>S</sub> = 10 A; dI <sub>S</sub> /dt = -100 A/μs; V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 50 V; T <sub>j</sub> = 25 °C	-	41	-	ns
Q <sub>r</sub>	recovered charge		-	75	-	nC

N-channel 100 V 36.6 mΩ standard level MOSFET in LFPAK33 designed specifically for high power PoE applications

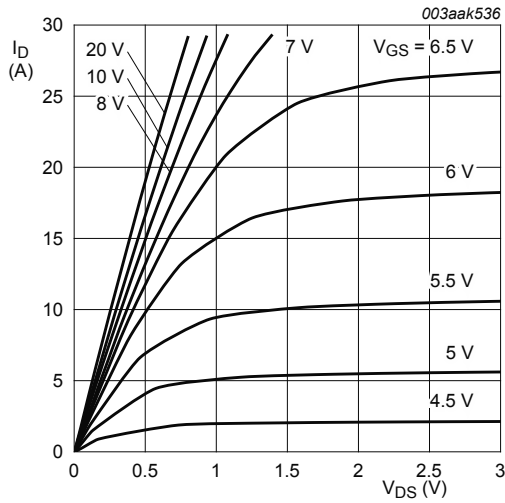


Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values

$T_j = 25^\circ\text{C}$

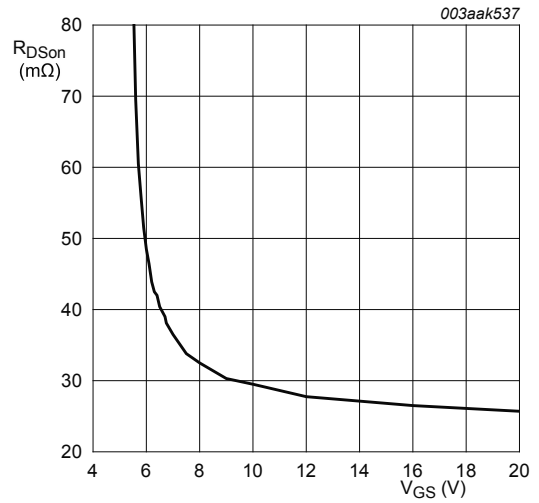


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

$T_j = 25^\circ\text{C}; I_D = 10\text{A}$

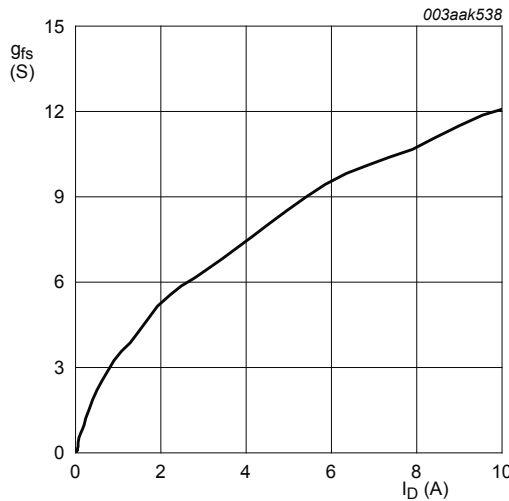


Fig. 8. Forward transconductance as a function of drain current; typical values

$T_j = 25^\circ\text{C}; V_{DS} = 10\text{V}$

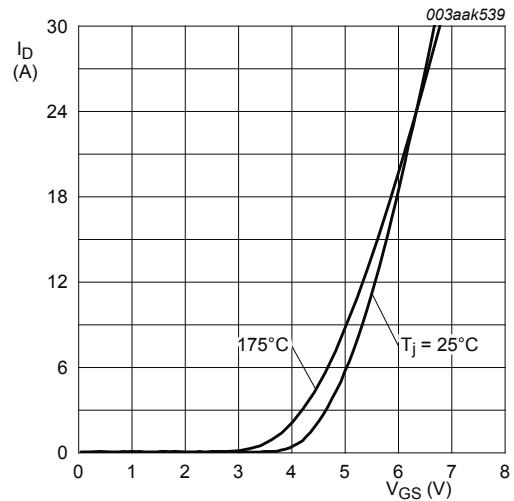


Fig. 9. Transfer characteristics; drain current as a function of gate-source voltage; typical values

$V_{DS} = 10\text{V}$

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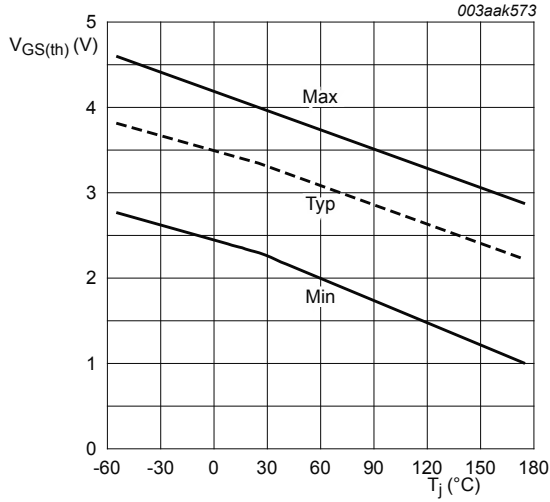


Fig. 10. Gate-source threshold voltage as a function of junction temperature

$$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$$

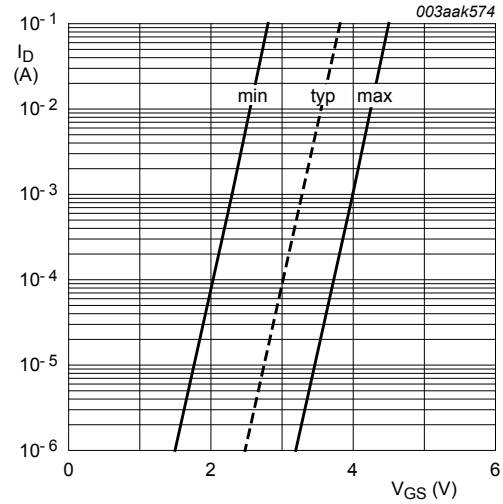


Fig. 11. Sub-threshold drain current as a function of gate-source voltage

$$T_j = 25^\circ\text{C}; V_{DS} = 5\text{V}$$

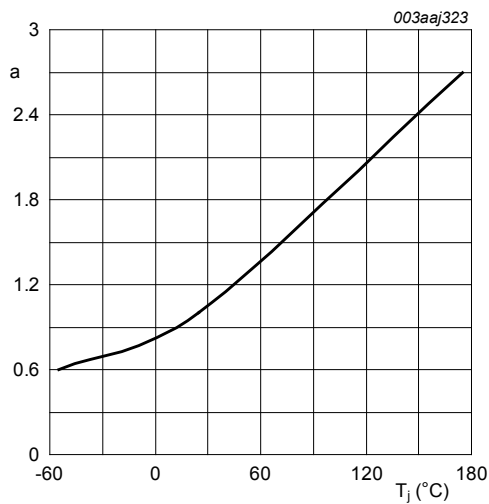


Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature

$$\alpha = \frac{R_{DSon}}{R_{DSon(25^\circ\text{C})}}$$

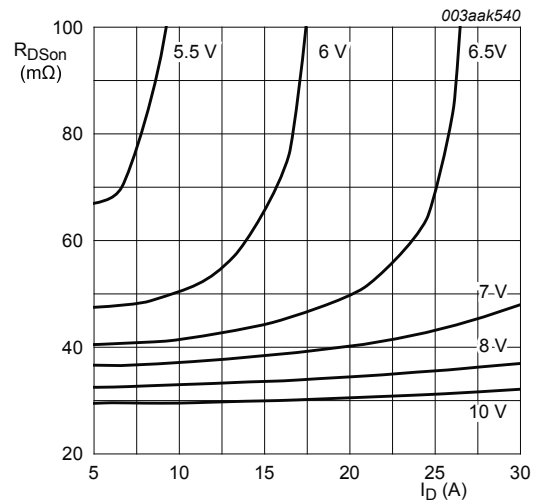


Fig. 13. Drain-source on-state resistance as a function of drain current; typical values

$$T_j = 25^\circ\text{C}$$

N-channel 100 V 36.6 mΩ standard level MOSFET in LFPAK33 designed specifically for high power PoE applications

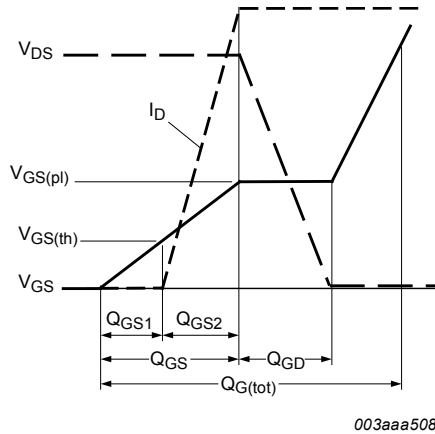


Fig. 14. Gate charge waveform definitions

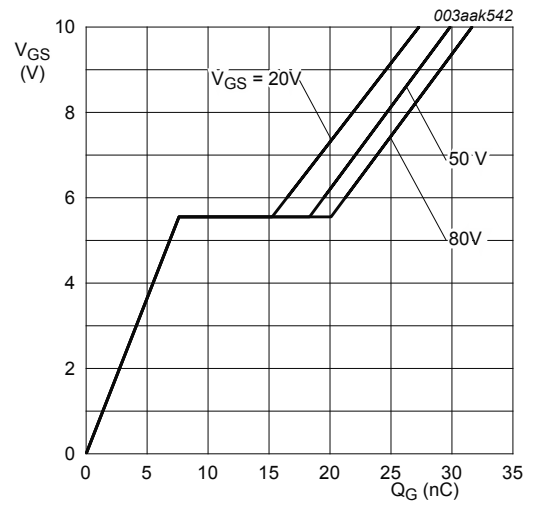


Fig. 15. Gate-source voltage as a function of gate charge; typical values

$T_j = 25^\circ\text{C}; I_D = 10\text{A}$

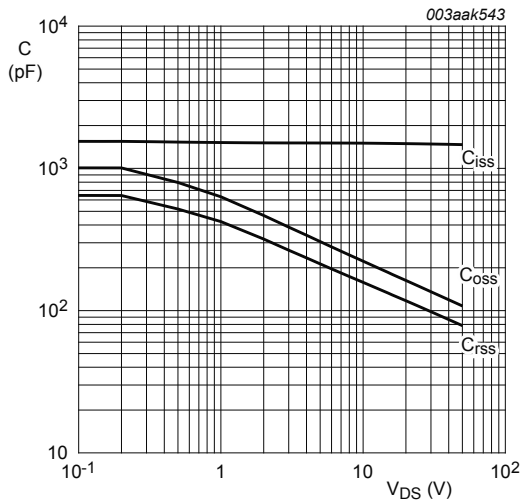


Fig. 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

$V_{GS} = 0\text{V}; f = 1\text{MHz}$

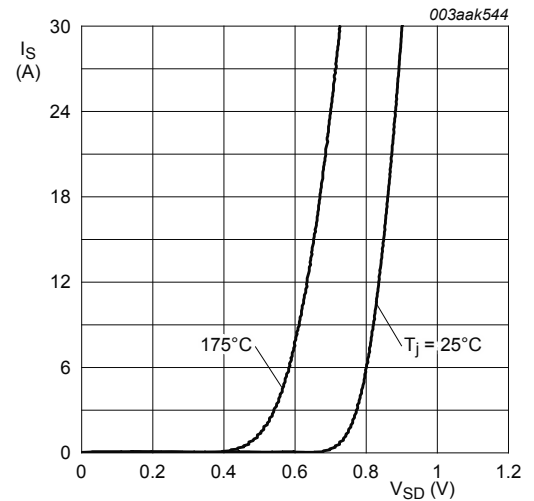


Fig. 17. Source current as a function of source-drain voltage; typical values

$V_{GS} = 0\text{V}$

N-channel 100 V 36.6 mΩ standard level MOSFET in LPAK33 designed specifically for high power PoE applications

### 11. Package outline

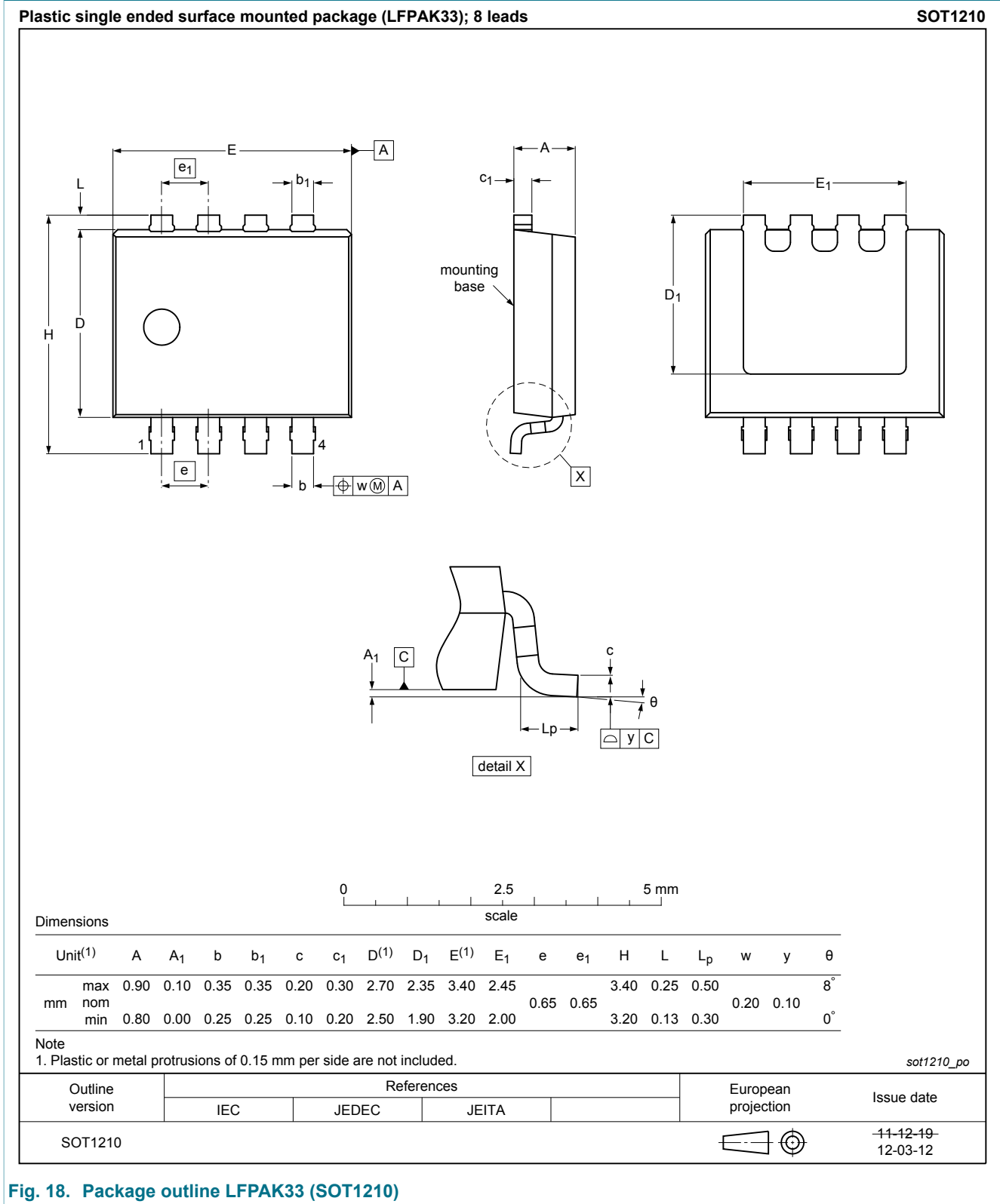


Fig. 18. Package outline LPAK33 (SOT1210)

## N-channel 100 V 36.6 mΩ standard level MOSFET in LPAK33 designed specifically for high power PoE applications

## 12. Legal information

### 12.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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- [2] The term 'short data sheet' is explained in section "Definitions".
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## 13. Contents

1	General description .....	1
2	Features and benefits .....	1
3	Applications .....	1
4	Quick reference data .....	1
5	Pinning information .....	2
6	Ordering information .....	2
7	Marking .....	2
8	Limiting values .....	2
9	Thermal characteristics .....	4
10	Characteristics .....	5
11	Package outline .....	10
12	Legal information .....	11
12.1	Data sheet status .....	11
12.2	Definitions .....	11
12.3	Disclaimers .....	11
12.4	Trademarks .....	12

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