



**THE DATASHEET OF
PSMN020-100YS,115**





PSMN020-100YS

N-channel 100V 20.5mΩ standard level MOSFET in LFPACK

26 March 2014

Product data sheet

1. General description

Standard level N-channel MOSFET in LFPACK package qualified to 175 °C. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

2. Features and benefits

- Advanced TrenchMOS provides low RDSon and low gate charge
- High efficiency gains in switching power converters
- Improved mechanical and thermal characteristics
- LFPACK provides maximum power density in a Power SO8 package

3. Applications

- DC-to-DC converters
- Lithium-ion battery protection
- Load switching
- Motor control
- Server power supplies

4. Quick reference data

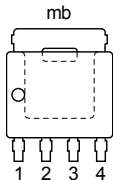
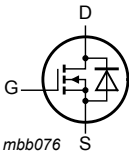
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{DS}	drain-source voltage	T _j ≥ 25 °C; T _j ≤ 175 °C	-	-	100	V
I _D	drain current	T _{mb} = 25 °C; V _{GS} = 10 V; Fig. 2	-	-	43	A
P _{tot}	total power dissipation	T _{mb} = 25 °C; Fig. 1	-	-	106	W
T _j	junction temperature		-55	-	175	°C
Static characteristics						
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 15 A; T _j = 100 °C; Fig. 13	-	-	37	mΩ
		V _{GS} = 10 V; I _D = 15 A; T _j = 25 °C; Fig. 14	-	15	20.5	mΩ
Dynamic characteristics						
Q _{GD}	gate-drain charge	V _{GS} = 10 V; I _D = 30 A; V _{DS} = 50 V; Fig. 15 ; Fig. 16	-	11.8	16.5	nC
Q _{G(tot)}	total gate charge		-	41	57.4	nC

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10\text{ V}$; $T_{j(\text{init})} = 25\text{ °C}$; $I_D = 43\text{ A}$; $V_{\text{sup}} \leq 100\text{ V}$; unclamped; $R_{GS} = 50\text{ }\Omega$; Fig. 4	-	-	103	mJ

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 <p>LPAK56; Power-SO8 (SOT669)</p>	 <p><i>mbb076</i></p>
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN020-100YS	LPAK56; Power-SO8	Plastic single-ended surface-mounted package (LPAK56; Power-SO8); 4 leads	SOT669

7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN020-100YS	20100

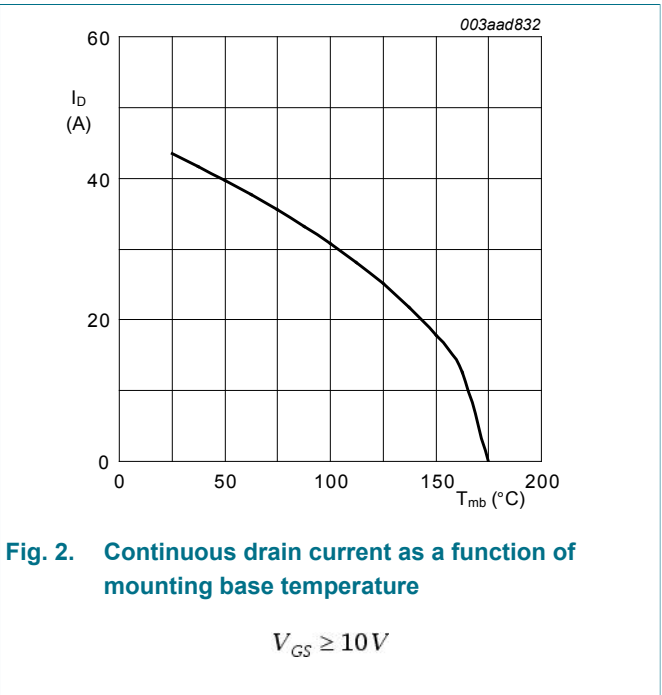
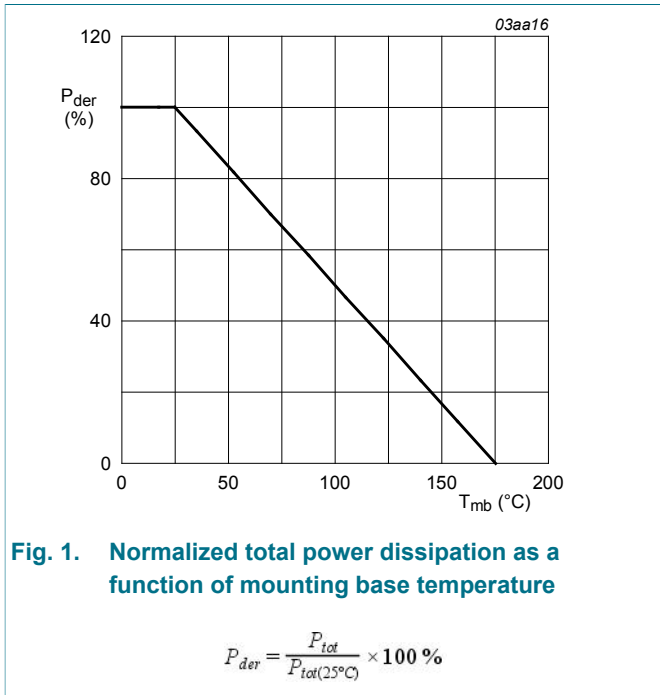
8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 175\text{ °C}$	-	100	V
V_{DGR}	drain-gate voltage	$T_j \leq 175\text{ °C}$; $T_j \geq 25\text{ °C}$; $R_{GS} = 20\text{ k}\Omega$	-	100	V
V_{GS}	gate-source voltage		-20	20	V
P_{tot}	total power dissipation	$T_{\text{mb}} = 25\text{ °C}$; Fig. 1	-	106	W

Symbol	Parameter	Conditions	Min	Max	Unit
I _D	drain current	V _{GS} = 10 V; T _{mb} = 100 °C; Fig. 2	-	30	A
		V _{GS} = 10 V; T _{mb} = 25 °C; Fig. 2	-	43	A
I _{DM}	peak drain current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C; Fig. 3	-	172	A
T _{stg}	storage temperature		-55	175	°C
T _j	junction temperature		-55	175	°C
T _{slid(M)}	peak soldering temperature		-	260	°C
Source-drain diode					
I _S	source current	T _{mb} = 25 °C	-	43	A
I _{SM}	peak source current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C	-	172	A
Avalanche ruggedness					
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	V _{GS} = 10 V; T _{j(init)} = 25 °C; I _D = 43 A; V _{sup} ≤ 100 V; unclamped; R _{GS} = 50 Ω; Fig. 4	-	103	mJ



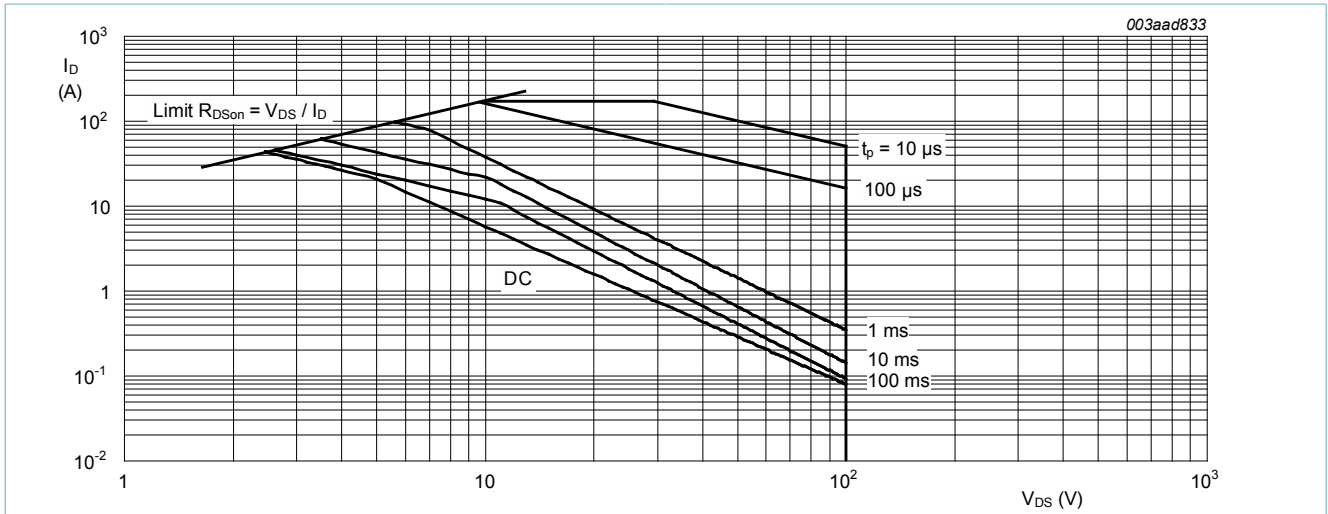
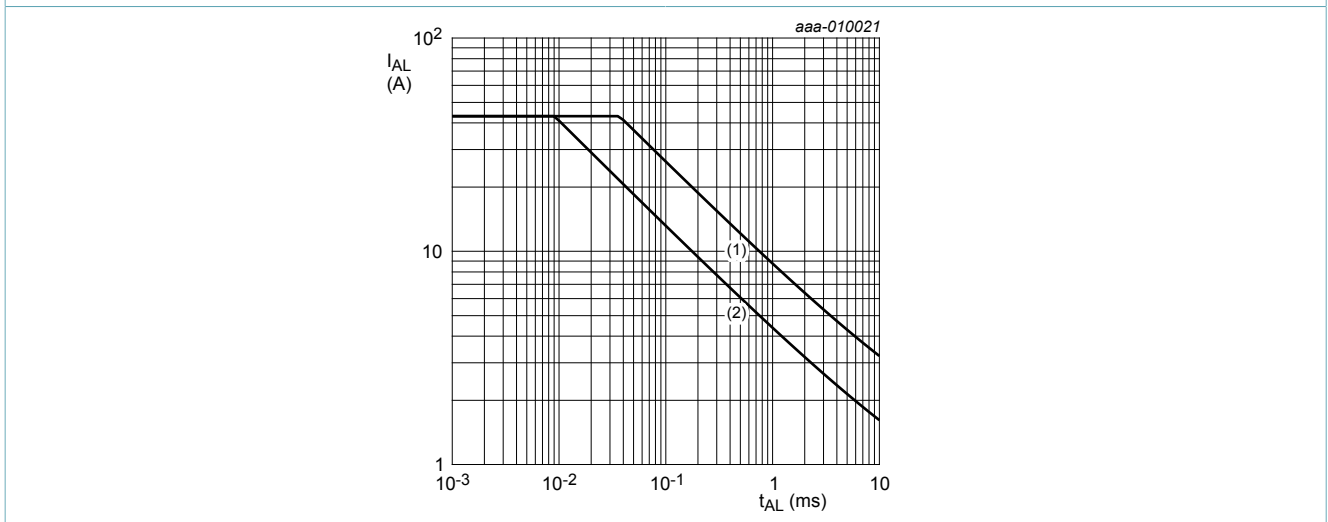


Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

$T_{mb} = 25\text{ }^\circ\text{C}; I_{DM}$ is single pulse



(1) $T_{j(\text{init})} = 25\text{ }^\circ\text{C}$; (2) $T_{j(\text{init})} = 100\text{ }^\circ\text{C}$

Fig. 4. Avalanche rating; avalanche current as a function of avalanche time

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5	-	0.63	1.42	K/W

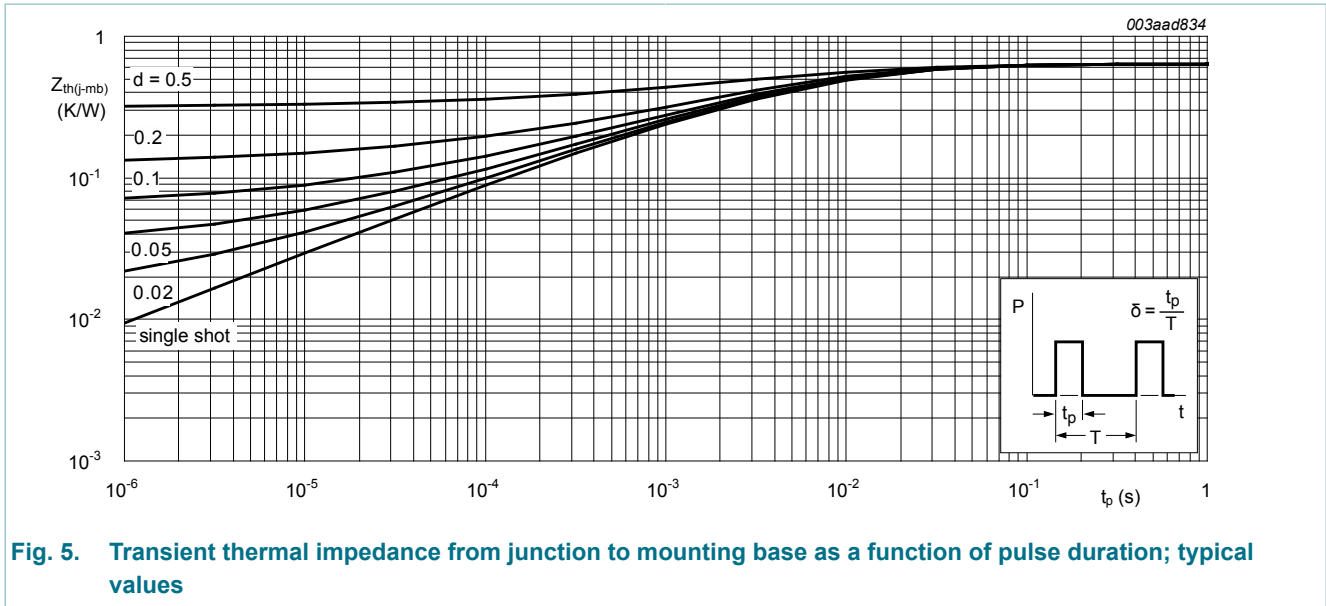


Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration; typical values

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 0.25 \text{ mA}; V_{GS} = 0 \text{ V}; T_J = -55 \text{ }^\circ\text{C}$	90	-	-	V
		$I_D = 0.25 \text{ mA}; V_{GS} = 0 \text{ V}; T_J = 25 \text{ }^\circ\text{C}$	100	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_J = 175 \text{ }^\circ\text{C};$ Fig. 11	0.95	-	-	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_J = 25 \text{ }^\circ\text{C};$ Fig. 12; Fig. 11	2	3	4	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_J = -55 \text{ }^\circ\text{C};$ Fig. 11	-	-	4.6	V
I_{DSS}	drain leakage current	$V_{DS} = 100 \text{ V}; V_{GS} = 0 \text{ V}; T_J = 125 \text{ }^\circ\text{C}$	-	-	100	μA
		$V_{DS} = 100 \text{ V}; V_{GS} = 0 \text{ V}; T_J = 25 \text{ }^\circ\text{C}$	-	0.06	2	μA
I_{GSS}	gate leakage current	$V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}; T_J = 25 \text{ }^\circ\text{C}$	-	10	100	nA
		$V_{GS} = -20 \text{ V}; V_{DS} = 0 \text{ V}; T_J = 25 \text{ }^\circ\text{C}$	-	10	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 15 \text{ A}; T_J = 100 \text{ }^\circ\text{C};$ Fig. 13	-	-	37	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 15 \text{ A}; T_J = 175 \text{ }^\circ\text{C};$ Fig. 13	-	39	57.4	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 15 \text{ A}; T_J = 25 \text{ }^\circ\text{C};$ Fig. 14	-	15	20.5	mΩ
R_G	internal gate resistance (AC)	$f = 1 \text{ MHz}$	-	0.6	1.2	Ω

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Dynamic characteristics						
Q _{G(tot)}	total gate charge	I _D = 30 A; V _{DS} = 50 V; V _{GS} = 10 V; Fig. 15 ; Fig. 16	-	41	57.4	nC
		I _D = 0 A; V _{DS} = 0 V; V _{GS} = 10 V	-	34	47.6	nC
Q _{GS}	gate-source charge	I _D = 30 A; V _{DS} = 50 V; V _{GS} = 10 V; Fig. 15 ; Fig. 16	-	10.2	14.3	nC
Q _{GS(th)}	pre-threshold gate-source charge	I _D = 30 A; V _{DS} = 50 V; V _{GS} = 10 V; Fig. 15	-	6.9	-	nC
Q _{GS(th-pl)}	post-threshold gate-source charge		-	3.4	-	nC
Q _{GD}	gate-drain charge	I _D = 30 A; V _{DS} = 50 V; V _{GS} = 10 V; Fig. 15 ; Fig. 16	-	11.8	16.5	nC
V _{GS(pl)}	gate-source plateau voltage	V _{DS} = 50 V; Fig. 15 ; Fig. 16	-	4.4	-	V
C _{iss}	input capacitance	V _{DS} = 50 V; V _{GS} = 0 V; f = 1 MHz; T _j = 25 °C; Fig. 17	-	2210	2980	pF
C _{oss}	output capacitance		-	167	226	pF
C _{rss}	reverse transfer capacitance		-	103	144	pF
t _{d(on)}	turn-on delay time	V _{DS} = 50 V; R _L = 1.7 Ω; V _{GS} = 10 V; R _{G(ext)} = 4.7 Ω; T _j = 25 °C	-	17.4	26.1	ns
t _r	rise time		-	18.1	27.2	ns
t _{d(off)}	turn-off delay time		-	37.8	56.7	ns
t _f	fall time		-	15	22.5	ns
Source-drain diode						
V _{SD}	source-drain voltage	I _S = 15 A; V _{GS} = 0 V; T _j = 25 °C; Fig. 18	-	0.8	1.2	V
t _{rr}	reverse recovery time	I _S = 10 A; dI _S /dt = 100 A/μs; V _{GS} = 0 V;	-	52	68	ns
Q _r	recovered charge	V _{DS} = 50 V	-	112	146	nC

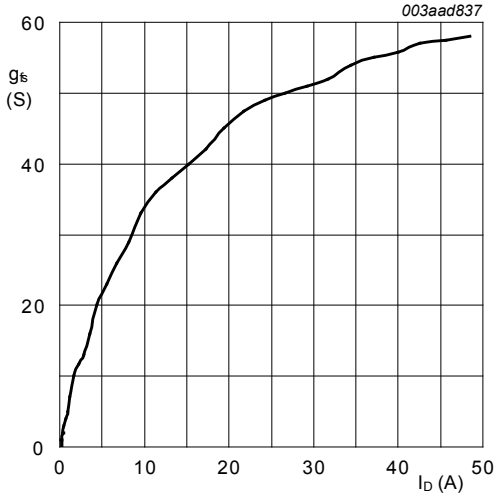


Fig. 6. Forward transconductance as a function of drain current; typical values

$$T_j = 25^\circ\text{C}; V_{DS} = 15\text{V}$$

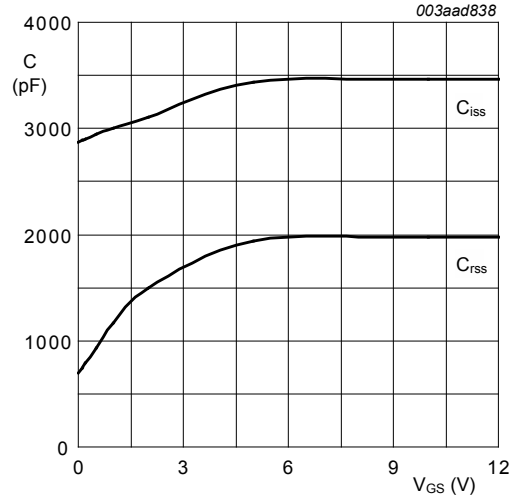


Fig. 7. Input and reverse transfer capacitances as a function of gate-source voltage; typical values

$$V_{DS} = 0\text{V}; f = 1\text{MHz}$$

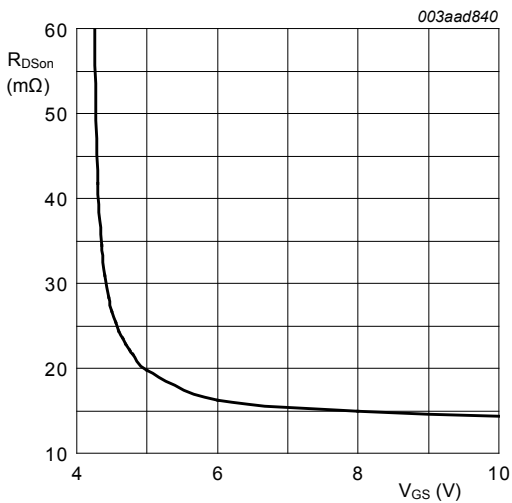


Fig. 8. Drain-source on-state resistance as a function of gate-source voltage; typical values

$$T_j = 25^\circ\text{C}; I_D = 10\text{A}$$

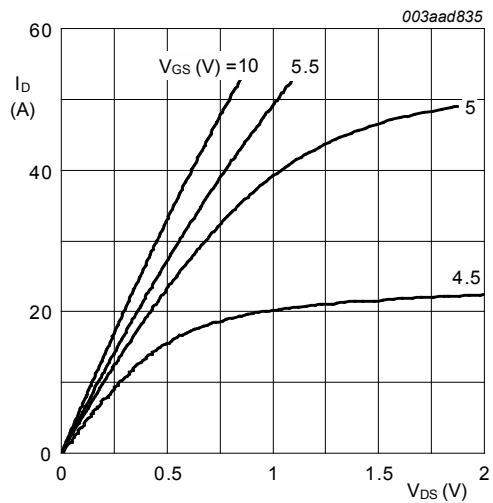


Fig. 9. Output characteristics: drain current as a function of drain-source voltage; typical values

$$T_j = 25^\circ\text{C}$$

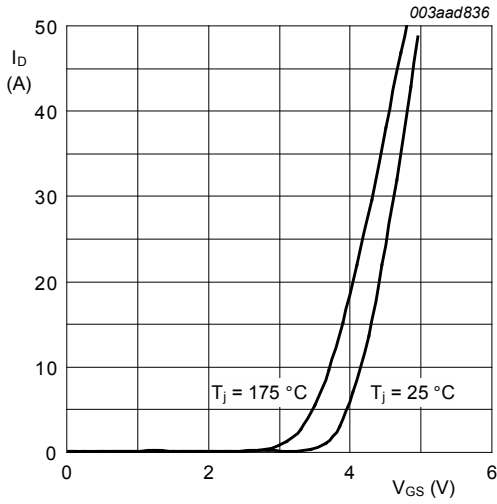


Fig. 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values

$$V_{DS} > I_D \times R_{DSon}$$

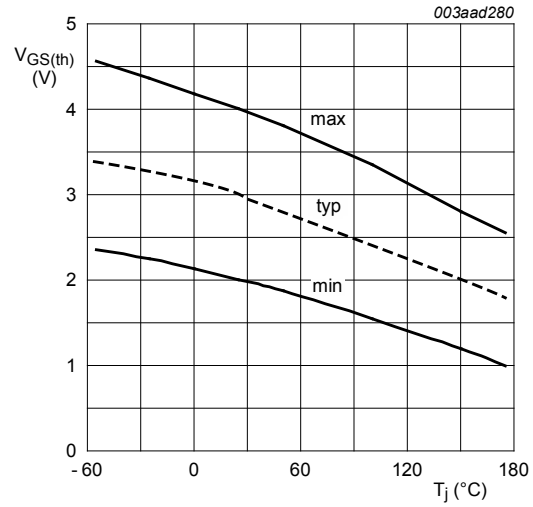


Fig. 11. Gate-source threshold voltage as a function of junction temperature

$$I_D = 1\text{ mA}; V_{DS} = V_{GS}$$

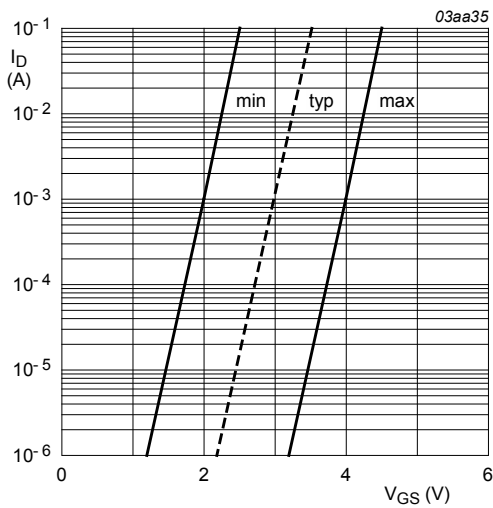


Fig. 12. Sub-threshold drain current as a function of gate-source voltage

$$T_j = 25\text{ °C}; V_{DS} = 5\text{ V}$$

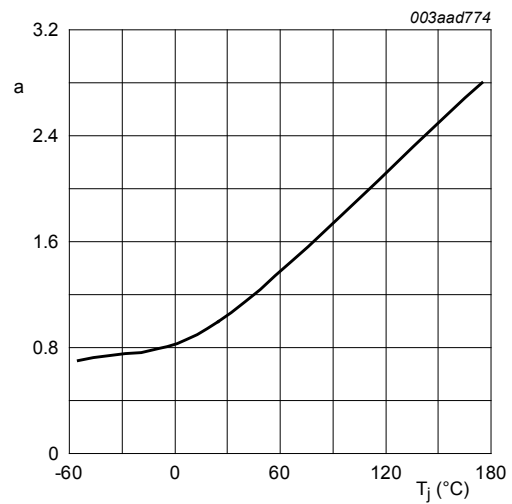


Fig. 13. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DSon}}{R_{DSon(25\text{ °C})}}$$

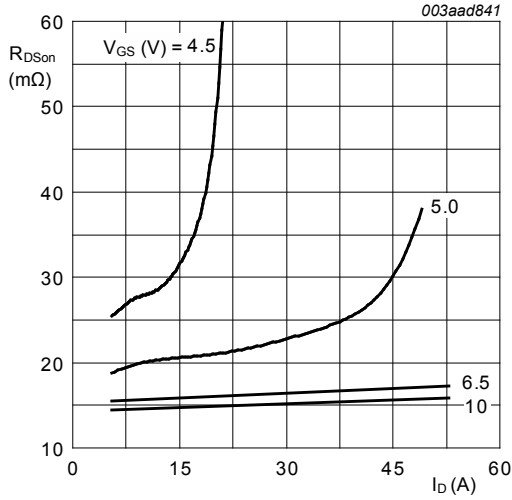


Fig. 14. Drain-source on-state resistance as a function of drain current; typical values

$T_j = 25^\circ C$

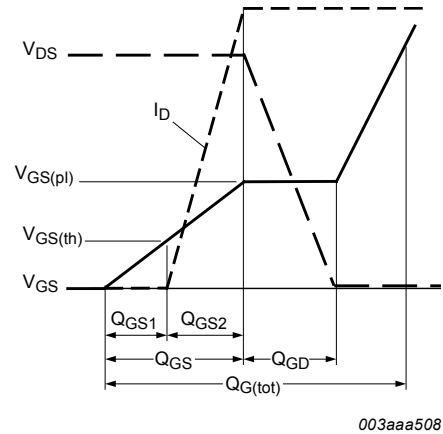


Fig. 15. Gate charge waveform definitions

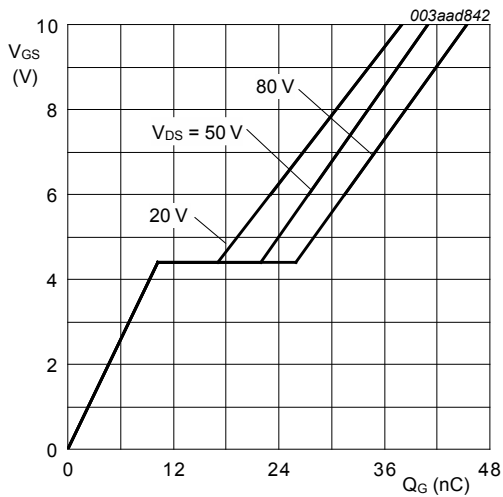


Fig. 16. Gate-source voltage as a function of gate charge; typical values

$T_j = 25^\circ C; I_D = 30A$

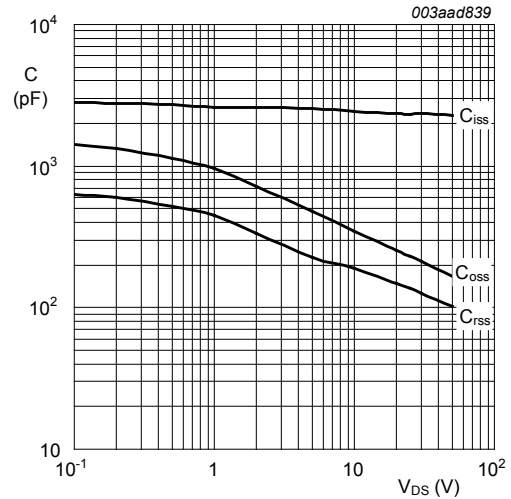


Fig. 17. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

$V_{GS} = 0V; f = 1MHz$

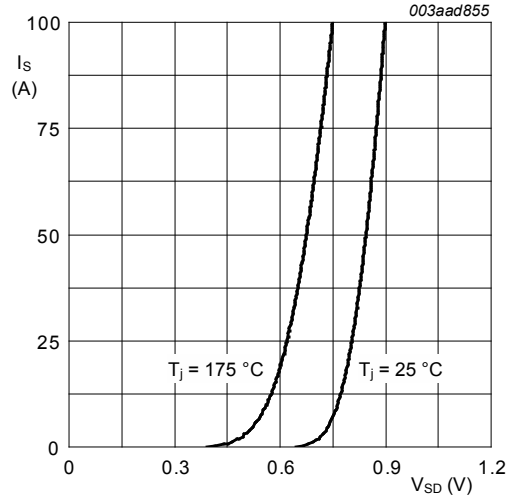
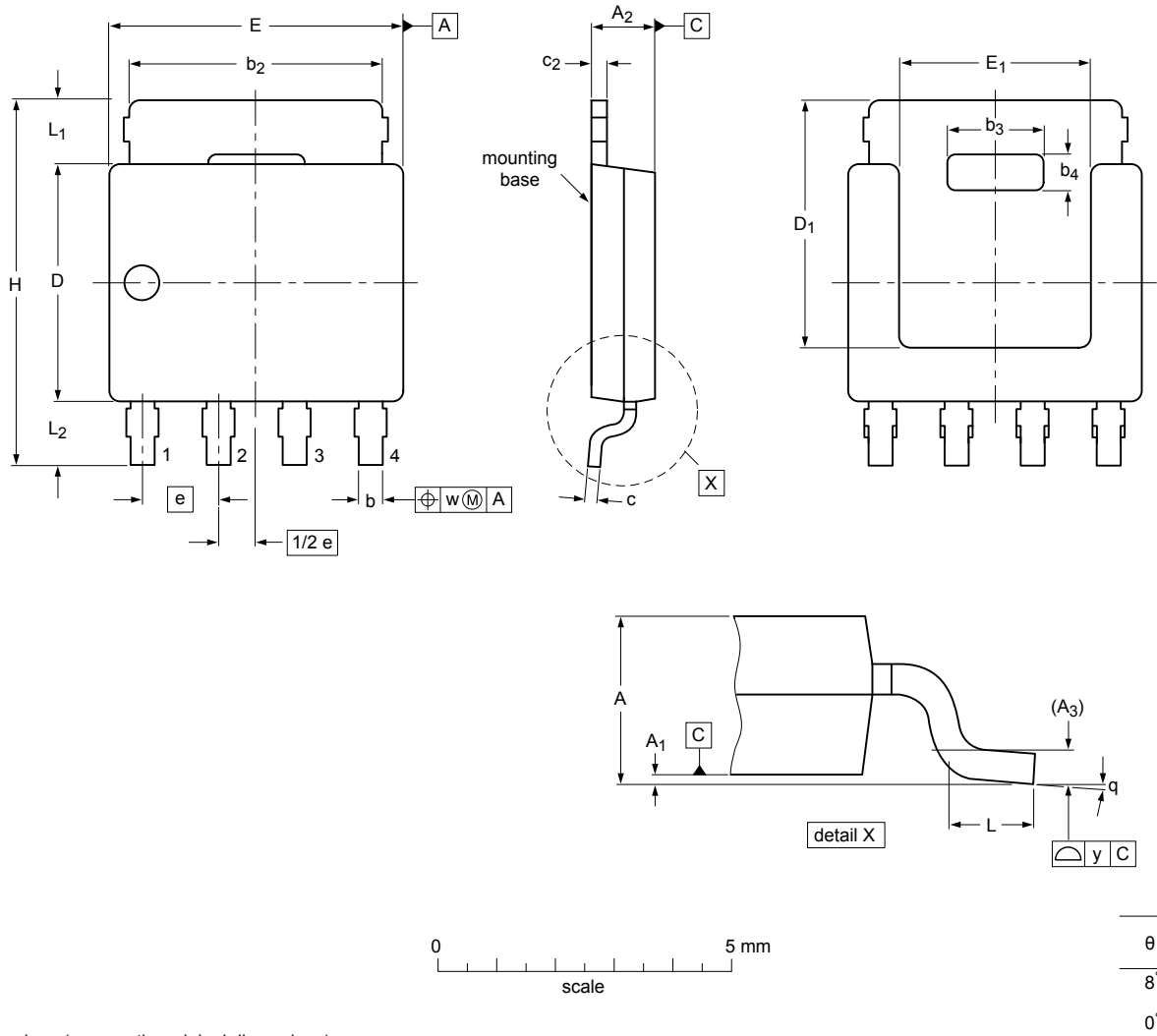


Fig. 18. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values

$$V_{GS} = 0V$$

11. Package outline

Plastic single-ended surface-mounted package (LPAK56; Power-SO8); 4 leads SOT669



Dimensions (mm are the original dimensions)

Unit ⁽¹⁾	A	A ₁	A ₂	A ₃	b	b ₂	b ₃	b ₄	c	c ₂	D ⁽¹⁾	D ₁ ⁽¹⁾	E ⁽¹⁾	E ₁ ⁽¹⁾	e	H	L	L ₁	L ₂	w	y
max	1.20	0.15	1.10		0.50	4.41	2.2	0.9	0.25	0.30	4.10	4.20	5.0	3.3		6.2	0.85	1.3	1.3		
nom				0.25											1.27					0.25	0.1
min	1.01	0.00	0.95		0.35	3.62	2.0	0.7	0.19	0.24	3.80		4.8	3.1		5.8	0.40	0.8	0.8		

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

sot669_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT669		MO-235				-11-03-25- 13-02-27

Fig. 19. Package outline LPAK56; Power-SO8 (SOT669)

12. Legal information

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