



**THE DATASHEET OF  
SQJ940EP-T1\_GE3**



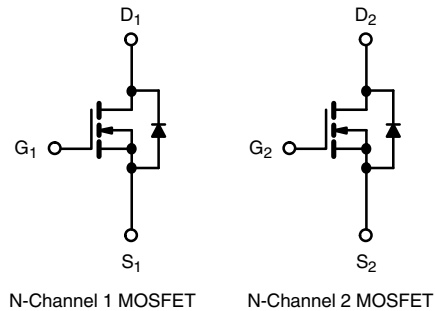
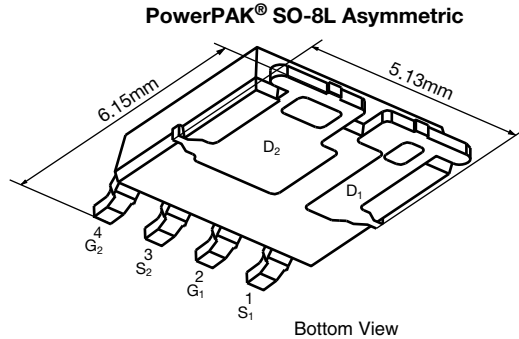
## Automotive Dual N-Channel 40 V (D-S) 175 °C MOSFETs



PRODUCT SUMMARY		
	N-CHANNEL 1	N-CHANNEL 2
$V_{DS}$ (V)	40	40
$R_{DS(on)}$ ( $\Omega$ ) at $V_{GS} = 10$ V	0.0160	0.0064
$R_{DS(on)}$ ( $\Omega$ ) at $V_{GS} = 4.5$ V	0.0188	0.0076
$I_D$ (A)	15	18
Configuration	Dual N	

### FEATURES

- TrenchFET® Power MOSFET
- AEC-Q101 Qualified<sup>d</sup>
- 100 %  $R_g$  and UIS Tested
- Material categorization:  
For definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



ORDERING INFORMATION	
Package	PowerPAK SO-8L Dual Asymmetric
Lead (Pb)-free and Halogen-free	SQJ940EP-T1-GE3

ABSOLUTE MAXIMUM RATINGS ( $T_C = 25$ °C, unless otherwise noted)				
PARAMETER	SYMBOL	N-CHANNEL 1	N-CHANNEL 2	UNIT
Drain-Source Voltage	$V_{DS}$	40	40	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$		
Continuous Drain Current <sup>a</sup>	$I_D$	$T_C = 25$ °C	15	A
		$T_C = 125$ °C	15	
Continuous Source Current (Diode Conduction) <sup>a</sup>	$I_S$	15	39	A
Pulsed Drain Current <sup>b</sup>	$I_{DM}$	60	72	
Single Pulse Avalanche Current	$I_{AS}$	20.5	35.5	mJ
Single Pulse Avalanche Energy	$E_{AS}$	21	63	
Maximum Power Dissipation <sup>b</sup>	$P_D$	$T_C = 25$ °C	48	W
		$T_C = 125$ °C	16	
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	- 55 to + 175		°C
Soldering Recommendations (Peak Temperature) <sup>e, f</sup>		260		

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	N-CHANNEL 1	N-CHANNEL 2	UNIT
Junction-to-Ambient	$R_{thJA}$	70	70	°C/W
Junction-to-Case (Drain)	$R_{thJC}$	3.3	3.5	

### Notes

- Package limited.
- Pulse test; pulse width  $\leq 300$   $\mu$ s, duty cycle  $\leq 2$  %.
- When mounted on 1" square PCB (FR4 material).
- Parametric verification ongoing.
- See solder profile ([www.vishay.com/doc?73257](http://www.vishay.com/doc?73257)). The PowerPAK SO-8L is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.



<b>SPECIFICATIONS</b> ( $T_C = 25\text{ }^\circ\text{C}$ , unless otherwise noted)								
PARAMETER	SYMBOL	TEST CONDITIONS			MIN.	TYP.	MAX.	UNIT
<b>Static</b>								
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$		N-Ch 1	40	-	-	V
		$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$		N-Ch 2	40	-	-	
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$		N-Ch 1	1.5	2	2.5	
		$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$		N-Ch 2	1.5	2	2.5	
Gate-Source Leakage	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$		N-Ch 1	-	-	$\pm 100$	nA
				N-Ch 2	-	-	$\pm 100$	
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{GS} = 0\text{ V}$	$V_{DS} = 40\text{ V}$	N-Ch 1	-	-	1	$\mu\text{A}$
		$V_{GS} = 0\text{ V}$	$V_{DS} = -40\text{ V}$	N-Ch 2	-	-	1	
		$V_{GS} = 0\text{ V}$	$V_{DS} = 40\text{ V}, T_J = 125\text{ }^\circ\text{C}$	N-Ch 1	-	-	50	
		$V_{GS} = 0\text{ V}$	$V_{DS} = 40\text{ V}, T_J = 125\text{ }^\circ\text{C}$	N-Ch 2	-	-	50	
		$V_{GS} = 0\text{ V}$	$V_{DS} = 40\text{ V}, T_J = 175\text{ }^\circ\text{C}$	N-Ch 1	-	-	150	
		$V_{GS} = 0\text{ V}$	$V_{DS} = 40\text{ V}, T_J = 175\text{ }^\circ\text{C}$	N-Ch 2	-	-	150	
On-State Drain Current <sup>a</sup>	$I_{D(on)}$	$V_{GS} = 10\text{ V}$	$V_{DS} \geq 5\text{ V}$	N-Ch 1	30	-	-	A
		$V_{GS} = 10\text{ V}$	$V_{DS} \geq 5\text{ V}$	N-Ch 2	30	-	-	
Drain-Source On-State Resistance <sup>a</sup>	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$	$I_D = 15\text{ A}$	N-Ch 1	-	0.0133	0.0160	$\Omega$
		$V_{GS} = 10\text{ V}$	$I_D = 20\text{ A}$	N-Ch 2	-	0.0053	0.0064	
		$V_{GS} = 10\text{ V}$	$I_D = 15\text{ A}, T_J = 125\text{ }^\circ\text{C}$	N-Ch 1	-	-	0.0270	
		$V_{GS} = 10\text{ V}$	$I_D = 20\text{ A}, T_J = 125\text{ }^\circ\text{C}$	N-Ch 2	-	-	0.0105	
		$V_{GS} = 10\text{ V}$	$I_D = 15\text{ A}, T_J = 175\text{ }^\circ\text{C}$	N-Ch 1	-	-	0.0334	
		$V_{GS} = 10\text{ V}$	$I_D = 20\text{ A}, T_J = 175\text{ }^\circ\text{C}$	N-Ch 2	-	-	0.0130	
		$V_{GS} = 4.5\text{ V}$	$I_D = 13\text{ A}$	N-Ch 1	-	0.0157	0.0188	
		$V_{GS} = 4.5\text{ V}$	$I_D = 18\text{ A}$	N-Ch 2	-	0.0063	0.0076	
Forward Transconductance <sup>b</sup>	$g_{fs}$	$V_{DS} = 15\text{ V}, I_D = 15\text{ A}$		N-Ch 1	-	64	-	S
		$V_{DS} = 15\text{ V}, I_D = 20\text{ A}$		N-Ch 2	-	102	-	
<b>Dynamic<sup>b</sup></b>								
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}$	$V_{DS} = 20\text{ V}, f = 1\text{ MHz}$	N-Ch 1	-	717	896	pF
		$V_{GS} = 0\text{ V}$	$V_{DS} = 20\text{ V}, f = 1\text{ MHz}$	N-Ch 2	-	1850	2313	
Output Capacitance	$C_{oss}$	$V_{GS} = 0\text{ V}$	$V_{DS} = 20\text{ V}, f = 1\text{ MHz}$	N-Ch 1	-	118	148	
		$V_{GS} = 0\text{ V}$	$V_{DS} = 20\text{ V}, f = 1\text{ MHz}$	N-Ch 2	-	272	340	
Reverse Transfer Capacitance	$C_{rss}$	$V_{GS} = 0\text{ V}$	$V_{DS} = 20\text{ V}, f = 1\text{ MHz}$	N-Ch 1	-	48	60	
		$V_{GS} = 0\text{ V}$	$V_{DS} = 20\text{ V}, f = 1\text{ MHz}$	N-Ch 2	-	98	123	
Total Gate Charge <sup>c</sup>	$Q_g$	$V_{GS} = 10\text{ V}$	$V_{DS} = 20\text{ V}, I_D = 6\text{ A}$	N-Ch 1	-	13.5	20	nC
		$V_{GS} = 10\text{ V}$	$V_{DS} = 20\text{ V}, I_D = 16\text{ A}$	N-Ch 2	-	31.8	48	
Gate-Source Charge <sup>c</sup>	$Q_{gs}$	$V_{GS} = 10\text{ V}$	$V_{DS} = 20\text{ V}, I_D = 6\text{ A}$	N-Ch 1	-	2.24	-	
		$V_{GS} = 10\text{ V}$	$V_{DS} = 20\text{ V}, I_D = 16\text{ A}$	N-Ch 2	-	5.5	-	
Gate-Drain Charge <sup>c</sup>	$Q_{gd}$	$V_{GS} = 10\text{ V}$	$V_{DS} = 20\text{ V}, I_D = 6\text{ A}$	N-Ch 1	-	2.06	-	
		$V_{GS} = 10\text{ V}$	$V_{DS} = 20\text{ V}, I_D = 16\text{ A}$	N-Ch 2	-	4.7	-	
Gate Resistance	$R_g$	$f = 1\text{ MHz}$		N-Ch 1	1.2	2.52	5	$\Omega$
				N-Ch 2	3	7.93	13	

**Notes**

- a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .
- b. Guaranteed by design, not subject to production testing.
- c. Independent of operating temperature.



SPECIFICATIONS ( $T_C = 25\text{ }^\circ\text{C}$ , unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Turn-On Delay Time <sup>c</sup>	$t_{d(on)}$	$V_{DD} = 20\text{ V}$ , $R_L = 20\text{ }\Omega$ $I_D \cong 1\text{ A}$ , $V_{GEN} = 10\text{ V}$ , $R_g = 1\text{ }\Omega$	N-Ch 1	-	4.8	7.2	ns
		$V_{DD} = 20\text{ V}$ , $R_L = 20\text{ }\Omega$ $I_D \cong 1\text{ A}$ , $V_{GEN} = 10\text{ V}$ , $R_g = 1\text{ }\Omega$	N-Ch 2	-	7.7	11.6	
Rise Time <sup>c</sup>	$t_r$	$V_{DD} = 20\text{ V}$ , $R_L = 20\text{ }\Omega$ $I_D \cong 1\text{ A}$ , $V_{GEN} = 10\text{ V}$ , $R_g = 1\text{ }\Omega$	N-Ch 1	-	9.3	14	
		$V_{DD} = 20\text{ V}$ , $R_L = 20\text{ }\Omega$ $I_D \cong 1\text{ A}$ , $V_{GEN} = 10\text{ V}$ , $R_g = 1\text{ }\Omega$	N-Ch 2	-	9.5	14.3	
Turn-Off Delay Time <sup>c</sup>	$t_{d(off)}$	$V_{DD} = 20\text{ V}$ , $R_L = 20\text{ }\Omega$ $I_D \cong 1\text{ A}$ , $V_{GEN} = 10\text{ V}$ , $R_g = 1\text{ }\Omega$	N-Ch 1	-	15.6	23.4	
		$V_{DD} = 20\text{ V}$ , $R_L = 20\text{ }\Omega$ $I_D \cong 1\text{ A}$ , $V_{GEN} = 10\text{ V}$ , $R_g = 1\text{ }\Omega$	N-Ch 2	-	47	70	
Fall Time <sup>c</sup>	$t_f$	$V_{DD} = 20\text{ V}$ , $R_L = 20\text{ }\Omega$ $I_D \cong 1\text{ A}$ , $V_{GEN} = 10\text{ V}$ , $R_g = 1\text{ }\Omega$	N-Ch 1	-	4.9	7.4	
		$V_{DD} = 20\text{ V}$ , $R_L = 20\text{ }\Omega$ $I_D \cong 1\text{ A}$ , $V_{GEN} = 10\text{ V}$ , $R_g = 1\text{ }\Omega$	N-Ch 2	-	13.5	20.3	
Source-Drain Diode Ratings and Characteristics <sup>b</sup>							
Pulsed Current <sup>a</sup>	$I_{SM}$		N-Ch 1	-	-	60	A
			N-Ch 2	-	-	72	
Forward Voltage	$V_{SD}$	$I_F = 8\text{ A}$ , $V_{GS} = 0\text{ V}$	N-Ch 1	-	0.8	1.2	V
		$I_F = 17\text{ A}$ , $V_{GS} = 0\text{ V}$	N-Ch 2	-	0.8	1.2	

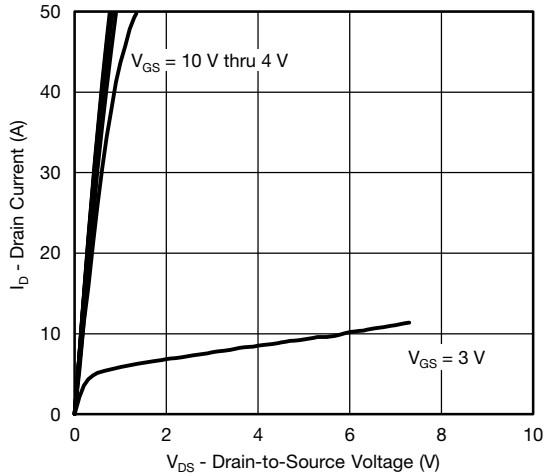
**Notes**

- Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .
- Guaranteed by design, not subject to production testing.
- Independent of operating temperature.

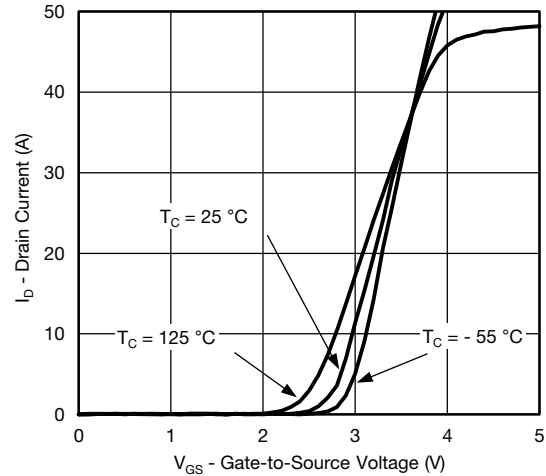
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



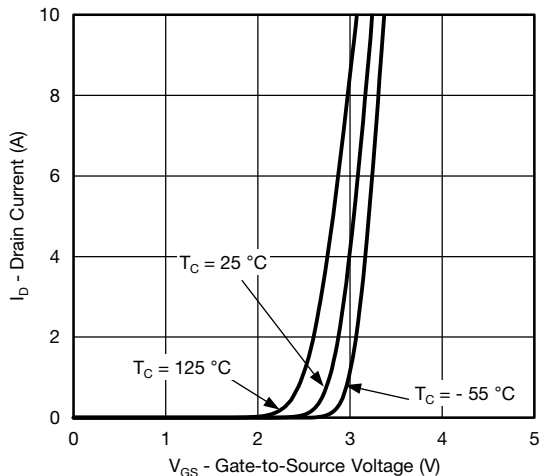
**N-CHANNEL 1 TYPICAL CHARACTERISTICS** ( $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise noted)



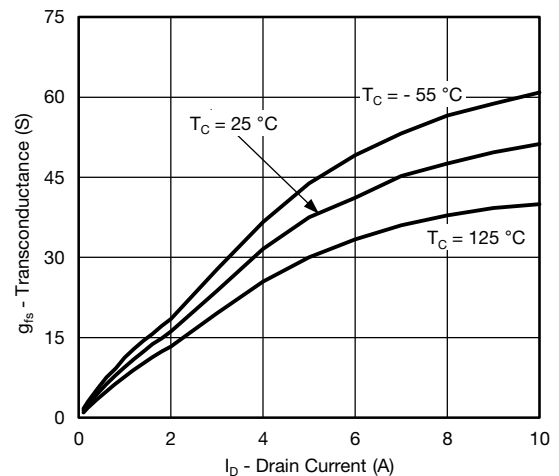
**Output Characteristics**



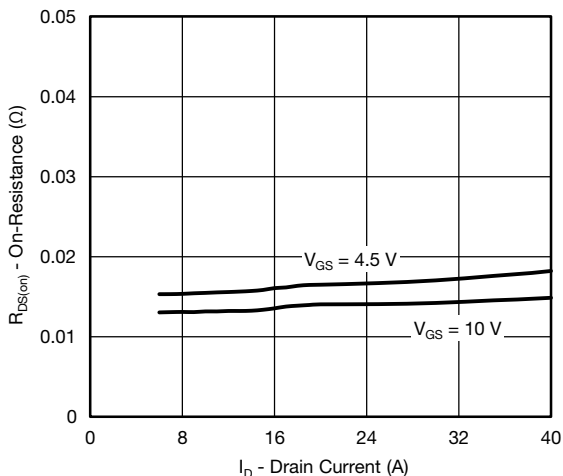
**Transfer Characteristics**



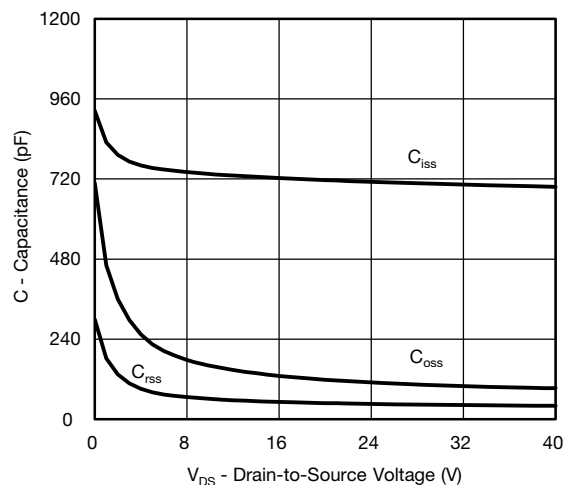
**Transfer Characteristics**



**Transconductance**



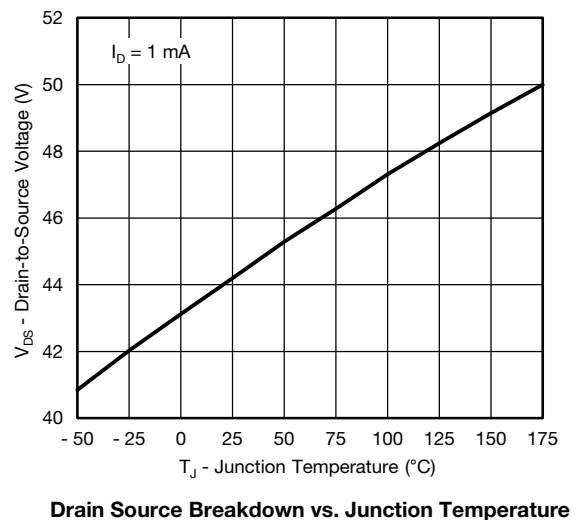
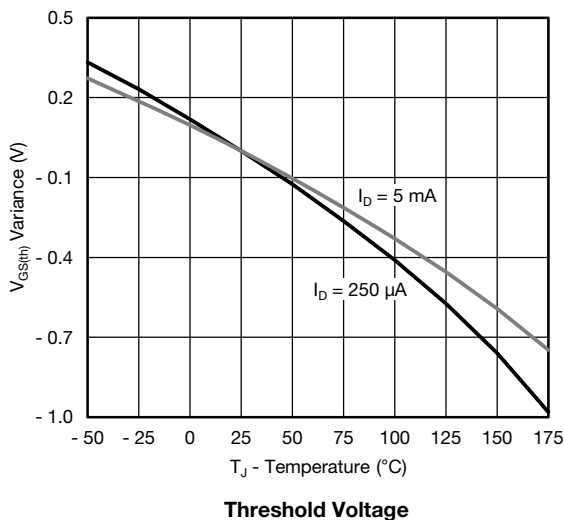
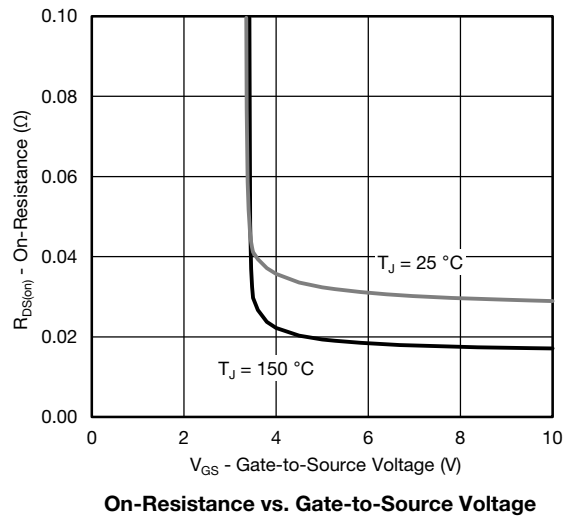
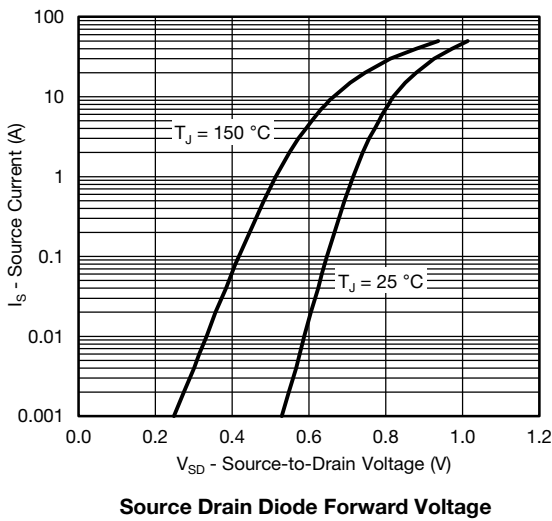
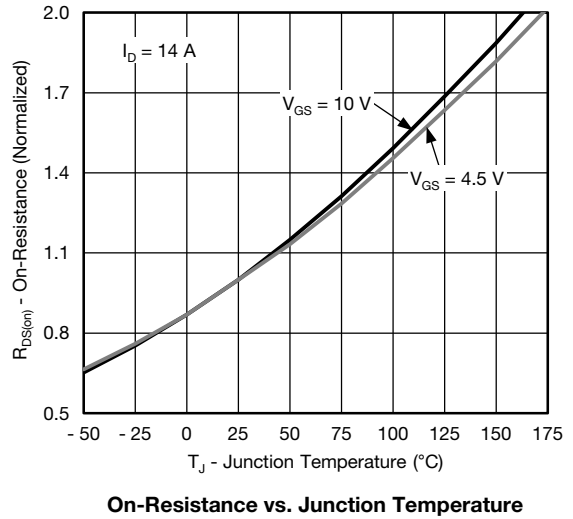
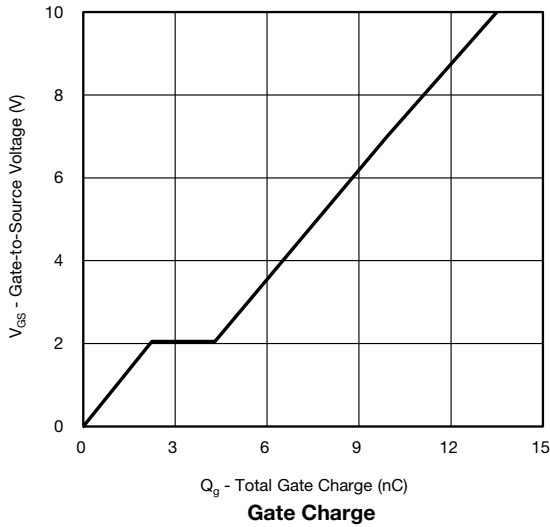
**On-Resistance vs. Drain Current**



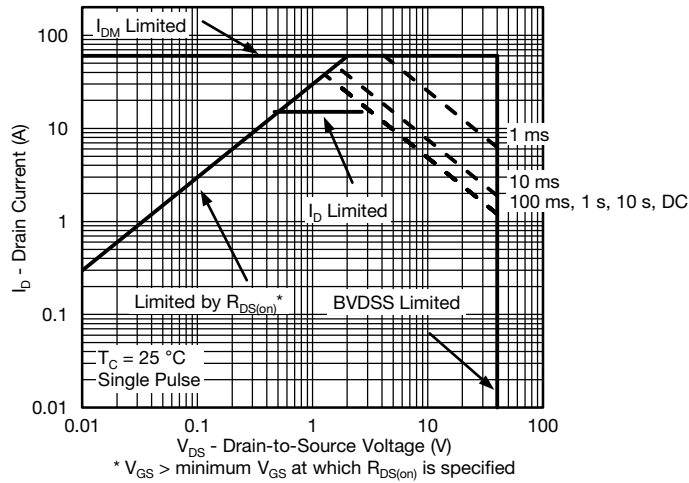
**Capacitance**



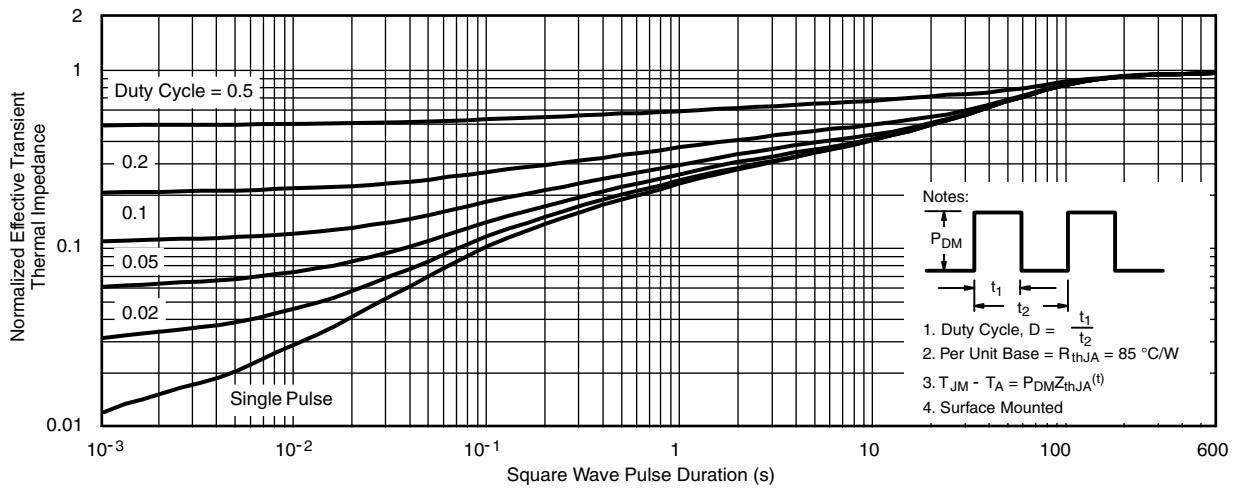
**N-CHANNEL 1 TYPICAL CHARACTERISTICS** ( $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise noted)



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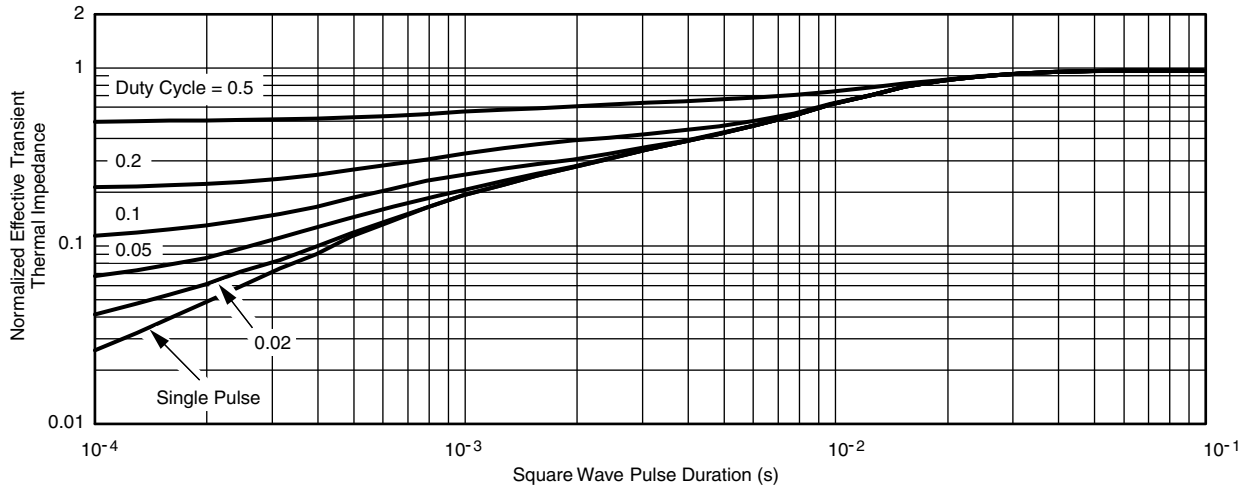


**Safe Operating Area**



**Normalized Thermal Transient Impedance, Junction-to-Ambient**

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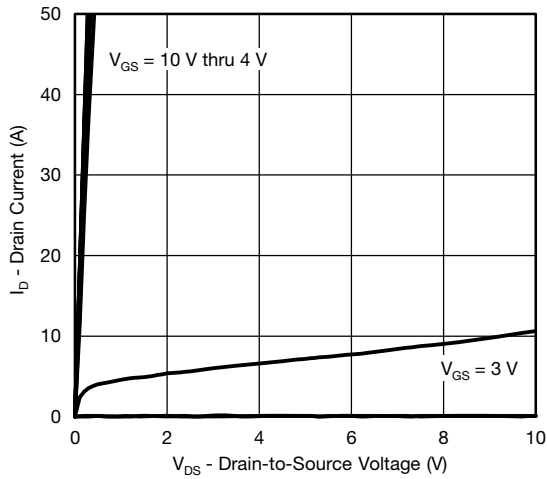
**Normalized Thermal Transient Impedance, Junction-to-Case**

**Note**

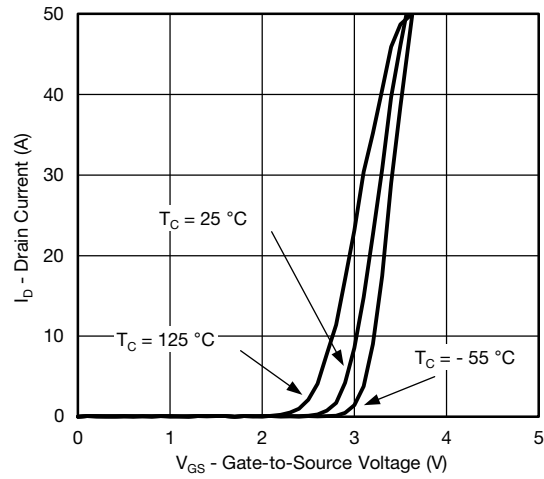
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 are given for general guidelines only to enable the user to get a “ball park” indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.



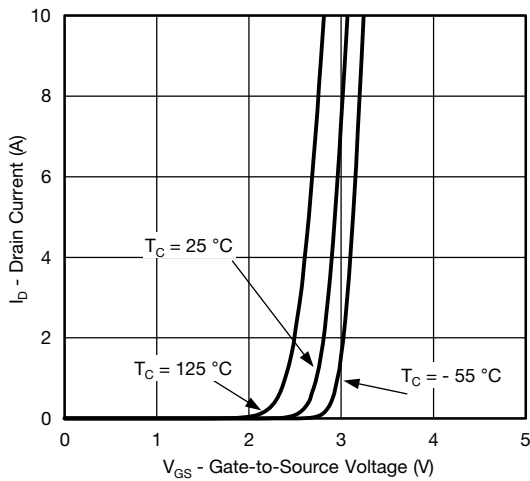
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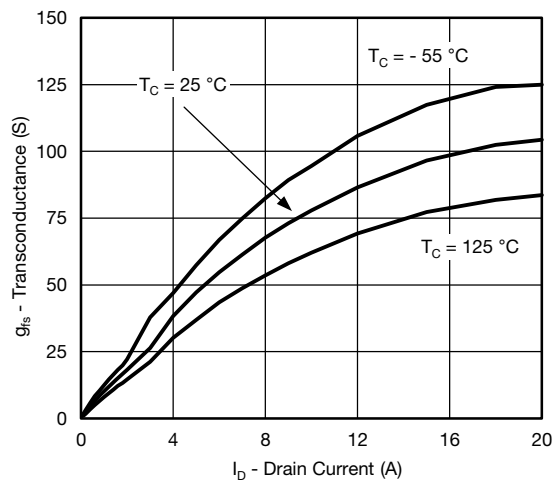
**Output Characteristics**



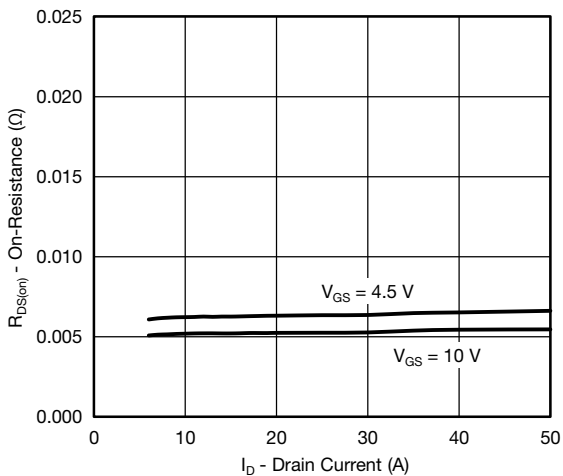
**Transfer Characteristics**



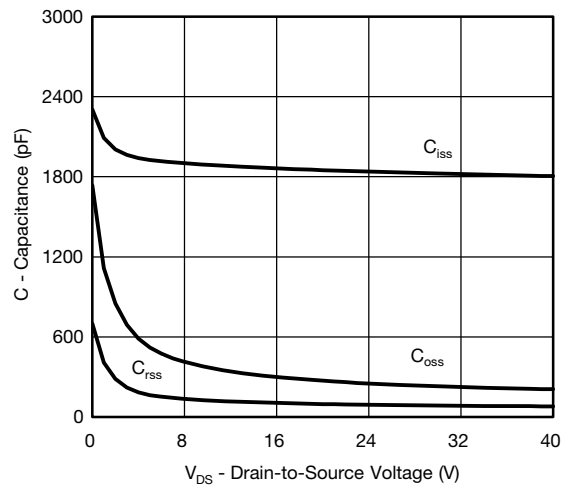
**Transfer Characteristics**



**Transconductance**



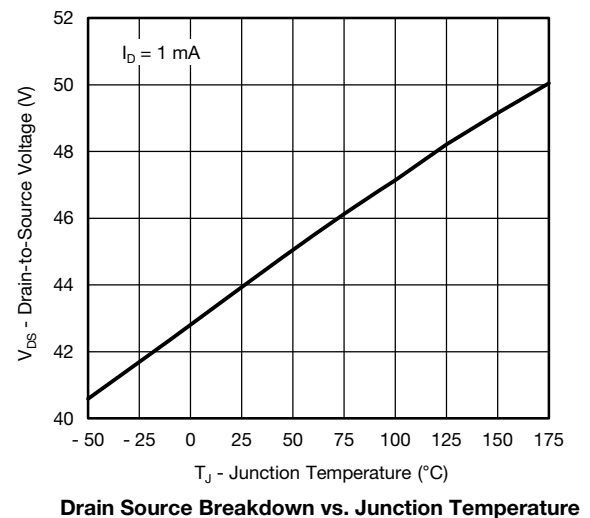
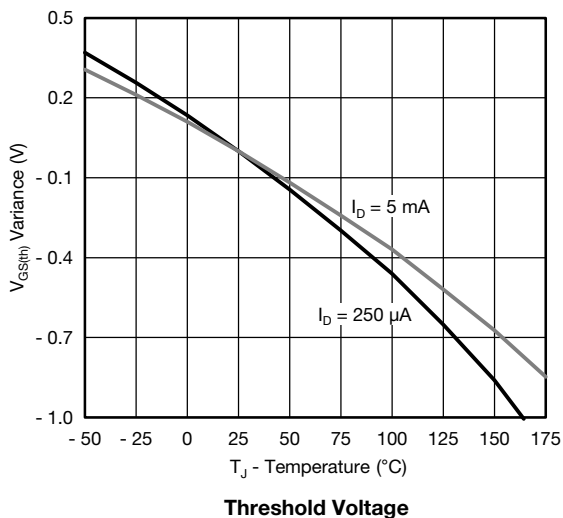
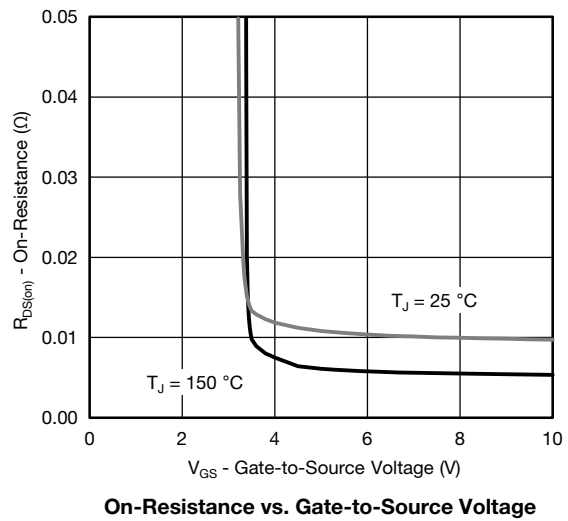
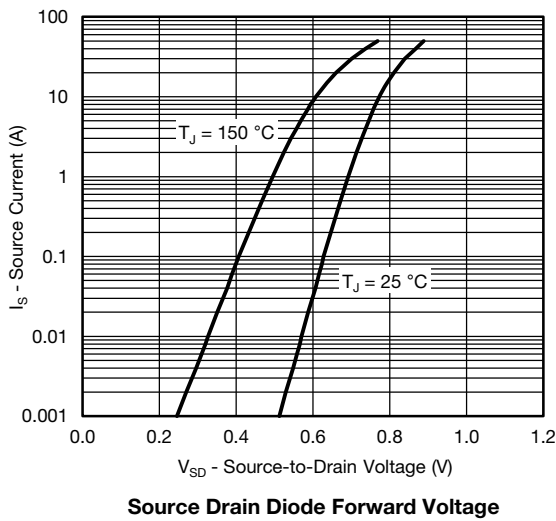
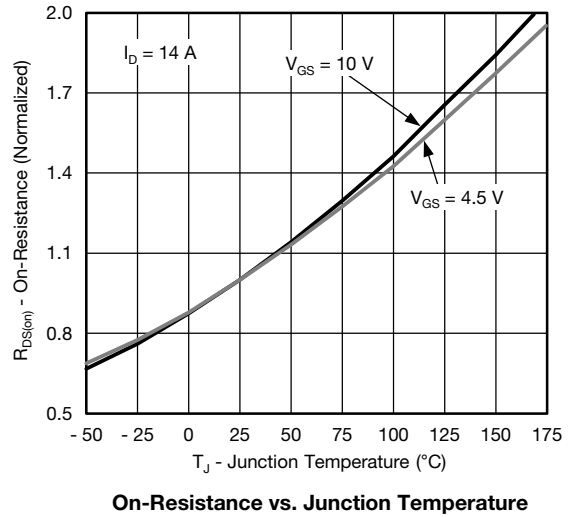
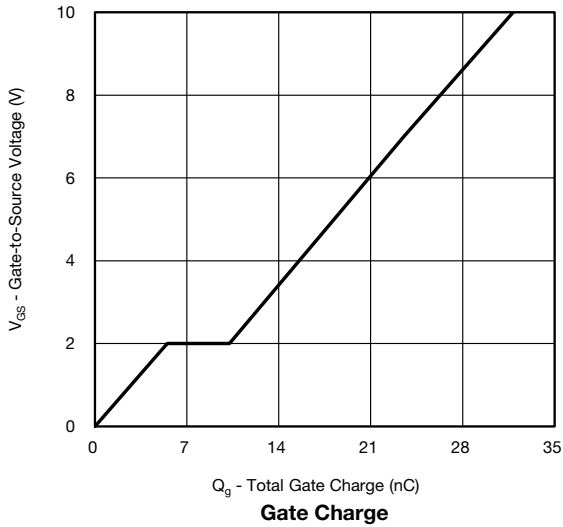
**On-Resistance vs. Drain Current**



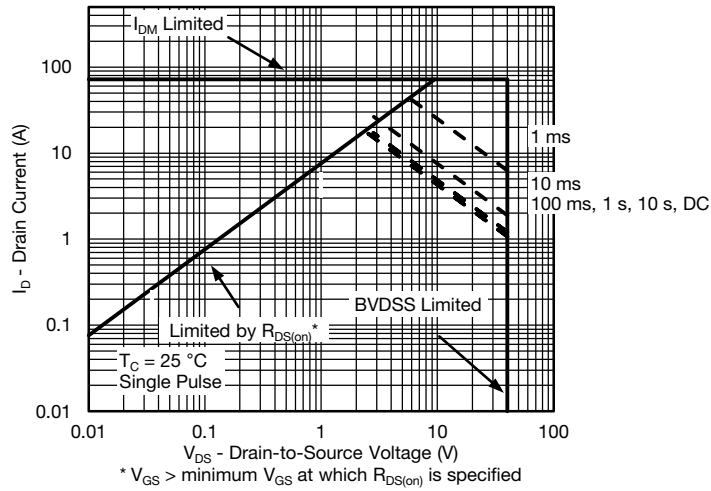
**Capacitance**



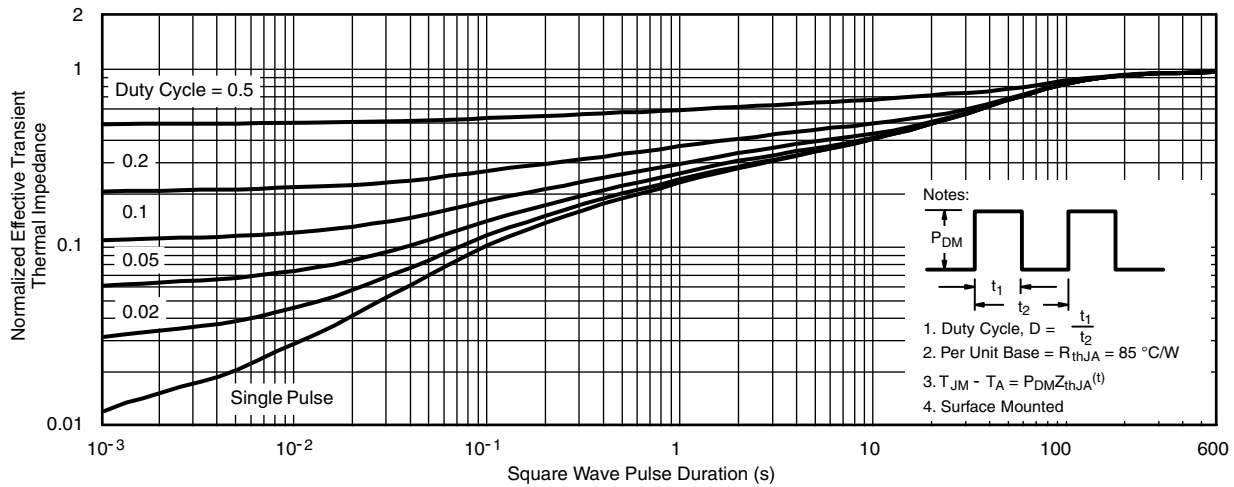
**N-CHANNEL 2 TYPICAL CHARACTERISTICS** ( $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise noted)



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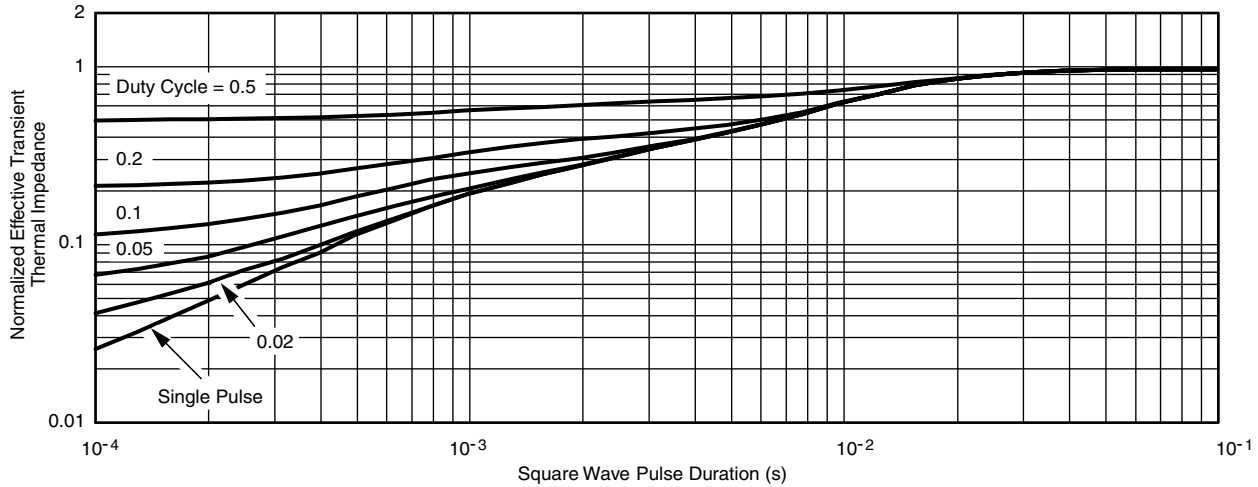
**Safe Operating Area**



**Normalized Thermal Transient Impedance, Junction-to-Ambient**



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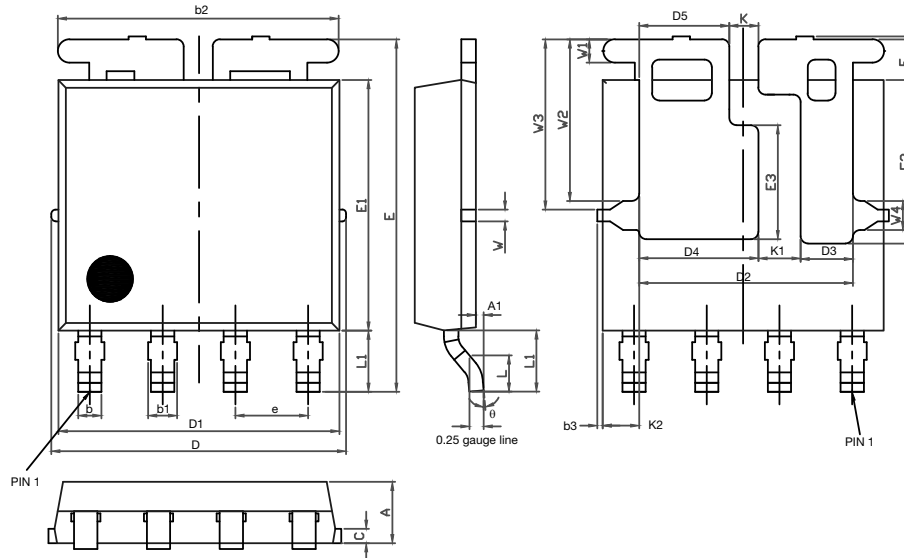
**Normalized Thermal Transient Impedance, Junction-to-Case**

**Note**

- The characteristics shown in the two graphs
  - Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)
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 are given for general guidelines only to enable the user to get a “ball park” indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see [www.vishay.com/ppg?62767](http://www.vishay.com/ppg?62767).

## PowerPAK<sup>®</sup> SO-8L Assymmetric Case Outline



DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.00	1.07	1.14	0.039	0.042	0.045
A1	0.00	0.06	0.13	0.000	0.003	0.005
b	0.33	0.41	0.48	0.013	0.016	0.019
b1	0.44	0.51	0.58	0.017	0.020	0.023
b2	4.80	4.90	5.00	0.189	0.193	0.197
b3	0.04	0.12	0.20	0.002	0.005	0.008
c	0.20	0.25	0.30	0.008	0.010	0.012
D	5.00	5.13	5.25	0.197	0.202	0.207
D1	4.80	4.90	5.00	0.189	0.193	0.197
D2	3.63	3.73	3.83	0.143	0.147	0.151
D3	0.81	0.91	1.01	0.032	0.036	0.040
D4	1.98	2.08	2.18	0.078	0.082	0.086
D5	1.47	1.57	1.67	0.058	0.062	0.066
e	1.20	1.27	1.34	0.047	0.050	0.053
E	6.05	6.15	6.25	0.238	0.242	0.246
E1	4.27	4.37	4.47	0.168	0.172	0.176
E2	2.75	2.85	2.95	0.108	0.112	0.116
E3	1.89	1.99	2.09	0.074	0.078	0.082
F	0.05	0.12	0.19	0.002	0.005	0.007
L	0.62	0.72	0.82	0.024	0.028	0.032
L1	0.92	1.07	1.22	0.036	0.042	0.048
K	0.41	0.51	0.61	0.016	0.020	0.024
K1	0.64	0.74	0.84	0.025	0.029	0.033
K2	0.54	0.64	0.74	0.021	0.025	0.029
W	0.13	0.23	0.33	0.005	0.009	0.013
W1	0.31	0.41	0.51	0.012	0.016	0.020
W2	2.72	2.82	2.92	0.107	0.111	0.115
W3	2.86	2.96	3.06	0.113	0.117	0.120
W4	0.41	0.51	0.61	0.016	0.020	0.024
θ	5°	10°	12°	5°	10°	12°

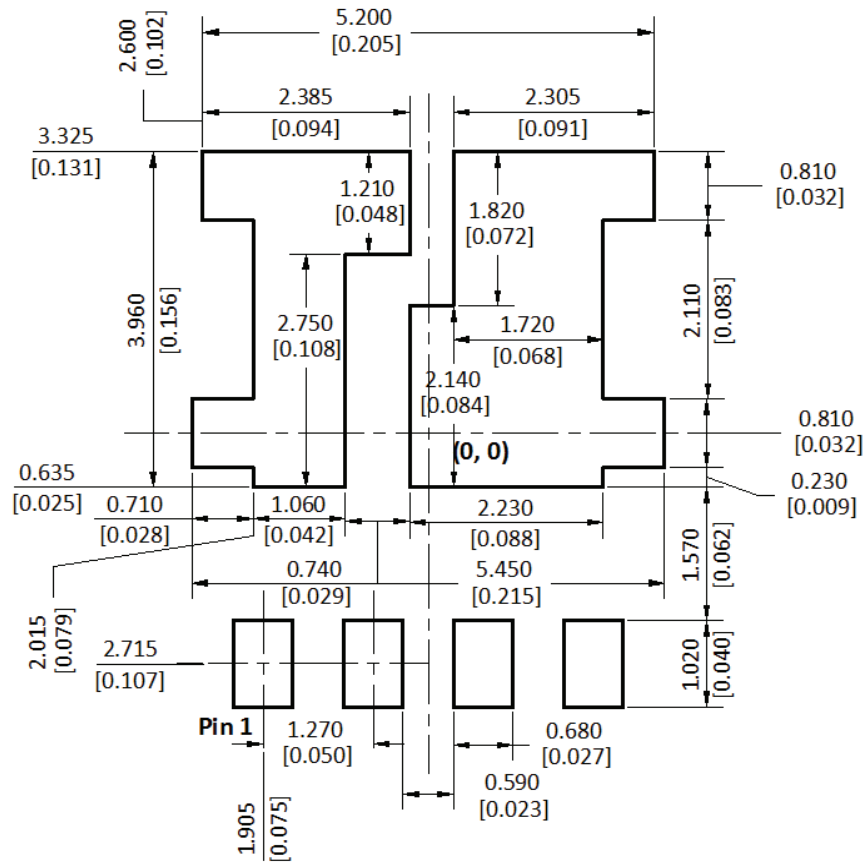
DWG: 6009

**Note**

- Millimeters will govern



## RECOMMENDED MINIMUM PADS FOR PowerPAK® SO-8L DUAL ASYMMETRIC





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