



**THE DATASHEET OF
BSC014N06NSATMA1**



MOSFET

OptiMOS™ Power-Transistor, 60 V

Features

- Optimized for high performance SMPS, e.g. sync. rec.
- 175°C rated
- 100% avalanche tested
- Superior thermal resistance
- N-channel
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21
- Higher solder joint reliability due to enlarged source interconnection

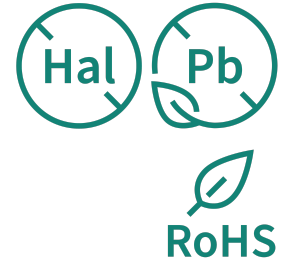
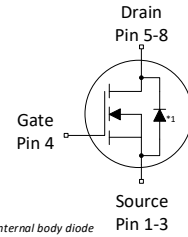
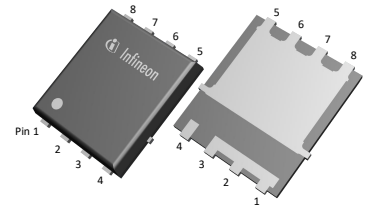
Product validation

Fully qualified according to JEDEC for Industrial Applications

Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS}	60	V
$R_{DS(on),max}$	1.45	mΩ
I_D	257	A
Q_{OSS}	100	nC
$Q_G(0V..10V)$	89	nC

PG-TDSON-8



Type/Ordering Code	Package	Marking	Related Links
BSC014N06NS	PG-TDSON-8	014N06NS	-



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1 Maximum ratings

unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Continuous drain current ¹⁾	I_D	-	-	257 182 31	A	$V_{GS}=10\text{ V}, T_C=25\text{ °C}$ $V_{GS}=10\text{ V}, T_C=100\text{ °C}$ $V_{GS}=10\text{ V}, T_A=25\text{ °C}, R_{thJA}=50\text{ K/W}^2)$
Pulsed drain current ³⁾	$I_{D,pulse}$	-	-	1028	A	$T_C=25\text{ °C}$
Avalanche energy, single pulse ⁴⁾	E_{AS}	-	-	580	mJ	$I_D=50\text{ A}, R_{GS}=25\text{ }\Omega$
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	-	-	188 3.0	W	$T_C=25\text{ °C}$ $T_A=25\text{ °C}, R_{thJA}=50\text{ K/W}^2)$
Operating and storage temperature	T_j, T_{stg}	-55	-	175	°C	-

¹⁾ Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature as specified. For other case temperatures please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.

²⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

³⁾ See Diagram 3 for more detailed information

⁴⁾ See Diagram 13 for more detailed information

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	0.5	0.8	K/W	-
Thermal resistance, junction - case, top	R_{thJC}	-	-	20	K/W	-
Device on PCB, 6 cm ² cooling area ⁵⁾	R_{thJA}	-	-	50	K/W	-

⁵⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 μm thick) copper area for drain connection. PCB is vertical in still air.

3 Electrical characteristics

unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	60	-	-	V	$V_{GS}=0\text{ V}, I_D=1\text{ mA}$
Gate threshold voltage	$V_{GS(th)}$	2.1	2.8	3.3	V	$V_{DS}=V_{GS}, I_D=120\text{ }\mu\text{A}$
Zero gate voltage drain current	I_{DSS}	-	0.5 10	1 100	μA	$V_{DS}=60\text{ V}, V_{GS}=0\text{ V}, T_j=25\text{ }^\circ\text{C}$ $V_{DS}=60\text{ V}, V_{GS}=0\text{ V}, T_j=125\text{ }^\circ\text{C}$
Gate-source leakage current	I_{GSS}	-	10	100	nA	$V_{GS}=20\text{ V}, V_{DS}=0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	1.2 1.6	1.45 2.2	m Ω	$V_{GS}=10\text{ V}, I_D=50\text{ A}$ $V_{GS}=6\text{ V}, I_D=12.5\text{ A}$
Gate resistance ⁶⁾	R_G	-	2	3	Ω	-
Transconductance	g_{fs}	75	150	-	S	$ V_{DS} >2 I_D R_{DS(on)max}, I_D=50\text{ A}$

⁶⁾ Defined by design. Not subject to production test

Table 5 Dynamic characteristics ⁷⁾

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	6500	8125	pF	$V_{GS}=0\text{ V}, V_{DS}=30\text{ V}, f=1\text{ MHz}$
Output capacitance	C_{oss}	-	1500	1875	pF	$V_{GS}=0\text{ V}, V_{DS}=30\text{ V}, f=1\text{ MHz}$
Reverse transfer capacitance	C_{rss}	-	59	118	pF	$V_{GS}=0\text{ V}, V_{DS}=30\text{ V}, f=1\text{ MHz}$
Turn-on delay time	$t_{d(on)}$	-	23	-	ns	$V_{DD}=30\text{ V}, V_{GS}=10\text{ V}, I_D=30\text{ A},$ $R_{G,ext}=2\text{ }\Omega$
Rise time	t_r	-	10	-	ns	$V_{DD}=30\text{ V}, V_{GS}=10\text{ V}, I_D=30\text{ A},$ $R_{G,ext}=2\text{ }\Omega$
Turn-off delay time	$t_{d(off)}$	-	43	-	ns	$V_{DD}=30\text{ V}, V_{GS}=10\text{ V}, I_D=30\text{ A},$ $R_{G,ext}=2\text{ }\Omega$
Fall time	t_f	-	11	-	ns	$V_{DD}=30\text{ V}, V_{GS}=10\text{ V}, I_D=30\text{ A},$ $R_{G,ext}=2\text{ }\Omega$

⁷⁾ Defined by design. Not subject to production test

Table 6 Gate charge characteristics ⁸⁾

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	28	-	nC	$V_{DD}=30\text{ V}, I_D=50\text{ A}, V_{GS}=0\text{ to }10\text{ V}$
Gate charge at threshold	$Q_{g(th)}$	-	18	-	nC	$V_{DD}=30\text{ V}, I_D=50\text{ A}, V_{GS}=0\text{ to }10\text{ V}$
Gate to drain charge	Q_{gd}	-	16	21	nC	$V_{DD}=30\text{ V}, I_D=50\text{ A}, V_{GS}=0\text{ to }10\text{ V}$

Table 6 Gate charge characteristics ⁸⁾

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Switching charge	Q_{sw}	-	26	-	nC	$V_{DD}=30\text{ V}$, $I_D=50\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate charge total	Q_g	-	89	104	nC	$V_{DD}=30\text{ V}$, $I_D=50\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate plateau voltage	$V_{plateau}$	-	4.3	-	V	$V_{DD}=30\text{ V}$, $I_D=50\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate charge total, sync. FET	$Q_{g(sync)}$	-	78	-	nC	$V_{DS}=0.1\text{ V}$, $V_{GS}=0\text{ to }10\text{ V}$
Output charge	Q_{oss}	-	100	125	nC	$V_{DD}=30\text{ V}$, $V_{GS}=0\text{ V}$

⁸⁾ See "Gate charge waveforms" for parameter definition. Defined by design. Not subject to production test

Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	156	A	$T_C=25\text{ °C}$
Diode pulse current	$I_{S,pulse}$	-	-	1028	A	$T_C=25\text{ °C}$
Diode forward voltage	V_{SD}	-	0.84	1.2	V	$V_{GS}=0\text{ V}$, $I_F=50\text{ A}$, $T_j=25\text{ °C}$
Reverse recovery time ⁹⁾	t_{rr}	-	52	83	ns	$V_R=30\text{ V}$, $I_F=50\text{ A}$, $di_F/dt=100\text{ A}/\mu\text{s}$
Reverse recovery charge ⁹⁾	Q_{rr}	-	139	-	nC	$V_R=30\text{ V}$, $I_F=50\text{ A}$, $di_F/dt=100\text{ A}/\mu\text{s}$

⁹⁾ Defined by design. Not subject to production test

4 Electrical characteristics diagrams

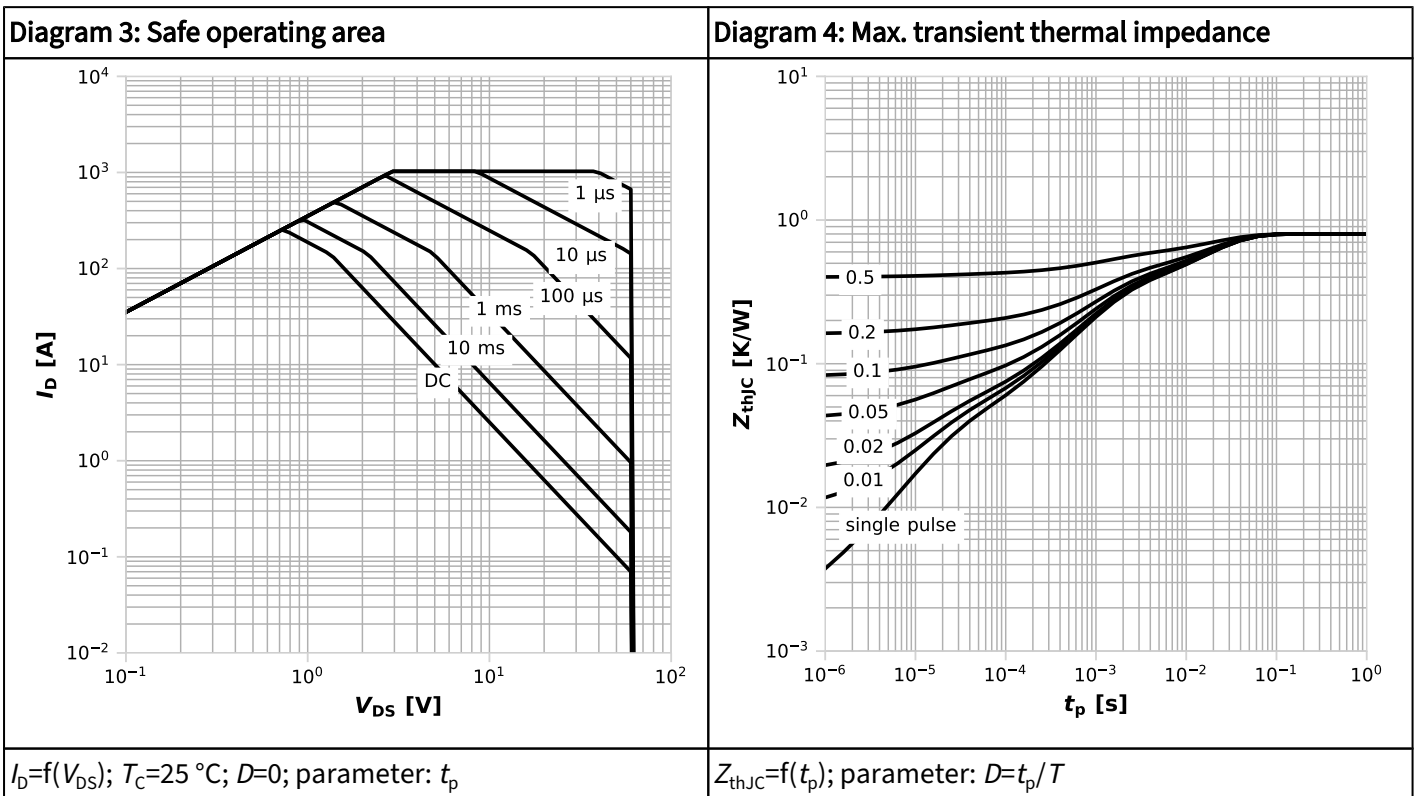
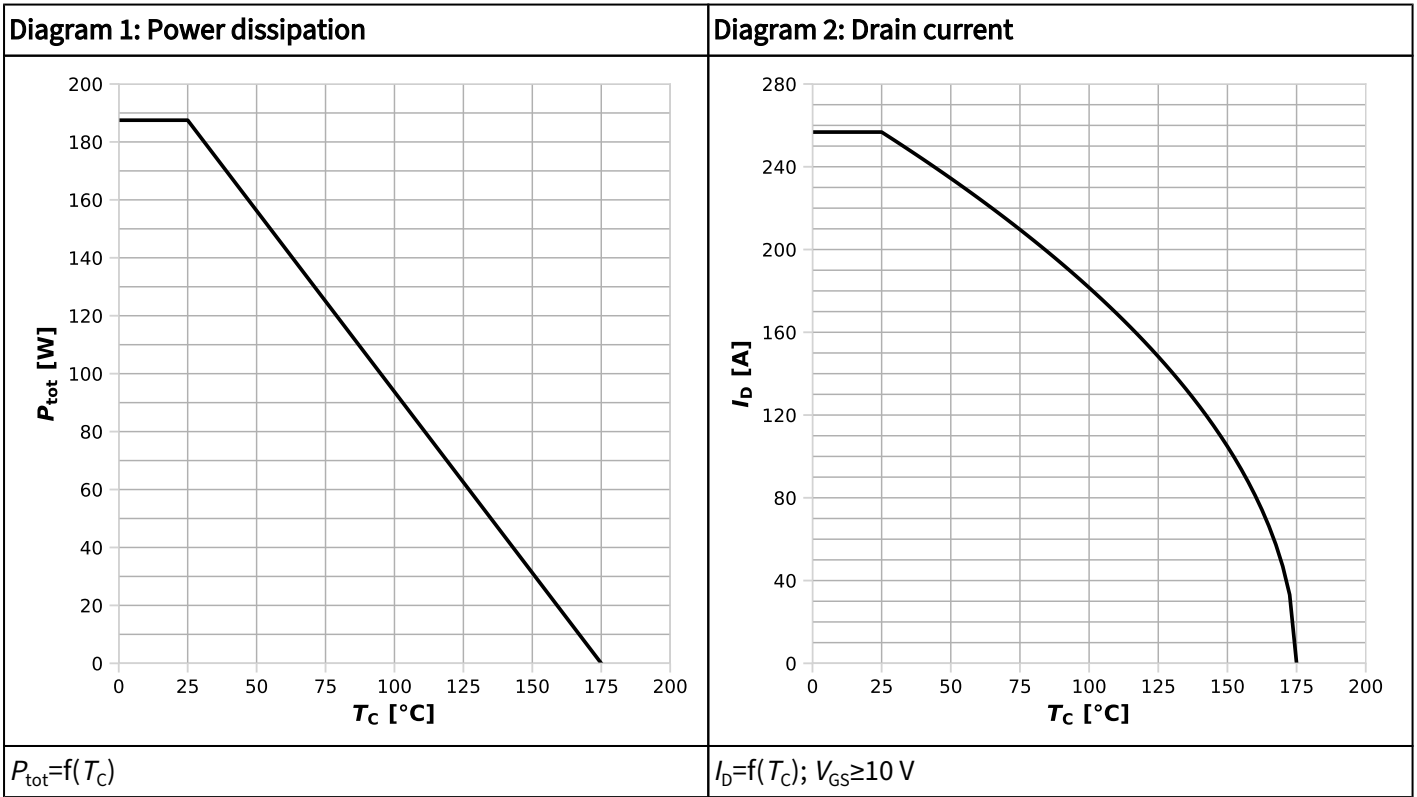
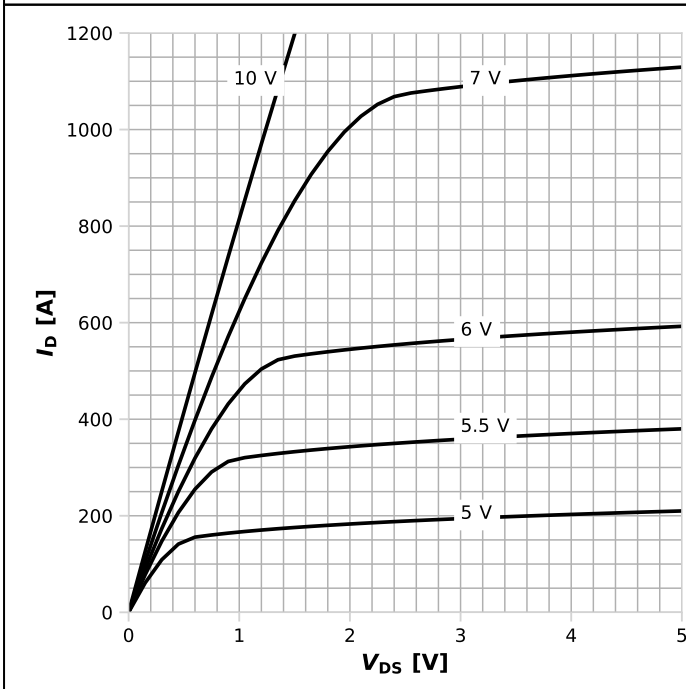
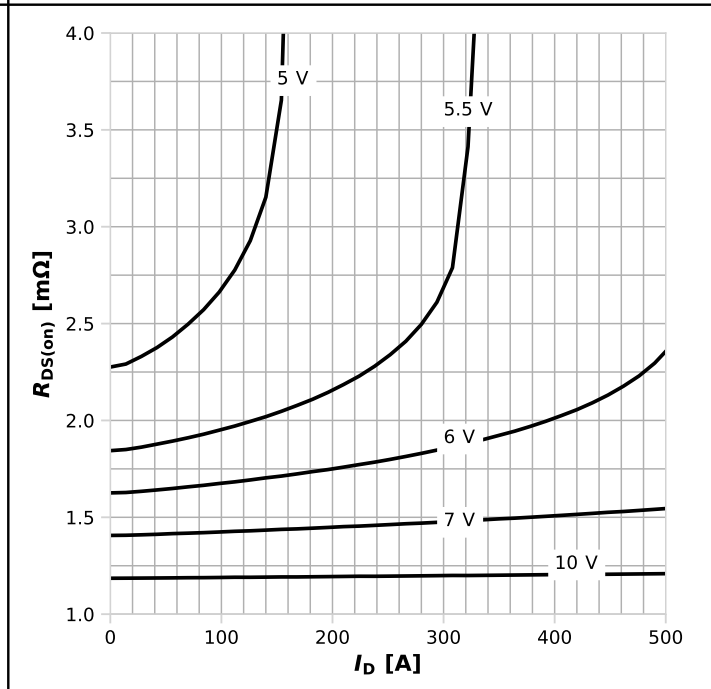


Diagram 5: Typ. output characteristics



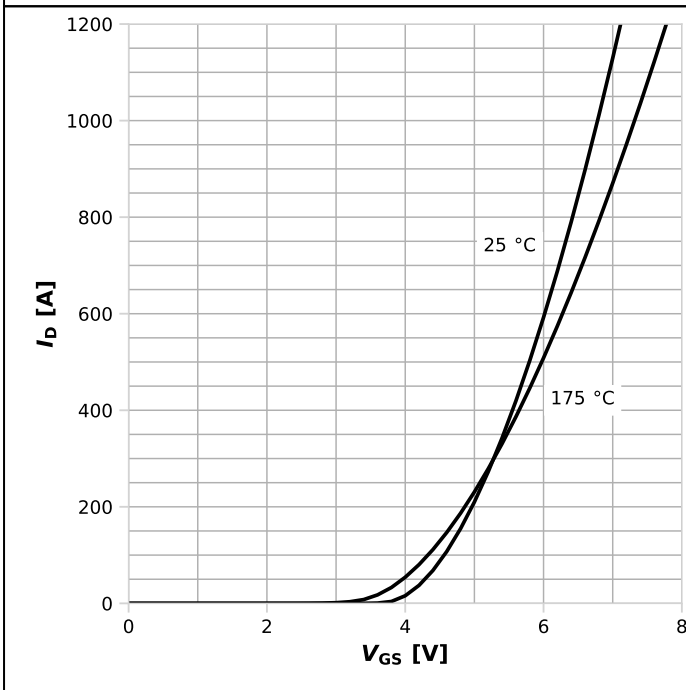
$I_D = f(V_{DS}), T_j = 25\text{ °C};$ parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



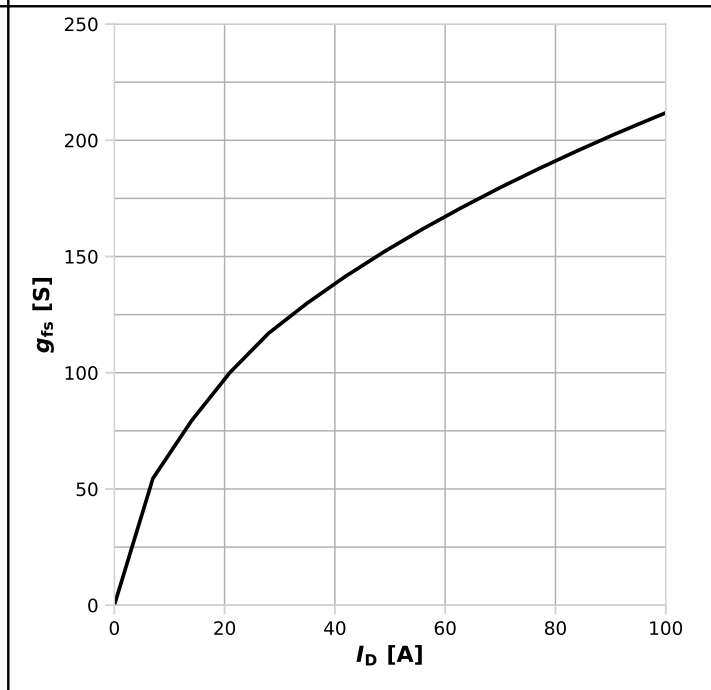
$R_{DS(on)} = f(I_D), T_j = 25\text{ °C};$ parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



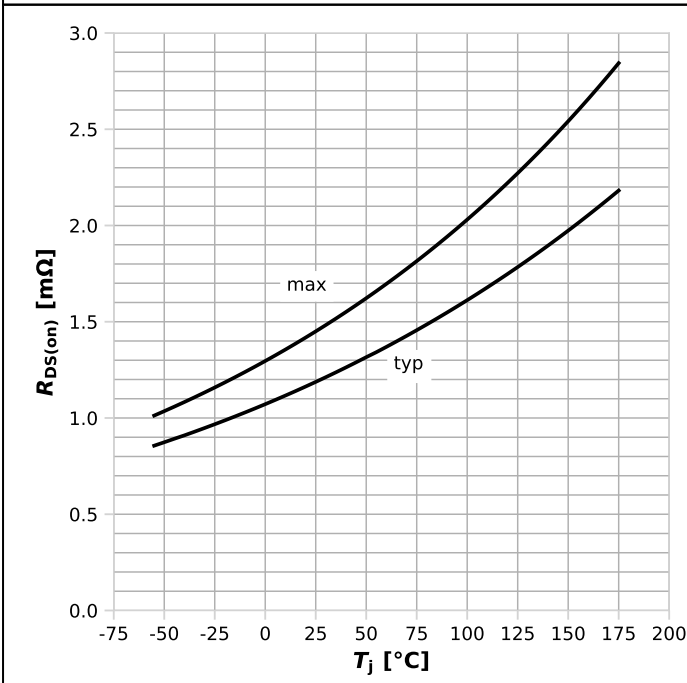
$I_D = f(V_{GS}), |V_{DS}| > 2|I_D|R_{DS(on)max};$ parameter: T_j

Diagram 8: Typ. forward transconductance



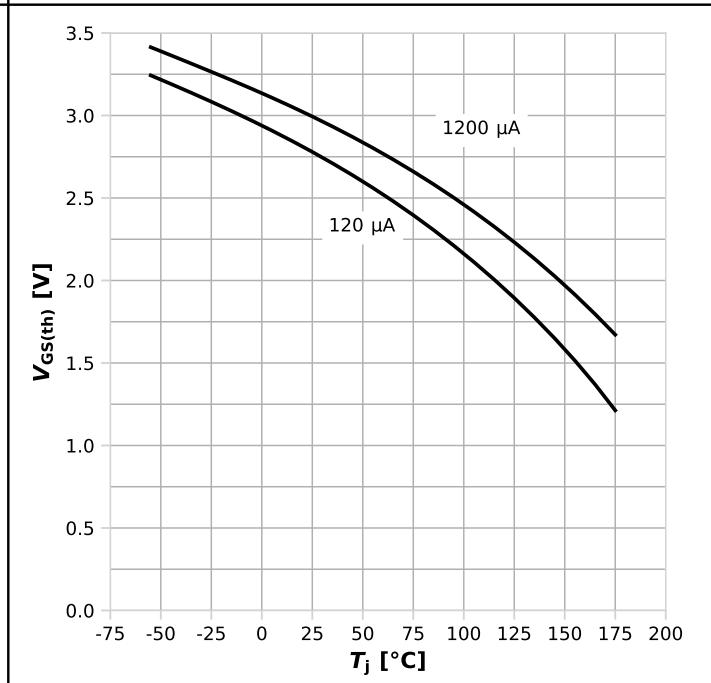
$g_{fs} = f(I_D); T_j = 25\text{ °C}$

Diagram 9: Drain-source on resistance



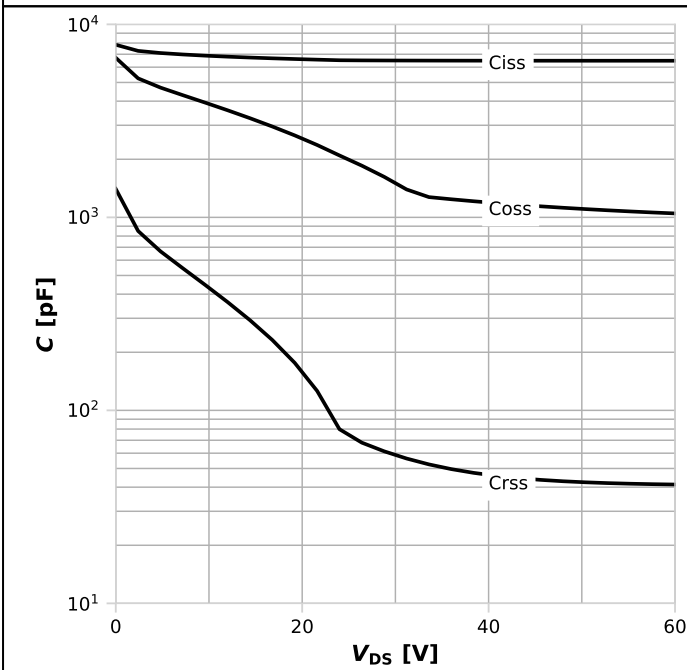
$R_{DS(on)}=f(T_j), I_D=50\text{ A}, V_{GS}=10\text{ V}$

Diagram 10: Typ. gate threshold voltage



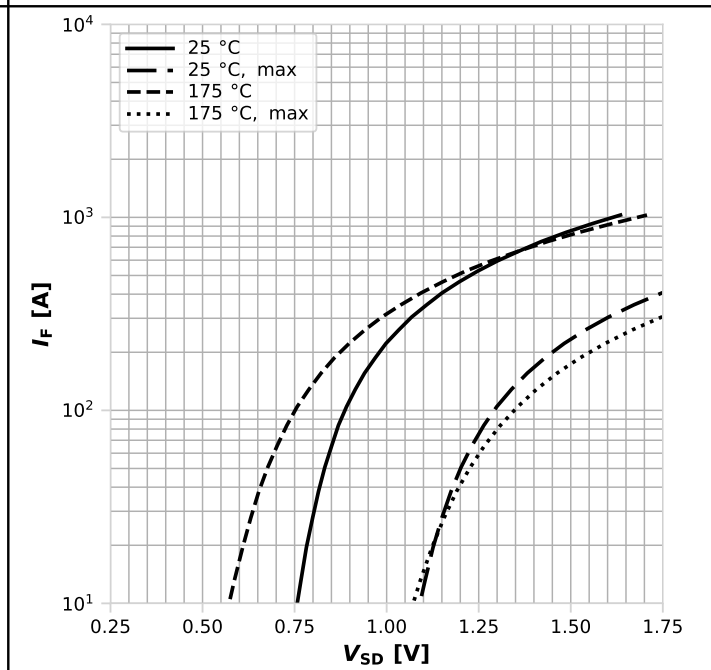
$V_{GS(th)}=f(T_j), V_{GS}=V_{DS};$ parameter: I_D

Diagram 11: Typ. capacitances



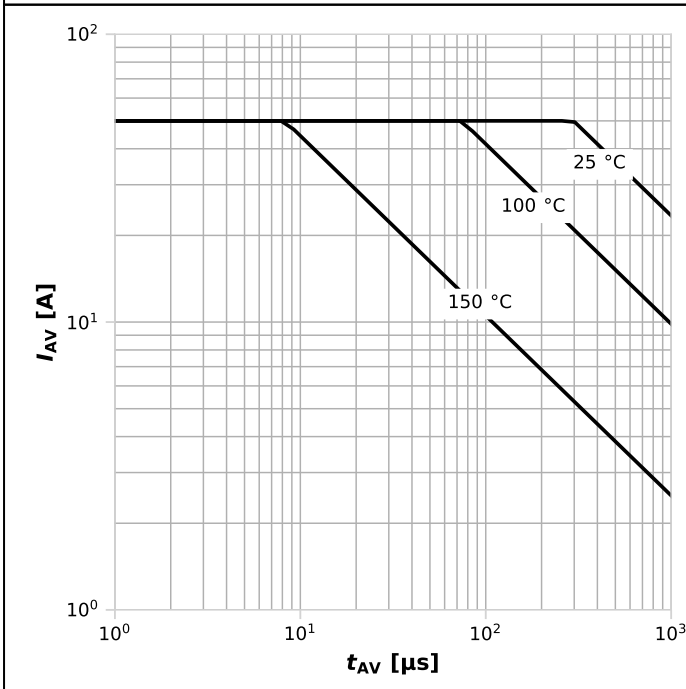
$C=f(V_{DS}); V_{GS}=0\text{ V}; f=1\text{ MHz}$

Diagram 12: Forward characteristics of reverse diode



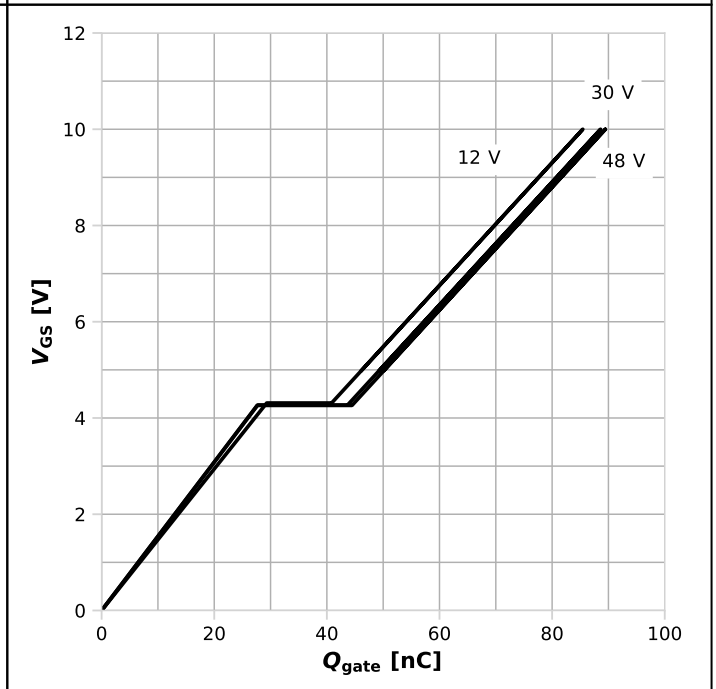
$I_F=f(V_{SD});$ parameter: T_j

Diagram 13: Avalanche characteristics



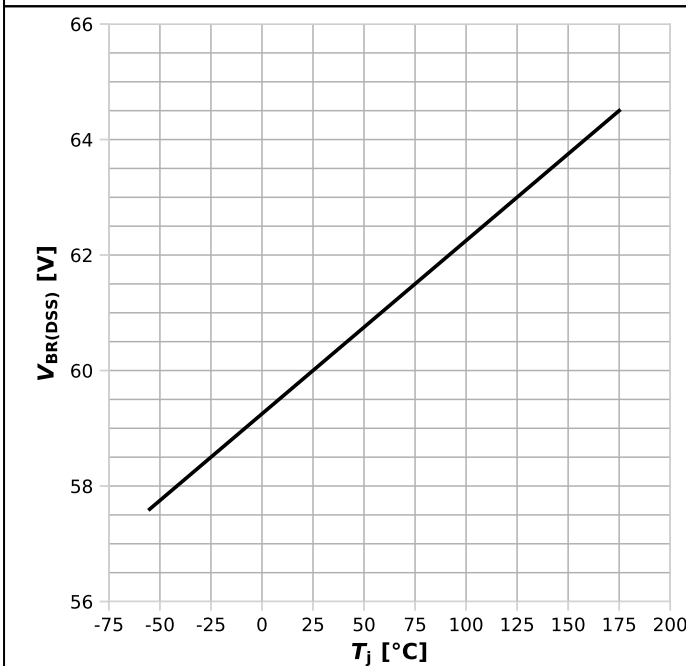
$I_{AS}=f(t_{AV}); R_{GS}=25 \Omega$; parameter: $T_{j(start)}$

Diagram 14: Typ. gate charge



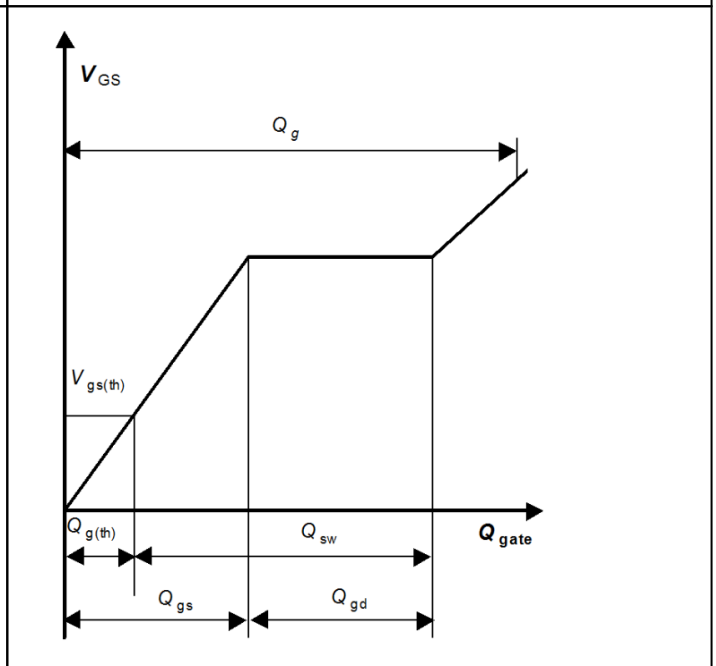
$V_{GS}=f(Q_{gate}); I_D=50 \text{ A pulsed}$; parameter: V_{DD}

Diagram 15: Drain-source breakdown voltage



$V_{BR(DSS)}=f(T_j); I_D=1 \text{ mA}$

Gate charge waveforms



-

5 Package Outlines

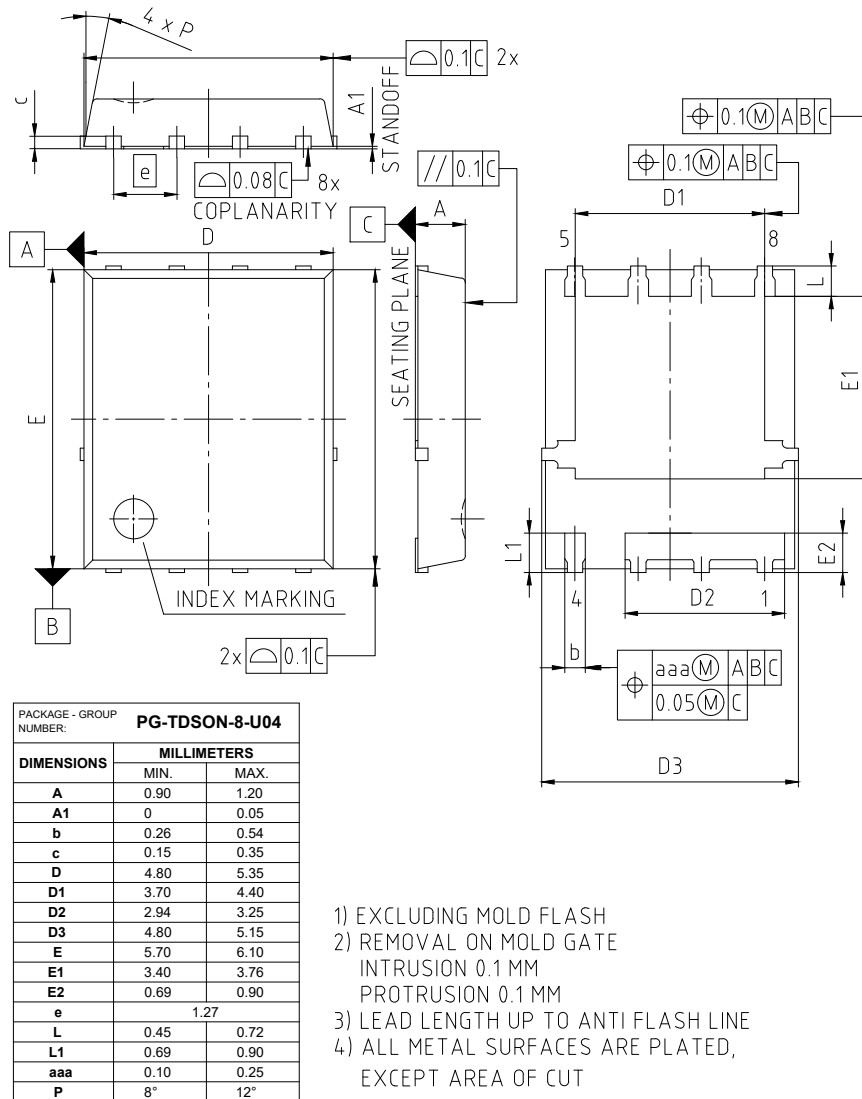


Figure 1 Outline PG-TDSON-8, dimensions in mm

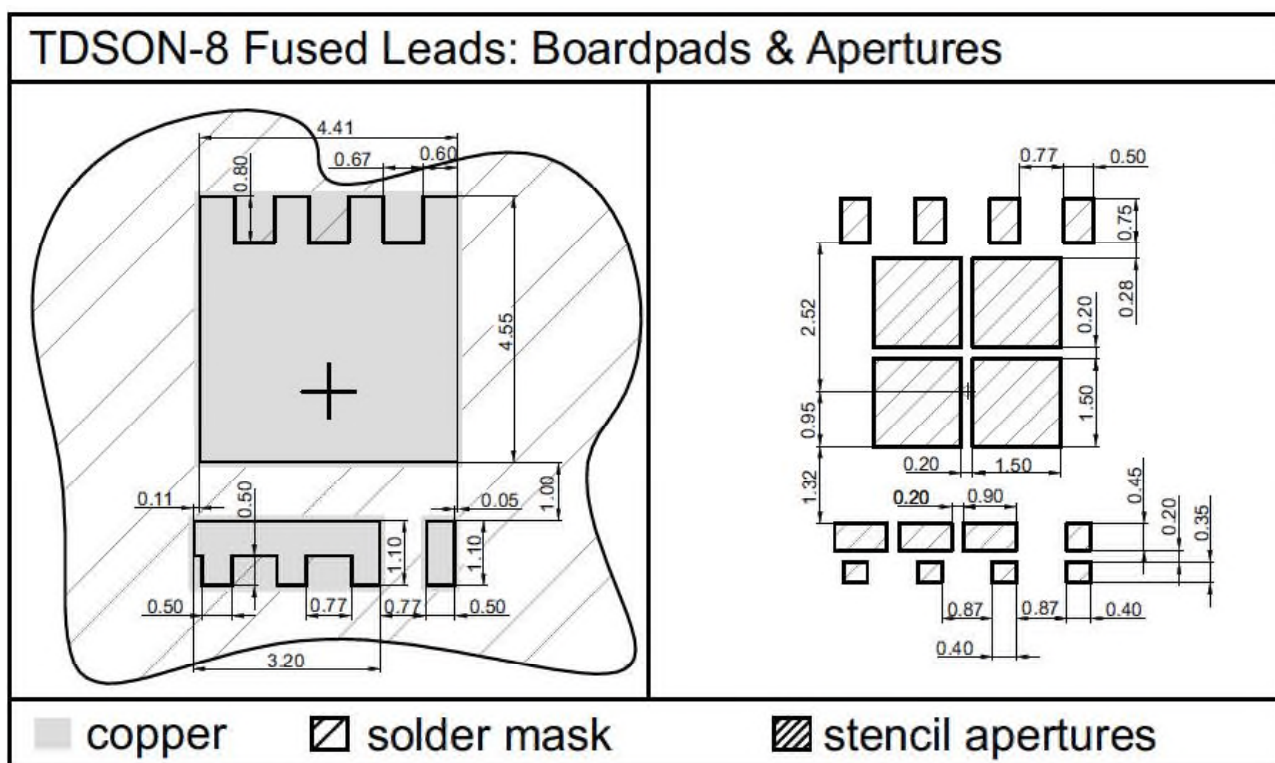


Figure 2 Outline PG-TDSON-8, dimensions in mm

Revision History

BSC014N06NS

Revision 2024-06-11, Rev. 2.6

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.3	2014-10-16	Rev.2.3
2.4	2020-02-28	Update current rating
2.5	2022-08-09	Update outline drawing and footnotes
2.6	2024-06-11	Upgrade Operating and storage temperature max to 175°C. Update drawings in section 5 Package Outlines. Production validation added on page1. Updated foot notes.

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