



THE DATASHEET OF
AP7341-18FS4-7



Description

The AP7341 is a low dropout regulator with high output voltage accuracy, low $R_{DS(ON)}$, high PSRR, low output noise and low quiescent current. This regulator is based on a CMOS process.

The AP7341 consists of a voltage reference, error amplifier, current limit circuit and an enable input to turn it on and off. With the integrated resistor network fixed output voltage versions can be delivered.

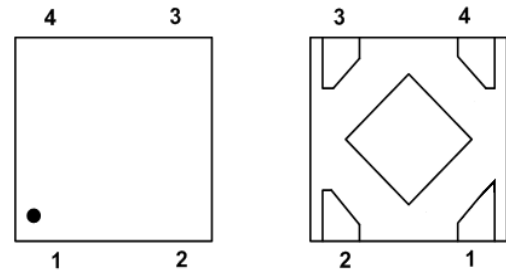
With its low power consumption and line and load transient response, the AP7341 is well suited for low power handheld communication equipment. The AP7341 is packaged in an X2-DFN1010-4 package and allows for smallest footprint and dense PCB layout.

Features

- Low V_{IN} and Wide V_{IN} Range: 1.7V to 5.25V
- Guarantee Output Current: 300mA
- V_{OUT} Accuracy $\pm 1\%$
- Ripple Rejection 75dB at 1kHz
- Low Output Noise, 60 μ Vrms from 10Hz to 100kHz
- Quiescent Current as Low as 35 μ A
- V_{OUT} Fixed 1.1V to 3.3V
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**

Notes: 1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
2. See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Pin Assignments



Top View X2-DFN1010-4 Bottom View

PIN1 – V_{OUT} , PIN2 – GND, PIN3 – EN, PIN4 – V_{IN}

Applications

- Smart Phone/Pad
- RF Supply
- Cameras
- Portable Video
- Portable Media Player
- Wireless Adapter
- Wireless Communication

Typical Applications Circuit

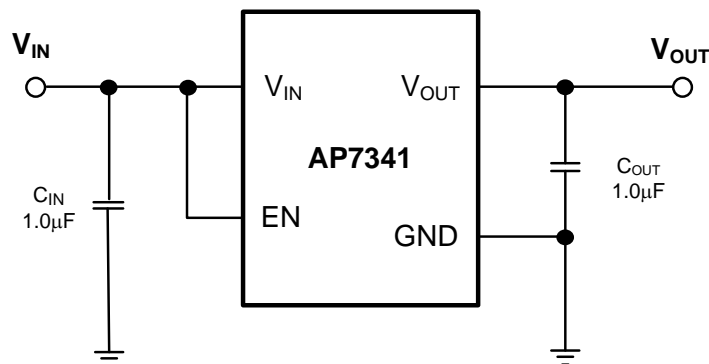
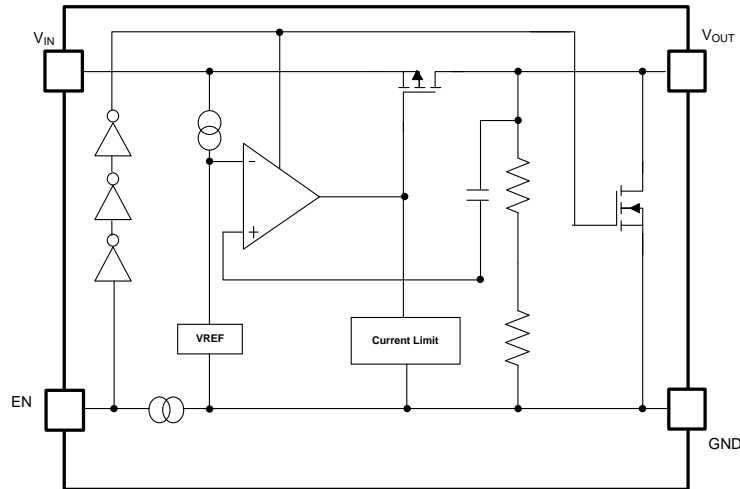


Figure 1 Typical Application Circuit

Functional Block Diagram



Pin Descriptions

Pin Number	Pin Name	Function
1	V _{OUT}	Power Output Pin
2	GND	Ground
3	EN	Enable Pin This pin should be driven either high or low and must not be floating. Driving this pin high enables the regulator, while pulling it low puts the regulator into shutdown mode
4	V _{IN}	Power Input Pin
—	Thermal Pad	In PCB layout, prefer to use large copper area to cover this pad for better thermal dissipation, then connect this area to GND or leave it open. However, do not use it as GND electrode function alone

Absolute Maximum Ratings (Note 4) (@T_A = +25°C, unless otherwise specified.)

Symbol	Parameter	Ratings	Unit
V _{IN}	Input Voltage	6.0	V
V _{CE}	Input Voltage EN	6.0	V
V _{OUT}	Output Voltage	-0.3 to V _{IN} + 0.3	V
I _{OUT}	Output Current	400	mA
P _D	Power Dissipation	400	mW
T _A	Operating Ambient Temperature	-40 to +85	°C
T _{STG}	Storage Temperature	-55 to +125	°C

Note: 4. a). Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
b). Ratings apply to ambient temperature at +25°C. The JEDEC High-K board design used to derive this data was a 2in. x 2in. multilayer board with 1oz internal power and ground planes and 2oz copper traces on the top and bottom of the board.

Recommended Operating Conditions (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

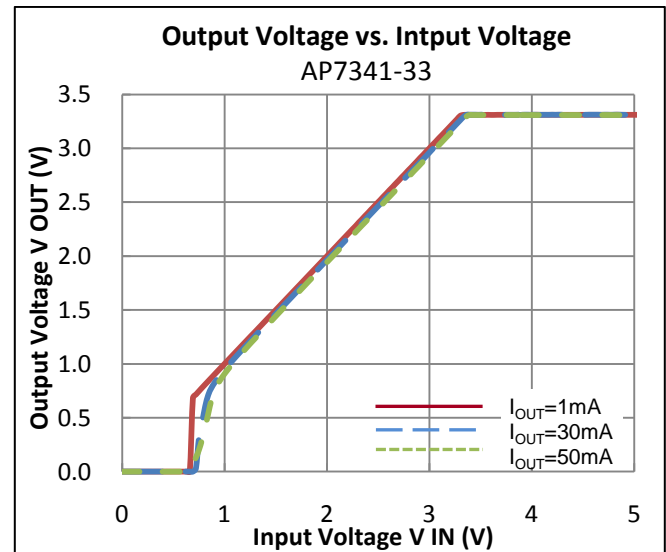
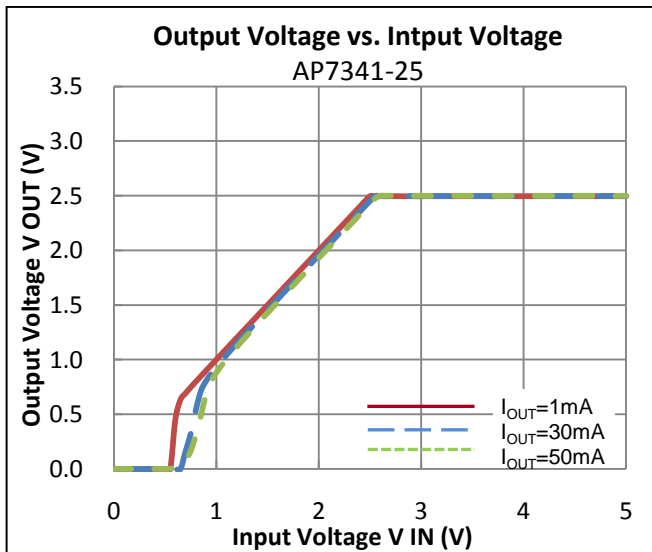
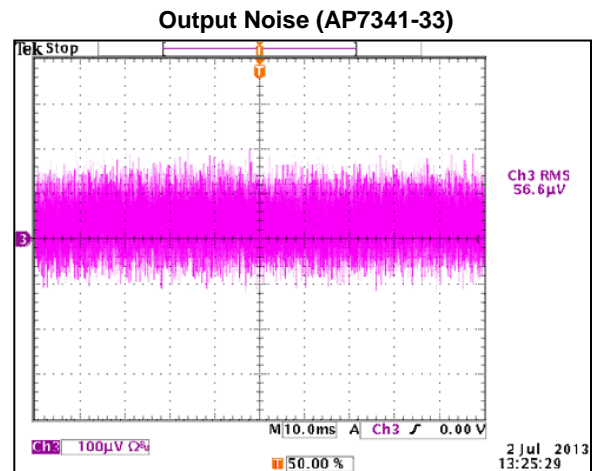
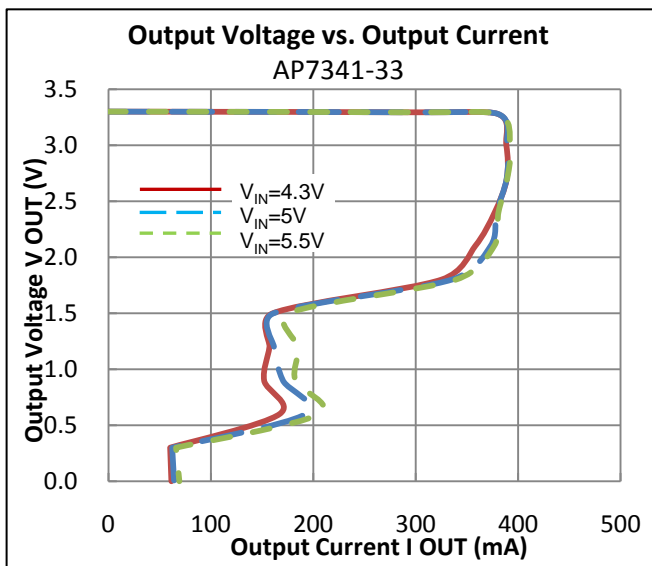
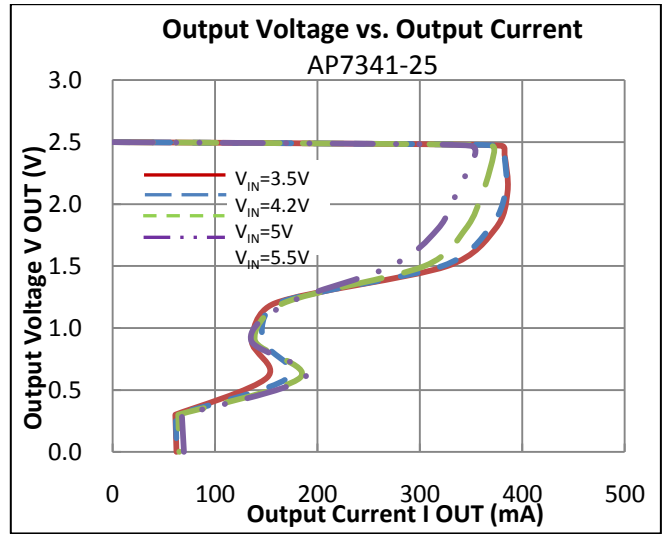
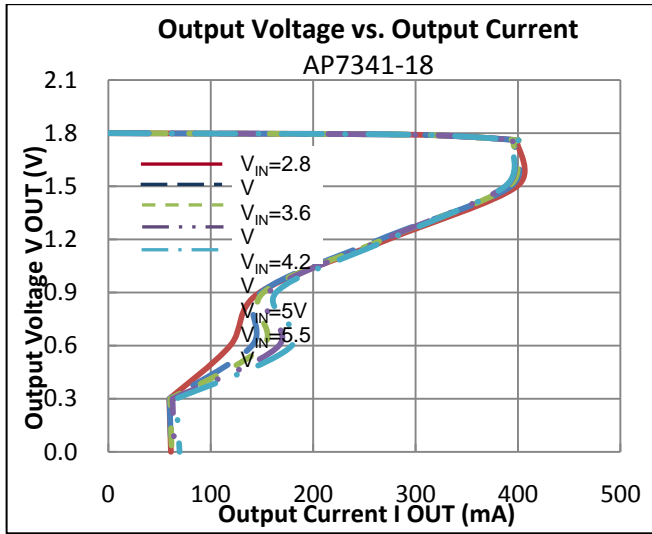
Symbol	Parameter	Min	Max	Unit
V_{IN}	Input Voltage	1.7	5.25	V
I_{OUT}	Output Current	0	300	mA
T_A	Operating Ambient Temperature	-40	+85	$^\circ\text{C}$

Electrical Characteristics (@ $T_A = +25^\circ\text{C}$, $V_{IN} = V_{EN} = V_{OUT} + 1.0\text{V}$, $C_{IN} = C_{OUT} = 1.0\mu\text{F}$, $I_{OUT} = 1.0\text{mA}$, unless otherwise specified.)

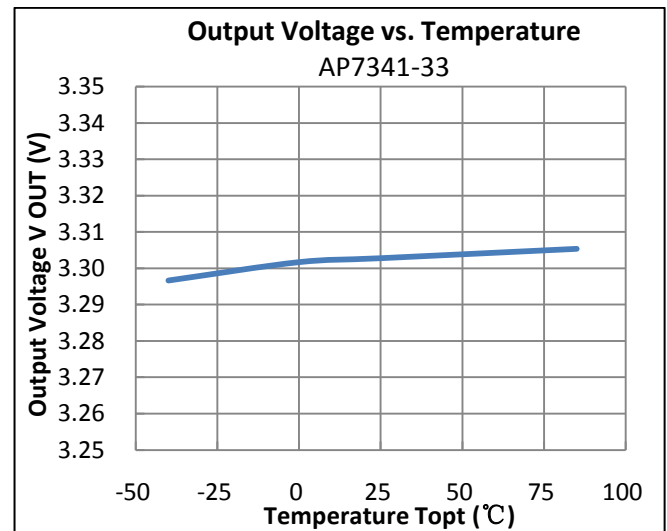
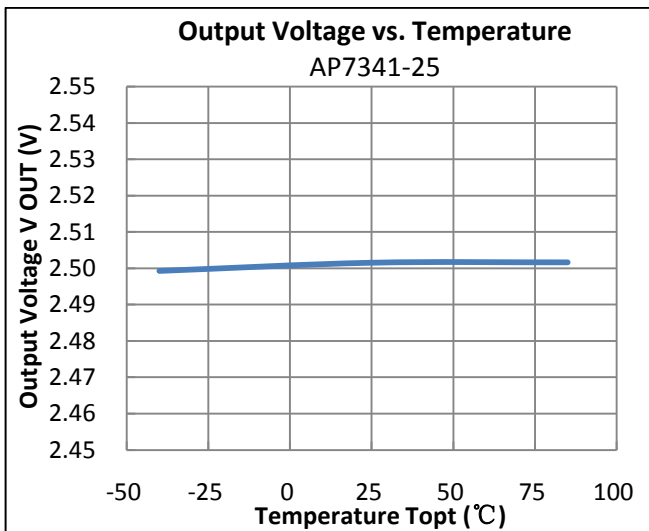
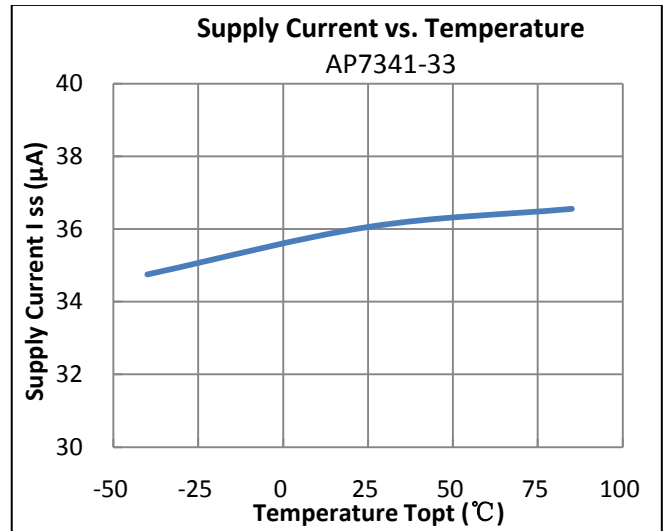
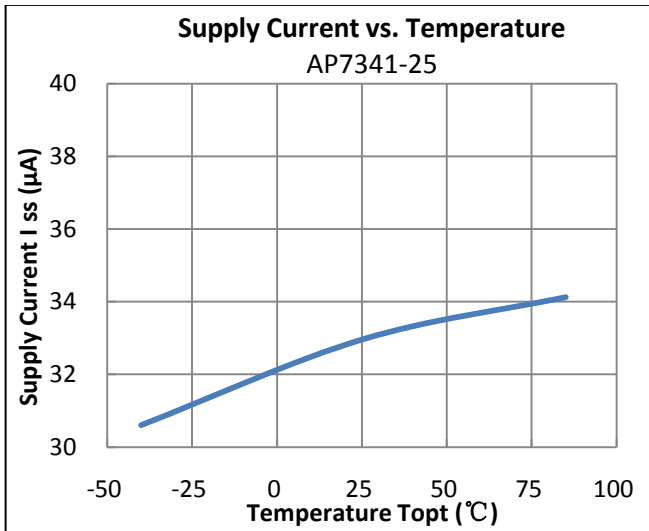
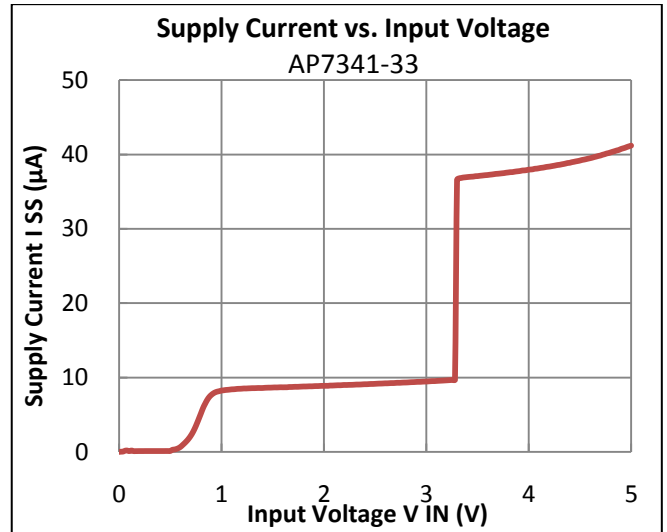
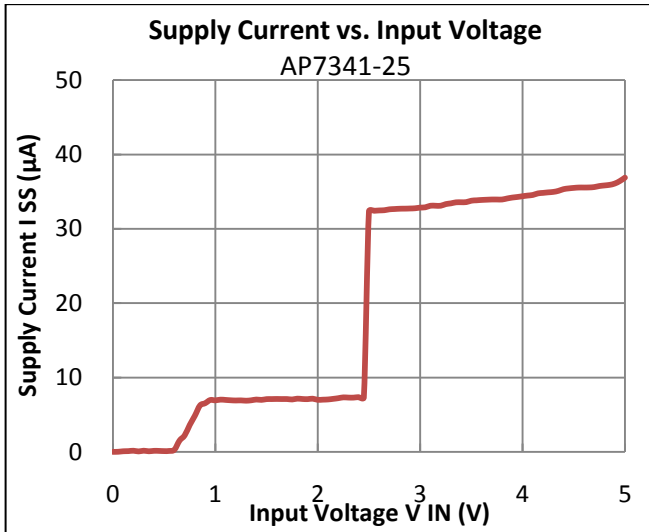
Parameter	Conditions	Min	Typ	Max	Unit	
Input Voltage	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	1.7	—	5.25	V	
Output Voltage Accuracy (Note 11)	$V_{IN} = V_{OUT-Nom} + 1.0\text{V}$ to 5.25V , $I_{OUT} = 1\text{mA}$ to 300mA	$T_A = +25^\circ\text{C}$	-1	—	1	%
		$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	-1.5	—	+1.5	
Line Regulation ($dV_{OUT}/dV_{IN}/V_{OUT}$)	$V_{IN} = (V_{OUT-Nom} + 1.0\text{V})$ to 5.25V , $I_{OUT} = 1.0\text{mA}$	—	0.02	0.1	%/V	
Load Regulation (dV_{OUT}/V_{OUT})	$V_{IN} = V_{OUT-Nom} + 1.0\text{V}$, $I_{OUT} = 1\text{mA}$ to 300mA	—	15	30	mV	
Quiescent Current (Note 6)	$I_{OUT} = 0\text{mA}$	—	35	50	μA	
$I_{STANDBY}$	$V_{EN} = 0\text{V}$ (Disabled)	—	0.01	1.0	μA	
Output Current	—	300	—	—	mA	
Fold-back Short Current (Note 7)	V_{OUT} Short to Ground	—	55	—	mA	
PSRR (Note 8)	$V_{IN} = [V_{OUT} + 1\text{V}] \text{VDC} + 0.2\text{Vp-pAC}$, $V_{OUT} \geq 1.8\text{V}$, $I_{OUT} = 30\text{mA}$	—	75	—	dB	
Output Noise Voltage (Notes 8 & 9)	$BW = 10\text{Hz}$ to 100kHz , $I_{OUT} = 30\text{mA}$	—	60	—	μVrms	
Dropout Voltage (Note 5)	$I_{OUT} = 150\text{mA}$	$1.1\text{V} \leq V_{OUT} < 1.5\text{V}$	—	0.50	0.62	V
		$1.5\text{V} \leq V_{OUT} < 1.7\text{V}$	—	0.38	0.47	
		$1.7\text{V} \leq V_{OUT} < 2.0\text{V}$	—	0.34	0.42	
		$2.0\text{V} \leq V_{OUT} < 2.5\text{V}$	—	0.28	0.36	
		$2.5\text{V} \leq V_{OUT} < 2.8\text{V}$	—	0.22	0.30	
		$2.8\text{V} \leq V_{OUT} \leq 3.3\text{V}$	—	0.21	0.27	
	$I_{OUT} = 300\text{mA}$	$V_{OUT} = 1.8\text{V}$	—	0.50	0.65	
		$V_{OUT} = 2.5\text{V}$	—	0.37	0.48	
	$V_{OUT} = 3.3\text{V}$	—	0.30	0.40		
Output Voltage Temperature Coefficient	$I_{OUT} = 30\text{mA}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	—	± 30	—	ppm/ $^\circ\text{C}$	
EN Input Low Voltage	—	0	—	0.5	V	
EN Input High Voltage	—	1.3	—	5.25	V	
EN Input Leakage	$V_{EN} = 0$, $V_{IN} = 5.0\text{V}$ or $V_{EN} = 5.0\text{V}$, $V_{IN} = 0\text{V}$	-1.0	—	+1.0	μA	
On Resistance of N-Channel for Auto-Discharge (Note 10)	$V_{IN} = 4.0\text{V}$, $V_{EN} = 0\text{V}$ (Disabled)	—	30	—	Ω	

- Notes:
5. Dropout voltage is the voltage difference between the input and the output at which the output voltage drops 2% below its nominal value.
 6. Quiescent current is defined here is the difference in current between the input and the output.
 7. Short circuit current is measured with V_{OUT} pulled to GND.
 8. This specification is guaranteed by design.
 9. To make sure lowest environment noise minimizes the influence on noise measurement.
 10. AP7341 has 2 options for output, built-in discharge and non-discharge.
 11. Potential multiple grades based on following output voltage accuracy.

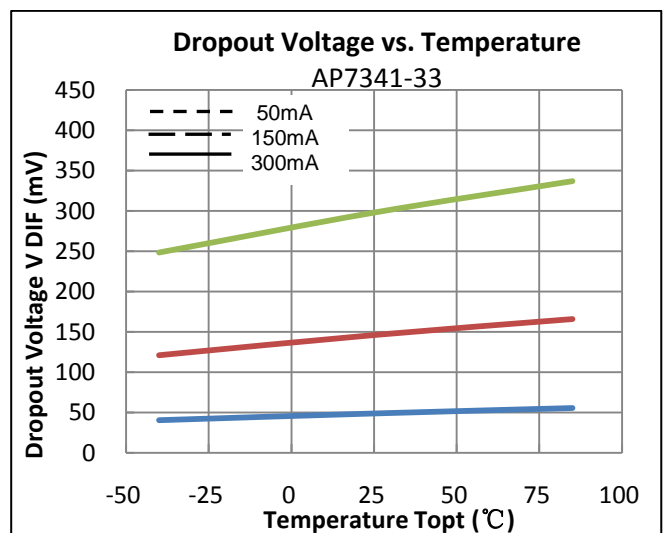
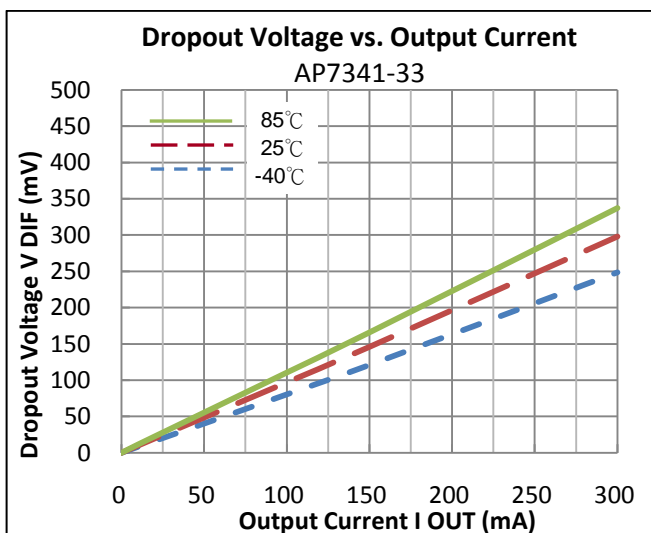
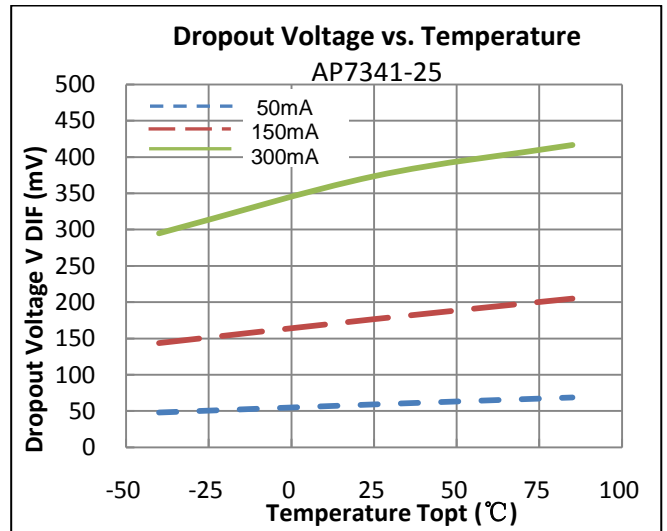
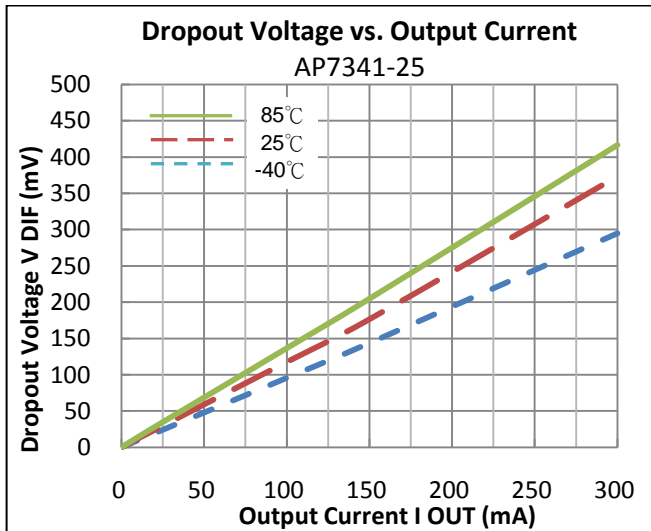
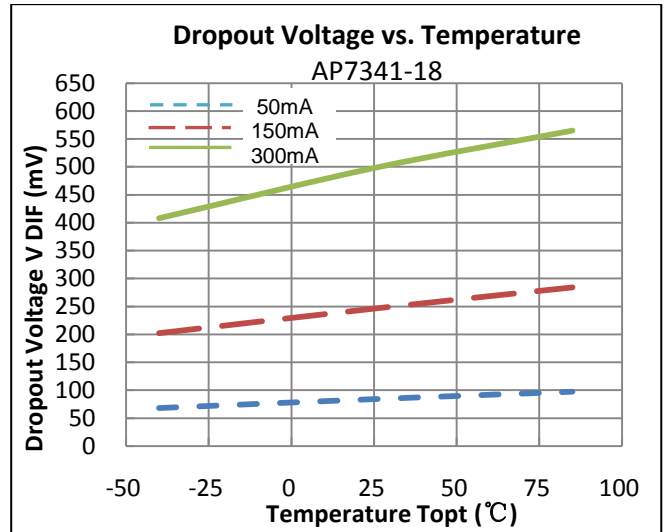
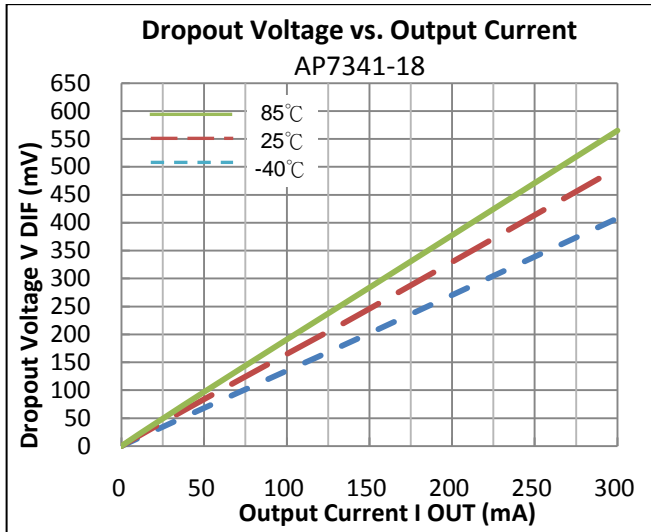
Typical Characteristics



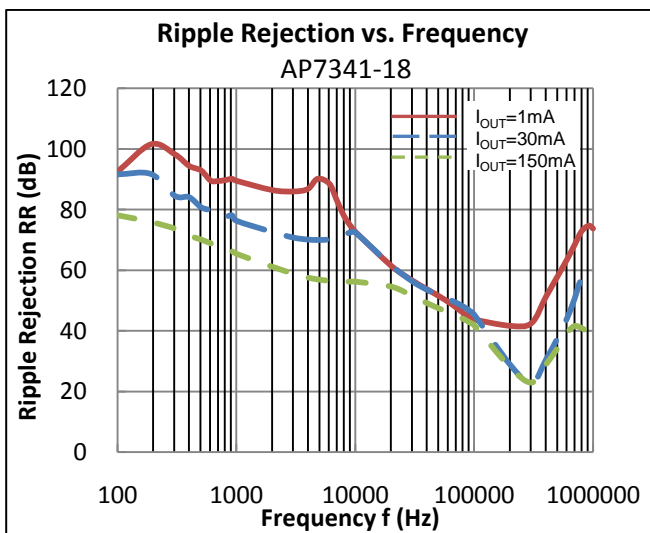
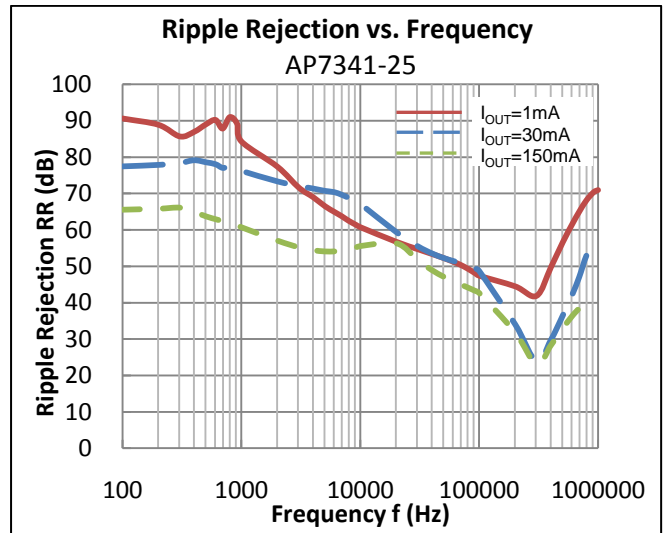
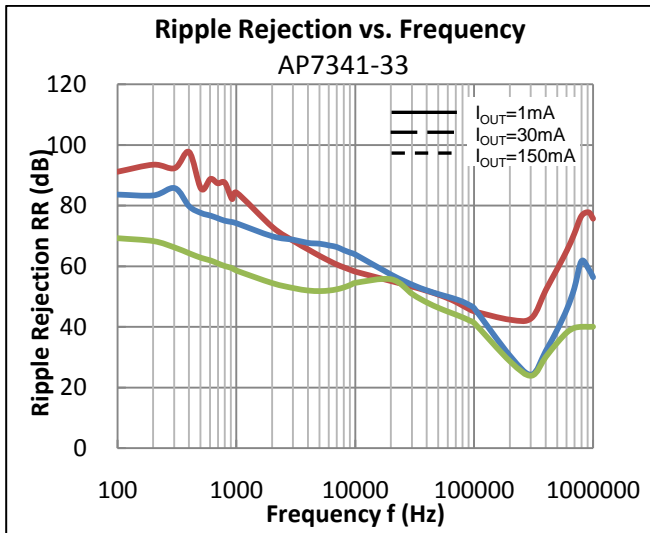
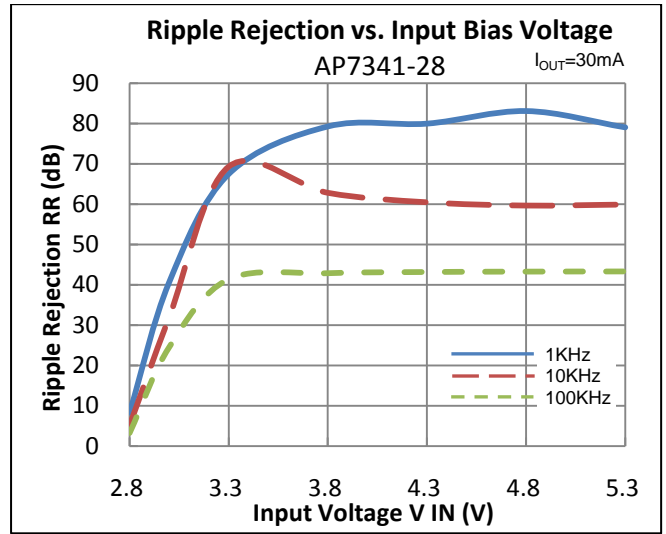
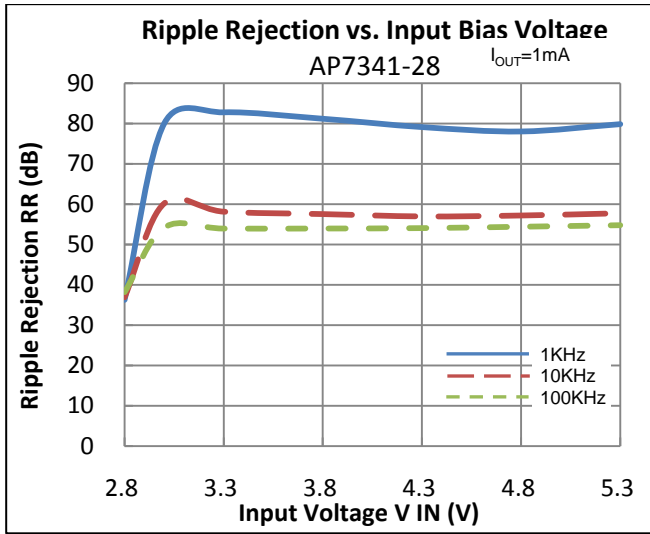
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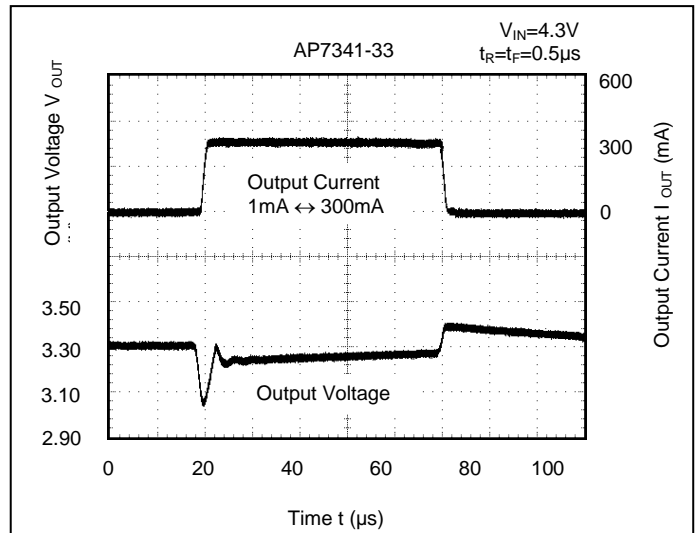
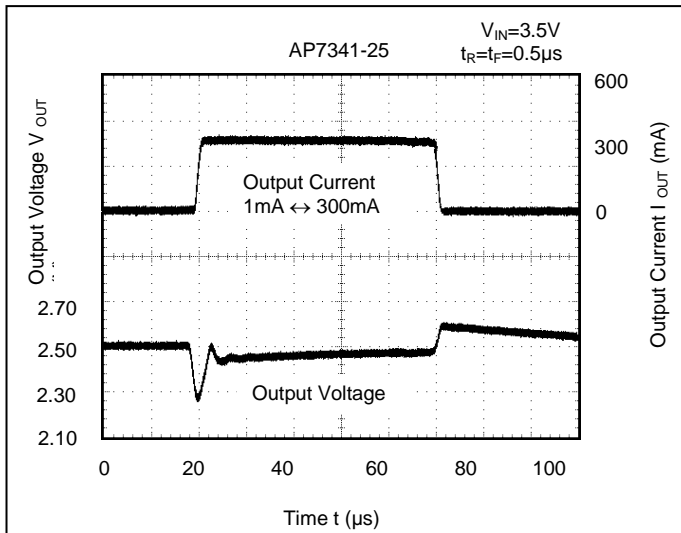
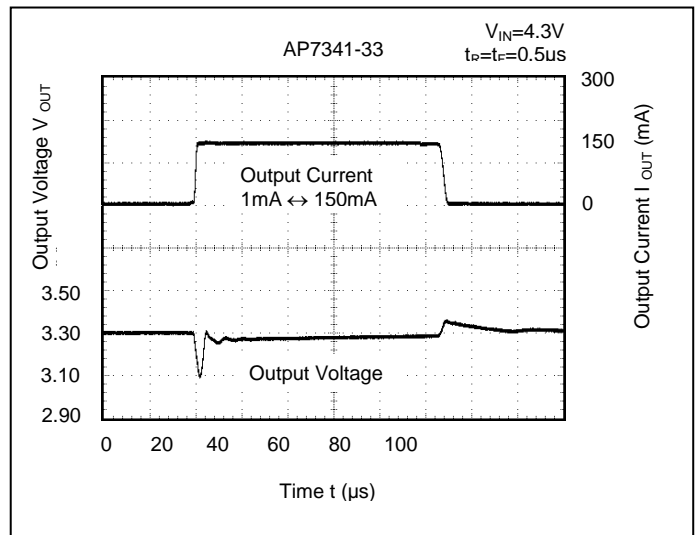
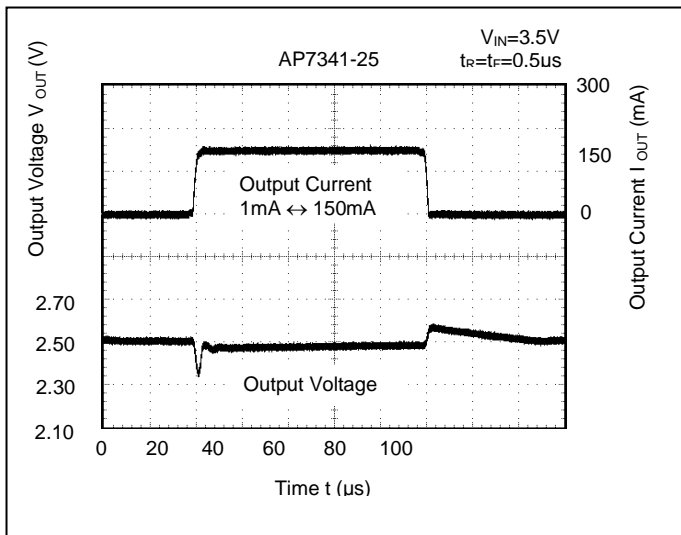
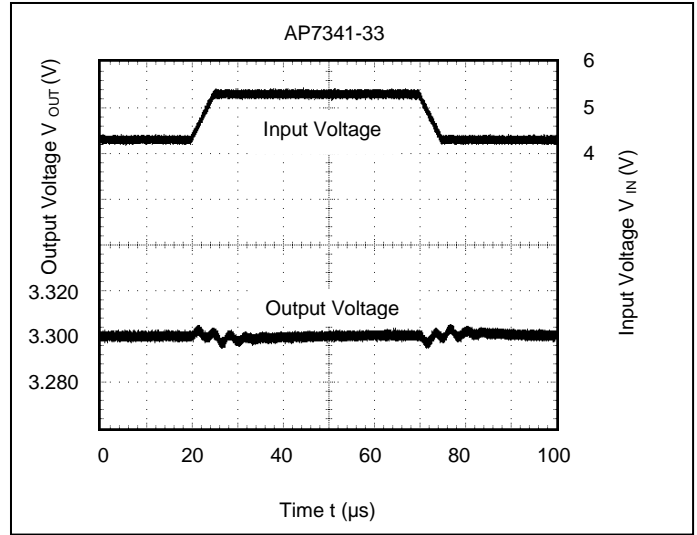
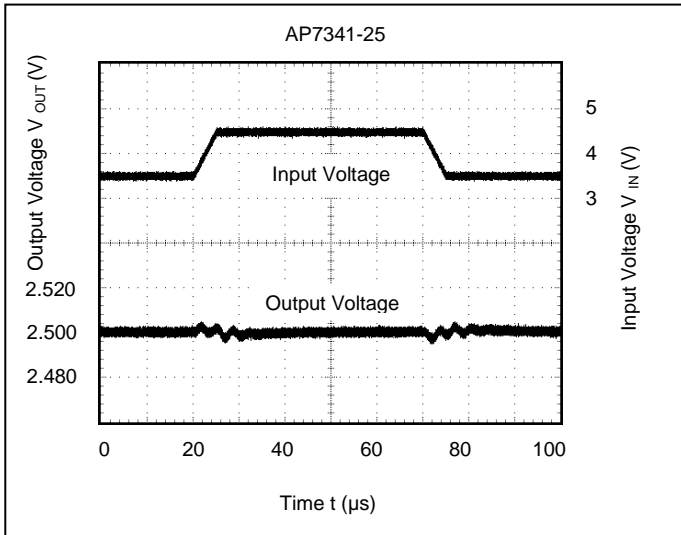
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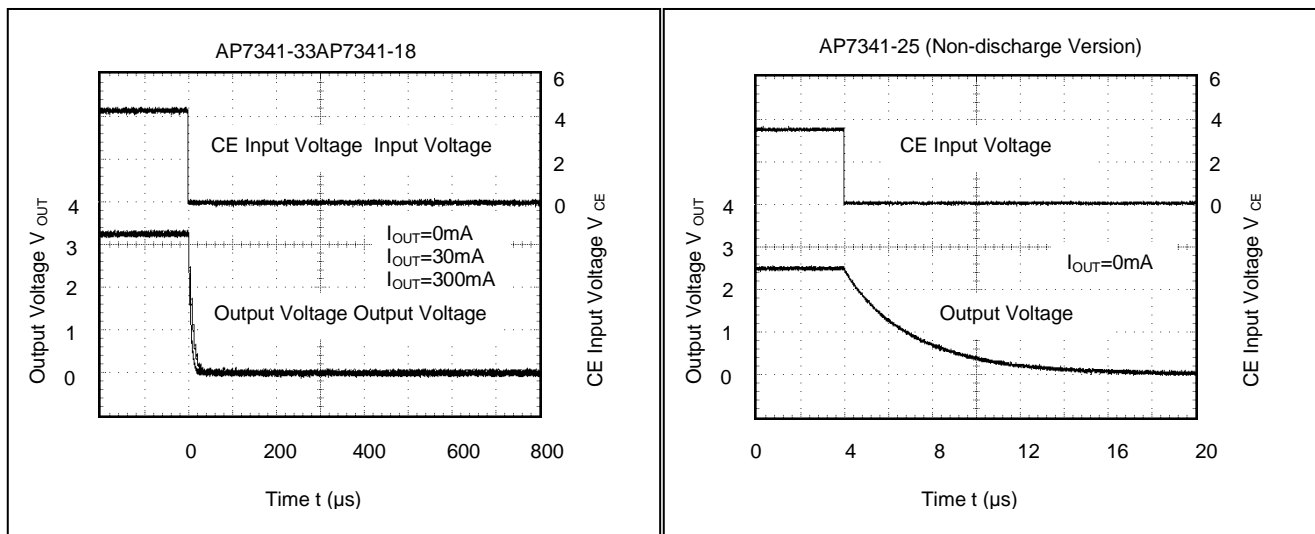
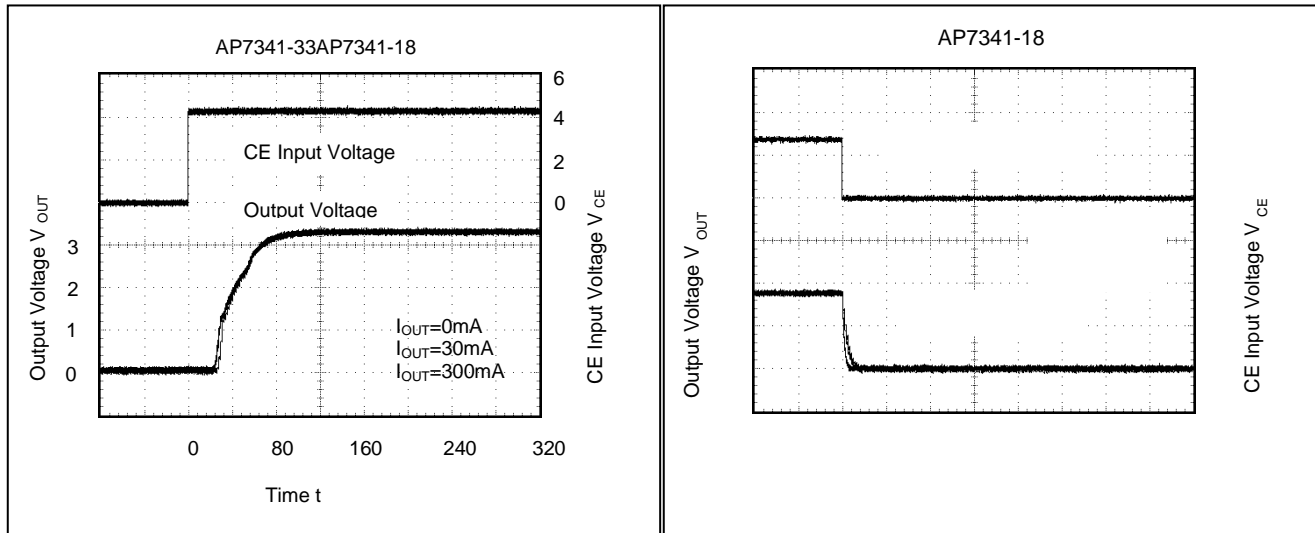
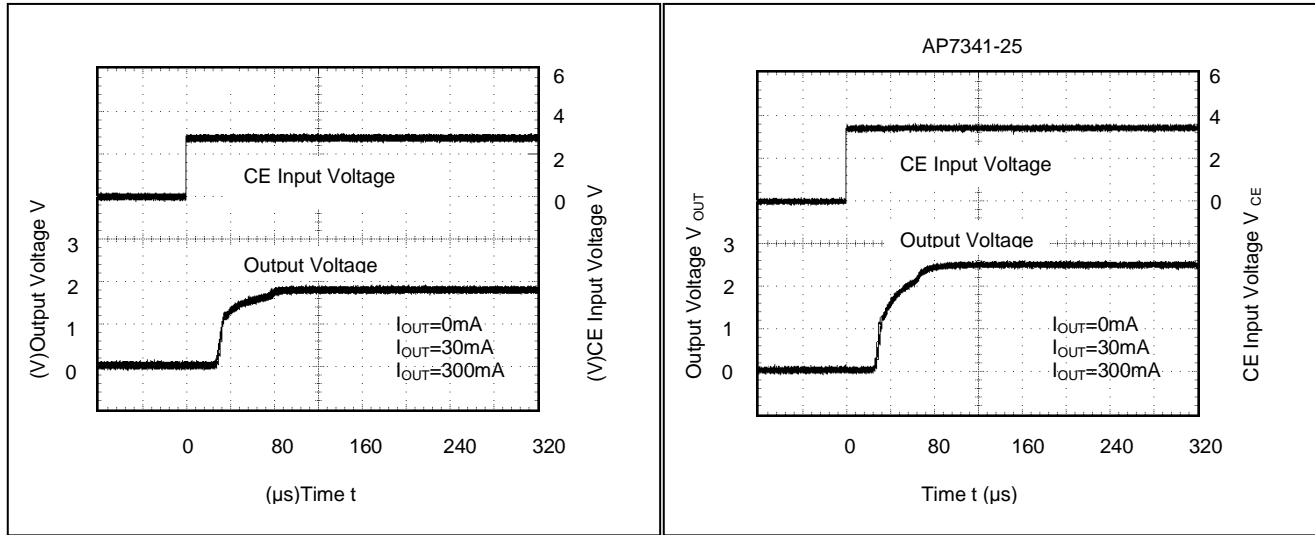
Typical Characteristics (Cont.)



Typical Characteristics (Cont.)



Typical Characteristics (Cont.)



Application Information

Output Capacitor

An output capacitor (C_{OUT}) is needed to improve transient response and maintain stability. The AP7341 is stable with very small ceramic output capacitors. The ESR (equivalent series resistance) and capacitance drives the selection. If the application has large load variations, it is recommended to utilize low-ESR bulk capacitors. It is recommended to place ceramic capacitors as close as possible to the load and the ground pin and care should be taken to reduce the impedance in the layout.

Input Capacitor

To prevent the input voltage from dropping during load steps it is recommended to utilize an input capacitor (C_{IN}). A minimum $0.47\mu\text{F}$ ceramic capacitor is recommended between V_{IN} and GND pins to decouple input power supply glitch. This input capacitor must be located as close as possible to the device to assure input stability and reduce noise. For PCB layout, a wide copper trace is required for both V_{IN} and GND pins.

Enable Control

The AP7341 is turned on by setting the EN pin high, and is turned off by pulling it low. If this feature is not used, the EN pin should be tied to V_{IN} pin to keep the regulator output on at all time. To ensure proper operation, the signal source used to drive the EN pin must be able to swing above and below the specified turn-on/off voltage thresholds listed in the Electrical Characteristics section.

Short Circuit Protection

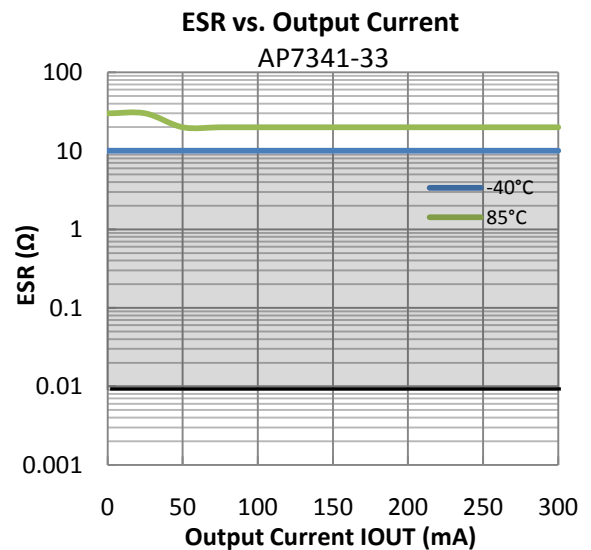
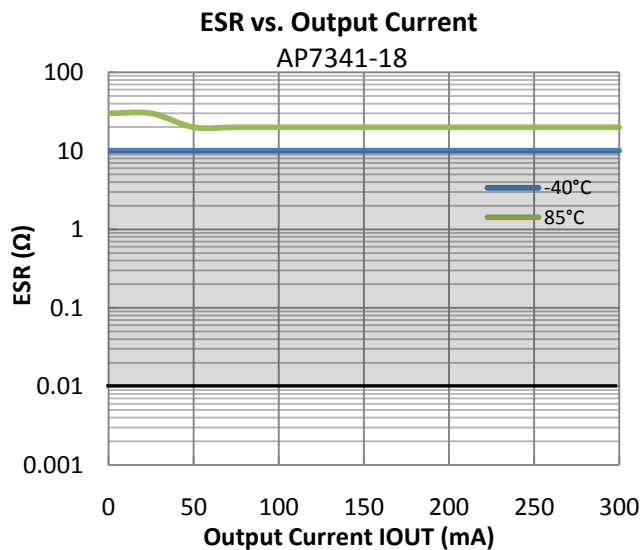
When V_{OUT} pin is short-circuit to GND, short circuit protection will be triggered and clamp the output current to approximately 60mA. This feature protects the regulator from overcurrent and damage due to overheating.

Layout Considerations

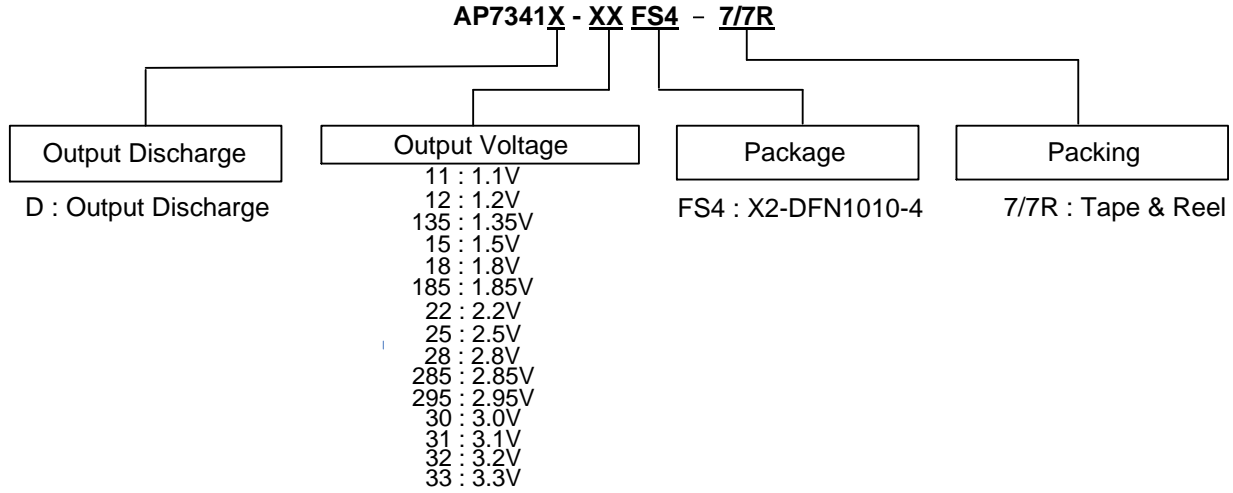
For good ground loop and stability, the input and output capacitors should be located close to the input, output, and ground pins of the device. The regulator ground pin should be connected to the external circuit ground to reduce voltage drop caused by trace impedance. Ground plane is generally used to reduce trace impedance. Wide trace should be used for large current paths from V_{IN} to V_{OUT} , and load circuit.

ESR vs. Output Current

Ceramic type output capacitor is recommended for this series; however, the other output capacitors with low ESR also can be used. The relations between I_{OUT} (Output Current) and ESR of an output capacitor are shown below. The stable region is marked as the hatched area in the graph. Measurement conditions: Frequency Band: 10Hz to 2MHz, Temperature: -40°C to $+85^{\circ}\text{C}$



Ordering Information (Note 12)



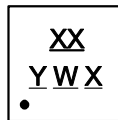
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			Quantity	Part Number Suffix
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AP7341D-XXFS4-7/7R	FS4	X2-DFN1010-4	5,000/Tape & Reel	-7/7R

Note: 12. For packaging details, go to our website at <http://www.diodes.com/products/packages.html>.

Marking Information

(1) X2-DFN1010-4

(Top View)



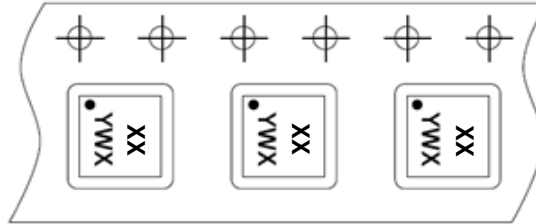
- XX : Identification Code
- Y : Year : 0~9
- W : Week : A~Z : 1~26 week;
a~z : 27~52 week; z represents 52 and 53 week
- X : A~Z : Internal code

Marking Information (Cont.)

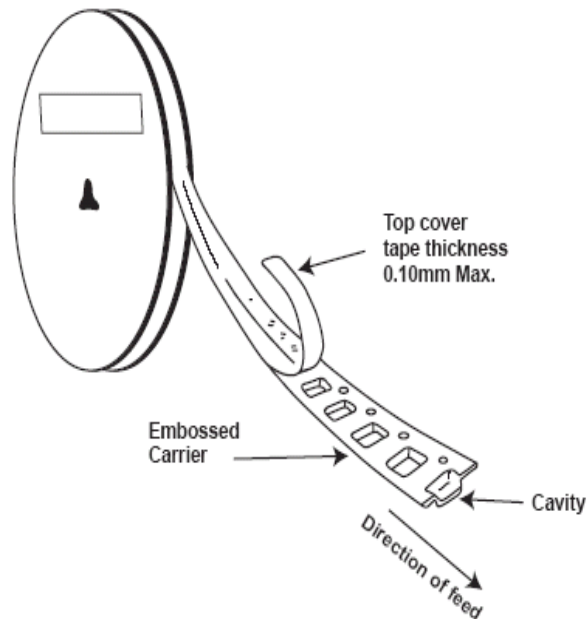
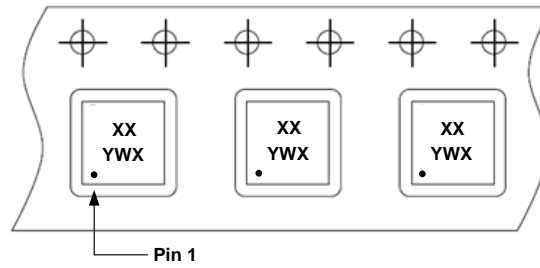
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AP7341-135FS4-7	X2-DFN1010-4	XF
AP7341-15FS4-7	X2-DFN1010-4	T3
AP7341-18FS4-7	X2-DFN1010-4	T4
AP7341-185FS4-7	X2-DFN1010-4	T5
AP7341-22FS4-7	X2-DFN1010-4	TH
AP7341-25FS4-7	X2-DFN1010-4	T6
AP7341-28FS4-7	X2-DFN1010-4	T7
AP7341-285FS4-7	X2-DFN1010-4	T8
AP7341-295FS4-7	X2-DFN1010-4	8A
AP7341-30FS4-7	X2-DFN1010-4	T9
AP7341-31FS4-7	X2-DFN1010-4	TC
AP7341-32FS4-7	X2-DFN1010-4	TD
AP7341-33FS4-7	X2-DFN1010-4	TE
AP7341D-11FS4-7	X2-DFN1010-4	UF
AP7341D-12FS4-7	X2-DFN1010-4	U2
AP7341D-135FS4-7	X2-DFN1010-4	XG
AP7341D-15FS4-7	X2-DFN1010-4	U3
AP7341D-18FS4-7	X2-DFN1010-4	U4
AP7341D-185FS4-7	X2-DFN1010-4	U5
AP7341D-22FS4-7	X2-DFN1010-4	UH
AP7341D-25FS4-7	X2-DFN1010-4	U6
AP7341D-28FS4-7	X2-DFN1010-4	U7
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AP7341D-31FS4-7	X2-DFN1010-4	UC
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AP7341-135FS4-7R	X2-DFN1010-4	4R
AP7341-15FS4-7R	X2-DFN1010-4	4C
AP7341-18FS4-7R	X2-DFN1010-4	4D
AP7341-185FS4-7R	X2-DFN1010-4	4E
AP7341-22FS4-7R	X2-DFN1010-4	4F
AP7341-25FS4-7R	X2-DFN1010-4	4G
AP7341-28FS4-7R	X2-DFN1010-4	4H
AP7341-285FS4-7R	X2-DFN1010-4	4J
AP7341-295FS4-7R	X2-DFN1010-4	4S
AP7341-30FS4-7R	X2-DFN1010-4	4K
AP7341-31FS4-7R	X2-DFN1010-4	4M
AP7341-32FS4-7R	X2-DFN1010-4	4N
AP7341-33FS4-7R	X2-DFN1010-4	4P
AP7341D-11FS4-7R	X2-DFN1010-4	5A
AP7341D-12FS4-7R	X2-DFN1010-4	5B
AP7341D-135FS4-7R	X2-DFN1010-4	5R
AP7341D-15FS4-7R	X2-DFN1010-4	5C
AP7341D-18FS4-7R	X2-DFN1010-4	5E
AP7341D-185FS4-7R	X2-DFN1010-4	5D
AP7341D-22FS4-7R	X2-DFN1010-4	5F
AP7341D-25FS4-7R	X2-DFN1010-4	5G
AP7341D-28FS4-7R	X2-DFN1010-4	5J
AP7341D-285FS4-7R	X2-DFN1010-4	5H
AP7341D-295FS4-7R	X2-DFN1010-4	5S
AP7341D-30FS4-7R	X2-DFN1010-4	5K
AP7341D-31FS4-7R	X2-DFN1010-4	5M
AP7341D-32FS4-7R	X2-DFN1010-4	5N
AP7341D-33FS4-7R	X2-DFN1010-4	5P

Tape Orientation

For AP7341-XXFS4-7 & AP7341D-XXFS4-7



For AP7341-XXFS4-7R & AP7341D-XXFS4-7R



Note: 13. The taping orientation of the other package type can be found on our website at <http://www.diodes.com/datasheets/ap02007.pdf>.

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