



## General Description

The [MxL7704](#) is a five output Universal PMIC optimized for powering low power FPGAs, DSPs, and microprocessors from 5V inputs. Four synchronous step down buck regulators range from 1.5A system power to 4A core power. A 100mA LDO provides a clean 1.5V to 3.6V power for auxiliary devices. All outputs support  $\pm 10\%$  margining and the two highest power outputs support dynamic voltage control to support processors that can utilize this function to save power. Through a 400kHz I<sup>2</sup>C interface, the customer can monitor an input voltage flag and PGOOD flags for each output. The I<sup>2</sup>C port can also be used to modify power up and down sequencing options, assign PGOOD outputs to the PGOOD pins, enable outputs and select switching frequency.

High switching frequency and a current mode architecture with internal compensation enable a very fast transient response to line and load changes without sacrificing stability and keeping board space to a minimum.

Fault protection features include input undervoltage lockout, overcurrent protection, and thermal protection. The MxL7704 is offered in a 5mm x 5mm QFN package.

Two pre-programmed standard products are available. The MxL7704-X has been optimized for powering the Xilinx® Zynq® Ultrascale+™ ZU2 and ZU3 MPSoCs. The bucks are pre-programmed to provide the core rail (0.85V up to 4A), DDR3L memory power (1.35V), I/O and system power (1.8V and 3.3V). Sequencing is tailored to the unique needs of the ZU2 and ZU3 MPSoCs, offering accelerated time to market with Xilinx® Zynq® Ultrascale+™ ZU2 and ZU3 devices. The MxL7704-A is designed to power a wide range of ARM® Cortex®-based processors (A7, A9, and A53) which use a more conventional sequencing scheme where the I/O rails power up first and core is last. The bucks provide the 1.2V core rail, 1.35V DDR3L power, 1.8V and 3.3V rails for I/O and system power. VTT is supported by the addition of the XRP2997 DDR Bus Termination Regulator.

## Features

- Input voltage range: 4.0V to 5.5V
- 4 Synchronous Buck Regulators
  - Internally compensated current mode
  - 1MHz to 2.1MHz switching frequency
  - Buck 1: 3.0V to 3.6V, 20mV step, 1.5A
  - Buck 2: 1.3V to 1.92V, 20mV step, 1.5A
  - Buck 3: 0.8V to 1.6V, 6.25mV step, 2.5A
  - Buck 4: 0.6V to 1.4V, 6.25mV step, 4A
- 100mA LDO 1.5V to 3.6V, 20mV step
- $\pm 2\%$  maximum total dc output error over line, load and temperature
- 3.3V/5V 400kHz I<sup>2</sup>C interface
  - Dynamic voltage scaling
  - Status monitoring by channel
  - Sequencing control
  - Input voltage status register
- Highly flexible conditional sequencing engine with external input
- 2 configurable PGOOD outputs
- Adjustable switching frequency
- 5mm x 5mm 32-pin QFN package
- Two standard factory programmed devices
  - MxL7704-A: IO rails up first, core last (1.2V)
  - MxL7704-X for Xilinx® ZU2 and ZU3 MPSoCs

## Applications

- Low power processor, ASIC and FPGA power
- Industrial control
- Test equipment
- POS terminals

Ordering Information - [Back Page](#)

## Revision History

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| Revision | Release Date | Change Description  |
|----------|--------------|---|
| 1A       | 2/28/18      | Initial Release   |
| 1B       | 7/3/18       | Added inductor value calculation to Minimum Effective $C_{OUT}$ section. Updated Output Voltage Scaling and I <sup>2</sup> C Operation sections and Register Descriptions 0x10 - 0x14. Updated ESD table. Added open drain to PG pin descriptions. Added sentence to PGOOD section and deleted sentence from Operations section about unassigned PG pin. Updated General Description and Features with -A and -X information. |

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# MxL7704 Specifications

## Absolute Maximum Ratings

**Important!** The stresses above what is listed under Table 1 may cause permanent damage to the device. This is a stress rating only—functional operation of the device above what is listed under Table 1 or any other conditions beyond what MaxLinear recommends is not implied. Exposure to conditions above what is listed under Table 3 for extended periods of time may affect device reliability. Solder reflow profile is specified in the IPC/JEDEC J-STD-020C standard.

**Table 1: Absolute Maximum Ratings**

| Parameter   | Minimum | Maximum                | Units |
|---|---------|------------------------|-------|
| $V_{IN}$ , $V_{IN1}$ , $V_{IN2}$ , $V_{IN3}$ , $V_{IN4}$ , 5V <sub>SY</sub> | -0.3    | 6                      | V     |
| SDA, SCL, VDDIO   | -0.3    | 6                      | V     |
| AN0, AN1  | -0.3    | 6                      | V     |
| PG1, PG2, GLOBAL EN, SEQ EN   | -0.3    | 6                      | V     |
| LDO   | -0.3    | 6                      | V     |
| $V_{OUT1}$ , $V_{OUT2}$ , $V_{OUT3}$ , $V_{OUT4}$                           | -0.3    | $V_{INx} - 0.3V^{(1)}$ | V     |
| Storage Temperature Range   | -55     | 150                    | °C    |
| Peak Package Body Temperature   |         | 260                    | °C    |

NOTE:

1. x = Buck number

## ESD Rating

**Table 2: ESD Rating**

| Parameter                  | Minimum | Maximum | Units |
|----------------------------|---------|---------|-------|
| HBM (Human Body Model)     |         | 2.5     | kV    |
| CDM (Charged Device Model) |         | 750     | V     |

## Operating Conditions

**Table 3: Operating Conditions**

| Parameter   | Minimum | Maximum               | Units |
|---|---------|-----------------------|-------|
| $V_{IN}$ , $V_{IN1}$ , $V_{IN2}$ , $V_{IN3}$ , $V_{IN4}$ , 5V <sub>SY</sub> | 4.0     | 5.5                   | V     |
| SDA, SCL, VDDIO   | 3.3     | 5.5                   | V     |
| AN0, AN1  | 0       | 3                     | V     |
| PG1, PG2, GLOBAL EN, SEQ EN   | 0       | 5.5                   | V     |
| LDO   | 0       | $V_{IN} - 0.3V^{(1)}$ | V     |
| LX1, LX2, LX3, LX4  | -1      | 5.5 <sup>(2)</sup>    | V     |
| Switching Frequency   | 1000    | 2100                  | kHz   |
| Junction Temperature Range ( $T_J$ )  | -40     | 125                   | °C    |
| Package Power Dissipation Max at 25°C                                       |         | 3.65                  | W     |
| Package Thermal Resistance $\Theta_{JA}$                                    |         | 27                    | °C/W  |

NOTES:

1. LDO set to 3.3V.

2. LX pin's DC range is -1V for less than 50ns.

## Electrical Characteristics

Specifications are for Operating Junction Temperature of  $T_J = 25^\circ\text{C}$  only; limits applying over the full Operating Junction Temperature range are denoted by a “\*”. Typical values represent the most likely parametric norm at  $T_J = 25^\circ\text{C}$ , and are provided for reference purposes only. Unless otherwise indicated,  $V_{IN} = 5V_{SYS} = 5.0V$ .

**Table 4: Electrical Characteristics**

| Symbol                         | Parameter   | Conditions   | • | Min                  | Typ | Max     | Units            |
|--------------------------------|---|--|---|----------------------|-----|---------|------------------|
| DC Specifications              |   |  |   |                      |     |         |                  |
| $V_{IN}$                       | Input DC voltage  |  | • | 4.0                  | 5.0 | 5.5     | V                |
| UVLO                           | Under Voltage Lockout   | Rising   |   |                      |     | 3.9     | V                |
|                                | Under Voltage Lockout Hysteresis                                | Falling  |   |                      | 210 |         | mV               |
| $I_{Q\_SHUTDOWN}$              | Shutdown Quiescent Current                                      | GLOBAL EN = logic LOW, All outputs <20% of set point or initial power applied.       |   |                      | 10  |         | $\mu\text{A}$    |
| $I_{Q\_OPERATING\_5V_{SYS}}$   | 5V <sub>SYS</sub> Operating Quiescent Current                   | GLOBAL EN = logic HIGH, All outputs in regulation no load. $f_{OSC} = 1.5\text{MHz}$ |   |                      | 8   |         | mA               |
| $T_{SD}$                       | Thermal Shutdown Threshold                                      | Temperature rising   |   |                      | 145 |         | $^\circ\text{C}$ |
| $T_{SDH}$                      | Thermal Shutdown Hysteresis                                     | Temperature falling  |   |                      | 20  |         | $^\circ\text{C}$ |
| Buck Regulators 1 – 4          |   |  |   |                      |     |         |                  |
| $V_{IN}$                       | Operational Voltage Range                                       |  | • | 4.0                  |     | 5.5     | V                |
| $V_{OUT}$ Accuracy             | Output Voltage Accuracy at Factory Programmed Initial Set Point | Load current = 10mA to full load<br>$V_{IN} = 5V_{SYS}$<br>= 4.0V to 5.5V            | • | -2                   |     | +2      | %                |
| $V_{OUT}$ Initial Accuracy     | Output Voltage Accuracy at Factory Programmed Initial Set Point | Load current = 10mA<br>$V_{IN} = 5V_{SYS}$<br>= 4.5V to 5.5V                         |   | -0.5                 |     | +0.5    | %                |
| Buck 1 $V_{OUT}$ Range         | Output Voltage Set Point Range                                  | 20mV resolution, 8 bit   |   | 3.0                  |     | 3.6     | V                |
| Buck 2 $V_{OUT}$ Range         | Output Voltage Set Point Range                                  | 20mV resolution, 8 bit   |   | 1.30                 |     | 1.92    | V                |
| Buck 3 $V_{OUT}$ Range         | Output Voltage Set Point Range                                  | 6.25mV resolution, 8 bit   |   | 0.800 <sup>(1)</sup> |     | 1.59375 | V                |
| Buck 4 $V_{OUT}$ Range         | Output Voltage Set Point Range                                  | 6.25mV resolution, 8 bit   |   | 0.600 <sup>(1)</sup> |     | 1.39375 | V                |
| $V_{OUT\_DYN}$                 | Dynamic Output Slew Rate  | Closed loop controlled   |   |                      | 10  |         | V/ms             |
| $V_{OUT\_SS}$<br>$V_{OUT\_SO}$ | Soft Start Slew Rate, and Soft Off Slew Rate                    | Closed loop controlled   |   |                      | 1   |         | V/ms             |

**NOTE:**

1. Limited by minimum  $t_{ON}$ . See Table 6 for Minimum Permissible  $V_{OUT}$  versus frequency.

## Electrical Characteristics (continued)

Specifications are for Operating Junction Temperature of  $T_J = 25^\circ\text{C}$  only; limits applying over the full Operating Junction Temperature range are denoted by a “\*”. Typical values represent the most likely parametric norm at  $T_J = 25^\circ\text{C}$ , and are provided for reference purposes only. Unless otherwise indicated,  $V_{IN} = 5V_{SYS} = 5.0V$ .

**Table 4: Electrical Characteristics (continued)**

| Symbol                            | Parameter  | Conditions                             | •    | Min  | Typ  | Max  | Units            |
|-----------------------------------|--|--|------|------|------|------|------------------|
| Buck Regulators 1 – 4 (continued) |  |  |      |      |      |      |                  |
| $V_{OUT\_DISCHARGE}$              | Pre-Bias Discharge Threshold   | Output falling                         |      |      | 200  |      | mV               |
| $R_{AD}$                          | Output Active Discharge Resistance   | Converter disabled and option selected |      |      | 78   |      | $\Omega$         |
| $I_{OUT}$                         | Full Load Rated Current  | Buck 1                                 | •    | 1.5  |      |      | A                |
|                                   |  | Buck 2                                 | •    | 1.5  |      |      | A                |
|                                   |  | Buck 3                                 | •    | 2.5  |      |      | A                |
|                                   |  | Buck 4                                 | •    | 4.0  |      |      | A                |
| $I_{CLIM}$                        | Peak Current Limit<br><br>These current limits help define maximum inductor ripple and to protect the internal power switches from an EOS event. | Buck 1                                 | •    | 2.5  | 3.4  | 4.5  | A                |
|                                   |  | Buck 2                                 | •    | 2.5  | 3.4  | 4.5  | A                |
|                                   |  | Buck 3                                 | •    | 3.5  | 4.5  | 5.5  | A                |
|                                   |  | Buck 4                                 | •    | 5.5  | 6.5  | 9.0  | A                |
| $V_{UVP}$                         | Under Voltage Protection Threshold   | Soft start completed, DVS inactive     |      |      | 70   |      | %                |
|                                   | UVP Deglitch   |  |      |      | 10   |      | $\mu\text{s}$    |
| $f_{OSC\_RANGE}$                  | Switching Frequency Programmable Range   | See <a href="#">Figure 8</a>           |      | 1000 |      | 2000 | kHz              |
| $f_{OSC}$                         | Default Switching Frequency  | Default 1001                           | -AQB |      | 1500 |      | kHz              |
|                                   |  | Default 0100                           | -XQB |      | 1000 |      | kHz              |
|                                   | Oscillator Accuracy  | At factory programmed set point        | •    | -10  |      | 10   | %                |
| $t_{ON-MIN}$                      | Minimum Controllable On-Time   | Full load                              |      |      | 92   | 120  | ns               |
| $R_{DSON (P)}$                    | Pin to Pin Resistance<br>PFET<br>High Side MOSFET  | Buck 1                                 |      |      | 146  |      | $\text{m}\Omega$ |
|                                   |  | Buck 2                                 |      |      | 146  |      | $\text{m}\Omega$ |
|                                   |  | Buck 3                                 |      |      | 67   |      | $\text{m}\Omega$ |
|                                   |  | Buck 4                                 |      |      | 60   |      | $\text{m}\Omega$ |
| $R_{DSON (N)}$                    | Pin To Pin Resistance<br>NFET<br>Low Side MOSFET   | Buck 1                                 |      |      | 103  |      | $\text{m}\Omega$ |
|                                   |  | Buck 2                                 |      |      | 103  |      | $\text{m}\Omega$ |
|                                   |  | Buck 3                                 |      |      | 32   |      | $\text{m}\Omega$ |
|                                   |  | Buck 4                                 |      |      | 27   |      | $\text{m}\Omega$ |

## Electrical Characteristics (continued)

Specifications are for Operating Junction Temperature of  $T_J = 25^\circ\text{C}$  only; limits applying over the full Operating Junction Temperature range are denoted by a “•”. Typical values represent the most likely parametric norm at  $T_J = 25^\circ\text{C}$ , and are provided for reference purposes only. Unless otherwise indicated,  $V_{IN} = 5V_{SYS} = 5.0V$ .

**Table 4: Electrical Characteristics (continued)**

| Symbol                     | Parameter   | Conditions   | • | Min  | Typ | Max | Units            |
|----------------------------|---|--|---|------|-----|-----|------------------|
| Low Dropout Regulator, LDO |   |  |   |      |     |     |                  |
| $V_{IN}$                   | Operational Voltage Range                                       |  | • | 4.0  |     | 5.5 | V                |
| $V_{OUT}$ Accuracy         | Output Voltage Accuracy at Factory Programmed Initial Set Point | Load current = 1mA to 100mA<br>$V_{IN} = 4.0V$ to $5.5V$                             | • | -2   |     | +2  | %                |
| $V_{OUT}$ Range            | Output Voltage Set Point Range                                  | 20mV resolution, 8 bit   |   | 1.5  |     | 3.6 | V                |
| $V_{OUT}$ Default          | Default Set Point   |  |   |      | 3.3 |     | V                |
| $V_{OUT\_DYN}$             | Dynamic Output Slew Rate  | Closed loop controlled, load = 25mA  |   |      | 10  |     | V/ms             |
| $V_{OUT\_SS}$              | Soft Start Slew Rate  | Closed loop controlled   |   |      | 1   |     | V/ms             |
| $I_{SC}$                   | Short Circuit Current Limit                                     | $3V3LDO = 0V$  | • | 120  | 230 | 260 | mA               |
| $V_{DO}$                   | Dropout Voltage (defined as a drop of 2% from initial value)    | Load current = 10mA  | • |      | 11  | 30  | mV               |
|                            |   | Load current = 100mA   | • |      | 210 | 300 | mV               |
| PSRR                       | Power Supply Rejection Ratio                                    | $f = 1\text{kHz}$ , $I_{OUT} = 10\text{mA}$ ,<br>$V_{IN} = 4.3V$ , $V_{OUT} = 3.3V$  |   |      | 56  |     | dB               |
|                            |   | $f = 10\text{kHz}$ , $I_{OUT} = 10\text{mA}$ ,<br>$V_{IN} = 4.3V$ , $V_{OUT} = 3.3V$ |   |      | 40  |     | dB               |
| $C_{OUT}$                  | Output Capacitor (ceramic)                                      | Capacitance (effective capacitance)  |   | 0.68 | 1.0 |     | $\mu\text{F}$    |
|                            |   | ESR  |   | 1    |     | 100 | m $\Omega$       |
| $\theta_n$                 | Supply Output Noise   | $10\text{ Hz} \leq f \leq 100\text{ kHz}$ ,<br>$V_{IN} = 4.3V$ , $V_{OUT} = 3.3V$    |   |      | 470 |     | $\mu\text{Vrms}$ |
| $R_{AD}$                   | Output Active Discharge Resistance                              | Converter disabled and option selected   |   |      | 78  |     | $\Omega$         |

## Electrical Characteristics (continued)

Specifications are for Operating Junction Temperature of  $T_J = 25^\circ\text{C}$  only; limits applying over the full Operating Junction Temperature range are denoted by a “\*”. Typical values represent the most likely parametric norm at  $T_J = 25^\circ\text{C}$ , and are provided for reference purposes only. Unless otherwise indicated,  $V_{IN} = 5V_{SYS} = 5.0V$ .

**Table 4: Electrical Characteristics (continued)**

| Symbol                     | Parameter                                 | Conditions  | • | Min  | Typ  | Max  | Units         |
|----------------------------|---|---|---|------|------|------|---------------|
| Power Good Outputs         |   |   |   |      |      |      |               |
|                            | Power Good Threshold                      | $V_{OUT}$ rising, at default $V_{OUT}$ set points | • | 85   | 90   | 95   | %             |
|                            | Power Good Hysteresis Buck 1 and LDO      | $V_{OUT}$ falling                                 |   |      | 122  |      | mV            |
|                            | Power Good Hysteresis Buck 3 and Buck 4   | $V_{OUT}$ falling                                 |   |      | 38   |      | mV            |
|                            | Power Good Hysteresis Buck 2              | $V_{OUT}$ falling                                 |   |      | 67   |      | mV            |
|                            | Power Good Assertion Delay, FB Rising     |   |   |      | 2    |      | ms            |
|                            | Power Good De-Assertion Delay, FB Falling |   |   |      | 65   |      | $\mu\text{s}$ |
| $V_{OL}$                   | Output Level Low                          | $I_{SINK} = 1\text{mA}$                           | • |      |      | 0.4  | V             |
| GLOBAL EN and SEQ EN Input |   |   |   |      |      |      |               |
| $V_{IL}$                   | Input low level                           |   |   |      |      | 0.8  | V             |
| $V_{IH}$                   | Input High Level                          |   |   | 2.0  |      |      | V             |
|                            | GLOBAL EN Input Current                   | GLOBAL EN = 5.5V                                  |   |      | 4    | 30   | $\mu\text{A}$ |
|                            | SEQ EN Input Current                      | SEQ EN = 5.5V                                     |   |      | 4    | 30   | $\mu\text{A}$ |
| Input Voltage Monitor Flag |   |   |   |      |      |      |               |
| $V_{TH\_RISING}$           | Input Voltage Good Threshold              | Voltage rising                                    |   | 4.59 | 4.63 | 4.7  | V             |
| $V_{TH\_FALLING}$          | Input Voltage Good Threshold              | Voltage falling                                   |   | 4.52 | 4.57 | 4.65 | V             |

## Electrical Characteristics (continued)

Specifications are for Operating Junction Temperature of  $T_J = 25^\circ\text{C}$  only; limits applying over the full Operating Junction Temperature range are denoted by a “•”. Typical values represent the most likely parametric norm at  $T_J = 25^\circ\text{C}$ , and are provided for reference purposes only. Unless otherwise indicated,  $V_{IN} = 5V_{SYS} = 5.0V$ .

**Table 4: Electrical Characteristics (continued)**

| Symbol                      | Parameter                                | Conditions                 | • | Min | Typ        | Max                          | Units                 |
|-----------------------------|--|----------------------------|---|-----|------------|------------------------------|-----------------------|
| ADC, Temperature Monitoring |  |                            |   |     |            |                              |                       |
|                             | Input range                              | $5V_{SYS} \geq 4.2V$       | • | 0   |            | $2.55 + \text{offset}^{(1)}$ | V                     |
|                             | Input range                              | $5V_{SYS} = 4.0V$          | • | 0   |            | 2.35                         | V                     |
|                             | Nominal Resolution                       | 8 bit                      |   |     | 10         |                              | mV/<br>LSB            |
|                             | INL                                      |                            |   |     |            | $\pm 2$                      | LSB                   |
|                             | DNL, Differential nonlinearity           |                            |   |     |            | $\pm 1$                      | LSB                   |
|                             | Full Scale Error                         |                            |   |     |            | $\pm 2$                      | LSB                   |
|                             | Zero Error (offset)                      |                            |   |     | +1         |                              | LSB                   |
|                             | Full Scale Error Temperature Coefficient |                            |   |     | $\pm 0.03$ | $\pm 0.05$                   | $\% / ^\circ\text{C}$ |
|                             | ADC Conversion Frequency                 |                            |   |     | 5.56       |                              | kHz                   |
|                             | Input capacitance                        |                            |   |     | 4          |                              | pF                    |
|                             | AN0/1 DC Input Impedance                 |                            |   |     | 10         |                              | M $\Omega$            |
| $T_{\text{RANGE}}$          | Temperature Monitoring Range             |                            |   | -40 |            | Thermal Shutdown             | $^\circ\text{C}$      |
| $T_{\text{RES}}$            | Temperature Monitoring Resolution        |                            |   |     | 1.06       |                              | $^\circ\text{C}$      |
| $T_{\text{ACCURACY}}$       | Temperature Monitoring Accuracy          | $25^\circ\text{C}$ (h'5F)  |   | -2  |            | 2                            | $^\circ\text{C}$      |
|                             |  | $105^\circ\text{C}$ (h'B4) |   | -7  |            | 7                            | $^\circ\text{C}$      |

**NOTE:**

1. Zero error (offset) specification shown below.

## Electrical Characteristics (continued)

Specifications are for Operating Junction Temperature of  $T_J = 25^\circ\text{C}$  only; limits applying over the full Operating Junction Temperature range are denoted by a “•”. Typical values represent the most likely parametric norm at  $T_J = 25^\circ\text{C}$ , and are provided for reference purposes only. Unless otherwise indicated,  $V_{IN} = 5V_{SYS} = 5.0V$ .

**Table 4: Electrical Characteristics (continued)**

| Symbol   | Parameter  | Conditions                                  | • | Min | Typ                  | Max | Units         |
|--|--|---|---|-----|----------------------|-----|---------------|
| I <sup>2</sup> C Interface – Default Address 7'b0101101 (0x2D), see Table 10 |  |   |   |     |                      |     |               |
| $V_{IL}$   | Input Low Level  |   |   |     |                      | 0.8 | V             |
| $V_{IH}$   | Input High Level   |   |   | 2.0 |                      |     | V             |
| $V_L$  | VDDIO Supply Voltage   |   |   | 3.0 |                      | 5.5 | V             |
| $V_{OL\_I2C}$  | SDA Logic Output Low Voltage                                     | 3mA sink current                            | • |     |                      | 0.8 | V             |
| $f_{SCL}$  | SCL Clock Frequency  |   | • |     |                      | 400 | kHz           |
| $t_{SCL\_H}$   | SCL Clock High Period  |   | • | 0.6 |                      |     | $\mu\text{s}$ |
| $t_{SCL\_L}$   | SCL Clock Low Period   |   | • | 1.3 |                      |     | $\mu\text{s}$ |
| $t_{SP}$   | I <sup>2</sup> C Spike Rejection Filter Pulse Width <sup>1</sup> |   | • | 0   |                      | 50  | ns            |
| $t_{SU\_DAT}$  | I <sup>2</sup> C Data Setup Time                                 |   | • | 100 |                      |     | ns            |
| $t_{HD\_DAT}$  | I <sup>2</sup> C Data Hold Time                                  |   | • | 0   |                      | 900 | ns            |
| $t_{R\_I2C}$   | SDA, SCL Rise Time   | $C_B$ = total capacitance of bus line in pF | • |     | $20 + 0.1 \cdot C_B$ | 300 | ns            |
| $t_{F\_I2C}$   | SDA, SCL Fall Time   | $C_B$ = total capacitance of bus line in pF | • |     | $20 + 0.1 \cdot C_B$ | 300 | ns            |
| $t_{BUF}$  | I <sup>2</sup> C Bus Free Time Between Stop and Start            |   | • | 1.3 |                      |     | $\mu\text{s}$ |
| $t_{SU\_STA}$  | I <sup>2</sup> C Repeated Start Condition Setup Time             |   | • | 0.6 |                      |     | $\mu\text{s}$ |
| $t_{HD\_STA}$  | I <sup>2</sup> C Repeated Start Condition Hold Time              |   | • | 0.6 |                      |     | $\mu\text{s}$ |
| $t_{SU\_STO}$  | I <sup>2</sup> C Stop Condition Setup Time                       |   | • | 0.6 |                      |     | $\mu\text{s}$ |
| $C_B$  | I <sup>2</sup> C Bus Capacitive Load                             |   | • |     |                      | 400 | pF            |
| $C_{SDA}$  | SDA Input Capacitance  |   | • |     |                      | 10  | pF            |
| $C_{SCL}$  | SCL Input Capacitance  |   | • |     |                      | 10  | pF            |

## Electrical Characteristics (continued)

Specifications are for Operating Junction Temperature of  $T_J = 25^\circ\text{C}$  only; limits applying over the full Operating Junction Temperature range are denoted by a “\*”. Typical values represent the most likely parametric norm at  $T_J = 25^\circ\text{C}$ , and are provided for reference purposes only. Unless otherwise indicated,  $V_{IN} = 5V_{SYS} = 5.0V$ .

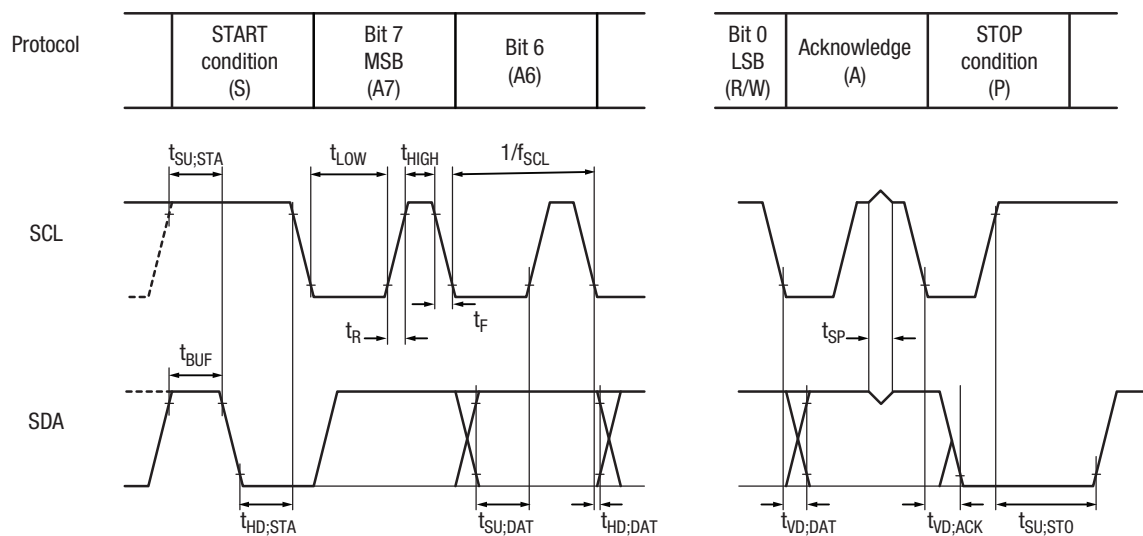


Figure 1: I<sup>2</sup>C Bus Timing Diagram

# Pin Information

## Pin Configuration

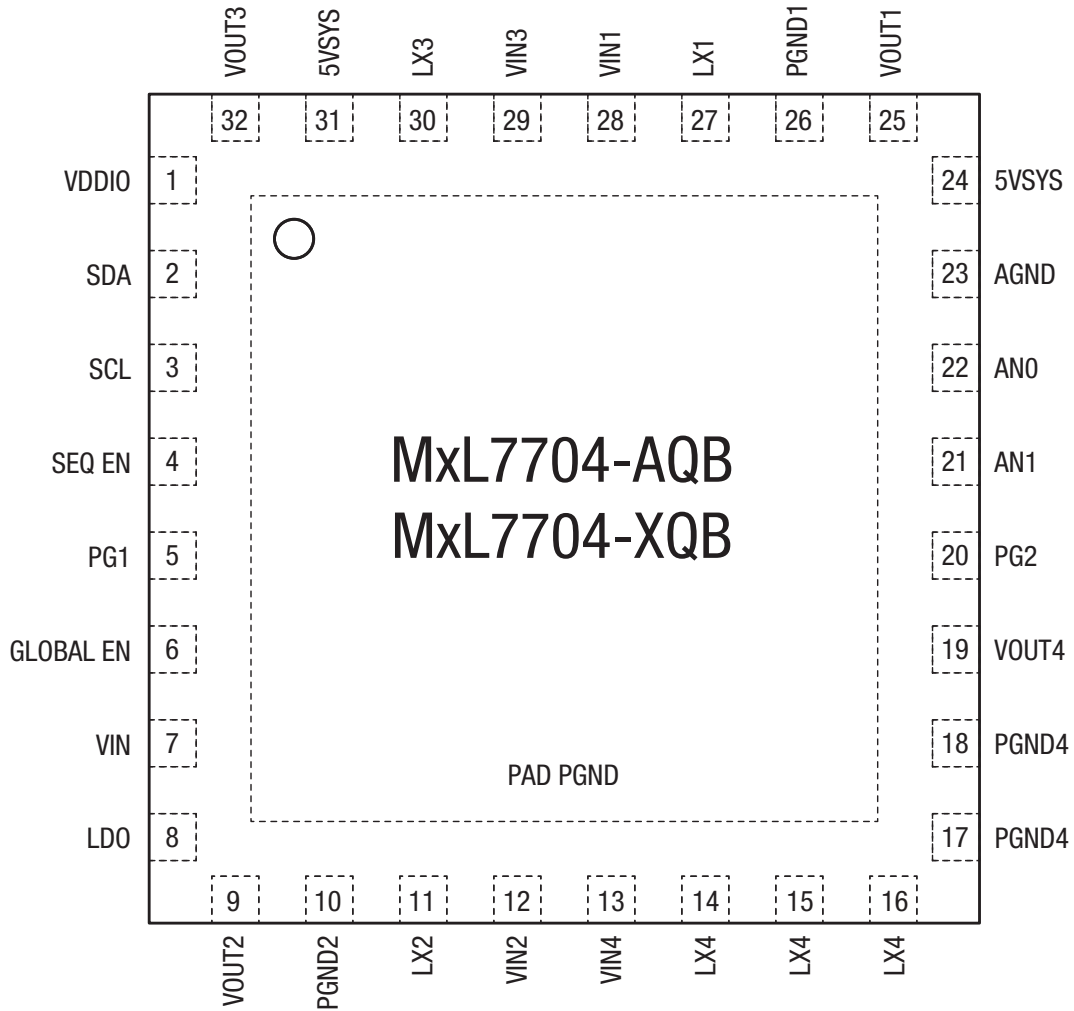


Figure 2: Pin Configuration (Top View)

## Pin Description

**Table 5: Pin Names and Descriptions**

| Pin Number | Pin Name  | Description  |
|------------|-----------|--|
| 1          | VDDIO     | Supply for I <sup>2</sup> C Interface, 3.3V to 5V nominal.   |
| 2          | SDA       | I <sup>2</sup> C Data  |
| 3          | SCL       | I <sup>2</sup> C Clock   |
| 4          | SEQ EN    | Sequence enable. Input which can be added as an external gate to the power up sequencing. Is effectively ANDed to the power up sequencing. As such, has no effect on power down sequencing. See register map. If not used, tie to 5VSYS pin. |
| 5          | PG1       | Power Good output 1, open drain. May consist of any ANDed output of all 5 regulators. See register map.  |
| 6          | GLOBAL EN | Chip enable. When pulled low, shuts down entire chip after power down sequencing complete.   |
| 7          | VIN       | Input supply to the LDO  |
| 8          | LDO       | Output of the 100mA LDO. May be programmed from 1.5V to 3.6V in 20mV steps.  |
| 9          | VOUT2     | Feedback pin for Buck 2. Buck 2 can be programmed from 1.3V to 1.92V in 20mV steps.  |
| 10         | PGND2     | Power Ground. Source of the low side MOSFET for Buck 2.  |
| 11         | LX2       | Switch node of Buck 2. Connect to output inductor.   |
| 12         | VIN2      | Input supply to Buck 2. Bypass to PGND.  |
| 13         | VIN4      | Input supply to Buck 4. Bypass to PGND.  |
| 14, 15, 16 | LX4       | Switch node of Buck 4. Connect to output inductor.   |
| 17, 18     | PGND4     | Power Ground. Source of the low side MOSFET for Buck 4.  |
| 19         | VOUT4     | Feedback pin for Buck 4. Buck 4 can be programmed from 0.6V to 1.39375V in 6.25mV steps  |
| 20         | PG2       | Power Good output 2, open drain. May consist of any ANDed output of all 5 regulators. See register map.  |
| 21         | AN1       | Input to ADC. If not used, tie to AGND.  |
| 22         | AN0       | Input to ADC. If not used, tie to AGND.  |
| 23         | AGND      | Signal Analog Ground. Connect to system ground.  |
| 24         | 5VSYS     | Filtered from VIN through a RC to provide internal circuits with clean 5V. Place a 100nF capacitor between this pin and AGND as close as possible to the IC.   |
| 25         | VOUT1     | Feedback pin for Buck 1. Buck 1 can be programmed from 3.0V to 3.6V in 20mV steps.   |
| 26         | PGND1     | Power Ground. Source of the low side MOSFET for Buck 1.  |
| 27         | LX1       | Switch node of Buck 1. Connect to output inductor.   |
| 28         | VIN1      | Input supply to Buck 1. Bypass to PGND.  |
| 29         | VIN3      | Input supply to Buck 3. Bypass to PGND.  |
| 30         | LX3       | Switch node of Buck 3. Connect to output inductor.   |
| 31         | 5VSYS     | Connect to 5V input. Unlike Pin 24, bypassing is unimportant.  |
| 32         | VOUT3     | Feedback pin for Buck 3. Buck 3 can be programmed from 0.8V to 1.59375V in 6.25mV steps.   |
| PAD        | PGND      | Package central pad. Connect to PGND.  |

# Typical Performance Characteristics

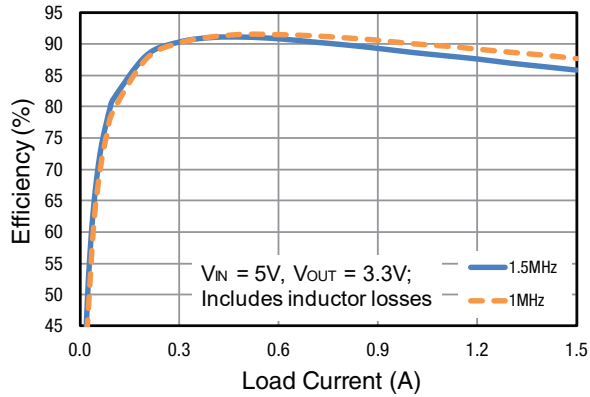


Figure 3: Buck 1 Efficiency

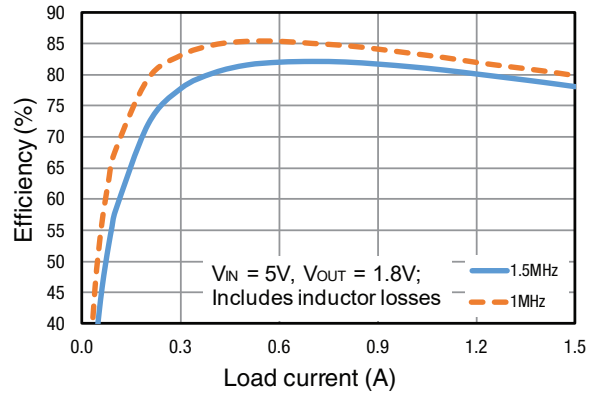


Figure 4: Buck 2 Efficiency

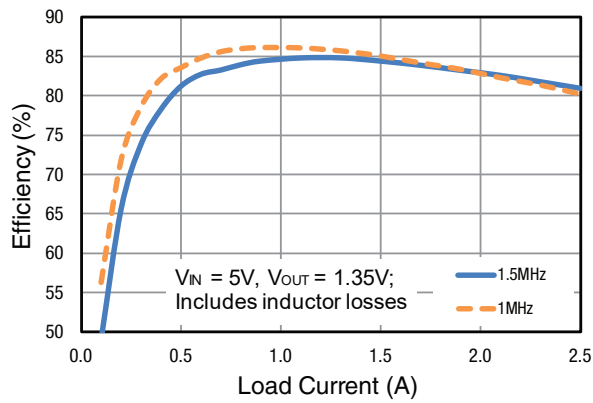


Figure 5: Buck 3 Efficiency

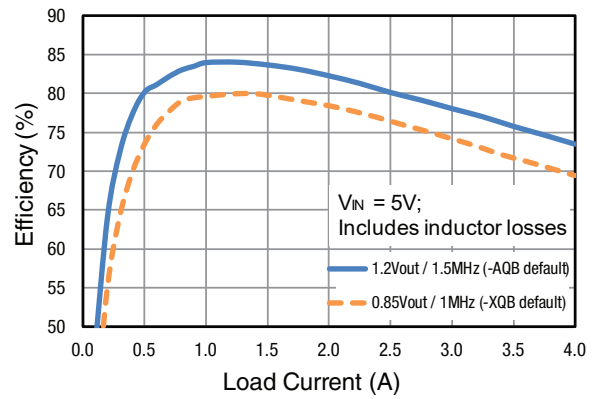


Figure 6: Buck 4 Efficiency

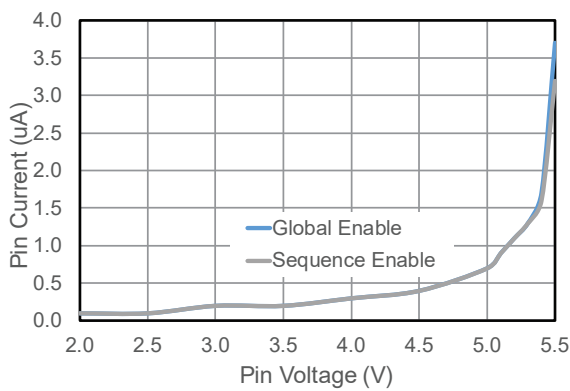


Figure 7: GLOBAL EN and SEQ EN Input Current vs Voltage

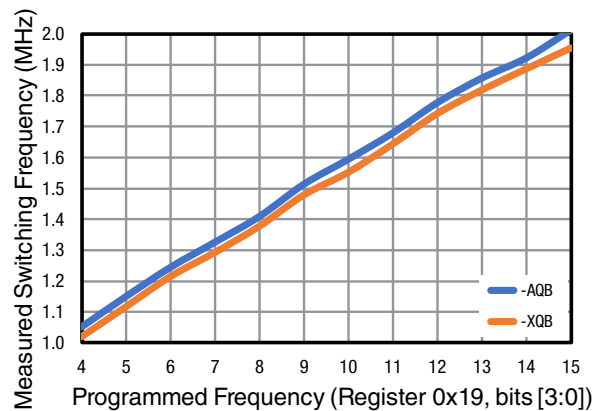


Figure 8: Measured vs Programmed Frequency

# Typical Performance Characteristics (Continued)

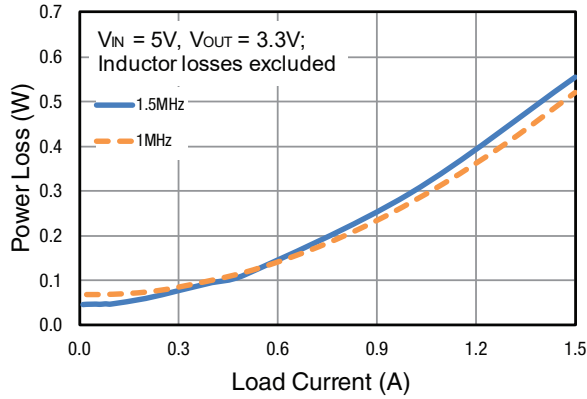


Figure 9: Buck 1 Power Loss

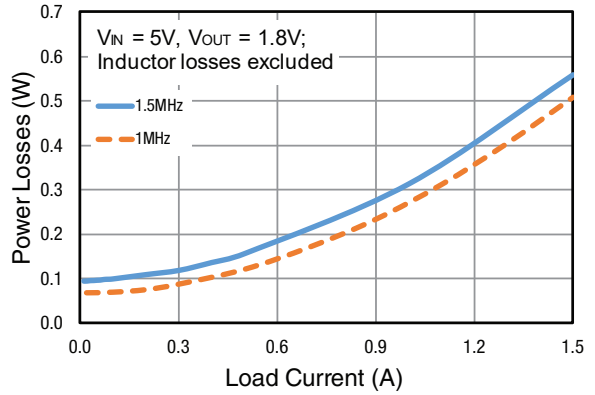


Figure 10: Buck 2 Power Loss

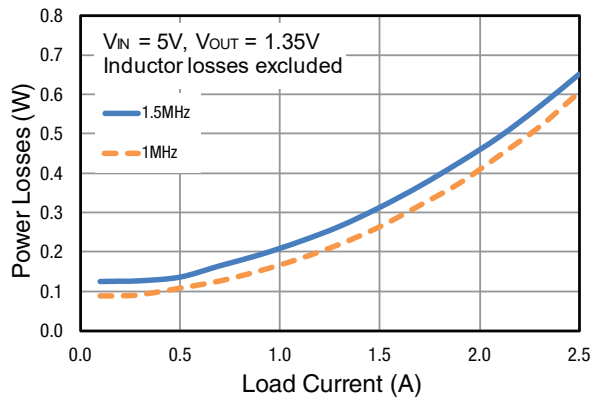


Figure 11: Buck 3 Power Loss

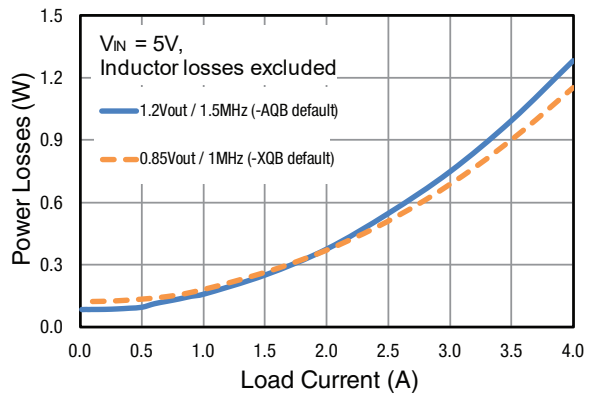


Figure 12: Buck 4 Power Loss

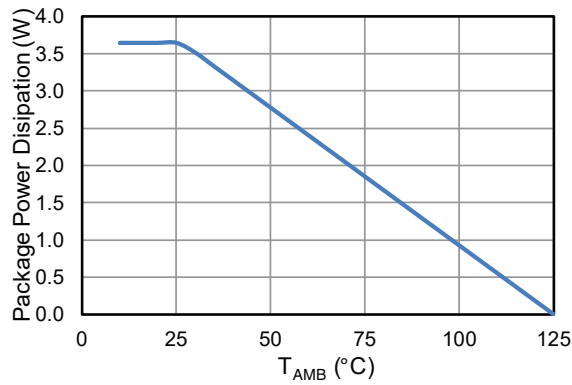


Figure 13: Package Derating

# Typical Performance Characteristics (Continued)

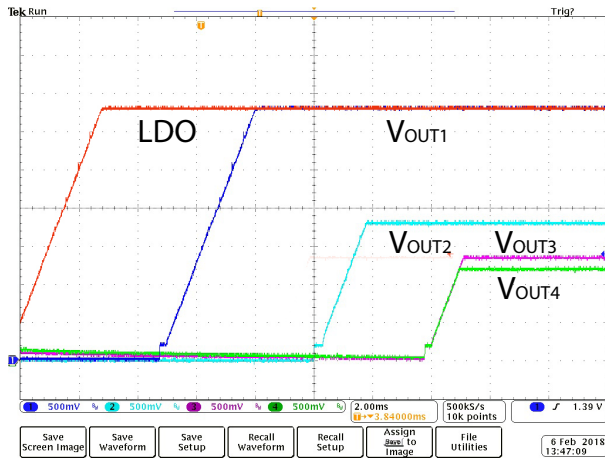


Figure 14: MxL7704-AQB Power-Up Sequencing

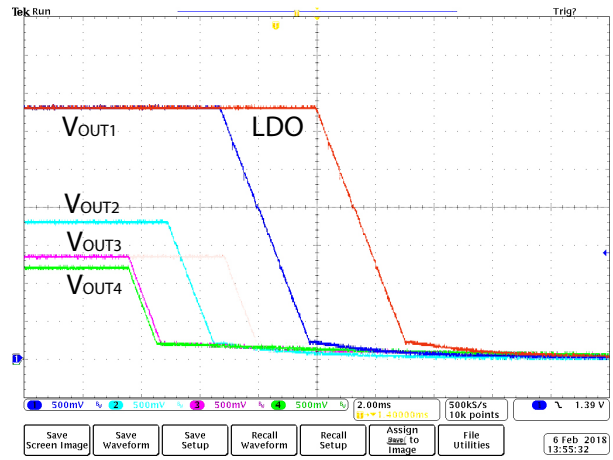


Figure 15: MxL7704-AQB Power-Down Sequencing

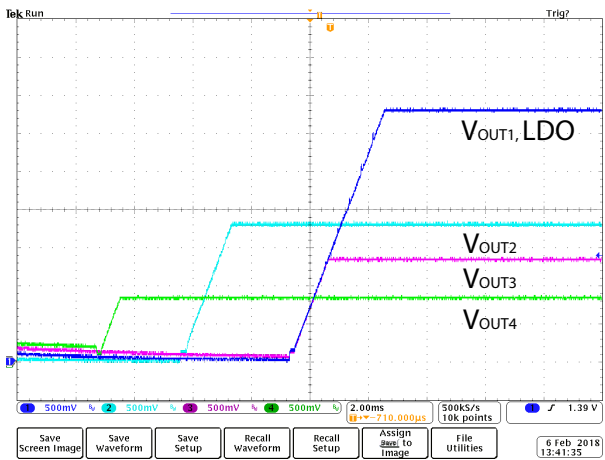


Figure 16: MxL7704-XQB Power-Up Sequencing

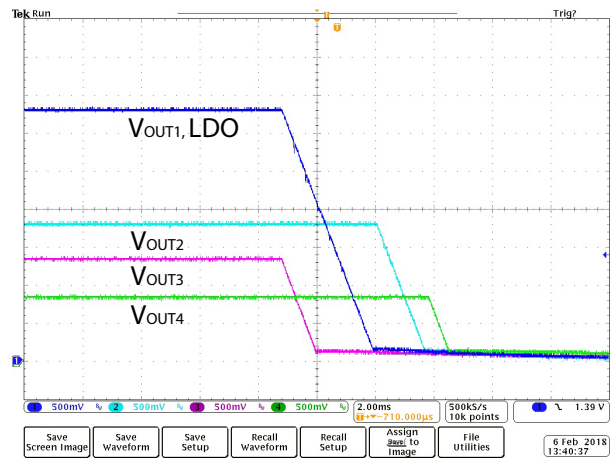


Figure 17: MxL7704-XQB Power-Down Sequencing

# Functional Block Diagram

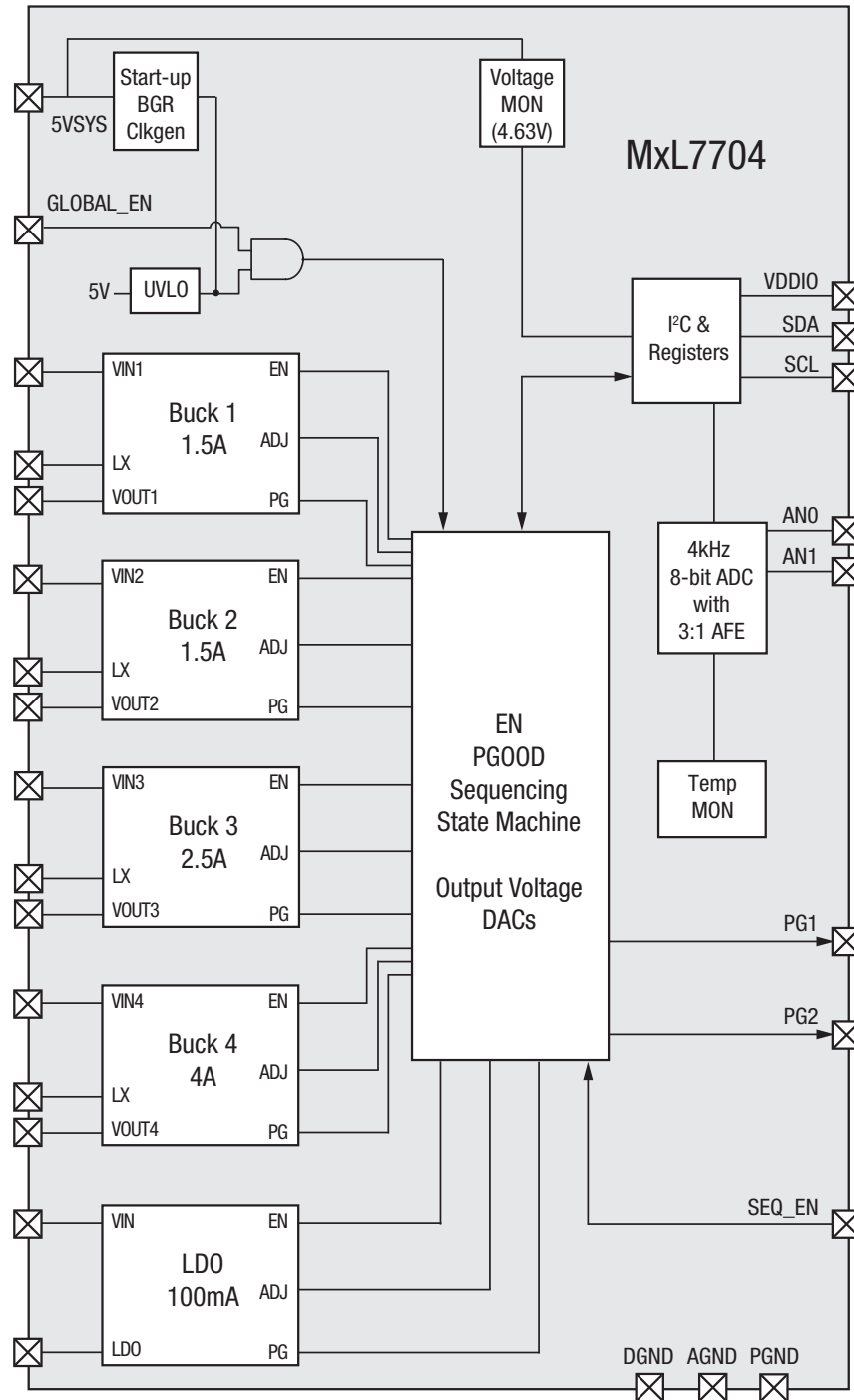


Figure 18: Functional Block Diagram

# Applications Information

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## Operation

MxL7704 is a 5 output Universal PMIC optimized for powering low power FPGAs, DSPs and microprocessors from a 5V input. Four independent buck regulators provide load currents of 1.5A for system power, 1.5A for I/O, 2.5A for memory and 4A for core power. A 100mA LDO provides a clean 1.5V to 3.6V power for auxiliary devices. All outputs support margining where the initial set point can be changed by an 8-bit code. All outputs also support Dynamic Voltage Scaling (DVS) where the output voltage can be dynamically ramped up or down at a preset rate to support processors that can utilize this function to save power.

The I<sup>2</sup>C interface allows the customer to monitor an input voltage flag and PGOOD flags for each output. The I<sup>2</sup>C port can also be used to modify the power up and power down sequencing options, assign power good outputs to PG1 and PG2 pins, enable the PMIC outputs and select the switching frequency.

All buck regulators employ peak current mode control architecture with internal compensation and high switching frequency. This provides fast transient response to load and line changes without sacrificing stability and keeping small component sizes on board.

Fault protection features include input undervoltage lockout (UVLO), output overcurrent protection (OCP), undervoltage protection (UVP) and over temperature (OTP) or thermal protection.

Two Power Good outputs are available (PG1, PG2).

Each channel has a soft start, soft stop function and a Dynamic Voltage Scaling Function (DVS).

## Output Voltage Scaling

All outputs support margining where the initial set point can be changed by an 8-bit code. The channel 1 range is from 3.0V to 3.6V with 20mV resolution. Note that the channel 1 regulation will be limited by duty cycle. The channel 2 dynamic range is from 1.3V to 1.92V with 20mV resolution, the channel 3 from 0.8V to 1.6V with 6.25mV resolution, and the channel 4 from 0.6V to 1.4V with 6.25mV resolution. The channel 3 and 4 lower regulation range will be limited by the minimum on time of 120ns. LDO dynamic range is from 1.5V to 3.6V with 20mV resolution. Rather than change the voltage divider resistances in the feedback path, the error amplifier reference is changed. This ensures that the gain of the control loop remains unchanged as the voltage is changed. When a voltage change is commanded, the output will slew at 10V/ms which minimizes latency when moving from low power states to high power states.

Although the 8-bit register will accept values outside those within the ranges listed above, the accuracy of the output is not guaranteed.

The LDO and buck output voltages can be changed via I<sup>2</sup>C. For more details, see the "[I<sup>2</sup>C Operation](#)" section.

## Sequencing

Power up and power down sequencing is controlled by setting registers 0x15, 0x16, 0x17 and 0x19. Each channel (BUCK or LDO) can be assigned to be in any of four groups (GROUP 0 thru 3) by programming register 0x15 and 0x16 (each of them has a 2-bit group register that assigns them to each of the four groups). When enabled through GLOBAL EN or the input voltage rising above the UVLO point, all outputs will be discharged by enabling the 78Ω discharge resistors. This ensures proper sequencing after an input voltage glitch.

The sequencing state machine starts with GROUP 0 and looks for any channels if assigned to it by their respective 2-bit group settings. If any channels are assigned to GROUP 0, the state machine starts them up at the same time, provided 5V<sub>SYS</sub> Under Voltage Lock-out (UVLO) has cleared and the outputs assigned to GROUP 0 have been discharged by the 78Ω resistor to <200mV. Once all GROUP 0 channels are up (all PGOODs are found with the 2ms blanking time added), the sequencing state machine moves to GROUP 1 and repeats the same process, omitting the wait of the output to be discharged to <200mV. It continues to GROUP2 and then GROUP 3. If one group is not up (at least one channel in the group is at fault or disabled thru register setting 0x16), all subsequent groups won't be started. If a group does not have any channels, it will be ignored and the sequencing state machine will move to the next one.

## Power Down Sequencing of Channels

After a normal power up sequence is completed, the power down sequencing can be controlled by pulling GLOBAL EN LOW. Power down sequencing of channels follows the reverse order of power up sequencing of channels (GROUP 3 thru 0). All channels will be sequenced down in one of the two methods, depending on the Soft Off Enable Setting (bit 6 of 0x19):

- Soft Off is enabled: Dynamically slewed down for Xms (where X = V<sub>out</sub>) then discharged through the 78Ω resistor (default).
- Soft Off is disabled: All channels will be immediately tri-stated and will be discharged by the 78Ω active discharge resistance.

If an output is not dynamically slewed down, the system will consider down sequencing complete for that channel immediately and the next channel in the sequence will begin its power down. For example, if all outputs are chosen to only have 78Ω discharge without dynamic soft-off, all regulators would effectively turn off at the same time (within limits of the state machine).

LDO by default has no ability to slew negative and thus will immediately be considered soft-off complete.

The MxL7704 uses a digitally controlled soft start and soft off. Each output, including the LDO, has an 8 bit Reference DAC feeding the error amplifier input. Although the registers will accept a value across the entire DAC range, the outputs are optimized for the output voltage ranges specified in the electrical table.

Note that after all channels are sequencing down by pulling GLOBAL EN LOW, the IC will be in a hard-reset mode.

When the IC is shut down via Thermal Shutdown (TSD), the channels will be immediately tri-stated and discharged by the 78Ω active discharge resistance. Bit 6 at register address 0x19 will be ignored.

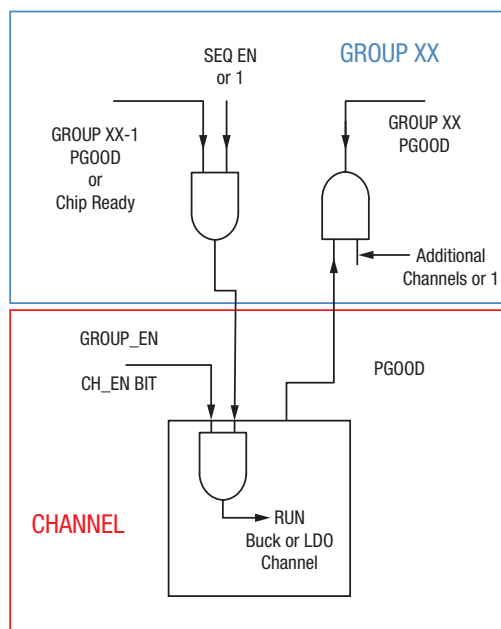


Figure 19: Sequencing

## SEQ EN and Channel Enable Bits

The SEQ EN pin input can be assigned to any of the sequence groups to allow an external signal to gate sequencing. This is accomplished by setting bits [7:6] of register 0x17, which will act as an enable to that group and all other subsequently higher groups. Given that each channel has its own channel enable (bits [4:0] of register 0x16), group enable needs to be enabled as well to effectively enable a channel. Having SEQ EN LOW at start will then gate the startup of the group that is assigned to it, and hence all other subsequent higher groups. Having SEQ EN HIGH at startup will void its effect (all group enables will be ON) on the Soft Start Sequencing.

One can always use SEQ EN (pulling HIGH/LOW) to turn on/off multiple groups/channels at any time by moving/setting SEQ EN Group Assign (bit [7:6] of register 0x17). If SEQ EN is pulled LOW, the group / channel(s) assigned to the SEQ EN will be shut down according to the Soft Off Enable setting (bit 6 of 0x19) without any power down sequencing. If SEQ EN is logic HIGH when GLOBAL EN is driven low it does not gate the sequential power down of the sequencing groups.

One can always use channel enable bits (bits [4:0] of the register 0x16) to gate sequencing through the I<sup>2</sup>C interface. However once power up sequencing is completed, the channel enable bits can only turn on or off particular channels.

## Changing Sequencing Registers While Operating

Sequencing registers may be changed while in operation to allow one to change the power down behavior vs the startup behavior. However, it is not recommended to write to these registers when the chip is powering up or down.

## PGOOD

The state of the PGOOD of each channel will gate power up of subsequent higher groups. The state of the PGOOD signals are reported in the status register 0x1A bits [4:0].

At the end of the soft start, PGOOD goes high after the 2ms PGOOD assertion delay. If a channel goes out of the regulation window for more than 65 $\mu$ s during regulation, PGOOD will go low. It will assert again after the 2ms assertion delay, assuming the channel is back into the regulation window. If the glitch is faster than 65 $\mu$ s, PGOOD will not record it.

During DVS, PGOOD will be blanked and held HIGH. Once DVS is done, PGOOD will be re-evaluated and an effective PGOOD will be updated.

In the event of a fault, PGOOD will be pulled low immediately.

The registers 0x17 and 0x18 are used to route PGOOD signals from all channels to PG1 and PG2 outputs respectively. Multiple channels can be assigned and PG1 or PG2 signals will be logic function AND of the selected PGOOD signals. If no channels are assigned to a PG pin, the pin will be high impedance.

## Input Voltage Monitor Flag

The device is continually monitoring voltage at the 5VSYS pin. The status of this pin will be kept in register 0x1A (bit [6:5]). Bit 5 provides the current status of this pin while bit 6 is “sticky” set once the 5VSYS pin is above 4.63V. If the voltage at the 5VSYS pin is above 4.63V, bit 5 will be set or vice versa. The host can poll these two bits to check the status of this pin. Bit 6 can only be cleared by the host writing “1” to it.

## Hot Start

If chip fault action is selected and a fault occurs, start up sequencing varies from a cold start where Global EN or UVLO enables the device.

Instead of discharging all outputs in all sequencing groups to <200mV, only the outputs in sequencing group 0 will be discharged. For example if there is no load on the outputs and the down sequencing actions soft-off and 78 $\Omega$  discharge are not selected, when one channel is faulted all other outputs will float at their set point. When the chip initiates the startup sequence, the 4 buck regulators will drive the outputs down as a natural function of the commanded output voltage. This is also true when using SEQ EN to turn groups on and off. An example of startup after a fault on buck 4 is shown in Figure 20.

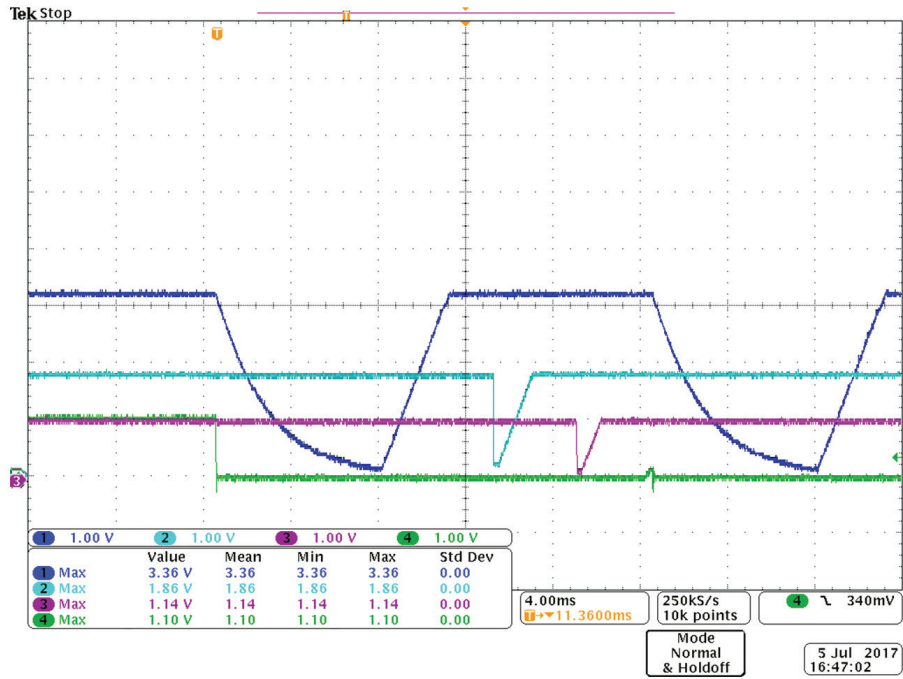


Figure 20: Example of Startup, After a Buck 4 Fault

Figure 20 was generated on an evaluation board with no external load and the 78Ω discharge disabled. The default state is to have the 78Ω discharge enabled from the factory.

## Sequencing Examples

### Example 1 Sequencing Using SEQ EN

- Sequencing Group 00: Buck 1, LDO
- Sequencing Group 01: Buck 2, SEQ EN
- Sequencing Group 10: Buck 3
- Sequencing Group 11: Buck 4

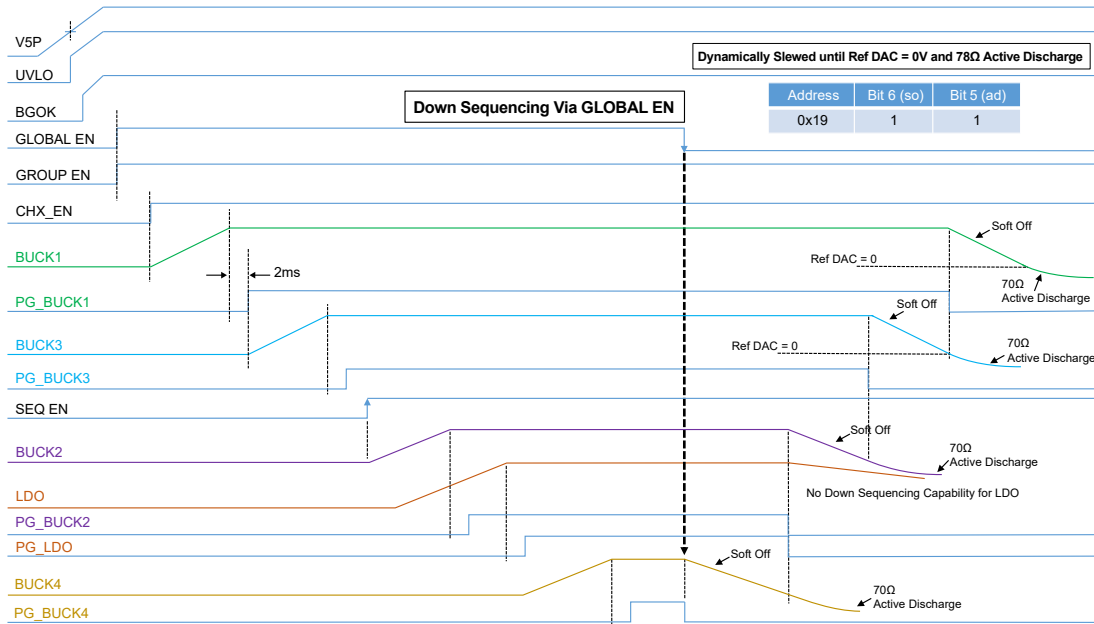


Figure 21: Example 1 Sequencing

Example 2 Sequencing Using SEQ EN

- Sequencing Group 00: Buck 1
- Sequencing Group 01: Buck 3
- Sequencing Group 10: Buck 2, LDO, SEQ EN
- Sequencing Group 11: Buck 4

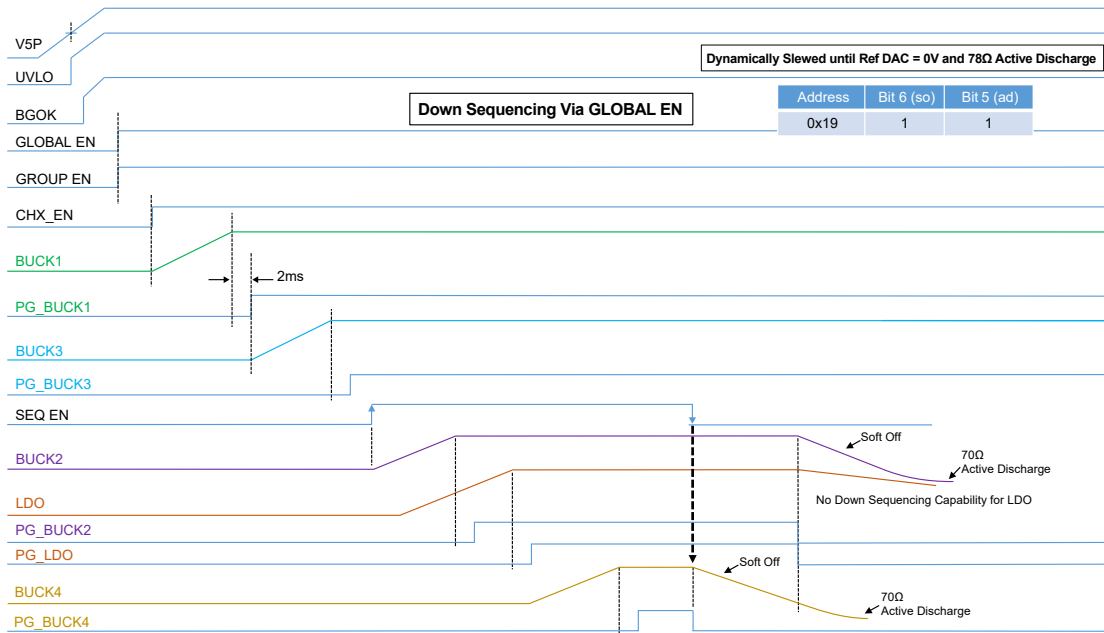


Figure 22: Example 2 Sequencing

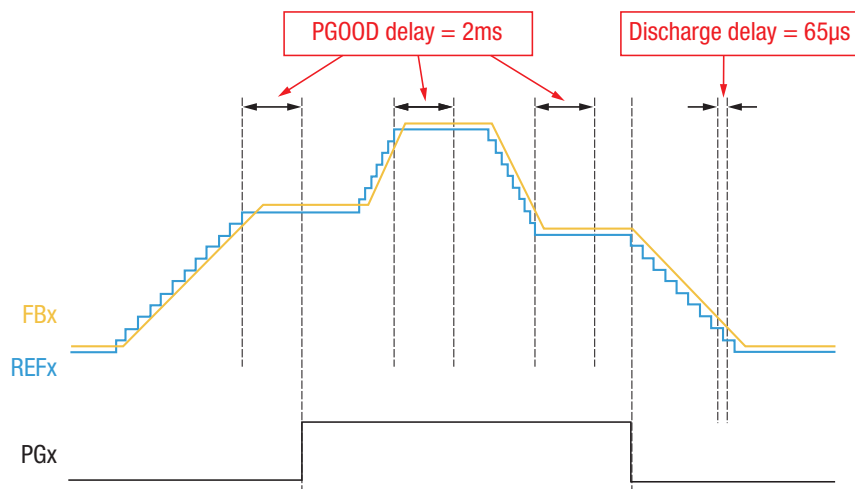


Figure 23: Power Good Timing

## Faults

### UVP (Under Voltage Protection)

A fault condition will be reported by the switching regulators and restart will be initiated if an under voltage is detected on the output. That channel will immediately tristate and apply the  $78\Omega$  discharge. If chip fault action is selected, the other outputs will all simultaneously power down based on their power down settings. Once all channels are powered down, a 1ms delay will gate the restart of the channel or chip. In restart, just as in initial power up, the first sequencing GROUP channels will be discharged to  $<200\text{mV}$  before power up sequence initiates.

### OVP (Output Over Voltage Protection)

In the event that an output is inadvertently connected to a source higher than the target voltage of the buck regulator, the buck regulator will do all it can to clamp that voltage. It is the natural response of the control loop to turn on the low side MOSFET to try and clamp the output voltage. The buck regulator will do so in an effort to protect the lower voltage, higher value circuitry to the point of destruction.

### OCP (Over Current Protection)

A current limit event occurs when the over current threshold is exceeded for 8 or more switching cycles. Once detected, the switches are placed into tristate. Just as with UVP, that channel will immediately tristate and apply the  $78\Omega$  discharge. If chip fault action is selected, the other outputs will all simultaneously power down based on their power down settings. Once all channels are powered down, a 1ms delay will gate the restart of the channel or chip.

Unlike initial power up where all outputs are discharged before sequencing initiates with sequencing group 0, during any “hot” restart, outputs for a given group are discharged prior to that group being enabled.

During soft-start, the OCP is disabled for the first 25% of the soft-start time period. If the output voltage is 1V, then soft-start time is 1ms and thus the current limit is enabled after the first 250µs. LDO OCP is activated after its soft start timer expires.

## Channel vs Chip Fault Actions

Register 0x19 bit 7 allows the user to choose whether a fault on a given channel will only affect that channel or cause an entire restart of the power system. If “channel” is selected, 0x19 bit 7 = 0, then when a fault occurs on any channel, that channel will fault and initiate a restart without affecting any of the other outputs.

If “chip” is selected, 0x19 bit 7 = 1, a fault on any channel will cause the other channels to down sequence together based on register 0x19 bit 6 setting and subsequently initiate power up sequence once channels discharge and the 1ms hiccup timer expires.

This register may be changed during chip operation. If the fault action is changed from channel to chip while the outputs are enabled and a fault had occurred previously, then the chip will “remember” that a fault had occurred and initiate a chip fault action. If the outputs are shut down when this change is made to the register no restart will occur.

## Thermal Design

Proper thermal design is critical in controlling device temperatures and in achieving robust designs. There are a number of factors that affect the thermal performance. One key factor is the temperature rise of the devices in the package which is a function of the thermal resistances of the package and the power being dissipated internally.

The thermal resistance of MxL7704 (27°C/W) is specified in the “Operating Ratings” section of this datasheet. The  $\theta_{JA}$  thermal resistance specification is based on the MxL7704 Evaluation Board operating without forced airflow. Since the actual board design in the final application will be different, the thermal resistances in the final design may be different from those specified.

The package thermal derating and power loss curves are shown in Figures 9 through 13.

## Layout Guidelines

Proper PCB layout is crucial in order to obtain good thermal and electrical performance.

For thermal considerations, it is essential to use a number of thermal vias to connect the central thermal pad to the ground layer(s).

In order to achieve good electrical and noise performance following steps are recommended:

1. Place the output inductor close to the LX pins and minimize the connection area. Doing this on the top layer is advisable.
2. Connect the central thermal pad of the power ground connections to as many layers as possible to enhance thermal conduction.
3. The output filtering capacitor needs to share the same power ground connection as the input filtering capacitor of the same buck converter. This should be connected to the signal ground plane with vias placed at the output filtering capacitors.
4. AC current loops formed by input filtering capacitors, output filtering capacitors, output inductors, and the regulator pins should be minimized.
5. AGND pins should be connected to the signal ground plane.
6. 5VSYS pin should have a low pass filter in front. A 100nF capacitor between 5VSYS and AGND should be placed as close as possible to the IC.

## I<sup>2</sup>C Operation

The interface will be 3.3V with tolerance to 5.5V.

Since there is no clock stretching allowed, the MxL7704 responds by not acknowledging (NAK) some I<sup>2</sup>C commands as a way to inform the host it cannot service them.

The MxL7704 will respond with a NAK if the delay between writing to the same LDO or VBUCKx register is less than 2.2ms (2ms + 10% internal oscillator accuracy). In addition, if multiple LDO or BUCK outputs are changed within 2.2ms of each other, then each output can only be changed once within those 2.2ms. The I<sup>2</sup>C master must wait at least 2.2ms after the last I<sup>2</sup>C write to the LDO or VBUCKx register before writing to them again.

Example 1: Changing outputs for VBUCK3 and VBUCK4

If writing to VBUCK3 followed by VBUCK4, then the I<sup>2</sup>C master must wait at least 2.2ms after the write to VBUCK4 before writing to VBUCK3 or VBUCK4 again.

Example 2: Changing all outputs

If writing to VLDO, VBUCK1, VBUCK2, VBUCK3 and VBUCK4, then the I<sup>2</sup>C master must wait for at least 2.2ms after the last write to these registers before writing to any of these registers again.

## Minimum t<sub>ON</sub> and Minimum Duty Cycle Limitation

Minimum on-time t<sub>ON</sub> of the MxL7704 is specified at 120ns. If a low duty cycle application requires a shorter t<sub>ON</sub>, regulation will be lost. The minimum permissible V<sub>OUT</sub> corresponding to switching frequency f can be calculated from:

$$\frac{V_{OUT}}{V_{IN}} = \frac{t_{ON}}{T} = t_{ON} \times f$$

$$V_{OUT} = V_{IN} \times f \times 120\text{ns}$$

Where V<sub>IN(max)</sub> = 5.5V

**Table 6: Minimum Permissible V<sub>OUT</sub>**

| f (MHz) | V <sub>OUT(min)</sub> (V) |
|---------|---------------------------|
| 1       | 0.660                     |
| 1.1     | 0.726                     |
| 1.2     | 0.792                     |
| 1.3     | 0.858                     |
| 1.4     | 0.924                     |
| 1.5     | 0.990                     |
| 1.6     | 1.056                     |
| 1.7     | 1.122                     |
| 1.8     | 1.188                     |
| 1.9     | 1.254                     |
| 2       | 1.320                     |
| 2.1     | 1.386                     |

## Buck 1 Operation at Low $V_{IN}$

When  $V_{IN} - V_{OUT}$  falls below 0.8V (ex.,  $V_{OUT} = 3.6V$ ,  $V_{IN} < 4.4V$ ) the controller will skip pulses to maintain regulation. Under steady-state operation, the controller will typically regulate with  $V_{IN}$  as low as 4.0V. If conditions result in dropout, the upper MOSFET has the ability to operate at 100% duty cycle. Operating at or near dropout may affect dynamic performance including load transient response and positive dynamic voltage scaling.

## Minimum Effective $C_{OUT}$

MxL7704 has internal feedback loop compensation. Each channel requires a minimum  $C_{OUT}$  in order to have a sufficient Phase Margin and stable feedback loop. The effective  $C_{OUT}$  for MxL7704-AQB and MxL7704-XQB is shown in Tables 7 and 8 respectively. Note that nominal capacitance will be higher than corresponding effective capacitance. Nominal capacitance, for a given set of operating conditions, must be calculated from manufacturer's datasheet by using applicable derating curves.

**Table 7: MxL7704-AQB Recommended L and  $C_{OUT}$**

| MxL7704-AQB |         |               |              |                                |
|-------------|---------|---------------|--------------|--------------------------------|
| f (MHz)     | Channel | $V_{OUT}$ (V) | L ( $\mu$ H) | Effective $C_{OUT}$ ( $\mu$ F) |
| 1.5         | 1       | 3.3           | 2.2          | 15                             |
|             | 2       | 1.8           | 1            | 20                             |
|             | 3       | 1.35          | 0.47         | 90                             |
|             | 4       | 1.2           | 0.47         | 110                            |

**Table 8: MxL7704-XQB Recommended L and  $C_{OUT}$**

| MxL7704-XQB |         |               |              |                                |
|-------------|---------|---------------|--------------|--------------------------------|
| f (MHz)     | Channel | $V_{OUT}$ (V) | L ( $\mu$ H) | Effective $C_{OUT}$ ( $\mu$ F) |
| 1           | 1       | 3.3           | 2.2          | 22                             |
|             | 2       | 1.8           | 2.2          | 27                             |
|             | 3       | 1.35          | 1            | 110                            |
|             | 4       | 0.85          | 0.47         | 210                            |

The following equation can be used to estimate the inductor value for different  $V_{OUT}$ .

$$L \geq \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{\Delta i \times f \times V_{IN}}$$

$V_{IN}$  = typical input voltage

$V_{OUT}$  = desired output voltage

f = switching frequency of the converter

$\Delta i$  = inductor ripple current

A good estimate for the inductor ripple current ( $\Delta i$ ) is 20% to 40% of the maximum output current. See  $I_{OUT}$  in Table 4.

If not using an output at the maximum output current, it is recommended to use an inductor value not to exceed 50% of the calculated inductor value with the maximum output current.

Note that the inductor must always have a higher rating than the maximum current because the current increases with decreasing inductance.

## Dynamic Voltage Scaling (DVS)

All four buck regulators support Dynamic Voltage Scaling. The dynamic output slew rate is 10V/ms (nominal). Note that it is not recommended to ramp up DVS (i.e. increase  $V_{OUT}$ ) at the maximum rated current. This may result in a premature over-current protection (OCP) event caused by the high inrush current due to the high slew rate of 10V/ms. As an example, consider Buck 4 of MxL7704-XQB operating at 1MHz with  $L=0.47\mu\text{H}$  and  $C_{OUT}(\text{effective}) = 210\mu\text{F}$ . The inrush current corresponding to DVS can be calculated from:

$$I_{INRUSH} = C_{OUT} \times \frac{\Delta V_{OUT}}{\Delta t}$$

$$I_{INRUSH} = 210\mu\text{F} \times (10\text{V/ms}) = 2.1\text{A}$$

The peak-to-peak inductor current ripple is 1.52A.

Therefore, peak inrush current is:

$$I_{INRUSH, PEAK} = 2.1\text{A} + (0.5 \times 1.52\text{A}) = 2.86\text{A}$$

Minimum current limit is 5.5A for Buck 4. Therefore, maximum permissible output current while using DVS is:

$$I_{OUT} = 5.5\text{A} - 2.86\text{A} = 2.64\text{A}$$

Similar analysis should be carried out to ensure that the inrush current of a large  $C_{OUT}$  does not result in a premature OCP.

## Analog to Digital Converter and Temperature Sensor

MxL7704 has a built in 8-bit Analog to Digital Converter (ADC) as well as a Temperature Sensor. The ADC has 3 analog inputs AN0, AN1 and TEMP. The AN0 and AN1 inputs are external analog signals that the user can apply for conversion. The TEMP input internally monitors the Temperature Sensor output. Temperature data can be read from register address 0x1B and is calculated according to the following:

$$\text{DECIMAL} = [(T_{\text{sensor}} - 25^\circ\text{C}) \times 1.06\text{LSB}/^\circ\text{C}] + 95$$

Where:

$T_{\text{sensor}}$  is the temperature of the internal sensor

1.06LSB/ $^\circ\text{C}$  is the nominal resolution of the DAC

Therefore, at an ambient of 25 $^\circ\text{C}$  the register should typically return a value of 95 (decimal), or 0x5F (hex) (when the four bucks are turned off to reduce internal heating).

Register addresses 0x1C and 0x1D contain the outputs corresponding to analog inputs AN0 and AN1 respectively. The ADC has a nominal Zero Error (offset) of typically +3 LSB. Therefore, an input voltage of 30mV is required to produce an output transition of 00 to 01. INL is calibrated at (1.75V+offset) and specified  $\pm 2\text{LSB}$ . For best ADC performance, the 5V<sub>SYS</sub> pin must be bypassed to AGND with a 10 $\mu\text{F}$ , 1 $\mu\text{F}$  and 0.1 $\mu\text{F}$  capacitor. The 0.1 $\mu\text{F}$  must be placed as close to the IC as possible. It is also recommended that a lowpass filter 0.1 $\mu\text{F}/100\Omega$  be used at AN0 and AN1 inputs.





## Register Information

### Slave I<sup>2</sup>C Address

| Device  | 7-Bit Address |
|---------|---------------|
| MxL7704 | 0x2D          |

### Register Map

Runtime registers may be changed through I<sup>2</sup>C

**Table 9: Register Map**

| Address | Register  | R/W                | Bit 7             | Bit 6       | Bit 5         | Bit 4    | Bit 3                    | Bit 2    | Bit 1       | Bit 0  |
|---------|---|--------------------|-------------------|-------------|---------------|----------|--------------------------|----------|-------------|--------|
| 0x00    | Revision ID                                       | R                  | Revision ID (7:0) |             |               |          |                          |          |             |        |
| 0x01    | ADC Enable  | R/W                |                   |             |               |          |                          |          |             | ADC EN |
| 0x02    | Phase Interleaving                                | R/W <sup>(1)</sup> | Buck 4[1:0]       |             | Buck 3[1:0]   |          | Buck 2[1:0]              |          | Buck 1[1:0] |        |
| 0x10    | Vout LDO  | R/W                | VLDO[7:0]         |             |               |          |                          |          |             |        |
| 0x11    | Vout Buck 1                                       | R/W                | VBuck1[7:0]       |             |               |          |                          |          |             |        |
| 0x12    | Vout Buck 2                                       | R/W                | VBuck2[7:0]       |             |               |          |                          |          |             |        |
| 0x13    | Vout Buck 3                                       | R/W                | VBuck3[7:0]       |             |               |          |                          |          |             |        |
| 0x14    | Vout Buck 4                                       | R/W                | VBuck4[7:0]       |             |               |          |                          |          |             |        |
| 0x15    | Buck Sequence Group Assignment                    | R/W                | Buck 4[1:0]       |             | Buck 3[1:0]   |          | Buck 2[1:0]              |          | Buck 1[1:0] |        |
| 0x16    | LDO Sequence Group Assignment and Channel Enables | R/W                | LDO[1:0]          |             |               | EN4      | EN3                      | EN2      | EN1         | ENL    |
| 0x17    | SEQ EN Assign and PG1 Routing                     | R/W                | EN Assign         |             |               | Buck 4   | Buck 3                   | Buck 2   | Buck 1      | LDO    |
| 0x18    | PG2 Routing                                       | R/W                |                   |             |               | Buck 4   | Buck 3                   | Buck 2   | Buck 1      | LDO    |
| 0x19    | Fault Actions, Down Sequencing, Frequency         | R/W                | Chip/Channel      | Soft Off EN | 78Ω discharge |          | FREQ[3:0] <sup>(1)</sup> |          |             |        |
| 0x1A    | PGOOD and UV                                      | R                  | TWARN 105C        | UV Flag     | UV Current    | PG Buck4 | PG Buck3                 | PG Buck2 | PG Buck1    | PG LDO |
| 0x1B    | Temp  | R                  | Temp[7:0]         |             |               |          |                          |          |             |        |
| 0x1C    | ADC0  | R                  | ADC1[7:0]         |             |               |          |                          |          |             |        |
| 0x1D    | ADC1  | R                  | ADC2[7:0]         |             |               |          |                          |          |             |        |

NOTE:

1. Must not be written dynamically.

## Default Values

**Table 10: Default Values**

| Address | Register  | Default Value -AQB | Default Value -XQB |
|---------|---|--------------------|--------------------|
| 0x00    | Revision ID                                       | 0xA0               |                    |
| 0x01    | ADC Enable  | 0x01               |                    |
| 0x02    | Phase Interleaving                                | 0xE4               |                    |
| 0x10    | Vout LDO  | 0xA5<br>3.3V       | 0xA5<br>3.3V       |
| 0x11    | Vout Buck 1                                       | 0xA5<br>3.3V       | 0xA5<br>3.3V       |
| 0x12    | Vout Buck 2                                       | 0x5A<br>1.8V       | 0x5A<br>1.8V       |
| 0x13    | Vout Buck 3                                       | 0xD8<br>1.35V      | 0xD8<br>1.35V      |
| 0x14    | Vout Buck 4                                       | 0xC0<br>1.20V      | 0x88<br>0.85V      |
| 0x15    | Buck Sequence Group Assignment                    | 0xF9               | 0x3B               |
| 0x16    | LDO Sequence Group Assignment and Channel Enables | 0x1F               | 0xDF               |
| 0x17    | SEQ EN Assign and PG1 Routing                     | 0x44               | 0x40               |
| 0x18    | PG2 Routing                                       | 0x1A               | 0x1E               |
| 0x19    | Fault Actions, Down Sequencing, Frequency         | 0xE9               | 0xE4               |
| 0x1A    | PGOOD and UV                                      | 0x7F               | 0x7F               |

## Register Descriptions

### V<sub>OUT</sub> LDO (0x10) – Read/Write

| Bit | Description   |
|-----|---|
| 7:0 | VLDO[7:0] Output voltage setting. 20mV resolution.<br>The device will NAK if the output has not completed the prior voltage change and a second voltage change is requested on this channel. See “ <a href="#">I<sup>2</sup>C Operation</a> ” section for details.<br>Although this register will accept any value in its range of 0x00 to 0xFF, the output voltage accuracy is not guaranteed outside the range stated in the electrical table. Note that 0xBF corresponds to 3.6V, the maximum LDO voltage. |

### V<sub>OUT</sub> Buck 1 (0x11) – Read/Write

| Bit | Description   |
|-----|---|
| 7:0 | VBuck1[7:0] Buck 1 Output voltage setting. 20mV resolution.<br>The device will NAK if the output has not completed the prior voltage change and a second voltage change is requested on this channel. See “ <a href="#">I<sup>2</sup>C Operation</a> ” section for details.<br>Although this register will accept any value in its range of 0x00 to 0xFF, the output voltage accuracy is not guaranteed outside the range stated in the electrical table. Note that 0xBF corresponds to 3.6V, the maximum Buck 1 voltage. |

### V<sub>OUT</sub> Buck 2 (0x12) – Read/Write

| Bit | Description   |
|-----|---|
| 7:0 | VBuck2[7:0] Output voltage setting. 20mV resolution.<br>The device will NAK if the output has not completed the prior voltage change and a second voltage change is requested on this channel. See “ <a href="#">I<sup>2</sup>C Operation</a> ” section for details.<br>Although this register will accept any value in its range of 0x00 to 0xFF, the output voltage accuracy is not guaranteed outside the range stated in the electrical table. Note that 0x60 corresponds to 1.92V, the maximum Buck 2 voltage.<br>Minimum controllable output voltage is a function of the selected frequency and the minimum on-time (see Table 6). |

### V<sub>OUT</sub> Buck 3 (0x13) – Read/Write

| Bit | Description  |
|-----|--|
| 7:0 | VBuck3[7:0] Output voltage setting. 6.25mV resolution.<br>The device will NAK if the output has not completed the prior voltage change and a second voltage change is requested on this channel. See “ <a href="#">I<sup>2</sup>C Operation</a> ” section for details.<br>Although this register will accept any value in its range of 0x00 to 0xFF, the output voltage accuracy is not guaranteed outside the range stated in the electrical table. Note that 0xFF corresponds to 1.59375V, the maximum Buck 3 voltage.<br>Minimum controllable output voltage is a function of the selected frequency and the minimum on-time (see Table 6). |

V<sub>OUT</sub> Buck 4 (0x14) – Read/Write

| Bit | Description  |
|-----|--|
| 7:0 | VBuck4[7:0] Output voltage setting. 6.25mV resolution.<br>The device will NAK if the output has not completed the prior voltage change and a second voltage change is requested on this channel. See " <a href="#">I<sup>2</sup>C Operation</a> " section for details.<br>Although this register will accept any value in its range of 0x00 to 0xFF, the output voltage accuracy is not guaranteed outside the range stated in the electrical table. Note that 0xDF corresponds to 1.39375V, the maximum Buck 4 voltage.<br>Minimum controllable output voltage is a function of the selected frequency and the minimum on-time (see Table 6). |

## Buck Sequence Group Assignment (0x15) – Read/Write

| Bit | Description |
|-----|-------------|
| 7:6 | Buck 4      |
| 5:4 | Buck 3      |
| 3:2 | Buck 2      |
| 1:0 | Buck 1      |

Sequencing. 2 bits assigns each buck regulator to a sequencing group. Sequencing powers up each group 00, 01, 10 and 11 in order and in power down sequencing, the order is reversed. Skipping a value has no effect on the power up.

## LDO Sequence Group Assignment and Channel Enables (0x16) – Read/Write

| Bit | Description |
|-----|-------------|
| 7:6 | LDO         |
| 5   | Unused      |
| 4   | EN4         |
| 3   | EN3         |
| 2   | EN2         |
| 1   | EN1         |
| 0   | ENL         |

Sequencing. 2 bits assigns LDO to a sequencing group. Skipping a value has no effect on the power up.

Channel enable. If OTP value 0 and assigned a slot in the sequencing, sequencing will stop at this device. To complete power up sequencing, the host must change this bit to 1.

## SEQ EN Assign and PG1 Routing (0x17) – Read/Write

| Bit | Description   |
|-----|---|
| 7:6 | SEQ EN Assign<br>Assigns the SEQ EN input to the sequence group. It is logically ANDed to the prior groups PGOOD. For example, if assigned to group 00, then the chip would enable, but no outputs would power on until SEQ EN is logic HIGH. This configuration might prove helpful when debugging system sequencing requirements. |
| 5   | unused  |
| 4   | PG1 Routing Buck 4<br>1: Will select the PG status of that output and AND it with others selected   |
| 3   | PG1 Routing Buck 3<br>1: Will select the PG status of that output and AND it with others selected   |
| 2   | PG1 Routing Buck 2<br>1: Will select the PG status of that output and AND it with others selected   |
| 1   | PG1 Routing Buck 1<br>1: Will select the PG status of that output and AND it with others selected   |
| 0   | PG1 Routing LDO<br>1: Will select the PG status of that output and AND it with others selected  |

## PG2 Routing (0x18) – Read/Write

| Bit | Description   |
|-----|---|
| 7:5 | unused  |
| 4   | PG2 Routing Buck 4<br>1: Will select the PG status of that output and AND it with others selected |
| 3   | PG2 Routing Buck 3<br>1: Will select the PG status of that output and AND it with others selected |
| 2   | PG2 Routing Buck 2<br>1: Will select the PG status of that output and AND it with others selected |
| 1   | PG2 Routing Buck 1<br>1: Will select the PG status of that output and AND it with others selected |
| 0   | PG2 Routing LDO<br>1: Will select the PG status of that output and AND it with others selected    |

## Fault Actions, Down Sequencing, Frequency (0x19) – Read/Write

| Bit | Description   |
|-----|---|
| 7   | Chip/Channel<br>0: Only the individual channel resets during a fault on that channel<br>1: Whole chip resets if any output faults   |
| 6   | Soft Off<br>0: disabled – immediate tri-state when shut down<br>1: will slew output to Ref DAC = 0V and then tri-state  |
| 5   | 78Ω discharge<br>0: disabled (this option may leave excessive charge on output capacitors and is NOT recommended)<br>1: connects 78Ω to ground when channel is shut down. If Bit 6 = 1, 78Ω will be connected once Ref DAC = 0V |
| 4   | Reserved  |
| 3:0 | FREQ<br>Switching Frequency 1MHz - 2.1MHz, 90kHz resolution 4-bit   |

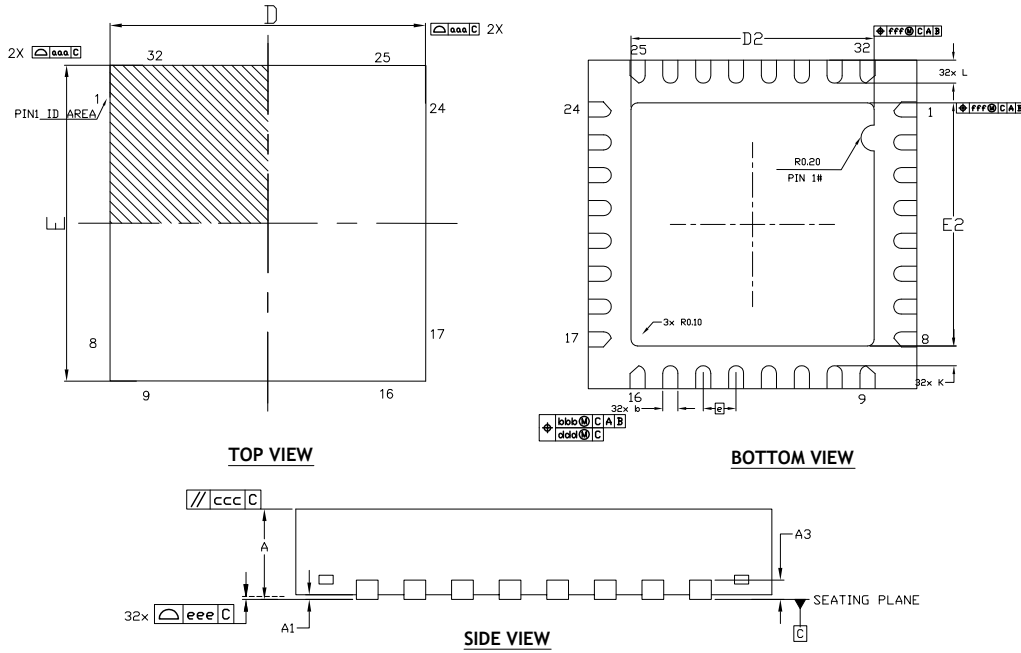
## PGOOD and UV (0x1A) – Read/Write

| Bit | Description   |
|-----|---|
| 7   | Will be set as the temperature warning flag if the device temperature goes over 105°C. When the device temperature drops below threshold, this bit will be cleared.   |
| 6   | UV Flag<br>Indicates the input voltage once fell below 4.63V after having once risen above it. If this bit is 0 and bit 5 is 1, it means the input has never risen above the UV threshold. <b>This is a sticky flag. It can ONLY be cleared by writing 1 to this bit. The register will update any cleared value every 250µs.</b> |
| 5   | Provides current status of 5V <sub>SYS</sub> pin.   |
| 4   | PG Buck 4<br>0: Output lower than 94% of target V <sub>OUT</sub> (nominal)  |
| 3   | PG Buck 3<br>0: Output lower than 94% of target V <sub>OUT</sub> (nominal)  |
| 2   | PG Buck 2<br>0: Output lower than 94% of target V <sub>OUT</sub> (nominal)  |
| 1   | PG Buck 1<br>0: Output lower than 94% of target V <sub>OUT</sub> (nominal)  |
| 0   | PG LDO<br>0: Output lower than 94% of target V <sub>OUT</sub> (nominal)   |

Notice: Writing to this register **ONLY** affects UV Flag (bit 6) of this register in the meaning of clearing the flag.

# Mechanical Dimensions

5mm x 5mm 32-Pin QFN



| DIM SYMBOL | MIN      | NOM     | MAX  |
|------------|----------|---------|------|
| A          | 0.80     | 0.85    | 0.90 |
| A1         | 0.00     | 0.02    | 0.05 |
| A3         | ---      | 0.20Ref | ---  |
| b          | 0.18     | 0.23    | 0.28 |
| D          | 5.00 BSC |         |      |
| E          | 5.00 BSC |         |      |
| e          | 0.50 BSC |         |      |
| D2         | 3.55     | 3.65    | 3.75 |
| E2         | 3.55     | 3.65    | 3.75 |
| L          | 0.30     | 0.35    | 0.40 |
| K          | 0.20     | —       | —    |
| aaa        | 0.15     |         |      |
| bbb        | 0.10     |         |      |
| ccc        | 0.10     |         |      |
| ddd        | 0.05     |         |      |
| eee        | 0.08     |         |      |
| fff        | 0.10     |         |      |
| N          | 32       |         |      |

**TERMINAL DETAILS**

- ALL DIMENSIONS ARE IN MILLIMETERS, ANGLES ARE IN DEGREES.
- DIMENSIONS AND TOLERANCE PER JEDEC MD-220.

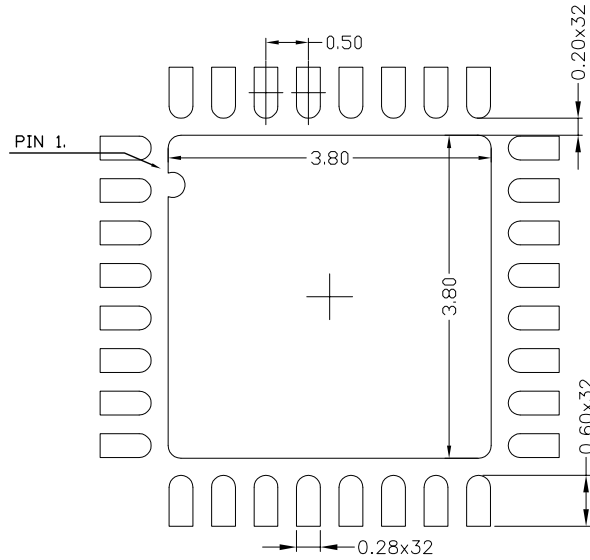
Drawing No.: POD-0000104

Revision: B.1

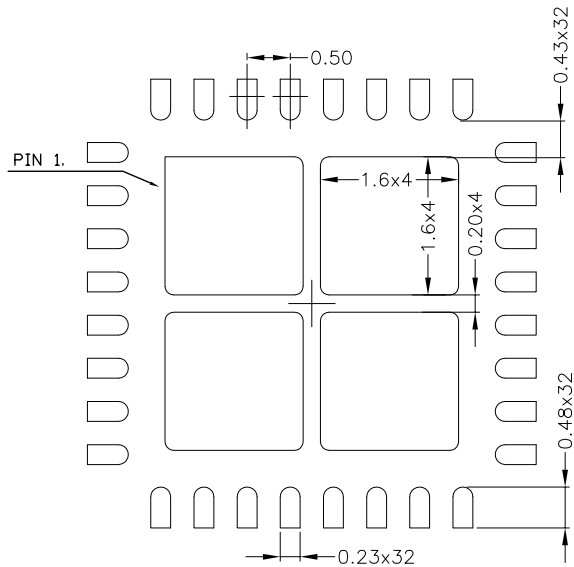
Figure 26: Mechanical Dimensions

# Recommended Land Pattern and Stencil

5mm x 5mm 32-Pin QFN



**TYPICAL RECOMMENDED LAND PATTERN**



**TYPICAL RECOMMENDED STENCIL**

Drawing No.: POD-00000104

Revision: B.1

**Figure 27: Recommended Land Pattern and Stencil**

# Ordering Information

**Table 11: Ordering Information<sup>(1)</sup>**

| Ordering Part Number | Operating Temperature Range    | Lead-Free          | Package                         | Packaging Method | OTP Configuration |
|----------------------|--------------------------------|--------------------|---------------------------------|------------------|-------------------|
| MxL7704-AQB-T        | -40°C ≤ T <sub>J</sub> ≤ 125°C | Yes <sup>(2)</sup> | 5mm x 5mm x 0.9mm<br>32-pin QFN | Tray             | See Table 10      |
| MxL7704-AQB-R        |                                |                    |                                 | Tape and Reel    |                   |
| MxL7704-XQB-T        |                                |                    |                                 | Tray             |                   |
| MxL7704-XQB-R        |                                |                    |                                 | Tape and Reel    |                   |
| MxL7704-A-EVB        | MxL7704-AQB Evaluation Board   |                    |                                 |                  |                   |
| MxL7704-X-EVB        | MxL7704-XQB Evaluation Board   |                    |                                 |                  |                   |

**NOTES:**

1. Refer to [www.exar.com/MxL7704](http://www.exar.com/MxL7704) for most up-to-date Ordering Information
2. Visit [www.exar.com](http://www.exar.com) for additional information on Environmental Rating.



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