



# ZVN4210A

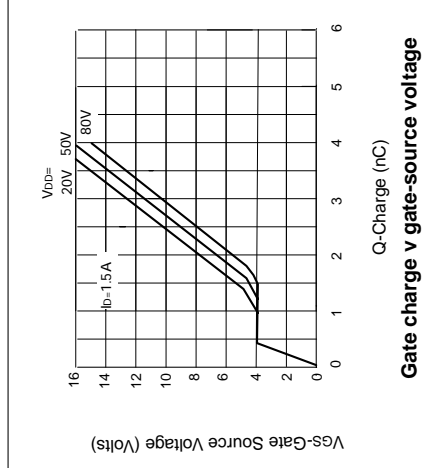
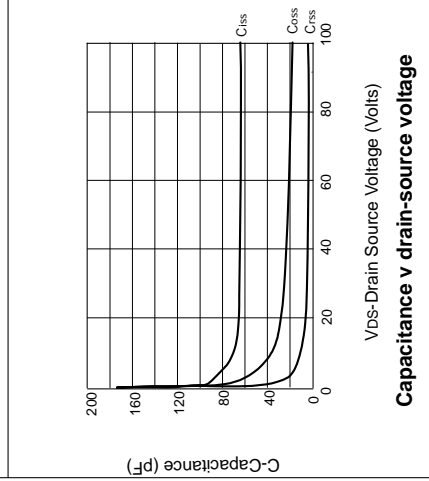
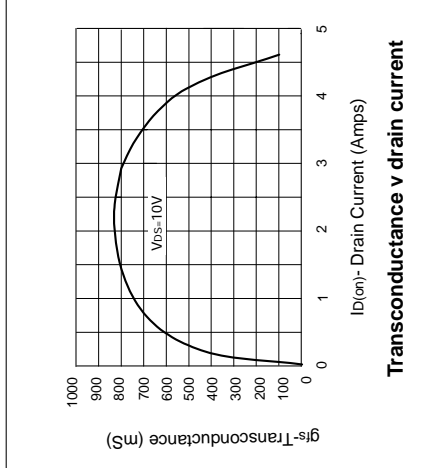
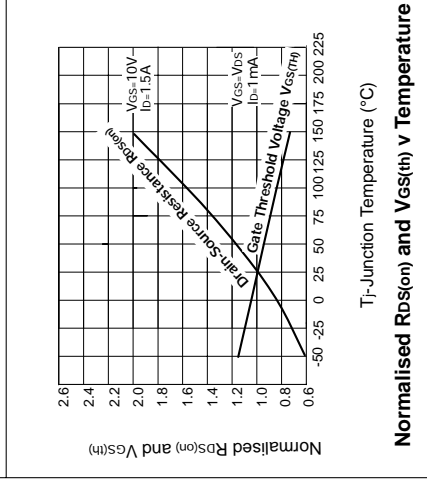
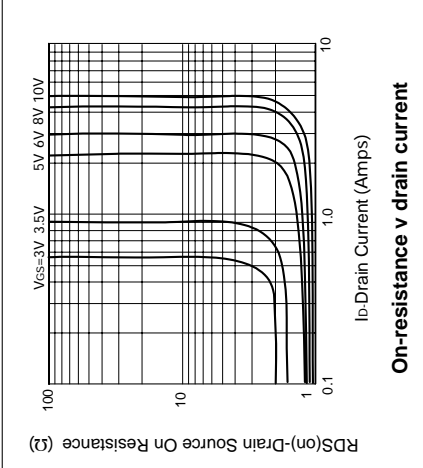
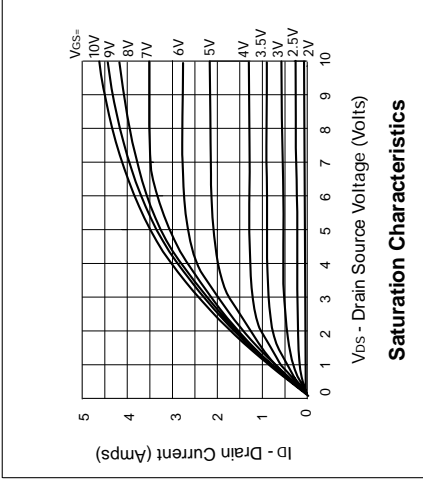
## N-CHANNEL ENHANCEMENT MODE VERTICAL DMOS FET

ISSUE 2 – MARCH 94

### FEATURES

- \* 100 Volt  $V_{DS}$
- \*  $R_{DS(on)} = 1.5\Omega$
- \* Spice model available

### TYPICAL CHARACTERISTICS



### ABSOLUTE MAXIMUM RATINGS

PARAMETER
Drain-Source Voltage
Continuous Drain Current at $T_{amb}=25^{\circ}$
Pulsed Drain Current
Gate-Source Voltage
Power Dissipation at $T_{amb}=25^{\circ}$ C
Operating and Storage Temperature Range

### ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL
Drain-Source Breakdown Voltage	$BV_{DSS}$
Gate-Source Threshold Voltage	$V_{GS(th)}$
Gate-Body Leakage	$I_{GSS}$
Zero Gate Voltage Drain Current	$I_{DSS}$
On-State Drain Current (1)	$I_{D(on)}$
Static Drain-Source On-State Resistance (1)	$R_{DS(on)}$
Forward Transconductance(1)(2)	$g_{fs}$
Input Capacitance (2)	$C_{iss}$
Common Source Output Capacitance (2)	$C_{oss}$
Reverse Transfer Capacitance (2)	$C_{rss}$
Turn-On Delay Time (2)(3)	$t_{d(on)}$
Rise Time (2)(3)	$t_r$
Turn-Off Delay Time (2)(3)	$t_{d(off)}$
Fall Time (2)(3)	$t_f$

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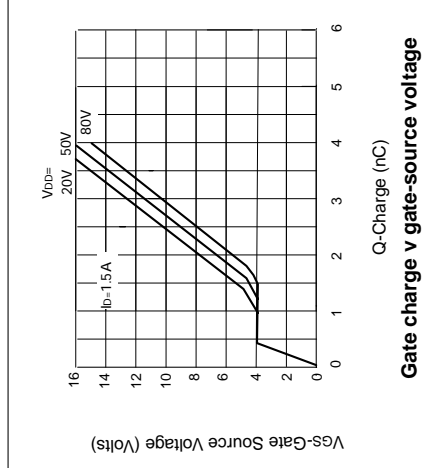
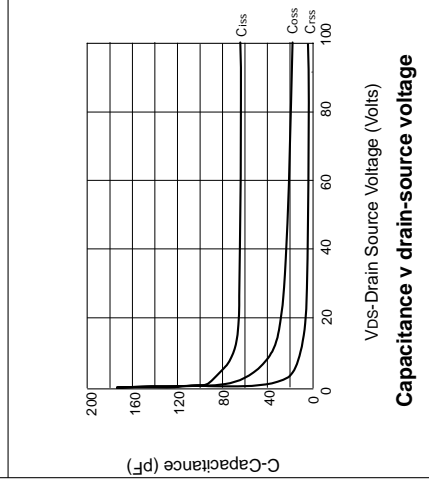
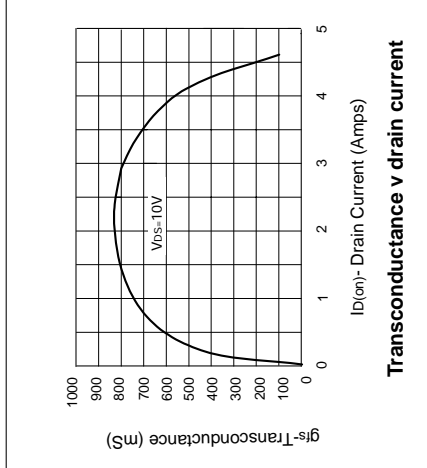
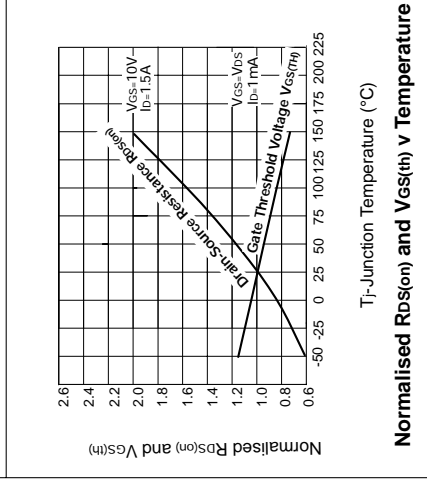
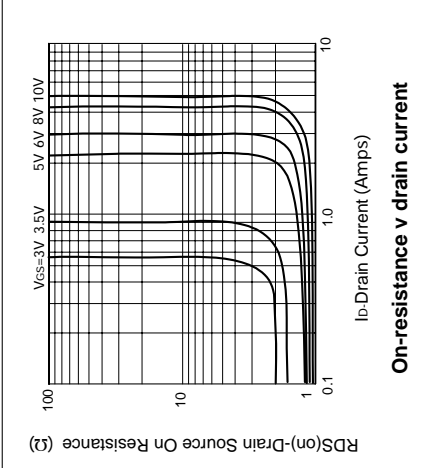
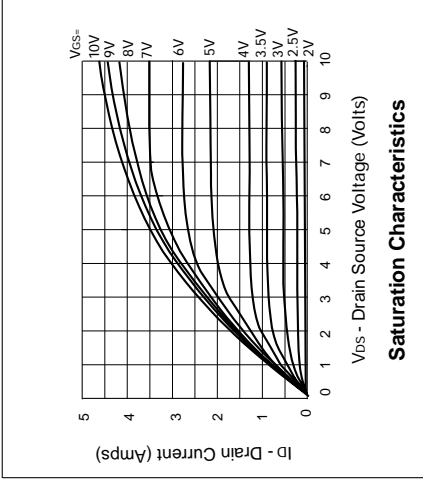
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Rise Time (2)(3)	$t_r$
Turn-Off Delay Time (2)(3)	$t_{d(off)}$
Fall Time (2)(3)	$t_f$

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- ⊖ [Diodes Incorporated Information](#)

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