THE DATASHEET OF

A3924KLVTR-T

www.win-source.net 0086-755-83957316

A3924

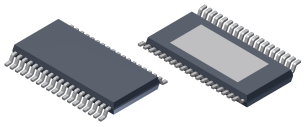
Automotive Full-Bridge MOSFET Driver

FEATURES AND BENEFITS

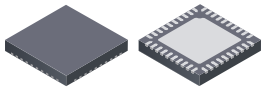
- Full-bridge MOSFET driver
- Bootstrap gate drive for N-channel MOSFET bridge
- Cross-conduction protection with adjustable dead time
- Charge pump for low supply voltage operation
- Programmable gate drive voltage
- 5.5 to 50 V supply voltage operating range
- Integrated logic supply
- Two integrated current sense amplifiers
- SPI-compatible serial interface
- Bridge control by direct logic inputs or serial interface
- TTL-compatible logic inputs
- Open-load detection
- Extensive programmable diagnostics
- Diagnostic verification
- Safety-assist features

PACKAGES:

38-Pin eTSSOP
(suffix LV)



40-Terminal eQFN
(suffix EV)



Not to scale

DESCRIPTION

The A3924 is an N-channel power MOSFET driver capable of controlling MOSFETs connected in a full-bridge (H-bridge) arrangement and is specifically designed for automotive applications with high-power inductive loads, such as brush DC motors solenoids and actuators.

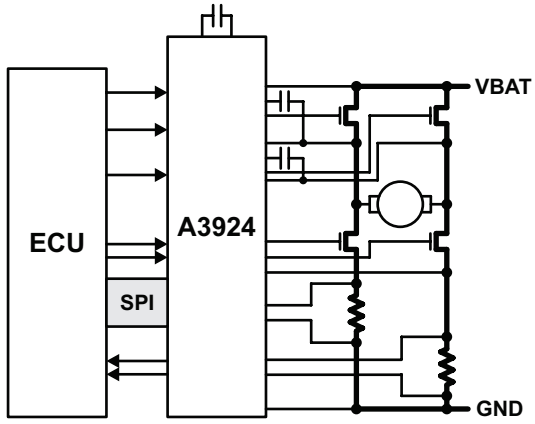
A unique charge pump regulator provides the programmable gate drive voltage for battery voltages down to 7 V and allows the A3924 to operate with a reduced gate drive, down to 5.5 V. A bootstrap capacitor is used to provide the above-battery supply voltage required for N-channel MOSFETs.

The full bridge can be controlled by independent logic level inputs or through the SPI-compatible serial interface. The external power MOSFETs are protected from shoot-through by programmable dead time.

Integrated diagnostics provide indication of multiple internal faults, system faults, and power bridge faults, and can be configured to protect the power MOSFETs under most short-circuit conditions. For safety-critical systems, the integrated diagnostic operation can be verified under control of the serial interface.

In addition to providing full access to the bridge control, the serial interface is also used to alter programmable settings such as dead time, VDS threshold, and fault blank time. Detailed diagnostic information can be read through the serial interface.

The A3924 is supplied in a 38-pin eTSSOP (suffix 'LV') and a 40-terminal eQFN package (suffix 'EV'). Both packages are lead (Pb) free with 100% matte-tin leadframe plating.



Typical Application – Functional Block Diagram

SELECTION GUIDE

Part Number	Packing [1]	Package
A3924KEVSR-J [2]	6000 pieces per reel	6 mm × 6 mm, 1.6 mm nominal height, wettable flank 40-terminal eQFN with exposed thermal pad
A3924KLVTR-T	4000 pieces per reel	9.7 mm × 4.4 mm, 1.2 mm nominal height 38-lead eTSSOP with exposed thermal pad

[1] Contact Allegro™ for additional packing options.
[2] Part variant A3924KEVSR-J is in production but have been determined to be LAST TIME BUY. This classification indicates that the product is obsolete and notice has been given. Sale of this device is currently restricted to existing customer applications. The device should not be purchased for new design applications because of obsolescence in the near future. Samples are no longer available. Status change date: April 1, 2024. Last-time buy date: July 31, 2024. Suggested replacement: A3922KLPTR-T.

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SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS [1][2]

Characteristic	Symbol	Notes	Rating	Unit
Load Supply Voltage	V_{BB}		–0.3 to 50	V
Analog Ground		AGND (Connect AGND to GND at package)	–0.1 to 0.1	V
Logic Supply Regulator Terminals	V_3	V3, V3BD	–0.3 to 6	V
Pumped Regulator Terminal	V_{REG}	VREG	–0.3 to 16	V
Charge Pump Capacitor Low Terminal	V_{CP1}	CP1	–0.3 to 16	V
Charge Pump Capacitor High Terminal	V_{CP2}	CP2	V_{CP1} – 0.3 to V_{REG} + 0.3	V
Battery Compliant Logic Input Terminals	V_{IB}	HA, HBn, LAn, LB, RESETn, ENABLE	–0.3 to 50	V
Logic Input Terminals	V_I	STRn, SCK, SDI	–0.3 to 6	V
Logic Output Terminals	V_O	SDO, SAL, SBL	–0.3 to 6	V
Diagnostic Output Terminal	V_{DIAG}	DIAG	–0.3 to 50	V
Sense Amplifier Inputs	V_{CSI}	CSPA, CSMA, CSPB, CSMB	–4 to 6.5	V
Sense Amplifier Output	V_{CSO}	CSOA, CSOB	–0.3 to 6	V
Bridge Drain Monitor Terminals	V_{BRG}	VBRG	–5 to 55	V
Bootstrap Supply Terminals	V_{CX}	CA, CB	–0.3 to V_{REG} + 50	V
High-Side Gate Drive Output Terminals	V_{GHX}	GHA, GHB	V_{CX} – 16 to V_{CX} + 0.3	V
Motor Phase Terminals	V_{SX}	SA, SB	V_{CX} – 16 to V_{CX} + 0.3	V
Low-Side Gate Drive Output Terminals	V_{GLX}	GLA, GLB	V_{REG} – 16 to 16	V
Bridge Low-Side Source Terminals	V_{LSS}	LSSA, LSSB	V_{REG} – 16 to V_{REG} + 0.3	V
Ambient Operating Temperature Range	T_A	Limited by power dissipation	–40 to 150	°C
Maximum Continuous Junction Temperature	$T_{J(max)}$		165	°C
Transient Junction Temperature	T_{Jt}	Overtemperature event not exceeding 10 seconds, lifetime duration not exceeding 10 hours, guaranteed by design characterization.	180	°C
Storage Temperature Range	T_{stg}		–55 to 150	°C

[1] With respect to GND. Ratings apply when no other circuit operating constraints are present.
[2] Lowercase “x” in pin names and symbols indicates a variable sequence character.

THERMAL CHARACTERISTICS: May require derating at maximum conditions; see Power Derating section

Characteristic	Symbol	Test Conditions [3]	Value	Unit
Package Thermal Resistance	$R_{\theta JA}$	EV package, 4-layer PCB based on JEDEC standard	23	°C/W
		EV package, 2-layer PCB with 3.8 in^2 copper each side	44	°C/W
		LV package, 4-layer PCB based on JEDEC standard	28	°C/W
		LV package, 2-layer PCB with 3.8 in^2 copper each side	38	°C/W
	$R_{\theta JP}$	EV package	2	°C/W
		LV package	2	°C/W

[3] Additional thermal information available on the Allegro website

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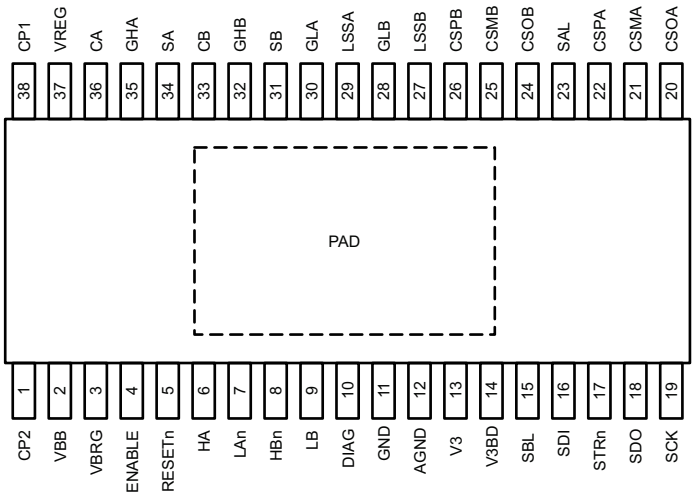
PINOUT DIAGRAMS AND TERMINAL LISTS



Package LP, 38-Pin eTSSOP Pinout Diagram

Terminal List Table

Terminal Name	Terminal Number	Terminal Description
AGND	12	Analog ground
CA	36	Phase A bootstrap capacitor
CB	33	Phase B bootstrap capacitor
CP1	38	Pump capacitor
CP2	1	Pump capacitor
CSMA	21	Phase A current sense amp – input
CSMB	25	Phase B current sense amp – input
CSOA	20	Phase A current sense amp output
CSOB	24	Phase B current sense amp output
CSPA	22	Phase A current sense amp + input
CSPB	26	Phase B current sense amp + input
DIAG	10	Programmable diagnostic output
ENABLE	4	Output enable
GHA	35	Phase A high-side gate drive
GHB	32	Phase B high-side gate drive
GLA	30	Phase A low-side gate drive
GLB	28	Phase B low-side gate drive
GND	11	Digital ground
HA	6	Phase A HS control
HBn	8	Phase B HS control

Terminal Name	Terminal Number	Terminal Description
LAn	7	Phase A LS control
LB	9	Phase B LS control
LSSA	29	Phase A low-side source
LSSB	27	Phase B low-side source
RESETn	5	Standby mode control
SA	34	Phase A motor connection
SAL	23	Phase A logic output
SB	31	Phase B motor connection
SBL	15	Phase B logic output
SCK	19	Serial clock input
SDI	16	Serial data input
SDO	18	Serial data output
STRn	17	Serial strobe (chip select) input
V3	13	Logic regulator reference
V3BD	14	Logic regulator bypass NPN base drive
VBB	2	Main power supply
VBRG	3	High-side drain voltage sense
VREG	37	Gate drive supply output
PAD	–	Thermal pad; connect to GND

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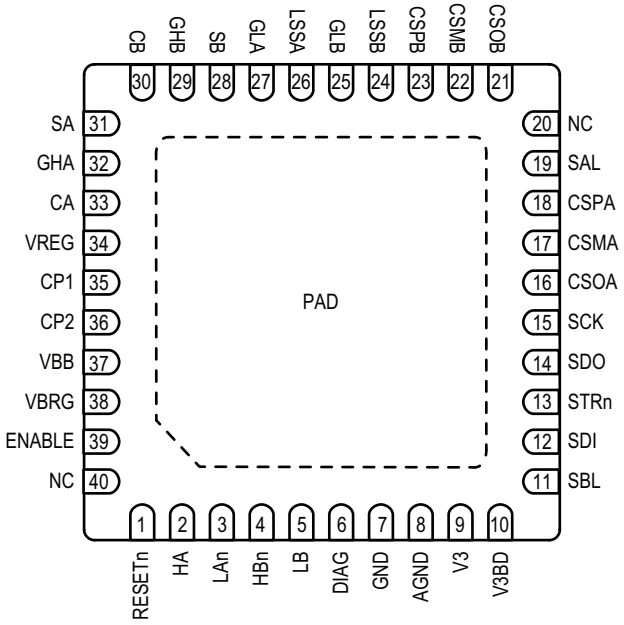

Package EV, 40-Pin eQFN Pinout Diagram

Terminal List Table

Terminal Name	Terminal Number	Terminal Description
AGND	8	Analog ground
CA	33	Phase A bootstrap capacitor
CB	30	Phase B bootstrap capacitor
CP1	35	Pump capacitor
CP2	36	Pump capacitor
CSMA	17	Phase A current sense amp – input
CSMB	22	Phase B current sense amp – input
CSOA	16	Phase A current sense amp output
CSOB	21	Phase B current sense amp output
CSPA	18	Phase A current sense amp + input
CSPB	23	Phase B current sense amp + input
DIAG	6	Programmable diagnostic output
ENABLE	39	Output enable
GHA	32	Phase A high-side gate drive
GHB	29	Phase B high-side gate drive
GLA	27	Phase A low-side gate drive
GLB	25	Phase B low-side gate drive
GND	7	Digital ground
HA	2	Phase A HS control
HBn	4	Phase B HS control

Terminal Name	Terminal Number	Terminal Description
LAn	3	Phase A LS control
LB	5	Phase B LS control
LSSA	26	Phase A low-side source
LSSB	24	Phase B low-side source
NC	20, 40	No connect
RESETn	1	Standby mode control
SA	31	Phase A motor control
SB	28	Phase B motor control
SAL	19	Phase A logic output
SBL	11	Phase B logic output
SCK	15	Serial clock input
SDI	12	Serial data input
SDO	14	Serial data output
STRn	13	Serial strobe (chip select) input
V3	9	Logic regulator reference
V3BD	10	Logic regulator bypass NPN base drive
VBB	37	Main power supply
VBRG	38	High-side drain voltage sense
VREG	34	Gate drive supply output
PAD	–	Thermal pad; connect to GND

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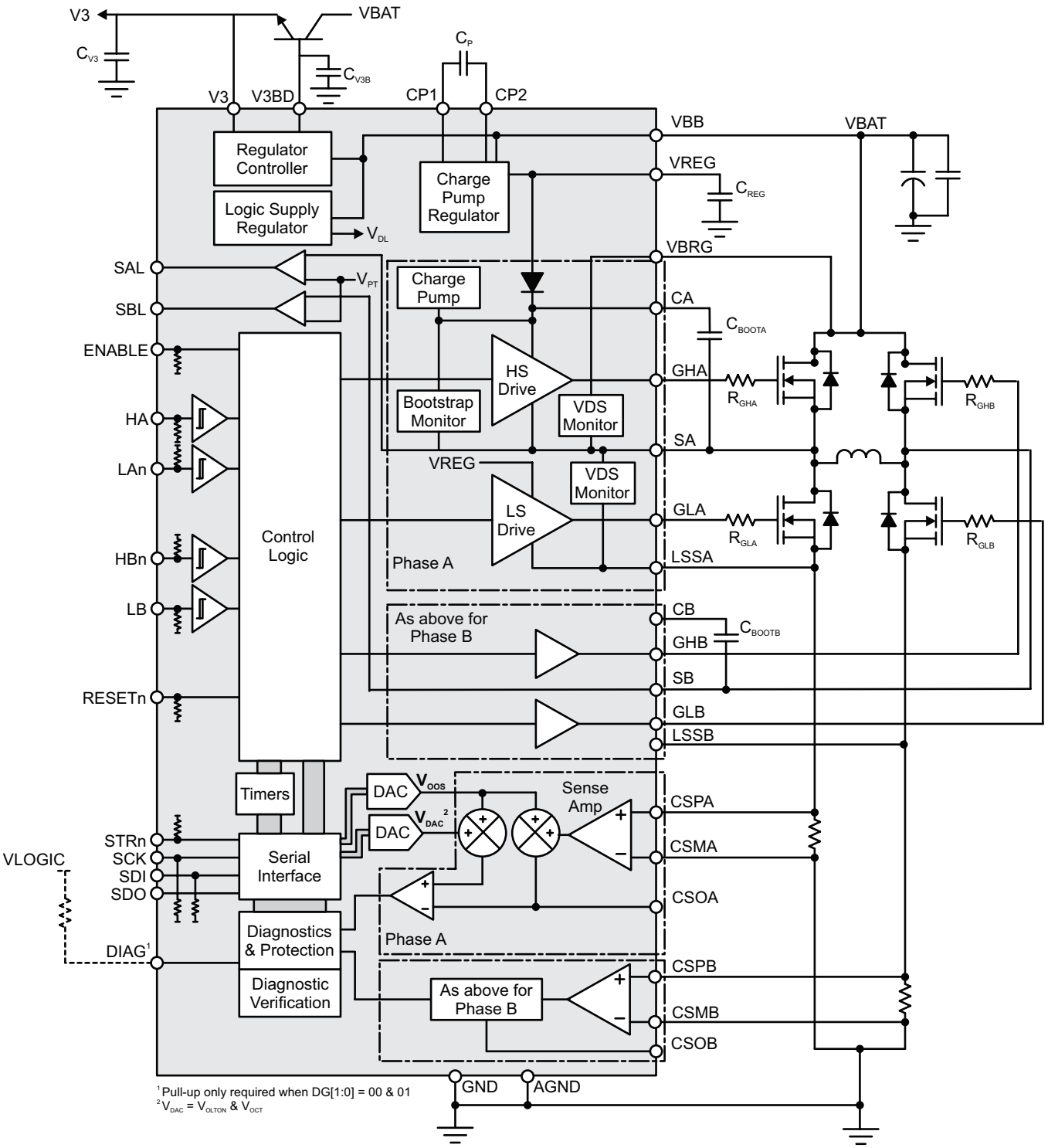

Functional Block Diagram

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ELECTRICAL CHARACTERISTICS: Valid at T_J = –40°C to 150°C, V_{BB} = 5.5 to 50 V, unless otherwise specified

Characteristic	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
SUPPLY AND REFERENCE							
VBB Functional Operating Range	V_{BB}	Operating; outputs active		6	–	50	V
		Operating; outputs disabled		5.5	–	50	V
		No unsafe states		0	–	50	V
VBB Quiescent Current	I_{BBQ}	RESETn = high, V_{BB} = 12 V, All gate drive outputs low		–	10	27	mA
	I_{BBS}	RESETn ≤ 300 mV, sleep mode		–	–	30	µA
Internal Logic Supply Regulator Voltage	V_{DL}			3.1	3.3	3.5	V
V3 Regulator Reference Voltage	V_3			3.1	3.3	3.5	V
V3BD Current Drive Output	I_{3BD}			–	–	–2	mA
VREG Output Voltage, VRG = 0	V_{REG}	EV package variant	V_{BB} ≥ 9 V, I_{VREG} = 0 to 27 mA	7.4	8	8.5	V
			7.5 V ≤ V_{BB} < 9 V, I_{VREG} = 0 to 20 mA	7.4	8	8.5	V
			6 V ≤ V_{BB} < 7.5 V, I_{VREG} = 0 to 10 mA	7.4	8	8.5	V
			5.5 V ≤ V_{BB} < 6 V, I_{VREG} ≤ 6 mA	7.4	8	8.5	V
		LV package variant	V_{BB} ≥ 9 V, I_{VREG} = 0 to 27 mA	7.5	8	8.5	V
			7.5 V ≤ V_{BB} < 9 V, I_{VREG} = 0 to 20 mA	7.5	8	8.5	V
			6 V ≤ V_{BB} < 7.5 V, I_{VREG} = 0 to 10 mA	7.5	8	8.5	V
			5.5 V ≤ V_{BB} < 6 V, I_{VREG} ≤ 6 mA	7.5	8	8.5	V
VREG Output Voltage, VRG = 1	V_{REG}	V_{BB} ≥ 9 V, I_{VREG} = 0 to 25 mA		9	13	13.8	V
		7.5 V ≤ V_{BB} < 9 V, I_{VREG} = 0 to 18 mA		9	13	13.8	V
		6 V ≤ V_{BB} < 7.5 V, I_{VREG} = 0 to 10 mA		7.9	–	–	V
		5.5 V ≤ V_{BB} < 6 V, I_{VREG} ≤ 5 mA		7.9	9.5	–	V
Bootstrap Diode Forward Voltage	V_{fBOOT}	I_D = 10 mA		0.4	0.7	1.0	V
		I_D = 100 mA		1.5	2.2	2.8	V
Bootstrap Diode Resistance	r_D	$r_{D(100\ mA)} = (V_{fBOOT(150\ mA)} - V_{fBOOT(50\ mA)}) / 100\ mA$		6	11	25	Ω
Bootstrap Diode Current Limit	I_{DBOOT}			250	500	750	mA
Top-Off Charge Pump Current Limit	I_{TOCPM}			–	100	–	µA
High-Side Gate Drive Static Load Resistance	R_{GSH}			250	–	–	kΩ
System Clock Period	t_{OSC}			42.5	50	57.5	ns

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ELECTRICAL CHARACTERISTICS (continued): Valid at T_J = –40°C to 150°C, V_{BB} = 5.5 to 50 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
GATE OUTPUT DRIVE						
Turn-On Time	t_r	C_{LOAD} = 10 nF, 20% to 80%	–	190	–	ns
Turn-Off Time	t_f	C_{LOAD} = 10 nF, 80% to 20%	–	120	–	ns
Pull-Up On-Resistance	$R_{DS(on)UP}$	T_J = 25°C, I_{GH} = –150 mA [1]	5	8	11	Ω
		T_J = 150°C, I_{GH} = –150 mA [1]	10	15	20	Ω
Pull-Down On-Resistance	$R_{DS(on)DN}$	T_J = 25°C, I_{GL} = 150 mA	1.5	2.4	4	Ω
		T_J = 150°C, I_{GL} = 150 mA	2.9	4	6	Ω
GHx Output Voltage High	V_{GHH}	Bootstrap capacitor fully charged	V_{CX} – 0.2	–	–	V
GHx Output Voltage Low	V_{GHL}	–10 µA [1] < I_{GH} < 10 µA	–	–	V_{SX} + 0.3	V
GLx Output Voltage High	V_{GLH}		V_{REG} – 0.2	–	–	V
GLx Output Voltage Low	V_{GLL}	–10 µA [1] < I_{GL} < 10 µA	–	–	V_{LSS} + 0.3	V
Gate-Source Voltage – MOSFET On	V_{GSon}	No faults present	V_{ROFF}	–	V_{REG}	V
GHx Passive Pull-Down	R_{GHPD}	V_{GHx} – V_{Sx} < 0.3 V	–	950	–	kΩ
GLx Passive Pull-Down	R_{GLPD}	V_{GLx} – V_{LSS} < 0.3 V	–	950	–	kΩ
Turn-Off Propagation Delay	$t_{P(off)}$	Input Change to unloaded gate output change (Figure 3), DT[5:0]=0	60	90	140	ns
Turn-On Propagation Delay	$t_{P(on)}$	Input Change to unloaded gate output change (Figure 3), DT[5:0]=0	50	80	130	ns
Propagation Delay Matching (Phase-to-Phase)	Δt_{PP}	Same state change, DT[5:0]=0	–	5	15	ns
Propagation Delay Matching (On-to-Off)	Δt_{OO}	Single phase, DT[5:0]=0	–	15	30	ns
Propagation Delay Matching (GHx-to-GLx)	Δt_{HL}	Same state change, DT[5:0]=0	–	–	20	ns
Dead Time (Turn-Off to Turn-On Delay)	t_{DEAD}	Default power-up state (Figure 3)	1.25	1.6	2.15	µs

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ELECTRICAL CHARACTERISTICS (continued): Valid at T_J = –40°C to 150°C, V_{BB} = 5.5 to 50 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
LOGIC INPUTS AND OUTPUTS						
Input Low Voltage	V_{IL}		–	–	0.8	V
Input High Voltage	V_{IH}	All logic inputs	2	–	–	V
Input Hysteresis	V_{Ihys}	All logic inputs	250	550	–	mV
Input Pull-Down HA, LB, SDI, SCK, ENABLE	R_{PD}	0 < V_{IN} < 5 V	–	50	–	kΩ
	I_{PD}	5 V < V_{IN} < 50 V, HA, LB, ENABLE	–	100	–	µA
Input Pull-Down RESETn	R_{PDR}	0 < V_{IN} < 5 V	–	50	–	kΩ
	I_{PDR}	5 V < V_{IN} < 50 V	–	100	–	µA
Input Pull-Up Current to VDL	R_{PU}	HBn, LAn, STRn, Input = 0 V	–	100	–	µA
Output Low Voltage	V_{OL}	I_{OL} = 1 mA	–	0.2	0.4	V
Output High Voltage	V_{OH}	I_{OL} = –1 mA [1]	2.4	–	–	V
Output Leakage [1]	I_O	SDO, 0 V < V_{SDO} < 3 V, STRn = 1	–1	–	1	µA
LOGIC I/O – DYNAMIC PARAMETERS						
Reset Pulse Width	t_{RST}		0.5	–	4.5	µs
Clock High Time	t_{SCKH}	A in Figure 2	50	–	–	ns
Clock Low Time	t_{SCKL}	B in Figure 2	50	–	–	ns
Strobe Lead Time	t_{STLD}	C in Figure 2	30	–	–	ns
Strobe Lag Time	t_{STLG}	D in Figure 2	30	–	–	ns
Strobe High Time	t_{STRH}	E in Figure 2	300	–	–	ns
Data Out Enable Time	t_{SDOE}	F in Figure 2	–	–	40	ns
Data Out Disable Time	t_{SDOD}	G in Figure 2	–	–	30	ns
Data Out Valid Time from Clock Falling	t_{SDOV}	H in Figure 2	–	–	40	ns
Data Out Hold Time from Clock Falling	t_{SDOH}	I in Figure 2	5	–	–	ns
Data In Setup Time to Clock Rising	t_{SDIS}	J in Figure 2	15	–	–	ns
Data in Hold Time from Clock Rising	t_{SDIH}	K in Figure 2	10	–	–	ns
Wake Up from Sleep	t_{EN}	C_{REG} = 2.2 µF	–	–	2	ms

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Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
CURRENT SENSE AMPLIFIERS						
Input Offset Voltage	V_{IOS}		–4	±1	+4	mV
Input Offset Voltage Drift	ΔV_{IOS}		–	±4	–	µV/°C
Input Bias Current [1]	I_{BIAS}	0 V < V_{CSP} < V_{DL}, 0 V < V_{CSM} < V_{DL}	–160	–	–60	µA
Input Offset Current [1]	I_{OS}	V_{ID} = 0, V_{CM} in range	–20	–	+20	µA
Input Common-Mode Range (DC)	V_{CM}	V_{ID} = 0	–1	–	2	V
Gain	A_V	Default power-up value	–	35	–	V/V
Gain Error	E_A	V_{CM} in range	–5	±2	5	%
Output Offset	V_{OOS}	Default power-up value	–	2.5	–	V
Output Offset Error	E_{VO}	V_{CM} in range, Gain = 10 V/V, V_{OOS} > 1 V	–5	–	5	%
		V_{CM} in range, Gain = 10 V/V, V_{OOS} ≤ 1 V	–75	–	75	mV
Small Signal –3 dB Bandwidth at Gain = 25	B_W	V_{IN} = 10 mVpp	500	–	–	kHz
Output Settling Time (to within 40 mV)	t_{SET}	V_{CSO} = 1 Vpp square wave Gain = 25 V/V, C_{OUT} = 200 pF	–	1	1.8	µs
Output Dynamic Range	V_{CSOUT}	–100 µA [1] < I_{CSO} < 100 µA	0.3	–	4.8	V
Output Voltage Clamp	V_{CSC}	I_{CSO} = –2 mA	4.9	5.1	5.5	V
Output Current Sink [1]	I_{CSsink}	V_{ID} = 0 V, V_{CSO} = 1.5 V, Gain = 25 V/V	200	–	–	µA
Output Current Sink (Boosted) [1][3]	$I_{CSsinkb}$	V_{OOS} = 1.5 V, V_{ID} = –50 mV, Gain = 25 V/V, V_{CSO} = 1.5 V	1	–	–	mA
Output Current Source [1]	$I_{CSsource}$	V_{ID} = 200 mV, V_{CSO} = 1.5 V, Gain = 25 V/V, Offset = 0 V	–	–	–1	mA
DC Common-Mode Rejection Ratio	CMRR	V_{CM} step from 0 to 200 mV, Gain = 25 V/V	60	–	–	dB
AC Common-Mode Rejection Ratio	CMRR	V_{CM} = 200 mVpp, 100 kHz, Gain = 25 V/V	–	62	–	dB
		V_{CM} = 200 mVpp, 1 MHz, Gain = 25 V/V	–	43	–	dB
Common-Mode Recovery Time (to within 100 mV)	t_{CMrec}	V_{CM} step from –4 V to +1 V, Gain = 25 V/V, C_{OUT} = 200 pF	–	1	–	µs
Output Slew Rate 10% to 90%	SR	V_{ID} step from 0 V to 175 mV, Gain = 25 V/V, C_{OUT} = 200 pF	–	10	–	V/µs
Input Overload Recovery (to within 40 mV)	t_{IDrec}	V_{ID} step from 250 mV to 0 V, Gain = 25 V/V, C_{OUT} = 200 pF	–	1	–	µs

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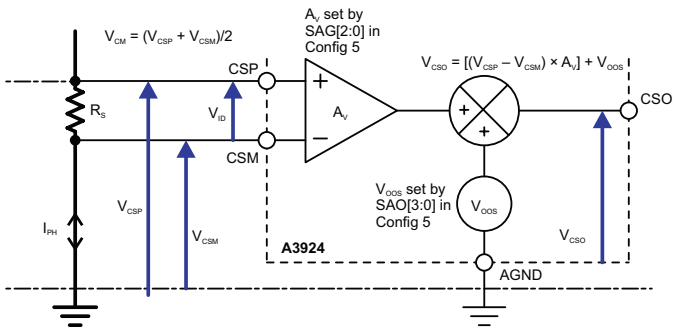

Figure 1: Typical Sense Amp Voltage Definitions

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ELECTRICAL CHARACTERISTICS (continued): Valid at T_J = –40°C to 150°C, V_{BB} = 5.5 to 50 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Diagnostics and Protection						
VREG Undervoltage, VRG = 0	V_{RON}	V_{REG} rising	6.3	6.5	6.8	V
	V_{ROFF}	V_{REG} falling	5.2	5.4	5.6	V
VREG Undervoltage, VRG = 1	V_{RON}	V_{REG} rising	7.5	7.95	8.2	V
	V_{ROFF}	V_{REG} falling	6.7	7	7.2	V
VREG Overvoltage Warning	V_{ROV}	V_{REG} rising	14.3	14.9	15.4	V
VREG Overvoltage Hysteresis	V_{ROVHys}		500	700	–	mV
VBB Overvoltage Warning	V_{BBOV}	V_{BB} rising	32	–	36	V
VBB Overvoltage Hysteresis	$V_{BBOVHys}$		1	–	–	V
VBB Undervoltage	V_{BBUV}	V_{BB} falling	–	4.0	–	V
VBB Undervoltage Hysteresis	$V_{BBUVHys}$		–	500	–	mV
VBB POR Voltage	V_{BBR}	V_{BB}	–	3.5	–	V
Bootstrap Undervoltage	V_{BCUV}	V_{BOOT} rising, $V_{BOOT} = V_{Cx} – V_{Sx}$	70	–	79	$\%V_{REG}$
Bootstrap Undervoltage Hysteresis	$V_{BCUVHys}$		–	14	–	$\%V_{REG}$
Gate Drive Undervoltage Warning HS	V_{GSHUV}	V_{GSH}	$V_{BOOT} – 1.2$	$V_{BOOT} – 1$	$V_{BOOT} – 0.8$	V
Gate Drive Undervoltage Warning LS	V_{GSLUV}	V_{GSL}	$V_{REG} – 1.2$	$V_{REG} – 1$	$V_{REG} – 0.8$	V
Regulator Undervoltage Warning	V_{3UV}	V_3 falling	2.45	2.7	2.85	V
Regulator Undervoltage Hysteresis	V_{3UVHys}		50	100	150	mV
Regulator Overvoltage Warning	V_{3OV}	V_3 rising	4	4.8	–	V
Regulator Overvoltage Hysteresis	V_{3OVHys}		–	100	–	mV
Logic Terminal Overvoltage Warning	V_{LOV}	V_L rising on HA, HBn, LAn, LB, RESETn, ENABLE, or DIAG	6.5	–	9	V
ENABLE Input Timeout	t_{ETO}		90	100	110	ms
VBRG Input Voltage	V_{BRG}	When VDS monitor is active	5.5	V_{BB}	50	V
VBRG Input Current	I_{VBRG}	V_{DSTH} = default, V_{BB} = 12 V, 0V < V_{BRG} < V_{BB}	–	–	500	µA
	I_{VBRGQ}	Sleep mode, V_{BB} < 35 V	–	–	5	µA
VBRG Disconnect Threshold	V_{BRO}	$V_{BB} – V_{BRG}$; default value, $V_{BB} \geq 6$ V	1.5	2	2.5	V
VBRG Disconnect Hysteresis	V_{BROHys}		–	250	–	mV
High-Side VDS Threshold	V_{DSTH}	Default power-up value	–	1.2	–	V
		$V_{BRG} \geq 7$ V	–	–	3.15	V
		5.5 V ≤ V_{BRG} < 7 V	–	–	1.5	V
High-Side VDS Threshold Offset [2]	V_{DSTHO}	High-side on, 200 mV ≤ V_{DSTH} ≤ 3.15 V	–200	±100	+200	mV
Low-Side VDS Threshold	V_{DSTL}	Default power-up value	–	1.2	–	V
		$V_{BB} \geq 5.5$V	–	–	3.15	V
Low-Side VDS Threshold Offset [2]	V_{DSTLO}	Low-side on, 300 mV ≤ V_{DSTL} ≤ 3.15 V	–300	±100	+300	mV
VDS Qualify Time	t_{VDQ}	Default power-up value (Figure 5)	1.25	1.6	2.15	µs
Phase Comparator Threshold	V_{PT}	Phase voltage Default power-up value	–	50	–	$\%V_{BRG}$
Overcurrent Voltage	V_{OCT}	Default power-up value	2.7	3	3.3	V
Overcurrent Qualify Time	t_{OCQ}	Default power-up value	6.75	7.5	8.25	µs
On-State Open-Load Threshold Voltage	V_{OLTON}	Default power-up value	200	225	250	mV

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ELECTRICAL CHARACTERISTICS (continued): Valid at T_J = –40°C to 150°C, V_{BB} = 5.5 to 50 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
DIAGNOSTICS AND PROTECTION (continued)						
Off-State Open-Load Threshold Voltage	V_{OLTOFF}		0.6	1	1.4	V
Off-State Sink Current on SB	I_{OLTS}		6	10	14	mA
Off-State Source Current on SA	I_{OLTT}	OLI = 0	–	100	–	µA
Off-State Source Current on SA	I_{OLTT}	OLI = 1	–	400	–	µA
Open-Load Timeout	t_{OLTO}		90	100	110	ms
DIAG Output: Fault Pulse Period	t_{FP}	DG[1:0]=0,1	90	100	110	ms
DIAG Output: Fault Pulse Duty Cycle	D_{FP}	DG[1:0]=0,1: Fault present	–	80	–	%
DIAG Output: Fault Pulse Duty Cycle	D_{FP}	DG[1:0]=0,1: No fault present	–	20	–	%
DIAG Output: Temperature Range	V_{TJD}	DG[1:0]=1,0	–	1440	–	mV
DIAG Output: Temperature Slope	A_{TJD}	DG[1:0]=1,0	–	–3.92	–	mV/°C
Temperature Warning Threshold	T_{JW}	Temperature increasing	125	135	145	°C
Temperature Warning Hysteresis	T_{JWHhys}		–	15	–	°C
Overtemperature Threshold	T_{JF}	Temperature increasing	170	175	180	°C
Overtemperature Hysteresis	T_{JHyst}	Recovery = $T_{JF} – T_{JHyst}$	–	15	–	°C
DIAGNOSTIC VERIFICATION						
LSS Open Threshold	V_{LSO}		4.5	5	5.5	V
LSS Open Threshold Hysteresis	V_{LSOHys}		–	500	–	mV
LSS Verification Current [1]	I_{LU}		–	–100	–	µA
Phase Test Pull-Down Current	I_{SD}		–	200	–	µA
Phase Test Pull-Up Current [1]	I_{SU}		–	–200	–	µA
Sense Amplifier Input Open Threshold (CSP, CSM)	V_{SAD}		–	2.2	–	V
Sense Amplifier Input Verification Current [1]	I_{SAD}		–	–20	–	µA

[1] For input and output current specifications, negative current is defined as coming out of (sourcing) the specified device terminal.
[2] VDS offset is the difference between the programmed threshold, V_{DSTH} or V_{DSTL}, and the actual trip voltage.
[3] If the amplifier output voltage (V_{CSO}) is more positive than the value demanded by the applied differential input (V_{ID}) and output offset (V_{OOS}) conditions, output current sink capability is boosted to enhance negative-going transient response.

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OVERCURRENT FAULT TIMING DIAGRAMS

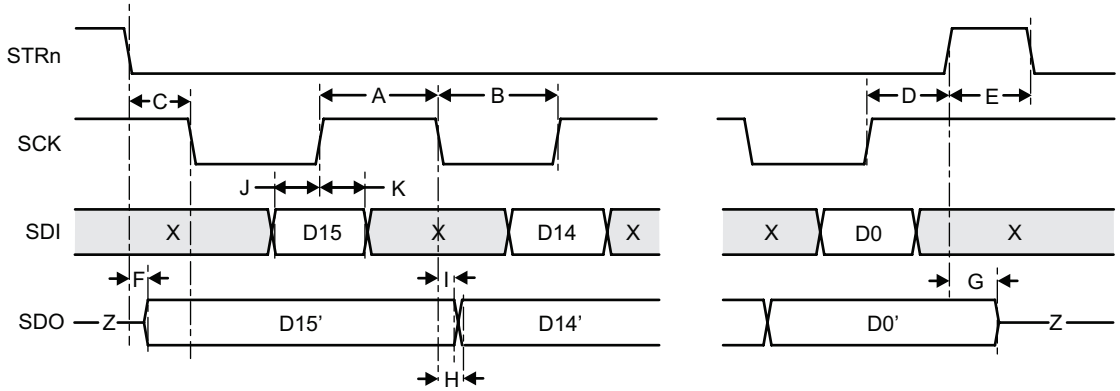

Figure 2: Serial Interface Timing

X = don't care; Z = high impedance (tri-state)

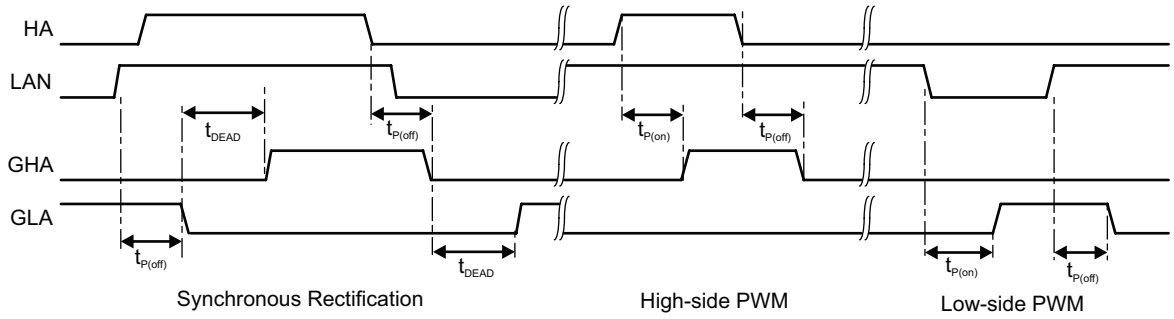

Figure 3a: Gate Drive Timing – Phase A Logic Control Inputs

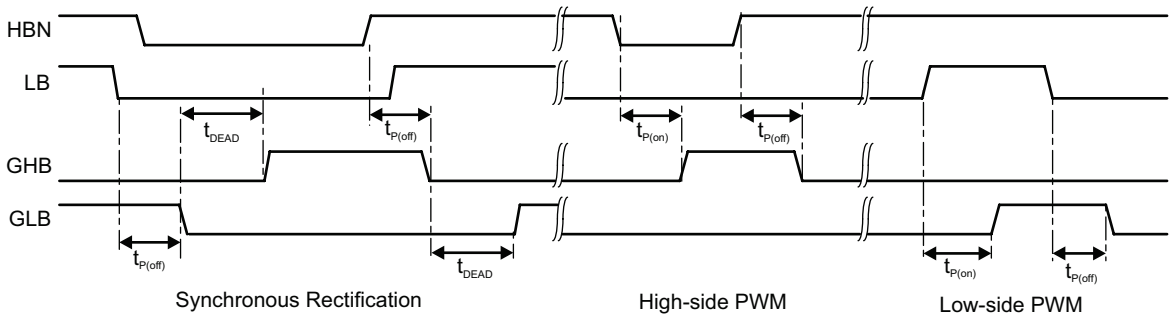

Figure 3b: Gate Drive Timing – Phase B Logic Control Inputs

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VDS FAULT TIMING DIAGRAMS

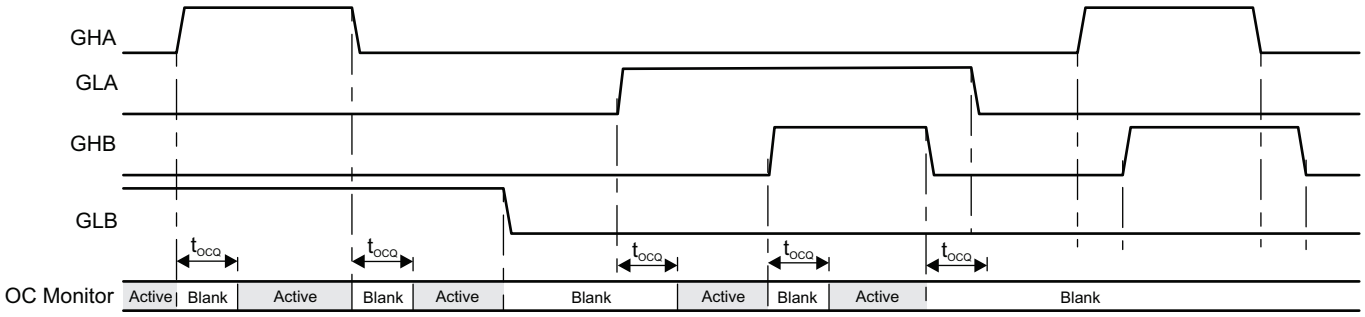

Figure 4: Overcurrent Fault Monitor – Blank Mode Timing (OCQ=1)

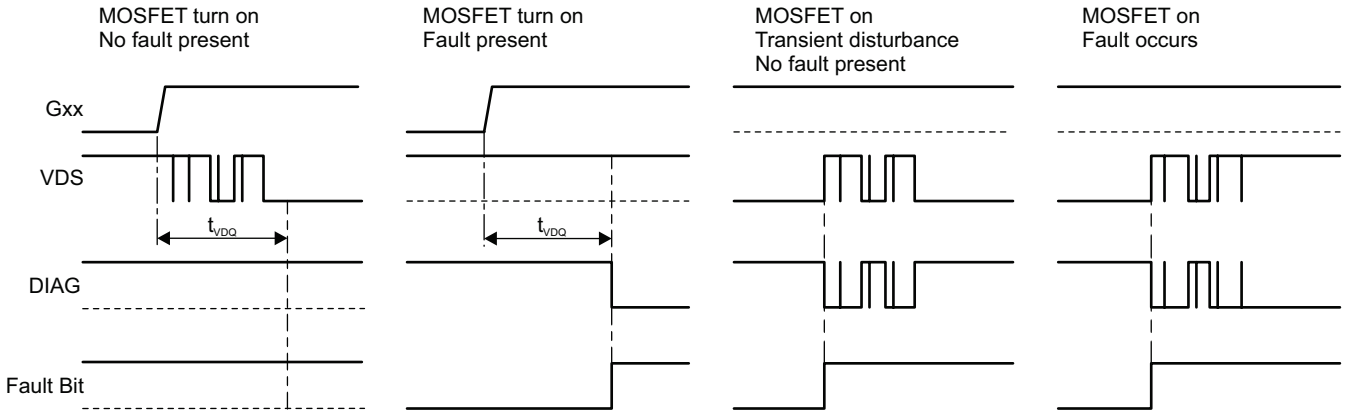

Figure 5a: VDS Fault Monitor – Blank Mode Timing (VDQ=1)

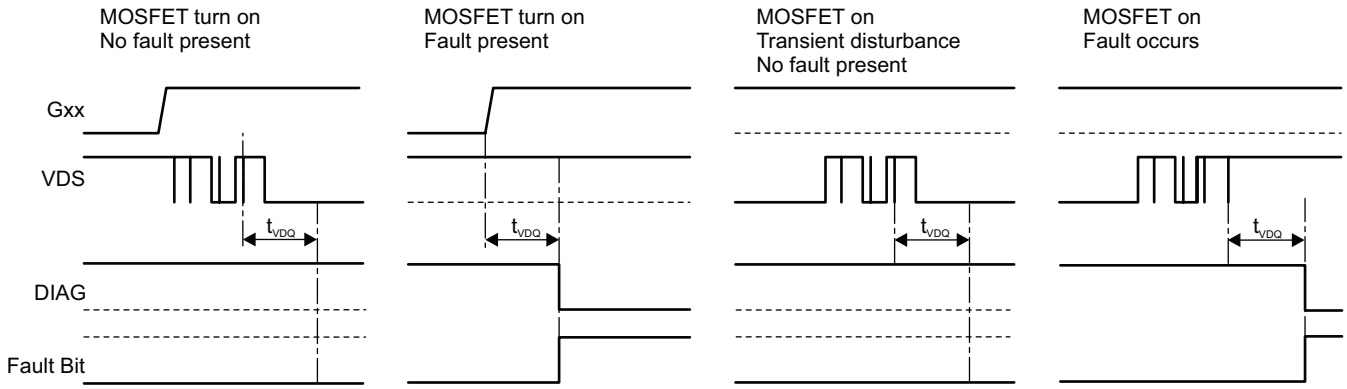

Figure 5b: VDS Fault Monitor – Debounce Mode Timing (VDQ=0)

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LOGIC TRUTH TABLES

Table 1: Control Logic Table: Control by Logic Inputs

Phase A					Phase B				
HA	LAn	GHA	GLA	SA	HBn	LB	GHB	GLB	SB
0	1	LO	LO	Z	1	0	LO	LO	Z
0	0	LO	HI	LO	1	1	LO	HI	LO
1	1	HI	LO	HI	0	0	HI	LO	HI
1	0	LO	LO	Z	0	1	LO	LO	Z

HI ≡ high-side FET active, LO ≡ low-side FET active.
Z ≡ high impedance, both FETs off.
All control register bits set to 0, RESETn = 1, ENABLE = 1.

Table 2: Control Logic Table: Control by Serial Register

Phase A					Phase B				
AH	AL	GHA	GLA	SA	BH	BL	GHB	GLB	SB
0	0	LO	LO	Z	0	0	LO	LO	Z
0	1	LO	HI	LO	0	1	LO	HI	LO
1	0	HI	LO	HI	1	0	HI	LO	HI
1	1	LO	LO	Z	1	1	LO	LO	Z

HI ≡ high-side FET active, LO ≡ low-side FET active.
Z ≡ high impedance, both FETs off.
Logic 0 input on HA,LB. Logic 1 input on LAn, HBn, RESETn = 1, ENABLE = 1.

Table 3: Control Combination Logic Table: Control by Logic Inputs & Serial Register

Phase A							Phase B						
HA	AH	LAn	AL	GHA	GLA	SA	HBn	BH	LB	BL	GHB	GLB	SB
0	0	1	0	LO	LO	Z	1	0	0	0	LO	LO	Z
0	0	X	1	LO	HI	LO	1	0	X	1	LO	HI	LO
0	0	0	X				1	0	1	X			
X	1	1	0	HI	LO	HI	X	1	0	0	HI	LO	HI
1	X	1	0				0	X	0	0			
X	1	X	1	LO	LO	Z	X	1	X	1	LO	LO	Z
X	1	0	X				X	1	1	X			
1	X	X	1				0	X	X	1			
1	X	0	X				0	X	1	X			

X ≡ don't care, HI ≡ high-side FET active, LO ≡ low-side FET active, Z ≡ high impedance, both FETs off.
RESETn = 1; ENBLE = 1.

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FUNCTIONAL DESCRIPTION

The A3924 is full-bridge (H-Bridge) MOSFET driver (pre-driver) requiring a single unregulated supply of 6 to 50 V. It includes an integrated linear regulator to supply the internal logic and a linear regulator controller to provide a 3.3 V supply for external circuits. All logic inputs are TTL compatible and can be driven by 3.3 or 5 V logic.

The four high-current gate drives are capable of driving a wide range of N-channel power MOSFETs, and are configured as a full-bridge driver with two high-side drives and two low-side drives. The A3924 provides all necessary circuits to ensure that all external power MOSFETs are fully enhanced at supply voltages down to 7 V. For extreme battery voltage drop conditions, correct functional operation is guaranteed at supply voltages down to 5.5 V, but with a reduced gate drive voltage.

Gate drives can be controlled directly through the logic input terminals or through an SPI-compatible serial interface. The sense of the logic inputs are arranged to allow each bridge to be driven by a single PWM input if required. Each bridge can also be driven by direct logic inputs or by two or four PWM signals, depending on the required complexity. The logic inputs are battery voltage compliant, meaning they can be shorted to ground or supply without damage up to the maximum battery voltage of 50 V.

Bridge efficiency can be enhanced by using the synchronous rectification ability of the drives. When synchronous rectification is used, cross-conduction (shoot-through) in the external bridge is avoided by an adjustable dead time. A hard-wired logic lockout ensures that high-side and low-side on any single phase cannot be permanently active at the same time.

A low-power sleep mode allows the A3924, the power bridge, and the load to remain connected to a vehicle battery supply without the need for an additional supply switch.

The A3924 includes a number of diagnostic features to provide indication of and/or protection against undervoltage, overvoltage, overtemperature, and power bridge faults. Detailed diagnostic information is available through the serial interface.

For systems requiring a higher level of safety integrity, the A3924 includes additional overvoltage monitors on the supplies and the control inputs. In addition, the integrated diagnostics include self-test and verification circuits to ensure verifiable diagnostic operation. When used in conjunction with appropriate system level control, these features can assist power drive systems using the A3924 to meet stringent ASIL D safety requirements.

The serial interface also provides access to programmable dead time, fault blanking time, programmable VDS threshold for short detection, and programmable thresholds and currents for open-load detection.

The A3924 includes a low-side current sense amplifier with programmable gain and offset. The amplifier is specifically designed for current sensing in the presence of high voltage and current transients. The A3924 can also check the connections from the current sense amplifier to the sensing link using integrated verification circuits.

Input and Output Terminal Functions

- **VBB:** Main power supply for internal regulators and charge pump. The main power supply should be connected to VBB through a reverse voltage protection circuit and should be decoupled with ceramic capacitors connected close to the supply and ground terminals.
- **VBRG:** Sense input to the top of the external MOSFET bridge. Allows accurate measurement of the voltage at the drain of the high-side MOSFETs in the bridge.
- **CP1, CP2:** Pump capacitor connection for charge pump. Connect a minimum 220 nF, typically 470 nF, ceramic capacitor between CP1 and CP2.
- **V3:** Reference input for the linear regulator controller. Connect to the emitter of an NPN pass element. Connect a 100 nF ceramic capacitor, C_{V3}, directly between the V3 terminal and the GND terminal.
- **V3BD:** Drive output for the base of an NPN pass element. Connect a 220 nF ceramic capacitor, C_{V3B}, directly between the V3BD terminal and the GND terminal.
- **VREG:** Programmable regulated voltage, 8 or 13 V, used to supply the low-side gate drivers and to charge the bootstrap capacitors. A sufficiently large storage capacitor must be connected to this terminal to provide the transient charging current.
- **GND:** Analog reference, digital, and power ground. Connect to supply ground—see layout recommendations.
- **AGND:** Analog reference ground. Connect to supply ground—see layout recommendations

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- **CA, CB:** High-side connections for the bootstrap capacitors and positive supply for high-side gate drivers.
- **GHA, GHB:** High-side, gate-drive outputs for external n-channel MOSFETs.
- **SA, SB:** Load phase connections. These terminals sense the voltages switched across the load. They are also connected to the negative side of the bootstrap capacitors and are the negative supply connections for the floating high-side drivers.
- **GLA, GLB:** Low-side, gate-drive outputs for external n-channel MOSFETs.
- **LSSA, LSSB:** Low-side return path for discharge of the capacitance on the MOSFET gates, connected to the common sources of the low-side external MOSFETs independently through a low impedance track.
- **HA:** Logic inputs with pull-down to control the high-side gate drive on phase A. Battery voltage compliant terminal.
- **HBn:** Logic inputs with pull-up to control the high-side gate drive on phase B. These are active low inputs. Battery voltage compliant terminal.
- **LAn:** Logic inputs with pull-up to control the low-side gate drive on phase A. These are active low inputs. Battery voltage compliant terminal.
- **LB:** Logic inputs with pull-down to control the low-side gate drive on phase B. Battery voltage compliant terminal.
- **SDI:** Serial data logic input with pull-down. 16-bit serial word input msb first.
- **SDO:** Serial data output. High impedance when STRn is high. Outputs bit 15 of the Status register, the fault flag, as soon as STRn goes low.
- **SCK:** Serial clock logic input with pull-down. Data is latched in from SDI on the rising edge of SCK. There must be 16 rising edges per write and SCK must be held high when STRn changes.
- **STRn:** Serial data strobe and serial access enable logic input with pull-up. When STRn is high, any activity on SCK or SDI is ignored and SDO is high impedance, allowing multiple SDI slaves to have common SDI, SCK and SDO connections.
- **CSPA, CSMA, CSPB, CSMB:** Current sense amplifier inputs.
- **CSOA, CSOB:** Current sense amplifier outputs.
- **DIAG:** Diagnostic output. Programmable output to provide one of four functions: fault flag, pulsed fault flag, temperature, and the programmed sense amplifier output offset voltage. Default is fault flag.
- **RESETn:** Resets faults when pulsed low. Forces low-power shutdown (sleep) when held low. Can be pulled to VBB.
- **ENABLE:** Deactivates all gate drive outputs when pulled low in direct mode or after a timeout in monitor mode. Provides an independent output deactivation, directly to the gate drive outputs, to allow a fast disconnect on the power bridge. Can be pulled to VBB.
- **SAL, SBL:** Logic level outputs representing the state of each phase determined by the output of a programmable threshold comparator.

Power Supplies

A single power supply voltage is required. The main power supply (V_{BB}) should be connected to VBB through a reverse voltage protection circuit. A 100 nF ceramic decoupling capacitor must be connected close to the supply and ground terminals.

An internal regulator provides the supply to the internal logic. All logic is guaranteed to operate correctly to below the regulator undervoltage levels, ensuring that the A3924 will continue to operate safely until all logic is reset when a power-on-reset state is present.

The A3924 will operate within specified parameters with V_{BB} from 5.5 to 50 V and will operate safely between 0 and 50 V under all supply switching conditions. This provides a very rugged solution for use in the harsh automotive environment.

PUMP REGULATOR

The gate drivers are powered by a programmable voltage internal regulator which limits the supply to the drivers and therefore the maximum gate voltage. At low supply voltage, the regulated supply is maintained by a charge pump boost converter which requires a pump capacitor, typically 470 nF, connected between the CP1 and CP2 terminals.

The regulated voltage (V_{REG}) can be programmed to 8 or 13 V and is available on the VREG terminal. The voltage level is selected by the value of the VRG bit. When VRG = 1, the voltage is set to 13 V when VRG = 0, the voltage is set to 8 V.

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A sufficiently large storage capacitor (see Applications section) must be connected to this terminal to provide the transient charging current to the low-side drivers and the bootstrap capacitors.

LINEAR REGULATOR CONTROLLER

An additional integrated 3.3 V regulator controller is provided for external logic level circuits, if required. This uses an external pass element to reduce internal power dissipation. The pass element, usually an NPN transistor, can be sized to provide the required current for any additional circuits.

The regulator output must always be decoupled by at least a 100 nF ceramic capacitor (C_{V3}) between the V3 terminal and GND.

Gate Drives

The A3924 is designed to drive external, low on-resistance, power n-channel MOSFETs. It will supply the large transient currents necessary to quickly charge and discharge the external MOSFET gate capacitance to reduce dissipation in the external MOSFET during switching. The charge current for the low-side drives and the recharge current for the bootstrap capacitors are provided by the capacitor on the VREG terminal. The charge current for the high-side drives is provided by the bootstrap capacitors connected between the Cx and Sx terminal, one for each phase. The charge and discharge rate of the gate of the MOSFET can be controlled using an external resistor in series with the connection to the gate of the MOSFET.

BOOTSTRAP SUPPLY

When the high-side drivers are active, the reference voltage for the driver will rise to close to the bridge supply voltage. The supply to the driver will then have to be above the bridge supply voltage to ensure that the driver remains active. This temporary high-side supply is provided by bootstrap capacitors, one for each high-side driver. These two bootstrap capacitors are connected between the bootstrap supply terminals (CA and CB) and the corresponding high-side reference terminal (SA and SB).

The bootstrap capacitors are independently charged to approximately V_{REG} when the associated reference Sx terminal is low. When the output swings high, the voltage on the bootstrap supply terminal rises with the output to provide the boosted gate voltage needed for the high-side n-channel power MOSFETs.

BOOTSTRAP CHARGE MANAGEMENT

The A3924 monitors the individual bootstrap capacitor charge voltages to ensure sufficient high-side drive. It also includes an optional bootstrap capacitor charge management system (bootstrap manager) to ensure that the bootstrap capacitor remains sufficiently charged under all conditions. The bootstrap manager is enabled by default, but it may be disabled by setting the DBM bit to 1. This may be required in systems where the output MOSFET switching must only be allowed by the controlling processor.

Before a high-side drive can be turned on, the bootstrap capacitor voltage must be higher than the turn-on voltage threshold ($V_{BCUV} + V_{BCUVHys}$). If this is not the case, then the A3924 will attempt to charge the bootstrap capacitor by activating the complementary low-side drive. Under normal circumstances, this will charge the capacitor above the turn-on voltage in a few microseconds, and the high-side drive will then be enabled. The bootstrap voltage monitor remains active while the high-side drive is active; furthermore, if the voltage drops below the turn-off voltage threshold (V_{BCUV}), a charge cycle is also initiated.

The bootstrap charge management circuit may actively charge the bootstrap capacitor regularly when the PWM duty cycle is very high, particularly when the PWM off-time is too short to permit the bootstrap capacitor to become sufficiently charged.

In some safety systems, the gate driver is not permitted to turn on a MOSFET without a direct command from the controller. In this case, the bootstrap manager may be disabled by setting the DBM bit to 1. If the bootstrap manager is disabled, then the user must ensure that the bootstrap capacitor does not become discharged below the bootstrap undervoltage threshold (V_{BCUV}), or a bootstrap fault will be indicated and the outputs disabled. This can happen with very high PWM duty cycles when the charge time for the bootstrap capacitor is insufficient to ensure a sufficient recharge to match the MOSFET gate charge transfer during turn on.

If, for any reason, the bootstrap capacitor cannot be sufficiently charged, a bootstrap fault will occur—see Diagnostics section for further details.

TOP-OFF CHARGE PUMP.

An additional “top-off” charge pump is provided for each phase, which will allow the high-side drive to maintain the gate voltage on the external MOSFET indefinitely, ensuring so-called 100% PWM if required. This is a low current trickle charge pump and is only operated after a high-side has been signaled to turn on. There is a small amount of bias current drawn from the Cx terminal to operate the floating high side circuit (<40 µA), and the charge pump simply provides enough drive to ensure the bootstrap voltage—and hence the gate voltage—will not droop due to this bias current.

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In some applications, a safety resistor is added between the gate and source of each MOSFET in the bridge. When a high-side MOSFET is held in the on-state, the current through the associated high-side gate-source resistor (R_{GSH}) is provided by the high-side driver and therefore appears as a static resistive load on the top-off charge pump. The minimum value of R_{GSH} for which the top-off charge pump can provide current, without dropping below the bootstrap undervoltage threshold, is defined in the Electrical Characteristics table.

In all cases, the charge required for initial turn-on of the high-side gate is always supplied by the bootstrap capacitor. If the bootstrap capacitor becomes discharged, the top-off charge pump alone will not provide sufficient current to allow the MOSFET to turn on.

HIGH-SIDE GATE DRIVE

High-side, gate-drive outputs for external n-channel MOSFETs are provided on pins GHA and GHB. External resistors between the gate drive output and the gate connection to the MOSFET (as close as possible to the MOSFET) can be used to control the slew rate seen at the gate, thereby controlling the di/dt and dv/dt of the voltage at the SA and SB terminals. GHx = 1 (or “high”) means that the upper half of the driver is turned on, and its drain will source current to the gate of the high-side MOSFET in the external motor-driving bridge, turning it on. GHx = 0 (or “low”) means that the lower half of the driver is turned on, and its drain will sink current from the external MOSFET’s gate circuit to the respective Sx terminal, turning it off.

The reference points for the high-side drives are the load phase connections (SA and SB). These terminals sense the voltages at the load connections. These terminals are also connected to the negative side of the bootstrap capacitors and are the negative supply reference connections for the floating high-side drivers. The discharge current from the high-side MOSFET gate capacitance flows through these connections, which should have low-impedance traces to the MOSFET bridge.

LOW-SIDE GATE DRIVE

The low-side, gate drive outputs on GLA and GLB are referenced to the LSS terminal. These outputs are designed to drive external n-channel power MOSFETs. External resistors between the gate drive output and the gate connection to the MOSFET (as close as possible to the MOSFET) can be used to control the slew rate seen at the gate, thereby providing some control of the di/dt and dv/dt of the voltage at the SA and SB terminals. GLx = 1 (or “high”) means that the upper half of the driver is turned on, and its drain will source current to the gate of the low-side MOSFET in the external power bridge, turning it on. GLx = 0 (or “low”) means that the lower half of the driver is turned on, and its drain will sink current from the external MOSFET’s gate circuit to the LSS terminal, turning it off.

The LSS terminal provides the return path for discharge of the capacitance on the low-side MOSFET gates. This terminal is connected independently to the common sources of the low-side external MOSFETs through a low-impedance track.

GATE DRIVE PASSIVE PULL-DOWN

Each gate drive output includes a discharge circuit to ensure that any external MOSFET connected to the gate drive output is held off when the power is removed. This discharge circuit appears as 400 kΩ between the gate drive and the source connections for each MOSFET. It is only active when the A3924 is not driving the output to ensure that any charge accumulated on the MOSFET gate has a discharge path even when the power is not connected.

DEAD TIME

To prevent cross-conduction (shoot-through) in any phase of the power MOSFET bridge, it is necessary to have a dead-time delay between a high- or low-side turn-off and the next complementary turn-on event. The potential for cross-conduction occurs when any complementary high-side and low-side pair of MOSFETs are switched at the same time (for example, at the PWM switch point). In the A3924, the dead time for both phases is set by the contents of the DT[5:0] bits in Config 0 register. These six bits contain a positive integer that determines the dead time by division from the system clock.

The dead time is defined as:

$$t_{DEAD} = n \times 50\ ns$$

where n is a positive integer defined by DT[5:0] and

t_{DEAD} has a minimum active value of 100 ns.

For example, when

DT[6:0] contains [11 0000] (= 48 in decimal), then t_{DEAD} = 2.4 µs, typically.

The accuracy of t_{DEAD} is determined by the accuracy of the system clock as defined in the Electrical Characteristics table. The range of t_{DEAD} is 100 ns to 3.15 µs. A value of 1, or 2 in DT[5:0] will set the minimum active dead time of 100 ns.

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If the dead-time is to be generated externally (for example, by the PWM output of a microcontroller), then entering a value of zero in DT[5:0] will disable the dead timer, and there will be no minimum dead time generated by the A3924. However, the logic that prevents permanent cross-conduction will still be active.

The internally generated dead time will only be present if the on command for one MOSFET occurs within one dead time after the off command for its complementary partner. In the case where one side of a phase drive is permanently off (for example, when using diode rectification with slow decay), then the dead time will not occur. In this case, the gate drive will turn on within the specified propagation delay after the corresponding phase input goes high. (see Figure 3)

Logic Control Inputs

Four logic level digital inputs provide direct control for the gate drives, one for each drive. These TTL threshold logic inputs can be driven from 3.3 or 5 V logic, and all have a typical hysteresis of 500 mV to improve noise performance. Each input can be shorted to the VBB supply, up to the absolute maximum supply voltage, without damage to the input.

Input HA is active-high and controls the high-side drive for phase A. LAn is active-low and controls the low-side drive for phase A. Similarly, HBn (active-low) and LB (active-high) control the high-side and low-side drives respectively for phase B. The logical relationship between the inputs and the gate drive outputs is defined in Table 1.

The logic sense of the inputs (active-high or active-low) are arranged to permit the bridge to be controlled with 1, 2, or 4 inputs. The control inputs to each phase can be driven together to control both high-side and low-side drives when synchronous rectification is used. Driving each phase with a single input in this way provides direction control with one input and slow decay, synchronous rectification PWM with the other input.

Driving all four control inputs together provides fast decay with synchronous rectification and can be used to control current in both directions with a single PWM input.

The two phases can also operate independently providing two half-bridge drives. In this case, the dead time, blank time, and VDS threshold will be common to both half bridge drives.

The gate drive outputs can also be controlled through the serial interface by setting the appropriate bit in the control register. In the control register, all bits are active-high. The logical relationship between the register bit setting and the gate drive outputs is defined in Table 2.

The logic inputs are combined (using logical OR) with the corresponding bits in the serial interface control register to determine the state of the gate drive. The logical relationship between the combination of logic input and register bit setting and the gate drive outputs is defined in Table 3. In most applications, either the logic inputs or the serial control will be used. When using only the logic inputs to control the bridge, the serial register should be left in the reset condition with all control bits set to 0. When using only the serial interface to control the bridge, the inputs should be tied such that the active-low inputs are connected to DL and the active high inputs connected to GND; that is, HA and LB should be tied to GND, and HBn and LAn should be tied to DL. The internal pull-up and pull-down resistors on these inputs ensure that they go to the inactive state should they become disconnected from the control signal level. However, connecting these inputs to a fixed level can allow detection of control input faults that would not be detected using only the internal pull-up or pull-down.

Internal lockout logic ensures that the high-side output drive and low-side output drive cannot be active simultaneously. When the control inputs request active high-side and low-side at the same time for a single phase, then both high-side and low-side gate drives will be forced low.

Output Disable

The ENABLE input is connected directly to the gate drive output command signal, bypassing all phase control logic. This input can be used to provide a fast output disable (emergency cutoff) or to provide non-synchronous fast decay PWM.

ENABLE can also be monitored by a watchdog timer by setting the EWD bit to 1. In watchdog mode, the first change of state on the ENABLE input will activate the gate drive outputs under command from the corresponding phase control signals, and a watchdog timer is started. The ENABLE input must then change state before the end of the ENABLE timeout period (t_{ETO}). If the ENABLE input does not change before the end of the timeout period, then all gate drive outputs will be driven low, and the ETO bit will be set in the Status register. Any following change of state on the ENABLE input will reactivate the gate drive outputs. The ETO bit remains in the Status register until cleared.

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Sleep Mode

RESETn is an active-low input that commands the A3924 to enter sleep mode. In sleep mode, the part is inactive and the current consumption from the VBB supply is reduced to a low level, defined by I_{BBS}. When RESETn is held low for longer than approximately 200 µs, the gate drive outputs are disabled and the current consumption from the VBB supply decays. Holding RESETn low for 1 ms will ensure the part is fully in sleep mode.

Taking RESETn high to wake from sleep mode clears all previously reported latched fault states and corresponding fault bits. When waking up from sleep mode, the protection logic ensures that the gate drive outputs are held off until the charge pump reaches its correct operating condition. The charge pump stabilizes in approximately 3 ms, under nominal conditions.

To allow the A3924 to start up without the need for an external logic input, the RESETn terminal can be pulled to VBB with an external pull-up resistor.

Note that, if the voltage on the RESETn terminal rises above the logic terminal overvoltage warning threshold, V_{LOV}, then the VLO bit will be set in the Status register.

RESETn can also be used to clear any fault conditions without entering sleep mode by taking it low for the reset pulse width (t_{RST}). Any latched fault conditions, such as short detection or bootstrap capacitor undervoltage, which disable the outputs, will be cleared. RESETn will not reset the fault bits in the Status registers.

Current Sense Amplifier

A programmable gain, differential sense amplifier is provided to allow the use of low-value sense resistors or current shunt as a low-side current sensing element. The input common-mode range of the CSP and CSM inputs and programmable output offset allows below ground current sensing typically required for low-side current sense in PWM control of motors, or other inductive loads, during switching transients. The output of the sense amplifier is available at the CSO outputs and can be used in peak or average current control systems. The output can drive up to 4.8 V to permit maximum dynamic range with higher input voltage A-to-D converters.

The gain of the sense amplifier is defined by the contents of the SAG[2:0] variable as:

SAG	Gain
0	10
1	15
2	20
3	25

SAG	Gain
4	30
5	35
6	40
7	50

The output offset, V_{OOS}, of the sense amplifier is defined by the contents of the SAO[3:0] variable as:

SAO	V_{OOS}
0	0
1	0
2	100 mV
3	100 mV
4	200 mV
5	300 mV
6	400 mV
7	500 mV

SAO	V_{OOS}
8	750 mV
9	1 V
10	1.25 V
11	1.5 V
12	1.75 V
13	2 V
14	2.25 V
15	2.5 V

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DIAGNOSTIC MONITORS

Multiple diagnostic features provide three levels of fault monitoring. These include critical protection for the A3924, monitors for operational voltages and states, and detection of power bridge and load fault conditions. All diagnostics, except for POR, serial transfer error and overtemperature can be masked by setting the appropriate bit in the mask registers.

Except for the two phase state outputs, the fault status is available from two sources, the DIAG output terminal and the status and diagnostic registers accessed through the serial interface.

DIAG Diagnostic Output

The DIAG terminal is a single diagnostic output signal that can be programmed by setting the contents of the DG[1:0] variable through the serial interface to provide one of three dedicated diagnostic signals:

- DG = 0: a general fault flag
- DG = 1: a pulsed fault flag
- DG = 2: a voltage representing the temperature of the internal silicon
- DG = 3: the sense amplifier output offset voltage

At power-up, or after a power-on-reset, the DIAG terminal outputs a general logic-level fault flag which will be active-low if a fault is present. This fault flag remains low while the fault is present or if one of the latched faults has been detected and the outputs disabled. When the general fault flag is reset the DIAG output will be high.

The pulsed fault output option provides a continuous low-frequency low-duty cycle pulsed output when a fault is present or if one of the latched faults has been detected and the outputs disabled. When the general fault flag is reset and no fault is present, the signal output on the DIAG terminal is continuous low-frequency, high-duty cycle pulses. The period of the DIAG signal in pulsed mode is defined by t_{FP} and is typically 100 ms. The two duty cycles are defined by D_{FP} and are typically 20% when a fault is present and 80% when no fault is present.

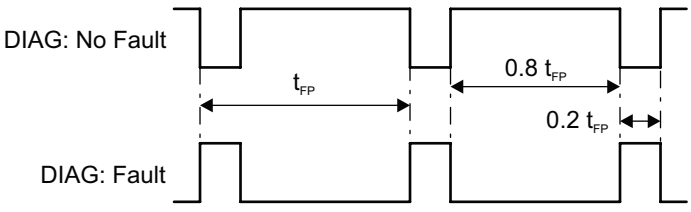

Figure 6: DIAG – Pulsed Output Mode

The temperature output option provides access to the internal voltage representing the surface temperature of the silicon.

The sense amplifier option provides the output offset voltage, (V_{OOS}) of the sense amplifier, defined by the contents of the SAO[3:0] bits in configuration register 5.

Diagnostic Registers

The serial interface allows detailed diagnostic information to be read from the diagnostic registers on the SDO output terminal at any time.

A system Status register provides a summary of all faults in a single read transaction. The Status register is always output on SDO when any register is written.

Table 4: Diagnostic Functions

Name	Diagnostic	Level
POR	Internal logic supply undervoltage causing power-on reset	Chip
OT	Chip junction overtemperature	Chip
SE	Serial transmission error	Chip
TW	High chip junction temperature warning	Monitor
VSO	VBB supply overvoltage (Load dump detection)	Monitor
VSU	VBB supply undervoltage	Monitor
VLO	Logic terminal overvoltage	Monitor
ETO	ENABLE watchdog timeout	Monitor
VRO	VREG output overvoltage	Monitor
VRU	VREG output undervoltage	Monitor
V3U	V3 Regulator output undervoltage	Monitor
V3O	V3 Regulator output overvoltage	Monitor
AHU	A high-side V_{GS} undervoltage	Monitor
ALU	A low-side V_{GS} undervoltage	Monitor
BHU	B high-side V_{GS} undervoltage	Monitor
BLU	B low-side V_{GS} undervoltage	Monitor
OCA	Overcurrent on phase A	Bridge
OCB	Overcurrent on phase B	Bridge
OL	Open load	Bridge
VA	Bootstrap undervoltage phase A	Bridge
VB	Bootstrap undervoltage phase B	Bridge
AHO	Phase A high-side V_{DS} overvoltage	Bridge
ALO	Phase A low-side V_{DS} overvoltage	Bridge
BHO	Phase B high-side V_{DS} overvoltage	Bridge
BLO	Phase B low-side V_{DS} overvoltage	Bridge

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The first bit (bit 15) of the Status register contains a common fault flag (FF), which will be high if any of the fault bits in the Status register have been set. This allows fault condition to be detected using the serial interface by simply taking STRn low. As soon as STRn goes low, the first bit in the Status register (bit 15) can be read on SDO to determine if a fault has been detected at any time since the last fault register reset. In all cases, the fault bits in the diagnostic registers are latched and only cleared after a fault register reset.

Note that FF (bit 15) does not provide the same function as the general fault flag output on the DIAG terminal when STRn is high and the DIAG output is in its default mode. The fault output on the DIAG terminal provides an indication that either a fault is present or the outputs have been disabled due to a latched fault state. FF provides an indication that a fault has occurred since the last fault reset and one or more fault bits have been set.

Chip-Level Protection

Chip-wide parameters critical for correct operation of the A3924 are monitored. These include maximum chip temperature, minimum internal logic supply voltage, and the serial interface transmission. These three monitors are necessary to ensure that the A3924 is able to respond as specified.

CHIP FAULT STATE: INTERNAL LOGIC UNDERVOLTAGE

The A3924 has an independent internal logic regulator to supply the internal logic. This is to ensure that external events, other than loss of supply, do not prevent the A3924 from operating correctly. The internal logic supply regulator will continue to operate with a low supply voltage, for example if the main supply voltage drops to a very low value during a severe cold-crank event. In extreme low-supply circumstances, or during power-up or power-down, an undervoltage detector ensures that the A3924 operates correctly. The logic supply undervoltage lockout cannot be masked as it is essential to guarantee correct operation over the full supply range.

When power is first applied to the A3924, the internal logic is prevented from operating, and all gate drive outputs are held in the off state until the internal regulator voltage (V_{DL}) exceeds the logic supply undervoltage lockout rising (turn-on) threshold, derived from the VBB POR threshold, V_{BBR}. At this point, all serial registers will be reset to their power-on state, and all fault states will be reset. The FF bit and the POR bit in the Status register will be set to one to indicate that a power-on-reset has taken place. The A3924 then goes into its fully operational state and begins operating as specified.

Once the A3924 is operational, the internal logic supply continues to be monitored. If, during the operational state, V_{DL} drops below logic supply undervoltage lockout falling (turn-off) threshold, derived from V_{BBR}, then the logical function of the A3924 cannot be guaranteed, and the outputs will be immediately disabled. The A3924 will enter a power-down state, and all internal activity, other than the logic regulator voltage monitor, will be suspended. If the logic supply undervoltage is a transient event, then the A3924 will follow the power-up sequence above as the voltage rises.

CHIP FAULT STATE: OVERTEMPERATURE

If the chip temperature rises above the overtemperature threshold (T_{JF}) the general fault flag will be active and the overtemperature bit (OT) will be set in the Status register. If ESF = 1 when an overtemperature is detected, all gate drive outputs will be disabled automatically. If ESF = 0, then no circuitry will be disabled, and action must be taken by the user to limit the power dissipation in some way so as to prevent overtemperature damage to the chip and unpredictable device operation. When the temperature drops below T_{JF} by more than the hysteresis value (T_{JFHys}), the fault state will be reset and when ESF = 1 the outputs re-enabled. The general fault flag remains active until the temperature drops below the temperature warning threshold (T_{JW}) by more than the hysteresis value (T_{JWHys}). The overtemperature bit remains in the Status register until reset.

CHIP FAULT STATE: SERIAL ERROR

If there are more than 16 rising edges on SCK, or if STRn goes high and there are fewer than 16 rising edges on SCK, or the parity is not odd, then the write will be cancelled without writing data to the registers, and the SE bit will be set to indicate a data transfer error. If the transfer is a write, then the Status register will not be reset. If the transfer is a diagnostic or verification result read, then the addressed register will not be reset.

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Operational Monitors

Parameters related to the safe operation of the A3924 in a system are monitored. These include parameters associated with external active and passive components, power supplies, and interaction with external controllers.

Voltages relating to driving the external power MOSFETs are monitored, specifically V_{REG}, each bootstrap capacitor voltage, and the V_{GS} of each gate drive output. The main supply voltage (V_{BB}) is only monitored for overvoltage and undervoltage events.

The logic inputs are capable of being shorted to the main supply voltage without damage, but any high voltage on these pins will be detected. In addition, a watchdog timer can be applied to the ENABLE input to verify continued operation of the external controller.

MONITOR: VREG UNDERVOLTAGE AND OVERVOLTAGE

The internal charge pump regulator supplies the low-side gate driver and the bootstrap charge current. It is critical to ensure that the regulated voltage (V_{REG}) at the VREG terminal is sufficiently high before enabling any of the outputs.

If VREG goes below the VREG undervoltage threshold (V_{ROFF}), the general fault flag will be active and the VREG undervoltage bit (VRU) will be set in the Diag 1 register. All gate drive outputs will go low, the motor drive will be disabled, and the motor will coast. When VREG rises above the rising threshold (V_{RON}), the gate drive outputs are re-enabled and the general fault flag is reset. The VRU bit remains in the Diag 1 register until cleared.

The VREG undervoltage monitor circuit is active during power-up, and all gate drives will be low until V_{REG} is greater than V_{RON}. Note that this is sufficient to turn on standard threshold external power MOSFETs at a battery voltage as low as 5.5 V, but the on-resistance of the MOSFET may be higher than its specified maximum.

The VREG undervoltage monitor can be disabled by setting the VRU bit in the mask register. Although not recommended, this can allow the A3924 to operate below its minimum specified supply voltage level with a severely impaired gate drive. The specified electrical parameters will not be valid in this condition.

The output of the VREG regulator is also monitored to detect any overvoltage applied to the VREG terminal.

If V_{REG} goes above the VREG undervoltage threshold (V_{ROV}), the general fault flag will be active and the VREG overvoltage bit (VRO) will be set in the Diag 1 register. No action will be taken as the gate drive outputs are protected from overvoltage by independent Zener clamps. When V_{REG} falls below V_{ROV} by more than the hysteresis voltage (V_{ROVHys}), the fault state is reset, but VRO bit remains in the Diag 1 register until cleared.

MONITOR: TEMPERATURE WARNING

If the chip temperature rises above the temperature warning threshold (T_{JW}), the general fault flag will be active and the hot warning bit (TW) will be set in the Status register. No action will be taken by the A3924. When the temperature drops below T_{JW} by more than the hysteresis value (T_{JWHys}), the general fault flag is reset but the TW bit remains in the Status register until cleared.

MONITOR: REGULATOR UNDERVOLTAGE AND OVERVOLTAGE

The output voltage of the linear regulator controller (V_3) at the V3 terminal is monitored to ensure it is within the correct limits. If V_3 drops below the logic regulator undervoltage threshold (V_{3UV}), the general fault flag will be active and the V3 undervoltage bit (V_{3U}) will be set in the Diag 0 register. No action will be taken by the A3924. When V_3 rises above the rising undervoltage threshold ($V_{3UV} + V_{3UVHys}$), the general fault flag is reset but the V_{3U} bit remains in the Diag 0 register until cleared.

If V_3 rises above the logic regulator overvoltage threshold (V_{3OV}), the general fault flag will be active and the V3 overvoltage bit (V_{3O}) will be set in the Diag 0 register. No action will be taken by the A3924. When V_3 falls below the falling undervoltage threshold ($V_{3OV} – V_{3OVHys}$), the general fault flag is reset but the V3O bit remains in the Diag 0 register until cleared.

MONITOR: VBB SUPPLY UNDERVOLTAGE AND OVERVOLTAGE

The main supply to the A3924 on the VBB terminal (V_{BB}) is monitored to indicate if the supply voltage is above, or has exceeded, its normal operating range (for example, during a load dump event). If V_{BB} rises above the VBB overvoltage warning threshold (V_{BBOV}), then the VSO bit will be set in the Diag 2 register and the general fault flag will be active. No other action will be taken. When V_{BB} falls below the falling VBB overvoltage warning threshold ($V_{BBOV} – V_{BBOVHys}$), the fault flag will be reset but the VSO bit remains in the Diag 2 register until cleared.

The main supply on the VBB terminal is also monitored to indicate if the supply voltage is below its normal operating range.

If V_{BB} goes below the VBB undervoltage threshold (V_{BBUV}), then the VSU bit will be set in the Diag 2 register and the general fault flag will be active. All gate drive outputs will go low, the motor drive will be disabled and the motor will coast. When V_{BB}

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rises above the rising VBB undervoltage threshold (V_{BBUV} + $V_{BBUVHys}$), the fault flag will be reset and the gate drive outputs are re-enabled. The VSU bit remains in the Diag 2 register until cleared.

MONITOR: VGS UNDERVOLTAGE

To ensure that the gate drive output is operating correctly, each gate drive output voltage is independently monitored, when active, to ensure the drive voltage (V_{GS}) is sufficient to fully enhance the power MOSFET in the external bridge.

If V_{GS}, on any active gate drive output, goes below the gate drive undervoltage warning (V_{GSUV}), the general fault flag will be active and the corresponding gate drive undervoltage bit (AHU, ALU, BHU or BLU) will be set in the Diag 0 register. No other action will be taken. When V_{GS} rises above V_{GSUV} the general fault flag will be reset. The fault bits remain in the Diag 0 register until cleared.

MONITOR: LOGIC TERMINAL OVERVOLTAGE

Seven of the logic terminals are capable of being shorted to the main supply voltage, up to 50 V, without damage. These terminals are HA, HBn, LAn, LB, RESETn, ENABLE, and DIAG. The voltage on these pins (V_L) is monitored to provide an indication of a short-to-battery fault. If V_L on any of the terminals rises above the logic terminal overvoltage warning threshold (V_{LOV}), then the VLO bit will be set in the Status register and the general fault flag will be active. If the fault is on one of the input terminals and the ESF bit is set, then all gate drive outputs will be disabled. A fault on the DIAG terminal will have no effect on the gate drive outputs. When V_L on all terminals falls below the logic terminal overvoltage warning threshold (V_{LOV}), the fault flag will be reset and the outputs will be reactivated. The VLO bit remains in the Status register until cleared.

MONITOR: ENABLE WATCHDOG TIMEOUT

The ENABLE input provides a direct connection to all gate drive outputs and can be used as a safety override to immediately deactivate the outputs. The ENABLE input is programmed to operate as a direct logic control by default, but it can be monitored by a watchdog timer by setting the EWD bit to 1. In the direct mode, the input is not monitored other than for input overvoltage as described in the Logic Terminal Overvoltage section above. In watchdog mode, the first change of state on the ENABLE input will activate the gate drive outputs under command from the corresponding phase control signals, and a watchdog timer is started. The ENABLE input must then change state before the end of the ENABLE timeout period (t_{ETO}). If the ENABLE input does not change before the end of the timeout period, then all gate drive outputs will be driven low, the ETO bit will be set in the Status register, and the general fault flag will be active. Any following change of state on the ENABLE input will reactivate the gate drive outputs and reset the general fault flag. The ETO bit remains in the Status register until cleared.

Power Bridge and Load Faults

BRIDGE: OVERCURRENT DETECT

The output from the sense amplifier can be compared to an overcurrent threshold voltage (V_{OCT}) to provide indication of overcurrent events. V_{OCT} is generated by a 4-bit DAC with a resolution of 300 mV and defined by the contents of the OCT[3:0] variable and the contents of the SAO[3:0] variable. V_{OCT} is approximately defined as:

$$V_{OCT} = [(n + 1) \times 300\ mV]$$

where n is a positive integer defined by OCT[3:0].

Any offset programmed on SAO[3:0] is applied to both the current sense amplifier outputs, CSOx, and the Overcurrent threshold (V_{OCT}), and has no effect on the overcurrent threshold (I_{OCT}). The relationship between the threshold voltage and the threshold current is approximately defined as:

$$I_{OCT} = \frac{V_{OCT}}{(R_S \times A_V)}$$

where V_{OCT} is the overcurrent threshold voltage programmed by OCT[3:0], R_S is the sense resistor value in Ω, and A_V is the sense amp gain defined by SAG[2:0].

The output from the overcurrent comparator is filtered by an overcurrent qualifier circuit. This circuit uses a timer to verify that the output from each comparator is indicating a valid overcurrent event. The qualifier can operate in one of two ways—debounce or blanking—selected by the OCQ bit.

In the default debounce mode, a timer is started each time a comparator output indicates on overcurrent detection when the corresponding low-side MOSFET is active. This timer is reset when the comparator changes back to indicate normal operation. If the debounce timer reaches the end of the timeout period, set by t_{OCQ}, then the overcurrent event is considered valid, and the corresponding overcurrent bit (OCA or OCB) will be set in the Diag 2 register.

In the optional blanking mode, a timer is started when a low-side gate drive is turned on. The output from the comparator is ignored (blanked) for the duration of the timeout period, set by

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t_{OCQ}. If a comparator output indicates an overcurrent event when the blanking timer is not active, then the overcurrent event is considered valid, and the corresponding overcurrent bit (OCA or OCB) will be set in the Diag 2 register.

The duration of the overcurrent qualifying timer (t_{OCQ}) is determined by the contents of the TOC[3:0] variable. t_{OCQ} is approximately defined as:

$$t_{OCQ} = n \times 500\ ns$$

where n is a positive integer defined by TOC[3:0].

When a valid overcurrent is detected, no action is taken. Only the OCA or OCB bits are set and remain in the Diag 2 register until cleared.

BRIDGE: OPEN-LOAD DETECT

Two open-load fault detection methods are provided: an on-state current monitor and an off-state open-load detector. An on-state is defined by the state of the gate drive outputs as one high-side switched on and the low-side in the opposite phase switched on. The resulting two combinations are the only ones where current can be passed through the low-side sense resistor. An off-state is defined by the state of the gate drive outputs as all MOSFETs switched off. In this state, the load connections are high impedance and can be used to detect the presence or otherwise of a load.

ON-STATE OPEN-LOAD DETECTION

When AOL = 0, the on-state open-load detection will be completely inactive. The on-state open-load detection is only enabled when AOL = 1 and either GHA and GLB are on together, or GHB and GLA are on together.

During the on-state, the A3924 compares the output from the sense amplifier against the open-load threshold voltage (V_{OLTON}) to provide indication of on-state open-load events. V_{OLTON} is generated by an internal 4-bit DAC with a resolution of 25 mV and defined by the contents of the OLT[3:0] variable. V_{OLTON} is approximately defined as:

$$V_{OLTON} = (n + 1) \times 25\ mV$$

where n is a positive integer defined by OLT[3:0].

Any offset programmed on SAO[3:0] is applied to both the current sense amplifier outputs, CSOx, and the V_{OLTON} threshold and has no effect on the open-load detect threshold current threshold (I_{OLT}). The relationship between the threshold voltage and the threshold current is approximately defined as:

$$I_{OLT} = \frac{V_{OLTON}}{(R_S \times A_V)}$$

where V_{OLTON} is the open-load threshold voltage programmed by OLT[3:0], R_S is the sense resistor value in Ω, and A_V is the sense amp gain defined by SAG[2:0].

If the output of the sense amplifier is less than V_{OLTON} during the on-state, then a timer is allowed to increment. If the output of the amplifier is higher than V_{OLTON} during the on-state, then the timer is reset. If the timer reaches the open-load timeout value t_{OLTO} (typically 100 ms), then the general fault flag will be active and the open-load fault bit (OL) will be set in the Diag 2 register indicating a valid open-load condition.

As soon as the output of the amplifier is higher than V_{OLTON} during the on-state, then the general fault flag will be reset but the OL bit remains in the Diag 2 register until cleared.

If the sense amplifier is not used in an application, then the on-state open-load detection can be completely disabled by setting AOL to 0.

OFF-STATE OPEN-LOAD DETECTION

When DOO = 1, the off-state open-load detection will be completely disabled. The off-state open-load detection is only enabled when DOO = 0 and all gate drive outputs are off. In the off-state, a current sink (I_{OLTS}) is applied to the SB terminal and a current source (I_{OLTT}) is applied to the SA terminal.

I_{OLTS} is typically 10 mA, which is low enough to allow the A3924 to survive a short to VBB on the SB terminal during the off-state without damage, and high enough to discharge any output capacitance in an acceptable time.

The value of I_{OLTT} is selected by the OLI bit. When OLI = 0, I_{OLTT} = 100 µA; when OLI = 1, I_{OLTT} = 400 µA.

The sink current (I_{OLTS}) pulls the SB terminal to ground, once any energy remaining in the load, when entering the off state, has dissipated. The source current (I_{OLTT}) applies a test current to the load. As the sink current is much larger than the source current, the current through the load will be the source current. The voltage at the SB terminal (VSB) should be close to zero and the voltages at the SA terminal with respect to that on the SB terminal (V_{SA}-V_{SB}) will allow the load resistance to be measured. V_{SA}-V_{SB} is compared to a fixed threshold (V_{OLTOFF}) of typically 1 V. If V_{SA}-V_{SB} is less than V_{OLTOFF}, then a load is assumed to be present. If V_{SA}-V_{SB} is greater than V_{OLTOFF}, then a timer is started. If the timer reaches the open-load timeout value t_{OLTO} (typically 100 ms), then the general fault flag will be active and the open-load fault bit (OL) will be set in the

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Diag 2 register indicating a valid open-load condition.

When OLI = 0, the threshold for load resistance is 10 kΩ; when OLI = 1, the threshold is 2.5 kΩ. So any load resistance greater than 10 kΩ or 2.5 kΩ respectively is indicated as an open load.

If the bridge exits, the off-state at any time before the timeout is complete, then the timer is reset without indicating an open load.

If V_{SA}-V_{SB} becomes less than V_{OLTOFF}, or if the bridge exits the off-state after the open-load fault condition has been detected, then the general fault flag will be reset, but the OL bit remains in the Diag 2 register until cleared.

BRIDGE: BOOTSTRAP CAPACITOR UNDERVOLTAGE FAULT

The A3924 monitors the individual bootstrap capacitor charge voltages to ensure sufficient high-side drive. It also includes an optional bootstrap capacitor charge management system (bootstrap manager) to ensure that the bootstrap capacitor remains sufficiently charged under all conditions. The bootstrap manager is enabled by default, but it may be disabled by setting the DBM bit to 1. This may be required in systems where the output MOSFET switching must only be allowed by the controlling processor.

If the bootstrap manager is disabled, then the user must ensure that the bootstrap capacitor does not become discharged below the bootstrap undervoltage threshold (V_{BCUV}), or a bootstrap fault will be indicated and the outputs disabled. This can happen with very high PWM duty cycles, when the charge time for the bootstrap capacitor is insufficient to ensure a sufficient recharge to match the MOSFET gate charge transfer during turn-on.

When the bootstrap manager is active, the bootstrap capacitor voltage must be higher than the turn-on voltage limit before a high-side drive can be turned on. If this is not the case, then the A3924 will attempt to charge the bootstrap capacitor by activating the complementary low-side drive. Under normal circumstances, this will charge the capacitor above the turn-on voltage in a few microseconds, and the high-side drive will then be enabled. The bootstrap voltage monitor remains active while the high-side drive is active, and if the voltage drops below the turn-off voltage, a charge cycle is also initiated.

If there is a fault that prevents the bootstrap capacitor charging during the managed recharge cycle, then the charge cycle will timeout after typically 200 µs, and the bootstrap undervoltage fault is considered to be valid. If the bootstrap manager is disabled and a bootstrap undervoltage is detected when a high-side MOSFET is active or being switched on then, the bootstrap undervoltage is immediately valid.

The action taken when a valid bootstrap undervoltage fault is detected and the fault reset conditions depend on the state of the ESF bit.

If ESF = 0, the fault state will be latched, the general fault flag will be active, the associated bootstrap undervoltage fault bit will be set, and the associated MOSFET will be disabled. The fault state and the general fault flag, but not the bootstrap undervoltage fault bit, will be reset by a low pulse on the RESETn input, by a power-on reset, or the next time the MOSFET is commanded to switch on. If the MOSFET is being driven with a PWM signal, then this will usually mean that the MOSFET will be turned on again each PWM cycle. If this is the case, and the fault condition remains, then a valid fault will again be detected after the timeout period and the sequence will repeat. In this case, the general fault flag will only be reset for the duration of the validation timer. The bootstrap undervoltage fault bit will only be cleared by a serial read of the Diag 2 register or by a power-on reset.

If ESF = 1, the fault will be latched, the general fault flag will be active, the associated bootstrap undervoltage fault bit will be set, and all MOSFETs will be disabled. The bootstrap undervoltage fault bit will remain set until cleared by a serial read of the Diag 2 register or by a power-on reset. The fault state and general fault flag will be reset by a low pulse on the RESETn input or by a power-on reset.

The bootstrap undervoltage monitor can be disabled by setting the VBS bit in the Mask 0 register. Although not recommended, this can allow the A3924 to operate below its minimum specified supply voltage level with a severely impaired gate drive. The specified electrical parameters may not be valid in this condition.

BRIDGE: MOSFET VDS OVERVOLTAGE FAULT

Faults on any external MOSFETs are determined by monitoring the drain-source voltage of the MOSFET and comparing it to a drain-source overvoltage threshold. There are two thresholds: V_{DSTH} for the high-side MOSFETs, and V_{DSTL} for the low-side. V_{DSTH} and V_{DSTL} are generated by internal DACs and are defined by the values in the VTH[5:0] and VTL[5:0] variables respectively. These variables provide the input to two 6-bit DACs with a least significant bit value of typically 50 mV. The output of the DAC produces the threshold voltage approximately defined as:

$$V_{DSTH} = n \times 50\,mV$$

where n is a positive integer defined by VTH[5:0], or:

$$V_{DSTL} = n \times 50\,mV$$

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where n is a positive integer defined by VTL[5:0].

The drain-source voltage for any low-side MOSFET is measured between the adjacent Sx terminal and the LSS terminal. Using the LSS terminal rather than the ground connection avoids adding any low-side current sense voltage to the real low-side drain-source voltage and avoids false VDS fault detection.

The drain-source voltage for any high-side MOSFET is measured between the adjacent Sx terminal and the VBRG terminal. Using the VBRG terminal rather than the VBB avoids adding any reverse diode voltage or high-side current sense voltage to the real high-side drain-source voltage and avoids false VDS fault detection.

The VBRG terminal is an independent low-current sense input to the top of the MOSFET bridge. It should be connected independently and directly to the common connection point for the drains of the power bridge MOSFETs at the positive supply connection point in the bridge. The input current to the VBRG terminal is proportional to the drain-source threshold voltage (V_{DSTH}), and is approximately:

$$I_{VBRG} = 11 \times V_{DSTH} + 160$$

where I_{VBRG} is the current into the VBRG terminal in µA, and V_{DSTH} is the drain-source threshold voltage described above.

Note that the VBRG terminal can withstand a negative voltage up to –5 V. This allows the terminal to remain connected directly to the top of the power bridge during negative transients, where the body diodes of the power MOSFETs are used to clamp the negative transient. The same applies to the more extreme case, where the MOSFET body diodes are used to clamp a reverse battery connection.

The output from each VDS overvoltage comparator is filtered by a VDS fault qualifier circuit. This circuit uses a timer to verify that the output from the comparator is indicating a valid VDS fault. The duration of the VDS fault qualifying timer (t_{VDQ}) is determined by the contents of the TVD[5:0] variable. t_{VDQ} is approximately defined as:

$$t_{VDQ} = n \times 100\ ns$$

where n is a positive integer defined by TVD[5:0]

The qualifier can operate in one of two ways: debounce mode, or blanking mode, selected by the VDQ bit.

In the default debounce mode, a timer is started each time the comparator output indicates a VDS fault detection when the corresponding MOSFET is active. This timer is reset when the comparator changes back to indicate normal operation. If the debounce timer reaches the end of the timeout period, set by t_{VDQ}, then the VDS fault is considered valid, and the corresponding VDS fault bit (ALO, AHO, BLO, or BHO) will be set in the diagnostic register.

In the optional blanking mode, a timer is started when a gate drive is turned on. The output from the VDS overvoltage comparator for the MOSFET being switched on is ignored (blanked) for the duration of the timeout period, set by t_{VDQ}. If the comparator output indicates an overcurrent event when the MOSFET is switched on, and the blanking timer is not active, then the VFS fault is considered valid, and the corresponding VDS fault bit (ALO, AHO, BLO, or BHO) will be set in the Diag 1 register.

The action taken when a valid VDS fault is detected and the fault reset conditions depend on the state of the ESF bit.

If ESF = 0 the fault state will be latched, the general fault flag will be active, the associated VDS fault bit will be set, and the associated MOSFET will be disabled. The fault state and the general fault flag will be reset by a low pulse on the RESETn input, by a serial read of the Diag 1 register, by a power-on reset or the next time the MOSFET is commanded to switch on. If the MOSFET is being driven with a PWM signal, then this will usually mean that the MOSFET will be turned on again each PWM cycle. If this is the case, and the fault conditions remains, then a valid fault will again be detected after the timeout period and the sequence will repeat. In this case, the general fault flag will only be reset for the duration of the validation timer. The VDS fault bit will only be cleared by a serial read of the Diag 1 register or by a power-on reset.

If ESF = 1, the fault will be latched, the general fault flag will be active, the associated VDS fault bit will be set, and all MOSFETs will be disabled. The fault state and the general fault flag will be reset by a serial read of the Diag 1 register, by a low pulse on the RESETn input or by a power-on reset. The VDS fault bit will only be reset by a serial read of the Diag 1 register or by a power-on reset.

If ESF = 0, care must be taken to avoid damage to the MOSFET where the VDS fault is detected. Although the MOSFET will be switched off as soon as the fault is detected at the end of the fault validation timeout, it is possible that it could still be damaged by excessive power dissipation and heating. To limit any damage to the external MOSFETs or the motor, the MOSFET should be fully disabled by logic inputs from the external controller.

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MOSFET FAULT STATE: SHORT TO SUPPLY

A short from either of the motor phase connections to the battery or VBB connection is detected by monitoring the voltage across the low-side MOSFETs in each phase using the respective Sx terminal and the LSSx terminal. This drain-source voltage is then compared to the low-side Drain-Source Threshold Voltage (V_{DSTL}). If the blanking timer is active, the output from the VDS overvoltage comparator will be ignored for t_{VDQ}. While the low-side VDS fault is detected, the associated VDS fault bit, ALO or BLO, will be set in the Diag 1 register and the associated MOSFET will be disabled. When ESF is set to 1, all MOSFETs will be disabled.

MOSFET FAULT STATE: SHORT TO GROUND

A short from either of the motor phase connections to ground is detected by monitoring the voltage across the high-side MOSFETs in each phase using the respective Sx terminal and the voltage at VBRG. This drain-source voltage is then compared to the high-side Drain-Source Threshold Voltage (V_{DSTH}). If the blanking timer is active the output from the VDS overvoltage comparator will be ignored for t_{VDQ}. While the low-side VDS fault is detected, the associated VDS fault bit, AHO or BHO, will be set in the Diag 1 register and the associated MOSFET will be disabled. When ESF is set to 1, all MOSFETs will be disabled.

MOSFET FAULT STATE: SHORTED WINDING

The short-to-ground and short-to-supply detection circuits will also detect a short across a motor phase winding. In most cases, a shorted winding will be indicated by a high-side and low-side fault latched at the same time in the Diag 1 register. In some cases, the relative impedances may only permit one of the shorts to be detected. In any case, when a short of any type is detected, the associated VDS fault bit, ALO, AHO, BLO, or BHO, will be set in the Diag 1 register and the associated MOSFET will be disabled.

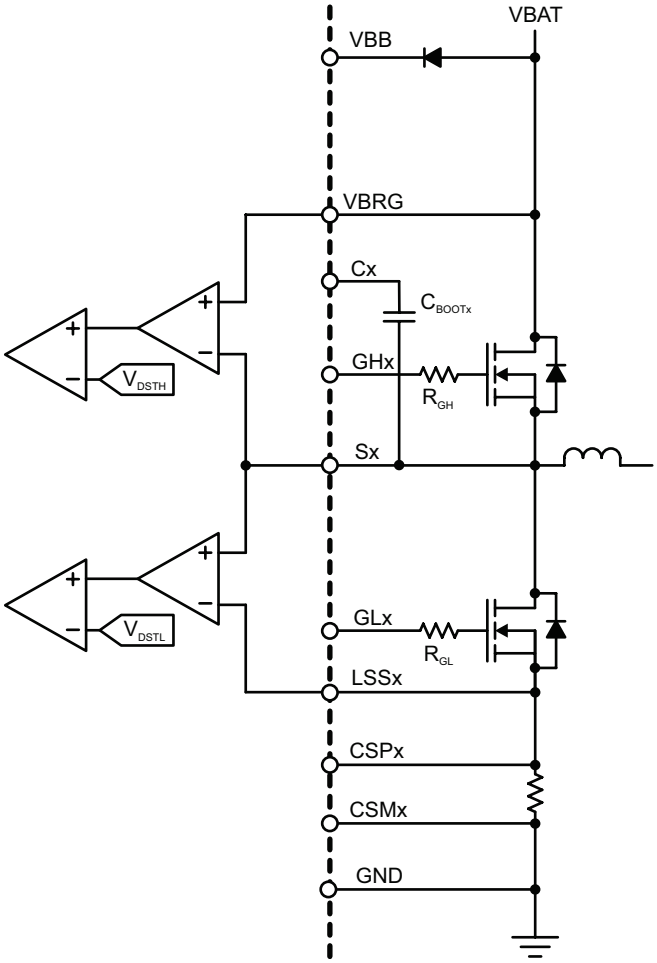

Figure 7: VDS Overvoltage Fault Detection

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Fault Action

The action taken when one of the diagnostic functions indicates a fault is listed in Table 5.

Table 5: Fault Actions

Fault Description	Disable Outputs		Fault State Latched
	ESF=0	ESF=1	
No Fault	No	No	–
Power-On Reset	Yes [1]	Yes [1]	No
VREG Undervoltage	Yes [1]	Yes [1]	No
Bootstrap Undervoltage	Yes [2]	Yes [1]	Yes
Logic Terminal Overvoltage	No	Yes [1]	No
Enable WD Timeout	Yes [1]	Yes [1]	No
Overtemperature	No	Yes [1]	No
VDS Fault	Yes [2]	Yes [1]	Yes
Serial Transmission Error	No	No	No
V3 Undervoltage	No	No	No
V3 Overvoltage	No	No	No
Vreg Overvoltage	No	No	No
VBB Undervoltage	Yes [1]	Yes [1]	No
VBB Overvoltage	No	No	No
VGS Undervoltage	No	No	No
Temperature Warning	No	No	No
Overcurrent	No	No	No
Open Load	No	No	No

[1] All gate drives in the affected bridge low, all MOSFETs in the affected bridge off
[2] Gate drive to the affected MOSFET low, only the affected MOSFET off

When a fault is detected, a corresponding fault state is considered to exist. In some cases, the fault state only exists during the time the fault is detected. In other cases, when the fault is only detected for a short time, the fault state is latched (stored) until reset. The faults that are latched are indicated in Table 5. Latched fault states are always reset when RESETn is taken low, a power-on-reset state is present, or when the associated fault bit is read through the serial interface. Any fault bits that have been set in the status or diagnostic register are only cleared when a power-on-reset state is present or when the associated fault bit is read through the serial interface. RESETn low will not clear the fault bits in the status or diagnostic registers.

The fault conditions power-on reset and VREG undervoltage are considered critical to the safe operation of the A3924 and the system. If these faults are detected, then the gate drive outputs are automatically driven low and all MOSFETs in the bridge held in the off-state. This state will remain until the fault is removed.

If the ENABLE watchdog monitor is enabled by setting EWD to 1, then this fault state is also considered critical to the safe operation of the A3924 and the system. If an ENABLE watchdog timeout is detected, then all gate drive outputs are driven low and all MOSFETs in the bridge held in the off-state. This state will remain until the watchdog timer is reset.

For the logic terminal overvoltage and overtemperature fault conditions, the action taken depends on the status of the ESF bit. If a fault is detected on any of these two diagnostics and ESF = 1, then all the gate drive outputs will be driven low and all MOSFETs in the bridge held in the off-state. This state will remain until the fault is removed. If ESF = 0, then the gate drive outputs will not be affected.

If a VDS fault or bootstrap undervoltage fault is detected, then the action taken will also depend on the status of the ESF bit, but these faults are handled as a special case. If a fault is detected on any of these two diagnostics and ESF = 1, then all the gate drive outputs will be driven low and all MOSFETs in the bridge held in the off-state. When ESF = 1, this fault state will be latched and remain until reset. If a VDS fault or bootstrap undervoltage fault is detected and ESF = 0, then only the gate drive output to the MOSFET where the fault was detected will be driven low and the MOSFET held in the off-state. When ESF = 0, the VDS fault or bootstrap undervoltage fault state will be latched but will be reset the next time the MOSFET is commanded to switch on.

For all other faults, the gate drive outputs will remain enabled.

Fault Masks

Individual diagnostics, except power-on reset, serial transmission error, and overtemperature, can be disabled by setting the corresponding bit in the mask register. Power-on reset cannot be disabled, because the diagnostics and the output control depend on the logic regulator to operate correctly. If a bit is set to one in the mask register, then the corresponding diagnostic will be completely disabled. No fault states for the disabled diagnostic will be generated, and no fault flags or diagnostic bits will be set. See Mask Register definition for bit allocation.

Care must be taken when diagnostics are disabled to avoid potentially damaging conditions.

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DIAGNOSTIC AND SYSTEM VERIFICATION

To comply with various aspects of safe system design, it is necessary for higher-level safety systems to verify that any diagnostics or functions used to guarantee safe operation must also be verified to ensure that theses critical functions are operating within specified tolerances.

There are four basic aspects to verification of diagnostic functions:

1. Verify connections
2. Verify comparators
3. Verify thresholds
4. Verify fault propagation

These have to be completed for each diagnostic. In addition, the operation of system functions not directly covered by diagnostics should also be verified.

The A3924 includes additional verification functions to help the system design comply with any safety requirements. Many of these functions can only be completed when the diagnostics are not required and must be commanded to run by the main system controller. These functions are referred to as “off-line” verification.

A few of the functions can be continuously active, but the results must be checked by the main system controller on a regular basis. These functions are referred to as “on-line” verification.

The frequency with which these off-line verification functions are run, or on-line verifications results are checked, will depend on the safety requirements of the system using the A3924.

Example methods of how to use these verification functions to verify system diagnostics are documented in the A3924 Safety Manual.

On-Line Verification

The following functions are permanently active and will set the appropriate bit in the verification result register to indicate that the verification has failed. No other action will be taken by the A3924. These verification functions verify that certain of the A3924 terminals are correctly connected to the power bridge circuit.

BRIDGE: VBRG DISCONNECTED

The VBRG terminal provides the common drain voltage reference for the high-side MOSFET VDS overvoltage detectors. If this becomes disconnected, then the high-side VDS detection will be invalid, and VDS overvoltage faults may not be detected. If VBRG is disconnected, the internal current sink from the input will ensure that the voltage at the VBRG terminal will fall. A comparator is provided to monitor the voltage between the main supply connection at the VBB terminal, and the voltage at VBRG ($V_{BB} – V_{BRG}$) is compared to the VBRG open threshold voltage (V_{BRO}), determined by the variable VTB[1:0] as:

$$V_{BRO} = (n + 1) \times 2\ V$$

where n is a positive integer defined by VTB[1:0] giving thresholds at 2 V, 4 V, 6 V, and 8 V.

Table 6: Verification Functions

Type	Function Verified	Operation
Connection	VBRG Connection	On-line
Connection	Phase connection	Off-line
Connection	Sense Amp Connection	On-line
Connection	LSS Connection	On-line
Monitor	Over current detectors	Off-line
Monitor	Phase state monitor	On-line
Diagnostic	Over temperature diagnostic	Off-line
Diagnostic	Temperature warning monitor	Off-line
Diagnostic	VBB undervoltage diagnostic	Off-line
Diagnostic	VBB overvoltage diagnostic	Off-line
Diagnostic	VREG diagnostics	Off-line
Diagnostic	VGS undervoltage diagnostic	Off-line
Diagnostic	Logic terminal diagnostic	Off-line
Diagnostic	Open load detectors	Off-line
Diagnostic	Bootstrap capacitor diagnostic	Off-line
Diagnostic	VDS overvoltage diagnostic	Off-line
Diagnostic	V3 regulator diagnotics	Off-line

If $V_{BB} – V_{BRG}$ exceeds the VBRG open threshold voltage, then the VBR bit will be set in the verification result register, all high-side VDS fault bits will be set in the Diag 1 register, and the general fault flag will be active. If ESF = 1, then all gate drive outputs will be disabled. When $V_{BB} – V_{BRG}$ falls below the falling VBRG open threshold voltage, $V_{BRO} – V_{BROHys}$, the fault flag will be reset and the outputs will be reactivated. The VBR bit remains in the verification result register until cleared and the VDS diagnostic bits remain in the Diag 1 register until cleared.

Note that, for accurate VBRG disconnect detection at V_{BB} less than 12 V, it is important to ensure the selected VBRG disconnect threshold (V_{BRO}) is no more than 4 V less than V_{BB}.

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BRIDGE: PHASE STATE MONITOR

The bridge phase connections at the SA and SB terminals are connected to a variable threshold comparator. The output of the comparator is then output at logic levels on the SAL and SBL terminals, and stored in the SAS and SBS phase state bits in the Verify Result 1 register, to provide a logic-level monitor of the state of the power bridge outputs to the load. The threshold for the two comparators, V_{PT}, is generated, as a ratio of the bridge voltage, by a 6-bit DAC and determined by the contents of the VPT[5:0] variable.

V_{PT} is approximately defined as:

$$V_{PT} = \frac{n}{64} V_{BRG}$$

where n is a positive integer defined by VPT[5:0].

V_{PT} can be programmed between 0 and 98.4% V_{BRG}.

SENSE AMPLIFIER DISCONNECT

Each sense amplifier includes continuous current sources, I_{SAD}, that will allow detection of an input open circuit condition. If an input open circuit is detected, then the SAD or SBD bit will be set in the verification result register depending on the sense amplifier.

BRIDGE: LSS DISCONNECTED

Each LSS terminal includes a continuous current source, I_{LU}, to V_{REG}, that will pull the LSS terminal up if there is no low-impedance path from LSS to ground. If the voltage at an LSS terminal with respect to ground rises above the LSS open threshold, V_{LSO}, then the LAD or LBD bit will be set in the Verify Result 0 register, the corresponding low-side VDS fault bit, ALO or BLO will be set in the Diag 1 register, and the general fault flag will be active. If ESF = 1, then all gate drive outputs will be disabled. When the voltage at the LSS terminal falls below the falling LSS open threshold voltage, $V_{LSO} - V_{LSOHys}$, the fault flag will be reset and the outputs will be reactivated. The LAD or LBD bit remains in the Verify Result 0 register until cleared and the VDS diagnostic bits remain in the Diag 1 register until cleared.

Off-Line Verification

The following functions are only active when commanded by setting the appropriate bit in the verification command register in addition to any required gate drive commands. If the function only verifies a connection, then a fail will set the appropriate bit in the verification result register. No other action will be taken by the A3924. If the function is to verify one of the diagnostic circuits in the A3924, then the verification is completed by checking that the associated fault bit is set in the diagnostic register.

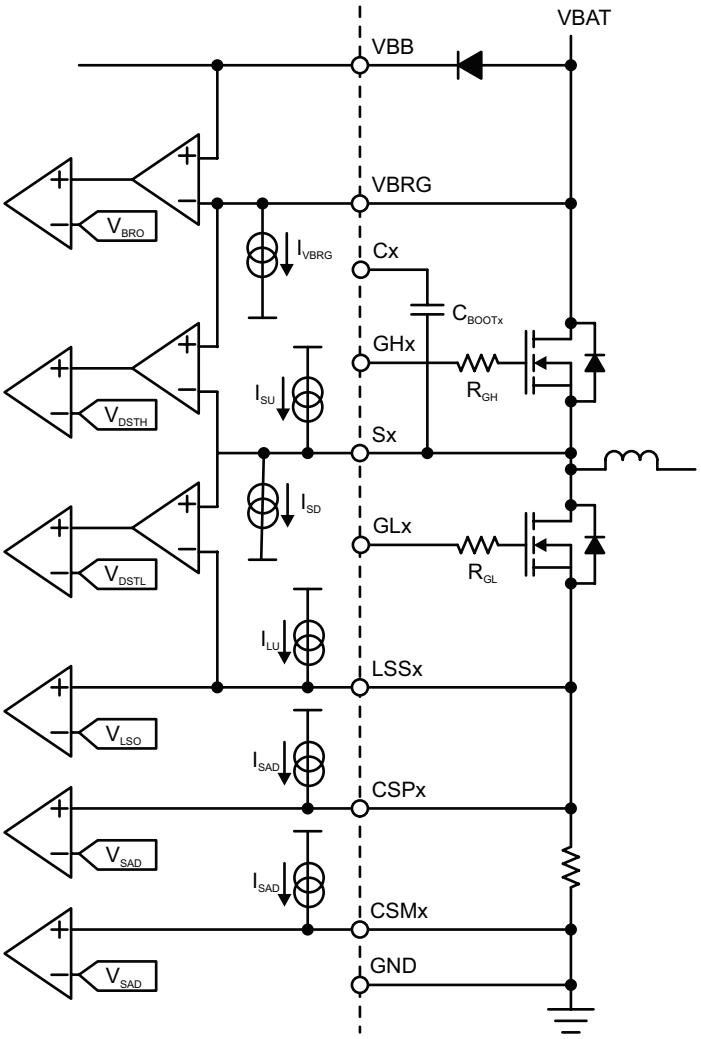

Figure 8: Bridge Terminal Connection Verification

BRIDGE: PHASE DISCONNECTED

The connections to each of the phases at the common node at the source of the high-side and the drain of the low-side MOSFET can be verified by a combination of MOSFET commands and test currents.

Both high-side and low-side tests must be performed to fully verify the connection for each phase.

Firstly, for the phase A high-side test, GHA is switched on using

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the serial command register bits or the logic input terminals. A pull-down current on phase A (I_{SD}) is then switched on by setting the YPH bit in the Verify Command 1 register to 1. The phase state monitor is then used to check that the SA connection is higher than the programmable threshold set by V_{PT}. If the phase state monitor output is high when YPH is reset to 0, then the PAC bit will be set in the Verify Result 0 register, indicating the phase A high-side is connected. The external controller is able to determine the time required to complete the verification as the PAC bit will only be set in the Verify Result 0 register when YPH is reset to 0. The high-side test is then repeated for phase B, with GHB switched on.

Secondly, for the phase A low-side test, GLA is switched on using the serial command register bits or the logic input terminals. A pull-up current on phase A (I_{SU}) is then switched on by setting the YPL bit in the Verify Command 1 register to 1. The phase state monitor is then used to check that the SA connection is lower than the programmable threshold set by V_{PT}. If the phase state monitor is low when YPL is reset to 0, then the PAC bit will be set in the Verify Result 0 register, indicating the phase B low-side is connected. The external controller is able to determine the time required to complete the verification as the PAC bit will only be set in the Verify Result 0 register when YPL is reset to 0. The low-side test is then repeated for phase B, with GLB switched on.

Note that, during verification of the phase connections, the VDS overvoltage detection should be masked to avoid a VDS fault condition being detected and disabling the MOSFET under verification.

VERIFY: VREG UNDERVOLTAGE

The VREG undervoltage detector is verified by setting the YRU bit in the Verify Command 0 register to 1. This applies a voltage to the comparator that is lower than the undervoltage threshold and should cause the general fault flag to be active and a VREG undervoltage fault bit, VRU, to be latched in the Diag 1 register. When YRU is reset to 0, the general fault flag will be reset and the VRU bit will remain set in the Diag 1 register until cleared. If the VRU bit is not set, then the verification has failed.

VERIFY: VREG OVERVOLTAGE

The VREG overvoltage detector is verified by setting the YRO bit in the Verify Command 0 register to 1. This applies a voltage to the comparator that is higher than the overvoltage threshold and should cause the general fault flag to be active and a VREG overvoltage fault bit, VRO, to be latched in the Diag 1 register. When YRO is reset to 0, the general fault flag will be reset and the VRO bit will remain set in the Diag 1 register until cleared. If the VRO bit is not set, then the verification has failed.

VERIFY: TEMPERATURE WARNING

The temperature warning detector is verified by setting the YTW bit in the Verify Command 0 register to 1. This applies a voltage to the comparator that is lower than the temperature warning threshold and should cause the general fault flag to be active and a temperature warning fault bit (TW) to be latched in the Status register. When YTW is reset to 0, the general fault flag will be reset and the TW bit will remain set in the Status register until cleared. If the TW bit is not set, then the verification has failed.

VERIFY: OVERTEMPERATURE

The overtemperature detector is verified by setting the YOT bit in the Verify Command 0 register to 1. This applies a voltage to the comparator that is higher than the overtemperature threshold and should cause the general fault flag to be active and an overtemperature fault bit (OT) to be latched in the Status register. When YOT is reset to 0, the general fault flag will be reset and the overtemperature fault will remain in the Status register until cleared. If the OT bit is not set, then the verification has failed.

VERIFY: V3 REGULATOR UNDERVOLTAGE

The V3 regulator undervoltage detector is verified by setting the Y3U bit in the Verify Command 0 register to 1. This applies a voltage to the comparator that is lower than the V3 undervoltage threshold and should cause the general fault flag to be active and a V3 undervoltage fault bit, V3U, to be latched in the Diag 0 register. When Y3U is reset to 0, the general fault flag will be reset and the V3U bit will remain set in the Diag 0 register until cleared. If the V3U bit is not set, then the verification has failed.

VERIFY: V3 REGULATOR OVERVOLTAGE

The V3 regulator overvoltage detector is verified by setting the Y3O bit in the Verify Command 0 register to 1. This applies a voltage to the comparator that is higher than the V3 overvoltage threshold and should cause the general fault flag to be active and a V3 overvoltage fault bit, V3O, to be latched in the Diag 0 register. When Y3O is reset to 0, the general fault flag will be reset and the V3O bit will remain set in the Diag 0 register until cleared. If the V3O bit is not set, then the verification has failed.

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VERIFY: VBB SUPPLY UNDERVOLTAGE

The VBB undervoltage detector is verified by setting the YSU bit in the Verify Command 0 register to1.This applies a voltage to the comparator that is higher than the VBB overvoltage threshold and should cause the general fault flag to be active and the VBB overvoltage fault bit (VSO) to be latched in the Diag 2 register. When YSU is reset to 0, the general fault flag will be cleared, and the VSU bit will remain set in the Diag 2 register until cleared. If the VSU bit is not set, then the verification has failed.

VERIFY: VBB SUPPLY OVERVOLTAGE

The VBB overvoltage detector is verified by setting the YSO bit in the Verify Command 0 register to 1. This applies a voltage to the comparator that is higher than the VBB overvoltage threshold and should cause the general fault flag to be active and the VBB overvoltage fault bit (VSO) to be latched in the Diag 2 register. When YSO is reset to 0, the general fault flag will be reset and the VSO bit will remain set in the Diag 2 register until cleared. If the VSO bit is not set, then the verification has failed.

VERIFY: VGS UNDERVOLTAGE

The VGS undervoltage high-side detectors are verified by setting the YGU bit in the Verify Command 1 register to 1 and switching on the corresponding low-side MOSFET in sequence using the serial command register bits or the logic input terminals. This should cause the general fault flag to be active and the high-side VGS undervoltage fault bit (AHU or BHU) to be latched in the Diag 0 register. The VGS undervoltage low-side detectors are verified by setting the YGU bit in the Verify Command 1 register to 1 and switching on the corresponding high-side MOSFET using the serial command register bits or the logic input terminals. This should cause the low-side VGS undervoltage fault bit to be latched in the Diag 0 register. This must be repeated for each MOSFET to verify all VGS undervoltage comparators. When YGU is reset to 0 or all gate drives are commanded off, then the general fault flag will be reset, but the VGS undervoltage fault bits will remain in the Diag 0 register until cleared. If any VGS fault bit is not set after all MOSFETs have been switched, then the verification has failed for the corresponding comparator.

VERIFY: BOOTSTRAP CAPACITOR UNDERVOLTAGE FAULT

The bootstrap capacitor undervoltage detectors are verified by setting the YBU bit in the Verify Command 0 register to 1 and switching on a high-side MOSFET using the serial Control register bits or the logic input terminals. This should cause the general fault flag to be active and the corresponding bootstrap undervoltage fault bit (VA or VB) to be latched in the Diag 2 register. This must be repeated for each high-side MOSFET to verify all bootstrap undervoltage comparators. When YBU is reset to 0 or all gate drives are commanded off, then the general fault flag will be reset, but the bootstrap undervoltage faults will remain in the Diag 2 register until cleared. If any bootstrap undervoltage fault bit is not set after all MOSFETs have been switched, then the verification has failed for the corresponding comparator.

VERIFY: MOSFET VDS OVERVOLTAGE FAULT

The VDS overvoltage high-side detectors are verified by setting the YDO bit in the Verify Command 1 register to 1 and switching on the corresponding low-side MOSFET using the serial Control register bits or the logic input terminals. This should cause the general fault flag to be active and the high-side VDS overvoltage fault bit (AHO or BHO) to be latched in the Diag 1 register. The low-side detectors are verified by setting the YDO bit in the Verify Command 1 register to 1 and switching on the corresponding high-side MOSFET using the serial command register bits or the logic input terminals. This should cause the low-side VDS overvoltage fault bit, ALO or BLO, to be latched in the Diag 1 register. This must be repeated for each MOSFET to verify all VDS overvoltage comparators. When YDO is reset to 0 or all gate drives are commanded off, then the general fault flag will be reset, but the VDS overvoltage faults will remain in the Diag 1 register until cleared. If any VDS overvoltage fault bit is not set after all MOSFETs have been switched, then the verification has failed.

VERIFY: LOGIC TERMINAL OVERVOLTAGE

The logic terminal overvoltage detector is verified by setting the YLO bit in the Verify Command 0 register to 1. This applies a voltage to the comparator that is higher than the logic input overvoltage threshold and should cause the logic overvoltage fault bit (VLO) to be latched in the diagnostic register. When YLO is reset to 0, the general fault flag will be reset, but the VLO bit will remain set in the Status register until cleared. If the VLO bit is not set, then the verification has failed.

VERIFY: ENABLE WATCHDOG TIMEOUT

The ENABLE watchdog timeout is verified by setting the EWD bit to 1 to select the watchdog mode and then changing the state of the ENABLE input. This change of state will enable the gate drive outputs under command from the corresponding phase control signals and will start the watchdog timer. The ENABLE input must then be held in this state. At the end of the timeout period (t_{ETO}), the ETO bit should be set in the Status register. If the ETO bit is not set, then the verification has failed.

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VERIFY: OVERCURRENT DETECT AND SENSE AMPLIFIER

The overcurrent detectors are verified by setting the YOC bit in the Verify Command 1 register to 1. This will force the output of each sense amplifier to its positive full-scale output which can then be measured at the sense amplifier output. The sense amplifier outputs remain connected to the overcurrent comparators and the full-scale outputs apply a voltage to the comparators that is higher than the overcurrent threshold. This should cause both overcurrent fault bits, OCA and OCB, to be latched in the Diag 2 register. When YOC is reset to 0, the sense amplifier outputs will return to normal operation, but the OCA and OCB bits will remain set in the Diag 2 register until cleared. If the OCA and OCB bits are not set, then the verification has failed for the corresponding comparator.

Note that, during verification of the overcurrent detector, the overcurrent threshold voltage (V_{OCT}) plus any offset programmed on SAO[3:0] (V_{OOS}) must not exceed the sense amplifier full-scale output of 4.8 V.

If $V_{OCT} + V_{OOS}$ exceeds the sense amplifier full-scale output, then the OCA and OCB bits will not be set and the verification will fail.

VERIFY: ON-STATE OPEN-LOAD DETECTION AND SENSE AMPLIFIER

The on-state open-load detector is verified by setting the AOL bit in the Config 4 register to 1, setting the YOL bit in the Verify Command 1 register to 1, and switching GLB or GLA on. Setting the YOL bit to 1 will force the output of the sense amplifier to its zero current output (zero differential input) which can then be measured at the sense amplifier output. The sense amplifier output remains connected to the open-load comparator and the zero current output applies a voltage to the comparator that is lower than the open-load threshold. When YOL is first set to 1, any on-state open-load fault is cleared and the open-load timer is reset by the A3924 to indicate that the timeout is complete and the OL fault bit should be reset in the Diag 2 register. When YOL and AOL are reset to 0, the sense amplifier output will return to normal operation, but the OL bit will remain set in the Diag 2 register until reset. If the OL bit is not set then the verification has failed. If YOL is reset to 0 before the timeout has completed, then the verification will be terminated without setting any fault bits.

VERIFY: OFF-STATE OPEN-LOAD DETECTION

The off-state open-load detector is verified in two steps. The first step verifies the current source, comparator, and timer. The second step verifies the current sink. In both cases, all gate drive outputs must be low and all MOSFETs held in the off-state. The DOO bit in the Config 5 register must be set to 0 to activate off-state open-load detection. The state of the OP bit in the Verify Command 1 register determines which phase will be verified. If OP = 0, the phase A off-state open-load detector will be verified. If OP = 1, the phase B off-state open-load detector will be verified.

The first off-state open-load detector verification is started by setting the YOU bit in the Verify Command 1 register to 1, with the OP bit in the Verify Command 1 register set to 0. This connects a resistor to the phase A open-load current source such that the input voltage to the comparator is greater than the open-load detection voltage. It also turns off the open-load current sink, clears any open load faults, and resets the open-load timer. At the end of the timeout period, the YOU bit will be reset by the A3924 to indicate that the timeout is complete and the OL fault bit should be set in the Diag 2 register. When YOU is reset to 0, the resistor will be disconnected from the open-load current source and the OL bit will remain set in the Diag 2 register until reset. If YOU is reset to 0 before the timeout has completed, then the verification will be terminated without setting any fault bits.

The first off-state open-load detector verification is then repeated, for Phase B, with the OP bit in the Verify Command 1 register set to 1.

The second off-state open-load detector verification is started by setting the YOD bit in the Verify Command 1 register to 1, with the OP bit in the Verify Command 1 register set to 0. This connects a resistor to the phase A open-load current sink and the open-load comparator input such that the input voltage to the comparator is greater than the open-load detection voltage. It also turns off the open-load current source, clears any open-load faults and resets the open-load timer. At the end of the timeout period, the YOD bit will be reset by the A3924 to indicate that the timeout is complete and the OL fault bit should be set in the Diag 2 register. When YOD is reset to 0, the resistor will be disconnected from the open-load current sink and the comparator and the OL bit will remain set in the Diag 2 register until reset. If YOD is reset to 0 before the timeout has completed, then the verification will be terminated without setting any fault bits.

The second off-state open-load detector verification is then repeated, for Phase B, with the OP bit in the Verify Command 1 register set to 1.

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SERIAL INTERFACE

Serial Registers Definition*

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0: Config 0	0	0	0	0	WR	TOC3	TOC2	TOC1	TOC0	DT5	DT4	DT3	DT2	DT1	DT0	P
						1	1	1	1	1	0	0	0	0	0	
1: Config 1	0	0	0	1	WR	OCT3	OCT2	OCT1	OCT0	VTL5	VTL4	VTL3	VTL2	VTL1	VTL0	P
						1	0	0	1	0	1	1	0	0	0	
2: Config 2	0	0	1	0	WR	OCQ	VDQ	VTB1	VTB0	VTH5	VTH4	VTH3	VTH2	VTH1	VTH0	P
						0	0	0	0	0	1	1	0	0	0	
3: Config 3	0	0	1	1	WR	OLT3	OLT2	OLT1	OLT0	TVD5	TVD4	TVD3	TVD2	TVD1	TVD0	P
						1	0	0	0	0	1	0	0	0	0	
4: Config 4	0	1	0	0	WR	AOL	EWD	OLI	VRG	VPT5	VPT4	VPT3	VPT2	VPT1	VPT0	P
						0	0	0	1	1	0	0	0	0	0	
5: Config 5	0	1	0	1	WR		DOO	SAO3	SAO2	SAO1	SAO0		SAG2	SAG1	SAG0	P
						0	0	1	1	1	1	0	1	0	1	
6: Verify Command 0	0	1	1	0	WR	YSU	YTW	YOT	YRO	YRU	YBU	YLO	YSO	Y3U	Y3O	P
						0	0	0	0	0	0	0	0	0	0	
7: Verify Command 1	0	1	1	1	WR	OP	YPH	YPL	YDO	YOC		YGU	YOL	YOU	YOD	P
						0	0	0	0	0	0	0	0	0	0	
8: Verify Result 0	1	0	0	0	0					PBC	PAC	VBR		LBD	LAD	P
						0	0	0	0	0	0	0	0	0	0	
9: Verify Result 1	1	0	0	1	0						SBS	SAS		SBD	SAD	P
						0	0	0	0	0	0	0	0	0	0	
10: Mask 0	1	0	1	0	WR	V3O	V3U	VBS	TW			BHU	BLU	AHU	ALU	P
						0	0	0	0	0	0	0	0	0	0	
11: Mask 1	1	0	1	1	WR	VRO	VRU	VS	VLO			BHO	BLO	AHO	ALO	P
						0	0	0	0	0	0	0	0	0	0	
12: Diag 0	1	1	0	0	0	V3O	V3U					BHU	BLU	AHU	ALU	P
						0	0	0	0	0	0	0	0	0	0	
13: Diag 1	1	1	0	1	0	VRO	VRU					BHP	BLO	AHO	ALO	P
						0	0	0	0	0	0	0	0	0	0	
14: Diag 2	1	1	1	0	0	VSO	VSU		VB	VA			OCB	OCA	OL	P
						0	0	0	0	0	0	0	0	0	0	
15: Control	1	1	1	1	WR	DG1	DG0	DBM	ESF			BH	BL	AH	AL	P
						0	0	0	1	0	0	0	0	0	0	
Status	FF	POR	SE		OT	TW	VS	VLO	ETO	VR	V3	LDF	BSU	GSU	DSO	P
	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	

* Power-on-reset value shown below each input register bit.

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A three-wire synchronous serial interface, compatible with SPI, is used to control the features of the A3924. The SDO terminal can be used during a serial transfer to provide diagnostic feedback and readback of the register contents.

The A3924 can be operated without the serial interface using the default settings and the logic control inputs; however, application specific configurations and several verifications functions are only possible by setting the appropriate register bits through the serial interface. In addition to setting the configuration bits, the serial interface can also be used to control the bridge MOSFETs directly.

The serial interface timing requirements are specified in the Electrical Characteristics table and illustrated in Figure 2. Data is received on the SDI terminal and clocked through a shift register on the rising edge of the clock signal input on the SCK terminal. STRn is normally held high, and it is only brought low to initiate a serial transfer. No data is clocked through the shift register when STRn is high, allowing multiple slave units to use common SDI and SCK connections. Each slave then requires an independent STRn connection. The SDO output assumes a high-impedance state when STRn is high, allowing a common data readback connection.

When 16 data bits have been clocked into the shift register, STRn must be taken high to latch the data into the selected register. When this occurs, the internal control circuits act on the new data, and the registers are reset depending on the type of transfer.

If there are more than 16 rising edges on SCK, or if STRn goes high and there are fewer than 16 rising edges on SCK, the write will be cancelled without writing data to the registers. In addition, the diagnostic register will not be reset, and the SE bit will be set to indicate a data transfer error. This fault condition can be cleared by a subsequent valid serial write and by a power-on reset.

The first four bits (D[15:12]) in a serial word are the register address bits, giving the possibility of 16 register addresses. The fifth bit—WR (D[11])—is the write/read bit. When WR is 1, the following 10 bits (D[10:1]) clocked in from the SDI terminal are written to the addressed register. When WR is 0, the following 10 bits (D[10:1]) clocked in from the SDI terminal are ignored, no data is written to the serial registers, and the contents of the addressed register are clocked out on the SDO terminal.

The last bit in any serial transfer (D[0]) is a parity bit that is set to ensure odd parity in the complete 16-bit word. Odd parity means that the total number of 1s in any transfer should always be an odd number. This ensures that there is always at least one bit set to 1 and one bit set to 0, and it allows detection of stuck-at faults on the serial input and output data connections. The parity bit is not stored but generated on each transfer.

Register data is output on the SDO terminal msb first while STRn is low, and it changes to the next bit on each falling edge of SCK. The first bit, which is always the FF bit from the Status register, is output as soon as STRn goes low.

Registers 8, 9, 12, 13, and 14 contain verification results and diagnostic fault indicators and are read only. If the WR bit for these registers is set to 1, then the data input through SDI is ignored, and the contents of the Status register is clocked out on the SDO terminal then reset as for a normal write. No other action is taken. If the WR bit for these registers is set to 0, then the data input through SDI is ignored, and the contents of the addressed register is clocked out on the SDO terminal, and the addressed register is reset.

In addition to the addressable registers, a read-only Status register is output on SDO for all register addresses when WR is set to 1. For all serial transfers, the first five bits output on SDO will always be the first five bits from the Status register.

Configuration Registers

Six registers are used to configure the operating parameters of the A3924.

CONFIG 0: BRIDGE TIMING SETTINGS:

- TOC[3:0], a 4-bit integer to set the overcurrent verification time (t_{OCQ}) in 500 ns increments.
- DT[6:0], a 7-bit integer to set the dead time (t_{DEAD}) in 50 ns increments.

CONFIG 1: BRIDGE MONITOR SETTING:

- OCT[3:0], a 4-bit integer to set the overcurrent threshold voltage (V_{OCT}) in 300 mV increments.
- VTL[5:0], a 6-bit integer to set the low-side drain-source threshold voltage (V_{DSTL}) in 50 mV increments.

CONFIG 2: BRIDGE MONITOR SETTING:

- OCQ, selects the overcurrent time qualifier mode, blank or debounce.
- VDQ, selects the VDS qualifier mode, blank or debounce.
- VTB[1:0], a 2-bit integer to set the VBRG disconnect threshold voltage (V_{BRO}) in 2 V increments.
- VTH[5:0], a 6-bit integer to set the high-side drain-source threshold voltage (V_{DSTH}) in 50 mV increments.

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CONFIG 3: BRIDGE MONITOR SETTING:

- OLT[3:0], a 4-bit integer to set the open-load threshold voltage (V_{OLT}) in 25 mV increments.
- TVD[5:0], a 6-bit integer to set the VDS fault verification time (t_{VDQ}) in 100 ns increments.

CONFIG 4: BRIDGE MONITOR SETTING:

- AOL, activates on-state open-load detection.
- EWD, activates ENABLE watchdog monitor.
- OLI, selects the open-load test current.
- VRG, selects the regulator and gate drive voltage.
- VPT[5:0], a 6-bit integer to set the phase comparator threshold voltage (V_{PT}) as a ratio of the bridge voltage (V_{BRG}) in 1.56% increments from 0 to 98.4%.

CONFIG 5: SENSE AMP GAIN AND OFFSET:

- DOO, disables the off-state open-load detection.
- SAO[3:0], a 4-bit integer to set the sense amplifier offset between 0 and 2.5 V.
- SAG[2:0], a 3-bit integer to set the sense amplifier gain between 10 and 50 V/V.

Verification Registers

Four registers are used to manage the system and diagnostic verification features.

VERIFY COMMAND 0:

Individual bits to initiate off-line verification tests for temperature, VREG, bootstrap, logic overvoltage, and VBB diagnostics.

VERIFY COMMAND 1:

Individual bits to initiate off-line verification tests for phase disconnect, VDS, VGS, overcurrent, and open-load diagnostics.

VERIFY RESULT 0 (READ-ONLY):

Individual bits holding the results of phase disconnect, VBRG open, and LSS open verification tests. These bits are reset on completion of a successful read of the register.

VERIFY RESULT 1 (READ-ONLY):

Individual bits holding the results of phase state and sense amp verification tests. These bits are reset on completion of a successful read of the register.

Diagnostic Registers

In addition to the read-only Status register, five registers provide detailed diagnostic management and reporting. Two mask register allow individual diagnostics to be disabled, and three read-only diagnostic registers provide fault bits for individual diagnostic tests and monitors. If a bit is set to one in the mask register, then the corresponding diagnostic will be completely disabled. No fault states for the disabled diagnostic will be generated, and no fault flags or diagnostic bits will be set. These bits in the diagnostic registers are cleared on completion of a successful read of the register.

MASK 0:

Individual bits to disable V3, bootstrap, temperature warning, and VGS diagnostic monitors.

MASK 1:

Individual bits to disable VREG, VBB, logic, and VDS diagnostic monitors.

DIAGNOSTIC 0 (READ-ONLY):

Individual bits indicating faults detected in V3 and VGS diagnostic monitors.

DIAGNOSTIC 1 (READ-ONLY):

Individual bits indicating faults detected in VREG and VDS diagnostic monitors.

DIAGNOSTIC 2 (READ-ONLY):

Individual bits indicating faults detected in VBB, bootstrap, overcurrent, and open-load diagnostic monitors.

Control Register

The Control register contains one control bit for each MOSFET and some system function settings:

- DBM: disabled bootstrap management function.
- DG[1:0], 2 bits select the output that is to be routed to the DIAG terminal. The options are a general, active-low fault flag, a pulsed fault flag, a voltage indicating the approximate chip junction temperature, or the sense amplifier output offset voltage.
- ESF: defines the action taken when a short is detected. See diagnostics section for details of fault actions.
- BH,BL: MOSFET Control bits for Phase B.
- AH,AL: MOSFET Control bits for Phase A.

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Status Register

There is one Status register in addition to the 16 addressable registers. When any register transfer takes place, the first five bits output on SDO are always the most significant five bits of the Status register, irrespective of whether the addressed register is being read or written. (see Serial Timing diagram). The content of the remaining eleven bits will depend on the state of the WR bit input on SDI. When WR is 1, the addressed register will be written, and the remaining eleven bits output on SDO will be the least significant ten bits of the Status register followed by a parity bit. When WR is 0, the addressed register will be read, and the remaining eleven bits will be the contents of the addressed register followed by a parity bit. The two verification result registers and the three diagnostic registers are read-only, and the remaining eleven bits output on SDO will always be the contents of the addressed register followed by a parity bit, irrespective of the state of the WR bit input on SDI.

The read-only Status register provides a summary of the chip status by indicating if any diagnostic monitors have detected a fault. The most significant three bits of the Status register indicate critical system faults. Bits 10, 9, and 8 provide indicators for specific individual monitors, and the remaining bits are derived from the contents of the three diagnostic registers. The contents and mapping to the diagnostic registers are listed in Table 7.

The first and most significant bit in the register is the diagnostic status flag (FF). This is high if any bits in the Status register are set. When STRn goes low to start a serial write, SDO outputs the diagnostic status flag. This allows the main controller to poll the A3924 through the serial interface to determine if a fault has been detected. If no faults have been detected, then the serial transfer may be terminated without generating a serial read fault, by ensuring that SCK remains high while STRn is low. When STRn goes high, the transfer will be terminated, and SDO will go into its high-impedance state.

The second most significant bit is the POR bit. At power-up or after a power-on reset, the FF bit and the POR bit are set, indicating to the external controller that a power-on reset has taken place. All other diagnostic bits are reset, and all other registers are returned to their default state. Note that a power-on reset only occurs when the output of the internal logic regulator rises above its undervoltage threshold. Power-on reset is not affected by the state of the VBB supply or the VREG regulator output. In general, the VR and VRU bits will also be set following a power-on reset, as the regulators will not have reached their respective rising undervoltage thresholds until after the register reset is completed.

The third bit in the Status register is the SE bit, which indicates that the previous serial transfer was not completed successfully.

Bits 11, 10, 8, and 7 are the fault bits for the four individual monitors OT, TW, VLO, and ETO. If one or more of these faults are no longer present, then the corresponding fault bits will be reset following a successful read of the Status register. Resetting only affects latched fault bits for faults that are no longer present. For any static faults that are still present (e.g. overtemperature), the corresponding fault bit will remain set after the reset.

The remaining bits (VS, VR, V3, LDF, BSU, GSU, and DSO) are all derived from the contents of the diagnostic registers.These bits are only cleared when the corresponding contents of the diagnostic are read and reset—they cannot be reset by reading the Status register. A fault indicated on any of the related diagnostic register bits will set the corresponding status bit to 1. The related diagnostic register must then be read to determine the exact fault and clear the fault state if the fault condition has cleared.

Table 7: Status Register Mapping

Status Register Bit	Diagnostic	Related Diagnostic Register Bits
FF	Status flag	None
POR	Power-on reset	None
SE	Serial error	None
VS	VBB monitor	VSU, VSO
OT	Overtemperature	None
TW	Temperature warning	None
VLO	Logic OV	None
ETO	ENABLE timeout	None
VR	VREG monitor	VRU. VRO
V3	V3 monitor	V3U, V3O
LDF	Load monitor	OCA, OCB, OL
BSU	Bootstrap UV	VA, VB
GSU	VGS UV	AHU, ALU, BHU, BLU
DSO	VDS OV	AHO, ALO, BHO, BLO

UV = undervoltage, OV = overvolage

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SERIAL REGISTER INTERFACE

Serial Register Reference*

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0: Config 0	0	0	0	0	WR	TOC3	TOC2	TOC1	TOC0	DT5	DT4	DT3	DT2	DT1	DT0	P
						1	1	1	1	1	0	0	0	0	0	
1: Config 1	0	0	0	1	WR	OCT3	OCT2	OCT1	OCT0	VTL5	VTL4	VTL3	VTL2	VTL1	VTL0	P
						1	0	0	1	0	1	1	0	0	0	

* Power-on-reset value shown below each input register bit.

Config 0

TOC[3:0] – OVERCURRENT VERIFICATION TIME

$$t_{OCQ} = n \times 500\ ns$$

where n is a positive integer defined by TOC[3:0]. For example, for the power-on-reset condition TOC[3:0] = [1111], then t_{OCQ} = 7.5 µs.

The range of t_{OCQ} is 0 to 7.5 µs.

DT[5:0] – DEAD TIME

$$t_{DEAD} = n \times 50\ ns$$

where n is a positive integer defined by DT[5:0]. For example, for the power-on-reset condition DT[5:0] = [10 0000], then t_{DEAD} = 1.6 µs.

The range of t_{DEAD} is 100 ns to 3.15 µs. Selecting a value of 1 or 2 will set the dead time to 100 ns. A value of zero disables the dead time.

P – PARITY BIT

Ensures an odd number of 1s in any serial transfer.

Config 1

OCT[3:0] – OVERCURRENT THRESHOLD

$$V_{OCT} = (n + 1) \times 300\ mV$$

where n is a positive integer defined by OCT[3:0]. For example, for the power-on-reset condition OCT[3:0] = [1001], then V_{OCT} = 3 V.

The range of V_{OCT} is 0.3 to 4.8 V.

VTL[5:0] – LOW-SIDE VDS OVERVOLTAGE THRESHOLD

$$V_{DSTL} = n \times 50\ mV$$

where n is a positive integer defined by VTL[5:0]. For example, for the power-on-reset condition VTL[5:0] = [01 1000], then V_{DSTL} = 1.2 V.

The range of V_{DSTL} is 0 to 3.15 V.

P – PARITY BIT

Ensures an odd number of 1s in any serial transfer.

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Serial Register Reference*

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2: Config 2	0	0	1	0	WR	OCQ	VDQ	VTB1	VTB0	VTH5	VTH4	VTH3	VTH2	VTH1	VTH0	P
						0	0	0	0	0	1	1	0	0	0	
3: Config 3	0	0	1	1	WR	OLT3	OLT2	OLT1	OLT0	TVD5	TVD4	TVD3	TVD2	TVD1	TVD0	P
						1	0	0	0	0	1	0	0	0	0	

* Power-on-reset value shown below each input register bit.

Config 2

OCQ – OVERCURRENT TIME QUALIFIER MODE

OCQ	Qualifier	Default
0	Debounce	D
1	Blanking	

VDQ – VDS FAULT QUALIFIER MODE

VDQ	Qualifier	Default
0	Debounce	D
1	Blank	

VTB[1:0] – VBRG DISCONNECT THRESHOLD

$$V_{BRO} = (n + 1) \times 2\ V$$

where n is a positive integer defined by VTB[1:0]. For example, for the power-on-reset condition VTB[1:0] = [00], then V_{BRO} = 2 V.

The range of V_{BRO} is 2 V to 8 V.

VTH[5:0] – HIGH-SIDE VDS OVERVOLTAGE THRESHOLD

$$V_{DSTH} = n \times 50\ mV$$

where n is a positive integer defined by VTH[5:0]. For example, for the power-on-reset condition VTH[5:0] = [01 1000], then V_{DSTH} = 1.2 V

The range of V_{DSTH} is 0 to 3.15 V.

P – PARITY BIT

Ensures an odd number of 1s in any serial transfer.

Config 3

OLT[3:0] – ON-STATE OPEN LOAD THRESHOLD

$$V_{OLT} = (n + 1) \times 25\ mV$$

where n is a positive integer defined by OLT[3:0]. For example, for the power-on-reset condition OL[3:0] = [1000], then V_{OLT} = 225 mV.

The range of V_{OLT} is 25 to 400 mV.

TVD[5:0] – VDS VERIFICATION TIME

$$t_{VDQ} = n \times 100\ ns$$

where n is a positive integer defined by TVD[5:0]. For example, for the power-on-reset condition TVD[5:0] = [01 0000], then t_{VDQ} = 1.6 µs

The range of t_{VDQ} is 0 to 6.3 µs.

P – PARITY BIT

Ensures an odd number of 1s in any serial transfer.

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Serial Register Reference*

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
4: Config 4	0	1	0	0	WR	AOL	EWD	OLI	VRG	VPT5	VPT4	VPT3	VPT2	VPT1	VPT0	P
						0	0	0	1	1	0	0	0	0	0	
5: Config 5	0	1	0	1	WR		DOO	SAO3	SAO2	SAO1	SAO0		SAG2	SAG1	SAG0	P
						0	0	1	1	1	1	0	1	0	1	

* Power-on-reset value shown below each input register bit.

Config 4

AOL – ON-STATE OPEN-LOAD DETECT

AOL	On-State Open-Load Detect	Default
0	Inactive	D
1	Active	

EWD – ENABLE WATCHDOG

EWD	ENABLE Watchdog	Default
0	Inactive	D
1	Active	

OLI – OFF-STATE OPEN-LOAD TEST CURRENT

OLI	Test Current	Default
0	100 µA	D
1	400 µA	

VRG – V_{REG} VOLTAGE LEVEL

VRG	V_{REG} Voltage	Default
0	8 V	
1	13 V	D

VPT[5:0] – PHASE COMPARATOR THRESHOLD.

$$V_{PT} = \frac{n}{64} V_{BRG}$$

where n is a positive integer defined by VPT[5:0]. For example, for the power-on-reset condition VPT[5:0] = [10 0000], then V_{PT} = 50% V_{BRG}.

The range of V_{PT} is 0 to 98.4% V_{BRG}.

P – PARITY BIT

Ensures an odd number of 1s in any serial transfer.

Config 5

SAO[3:0] – SENSE AMP OFFSET

SAO	Offset	Default
0	0 mV	
1	0 mV	
2	100 mV	
3	100 mV	
4	200 mV	
5	300 mV	
6	400 mV	
7	500 mV	
8	750 mV	
9	1 V	
10	1.25 V	
11	1.5 V	
12	1.75 V	
13	2 V	
14	2.25 V	
15	2.5 V	D

where SAO is a positive integer defined by SAO[3:0].

SAG[2:0] – SENSE AMP GAIN

SAG	Gain	Default
0	10	
1	15	
2	20	
3	25	
4	30	
5	35	D

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SAG	Gain	Default
6	40	
7	50	

where SAG is a positive integer defined by SAG[2:0].

Config 5 (continued)

DOO – OFF-STATE OPEN-LOAD DETECT

DOO	Off-State Open-Load Detect	Default
0	Active	D
1	Inactive	

P – PARITY BIT

Ensures an odd number of 1s in any serial transfer.

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Serial Register Reference*

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
6: Verify Command 0	0	1	1	0	WR	YSU	YTW	YOT	YRO	YRU	YBU	YLO	YSO	Y3U	Y3O	P
						0	0	0	0	0	0	0	0	0	0	
7: Verify Command 1	0	1	1	1	WR	OP	YPH	YPL	YDO	YOC		YGU	YOL	YOU	YOD	P
						0	0	0	0	0	0	0	0	0	0	

* Power-on-reset value shown below each input register bit.

Verify Command 0

YSU – VBB SUPPLY UNDERVOLTAGE

YTW – TEMPERATURE WARNING

YOT – OVERTEMPERATURE

YRO – VREG OVERVOLTAGE

YRU – VREG UNDERVOLTAGE

YBU – BOOTSTRAP UNDERVOLTAGE

YLO – LOGIC OVERVOLTAGE

YSO – VBB SUPPLY OVERVOLTAGE

Y3U – V3 UNDERVOLTAGE

Y3O – V3 OVERVOLTAGE

Yxx	Verification	Default
0	Inactive	D
1	Active	

P – PARITY BIT

Ensures an odd number of 1s in any serial transfer.

Verify Command 1

OP

OP	Off-State Open-Load Phase Select	Default
0	Phase A	D
1	Phase B	

YPH – PHASE CONNECT HIGH-SIDE

YPL – PHASE CONNECT LOW-SIDE

YDO – VDS OVERVOLTAGE

YOC – OVERCURRENT

YGU – VGS UNDERVOLTAGE

YOL – ON-STATE OPEN-LOAD

YOU – OFF-STATE OPEN-LOAD CURRENT SOURCE

YOD – OFF-STATE OPEN-LOAD CURRENT SINK

Yxx	Verification	Default
0	Inactive	D
1	Active and Initiate	

P – PARITY BIT

Ensures an odd number of 1s in any serial transfer.

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Serial Register Reference*

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
8: Verify Result 0	1	0	0	0	0					PBC	PAC	VBR		LBD	LAD	P
						0	0	0	0	0	0	0	0	0	0	
9: Verify Result 1	1	0	0	1	0						SBS	SAS		SBD	SAD	P
						0	0	0	0	0	0	0	0	0	0	

* Power-on-reset value shown below each input register bit.

Verify Result 0 (read-only)

PBC – PHASE B CONNECT

PAC – PHASE A CONNECT

VBR – VBRG DISCONNECT

LBD – LSSB DISCONNECT

LAD – LSSA DISCONNECT

xxx	Verification Result	Default
0	Not Detected	D
1	Detected	

P – PARITY BIT

Ensures an odd number of 1s in any serial transfer.

Verify Result 1 (read-only)

SBS – PHASE B STATE

SAS – PHASE A STATE

SBD – SENSE AMP DISCONNECT

SAD – SENSE AMP DISCONNECT

xxx	Verification Result	Default
0	Not Detected	D
1	Detected	

P – PARITY BIT

Ensures an odd number of 1s in any serial transfer.

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Serial Register Reference*

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
10: Mask 0	1	0	1	0	WR	V3O	V3U	VBS	TW			BHU	BLU	AHU	ALU	P
						0	0	0	0	0	0	0	0	0	0	
11: Mask 1	1	0	1	1	WR	VRO	VRU	VS	VLO			BHO	BLO	AHO	ALO	P
						0	0	0	0	0	0	0	0	0	0	

* Power-on-reset value shown below each input register bit.

Mask 0

V3O – V3 OVERVOLTAGE

V3U – V3 UNDERVOLTAGE

VBS – BOOTSTRAP UNDERVOLTAGE

TW – TEMPERATURE WARNING

BHU – PHASE B HIGH-SIDE VGS UNDERVOLTAGE

BLU – PHASE B LOW-SIDE VGS UNDERVOLTAGE

AHU – PHASE A HIGH-SIDE VGS UNDERVOLTAGE

ALU – PHASE A LOW-SIDE VGS UNDERVOLTAGE

xxx	Fault Mask	Default
0	Fault Detection Permitted	D
1	Fault Detection Disabled	

P – PARITY BIT

Ensures an odd number of 1s in any serial transfer.

Mask 1

VRO – VREG OVERVOLTAGE

VRU – VREG UNDERVOLTAGE

VS – VBB OUT OF RANGE

VLO – LOGIC OVERVOLTAGE

BHO – PHASE B HIGH-SIDE VDS OVERVOLTAGE

BLO – PHASE B LOW-SIDE VDS OVERVOLTAGE

AHO – PHASE A HIGH-SIDE VDS OVERVOLTAGE

ALO – PHASE A LOW-SIDE VDS OVERVOLTAGE

xxx	Fault Mask	Default
0	Fault Detection Permitted	D
1	Fault Detection Disabled	

P – PARITY BIT

Ensures an odd number of 1s in any serial transfer.

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Serial Register Reference*

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
12: Diag 0	1	1	0	0	0	V3O	V3U					BHU	BLU	AHU	ALU	P
						0	0	0	0	0	0	0	0	0	0	
13: Diag 1	1	1	0	1	0	VRO	VRU					BHP	BLO	AHO	ALO	P
						0	0	0	0	0	0	0	0	0	0	
14: Diag 2	1	1	1	0	0	VSO	VSU		VB	VA			OCB	OCA	OL	P
						0	0	0	0	0	0	0	0	0	0	

* Power-on-reset value shown below each input register bit.

Diag 0 (read-only)

V3O – V3 OVERVOLTAGE

V3U – V3 UNDERVOLTAGE

BHU – PHASE B HIGH-SIDE VGS UNDERVOLTAGE

BLU – PHASE B LOW-SIDE VGS UNDERVOLTAGE

AHU – PHASE A HIGH-SIDE VGS UNDERVOLTAGE

ALU – PHASE A LOW-SIDE VGS UNDERVOLTAGE

xxx	Fault
0	No Fault Detected
1	Fault Detected

P PARITY BIT

Ensures an odd number of 1s in any serial transfer.

Diag 1 (read-only)

VRO – VREG OVERVOLTAGE

VRU – VREG UNDERVOLTAGE

BHO – PHASE B HIGH-SIDE VDS OVERVOLTAGE

BLO – PHASE B LOW-SIDE VDS OVERVOLTAGE

AHO – PHASE A HIGH-SIDE VDS OVERVOLTAGE

ALO – PHASE A LOW-SIDE VDS OVERVOLTAGE

xxx	Fault
0	No Fault Detected
1	Fault Detected

P – PARITY BIT

Ensures an odd number of 1s in any serial transfer.

Diag 2 (read-only)

VSO – VBB OVERVOLTAGE

VSU – VBB UNDERVOLTAGE

VB – PHASE B BOOTSTRAP UNDERVOLTAGE

VA – PHASE A BOOTSTRAP UNDERVOLTAGE

OCB – OVERCURRENT ON PHASE B

OCA – OVERCURRENT ON PHASE A

OL – OPEN LOAD

xxx	Fault
0	No Fault Detected
1	Fault Detected

P – PARITY BIT

Ensures an odd number of 1s in any serial transfer.

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Serial Register Reference*

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
15: Control	1	1	1	1	WR	DG1	DG0	DBM	ESF			BH	BL	AH	AL	P
						0	0	0	1	0	0	0	0	0	0	

* Power-on-reset value shown below each input register bit.

Control

DG[1:0] – SELECTS SIGNAL ROUTED TO DIAG WHEN STRn = 1

DG1	DG0	Signal on DIAG pin	Default
0	0	Fault– low true	D
0	1	Pulse Fault	
1	0	Temperature	
1	1	Sense amplifier	

DBM – DISABLE BOOTSTRAP MANAGER

DBM	Bootstrap Manager	Default
0	Active	D
1	Disabled	

ESF – ENABLE STOP ON FAIL

ESF	Recirculation	Default
0	No Stop on Fail. Report Fault	
1	Stop on Fail. Report Fault.	D

BH – PHASE B, HIGH-SIDE GATE DRIVE

BL – PHASE B, LOW-SIDE GATE DRIVE

AH – PHASE A, HIGH-SIDE GATE DRIVE

AL – PHASE A, LOW-SIDE GATE DRIVE

See Tables 2 and 3 for control logic operation.

P – PARITY BIT

Ensures an odd number of 1s in any serial transfer.

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Serial Register Reference*

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Status	FF	POR	SE		OT	TW	VS	VLO	ETO	VR	V3	LDF	BSU	GSU	DSO	P
	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	

* Power-on-reset value shown below each input register bit.

Status (read-only)

FF – DIAGNOSTIC REGISTER FLAG

POR – POWER-ON-RESET

SE – SERIAL ERROR

OT – OVERTEMPERATURE

TW – HIGH TEMPERATURE WARNING

VS – VBB OUT OF RANGE

VLO – LOGIC OVERVOLTAGE

ETO – ENABLE WATCHDOG TIMEOUT

VR – VREG OUT OF RANGE

V3 – V3 OUT OF RANGE

LDF – LOAD FAULT

BSU – BOOTSTRAP UNDERVOLTAGE

GSU – VGS UNDERVOLTAGE

DSO – VDS OVERVOLTAGE

xxx	Status
0	No Fault Detected
1	Fault Detected

P – PARITY BIT

Ensures an odd number of 1s in any serial transfer.

Status Register Bit Mapping

Status Register Bit	Related Diagnostic Register Bits
FF	None
POR	None
SE	None
OT	None
TW	None
VS	VSU, VSO
VLO	None
ETO	None
VR	VRU, VRO
V3	V3U, V3O
LDF	OC, OL
BSU	VA, VB
GSU	AHU, ALU, BHU, BLU
DSO	AHO, ALO, BHO, BLO

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APPLICATION INFORMATION

Power Bridge PWM Control

The A3924 provides individual high-side and low-side controls for each MOSFET drive in the bridge. This allows any full-bridge control scheme to be implemented by providing four input control signals. In addition, the sense of the control inputs to the A3924 are arranged to permit most of the common control schemes with only one or two control inputs.

When current in a load is only required to be controlled in a single direction during a specific operation, the most common control scheme used is slow decay with synchronous rectification. This applies two complementary PWM signal to one side of the bridge, while holding the other side of the bridge with one MOSFET on and the other off. The control inputs in the A3924 for each side of the bridge are a complementary pair. For phase A, the high-side control input is active-high, and the low-side is active-low. This means that the gate drives can be driven in a complementary mode with a single PWM input signal connected directly to both high-side and low-side control inputs. A dead timer is provided for each phase to ensure that current shoot-through (cross-conduction) is avoided. Figure 9 shows the control signal connections and the bridge operation for each combination. The graph shows the approximate effect of the PWM duty cycle on the average load current for each state of the DIR control signal. In this case, the current will only flow in one direction for each state of the DIR signal.

The sense of the control inputs are also complementary for each phase in a bridge. Phase A, high-side control input is active-high, while phase B high-side control input is active-low. This means that it is also possible to drive each bridge in fast decay mode (4-quadrant control) with a single PWM input signal, as shown in Figure 10. In this case, the single PWM signal can be used to control the average load current in both positive and negative directions. 100% duty cycle gives full positive load current, 0% gives full negative, and 50% gives zero average load current.

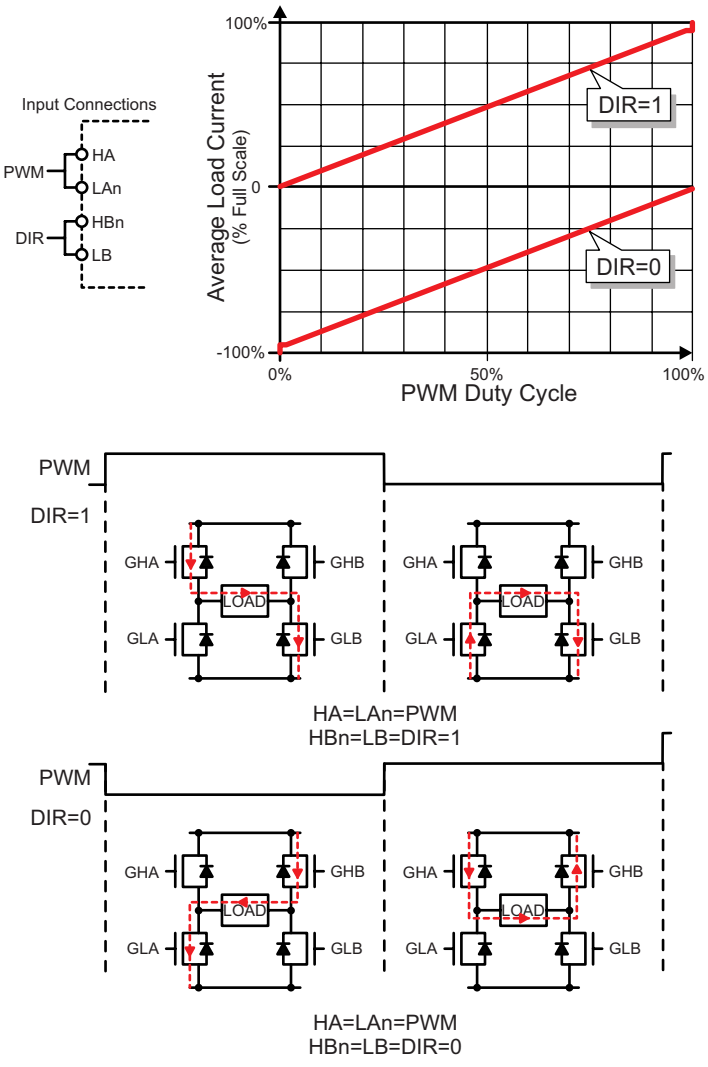

Figure 9: PWM and DIR Inputs, Slow Decay, SR

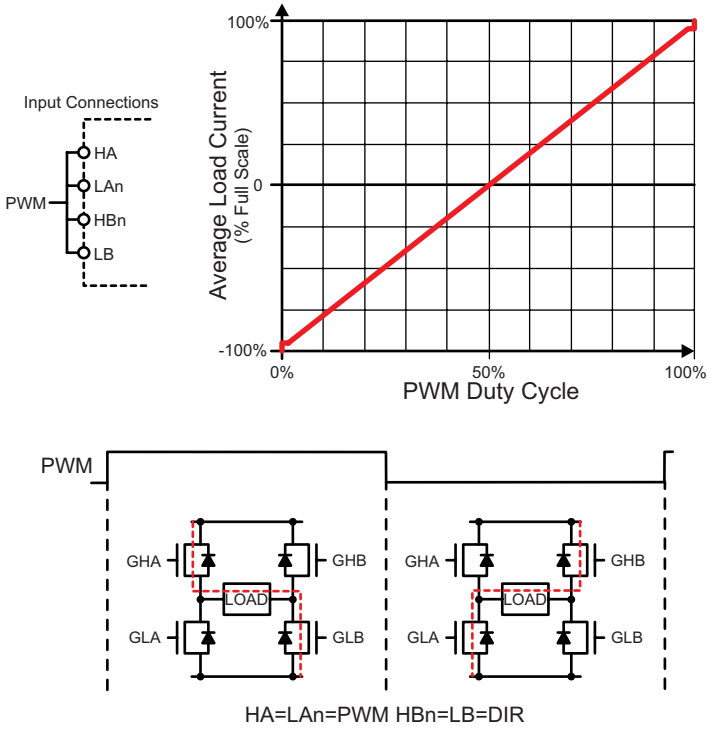

Figure 10: Single PWM Input, Fast Decay, SR

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Current Sense Amplifier Configuration

The gain (A_V) of the current sense amplifier is defined by the contents of the SAG[2:0] variable as:

SAG	GAIN
0	10
1	15
2	20
3	25

SAG	GAIN
4	30
5	35
6	40
7	50

The output offset zero point (output voltage corresponding to zero differential input voltage), V_{OOS}, is defined by the contents of the SAO[3:0] variable as:

SAO	V_{OOS}
0	0
1	0
2	100 mV
3	100 mV
4	200 mV
5	300 mV
6	400 mV
7	500 mV

SAO	V_{OOS}
8	750 mV
9	1 V
10	1.25 V
11	1.5 V
12	1.75 V
13	2 V
14	2.25 V
15	2.5 V

The current sense amplifier voltage output (V_{CSO}) is defined as:

$$V_{CSO} = [(V_{CSP} - V_{CSM}) \times A_V] + V_{OOS}$$

where ($V_{SCP} - V_{CSM}$) is the difference between the sense amplifier inputs, A_V is the gain and V_{OOS} is the offset.

The gain and output offset are selected to ensure the voltage at the C_{SO} output remains within the sense amplifier dynamic range (V_{CSOUT}) for both positive and negative current directions.

Figure 11 shows the effects that changing the gain and output offset have on the voltage at the C_{SO} output.

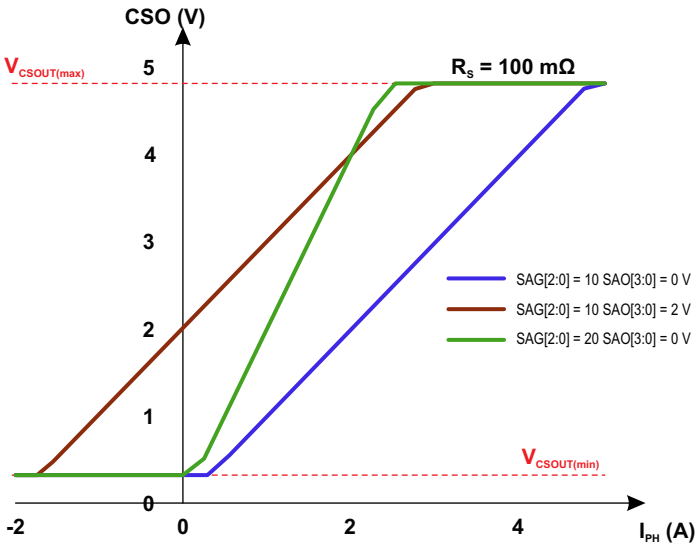

Figure 11: Positive and Negative Current Sensing with R_S = 100 mΩ

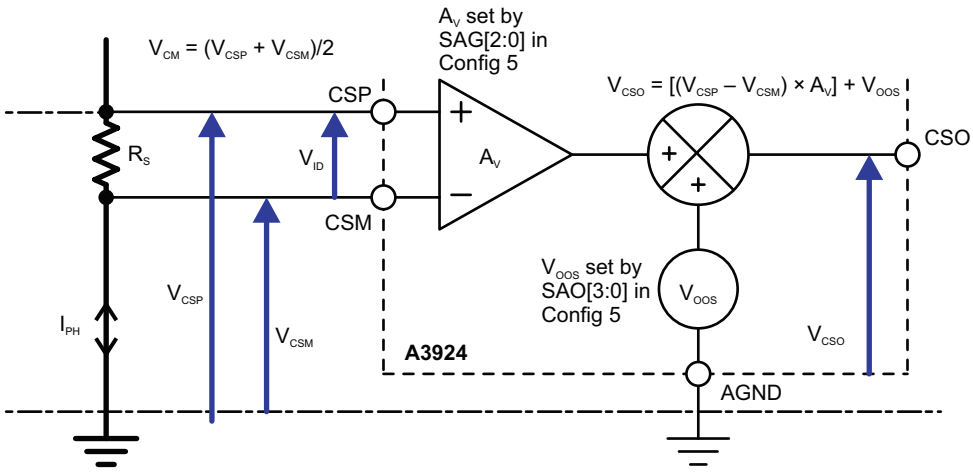

Figure 12: Typical Sense Amp Voltage Definitions

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Dead Time Selection

The choice of power MOSFET and external series gate resistance determines the selection of the dead time (t_{DEAD}). The t_{DEAD} should be made long enough to ensure that one MOSFET has stopped conducting before the complementary MOSFET starts conducting. This should also account for the tolerance and variation of the MOSFET gate capacitance, the series gate resistance, and the on-resistance of the driver in the A3924.

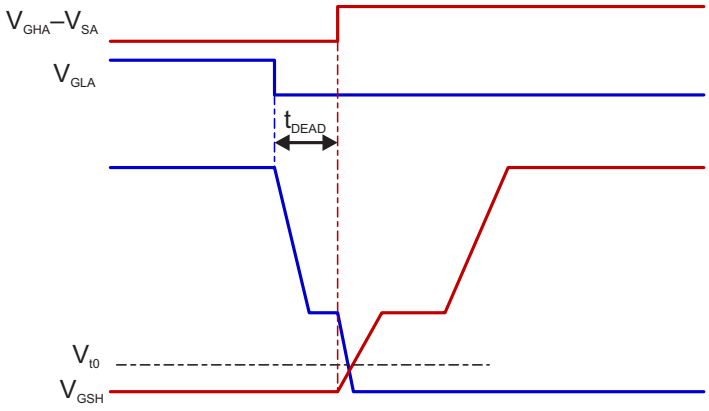

Figure 13: Minimum Dead Time

Figure 13 shows the typical switching characteristics of a pair of complementary MOSFETs. Ideally, one MOSFET should start to turn on just after the other has completely turned off. The point at which a MOSFET starts to conduct is the threshold voltage (V_{t0}). t_{DEAD} should be long enough to ensure that the gate-source voltage of the MOSFET that is switching off is just below V_{t0} before the gate-source voltage of the MOSFET that is switching on rises to V_{t0}. This will be the minimum theoretical t_{DEAD}, but in practice t_{DEAD} will have to be longer than this to accommodate variations in MOSFET and driver parameters for process variations and overtemperature.

Bootstrap Capacitor Selection

The A3924 requires two bootstrap capacitors: C_A and C_B. To simplify this description of the bootstrap capacitor selection criteria, generic naming is used here. For example, C_{BOOT}, Q_{BOOT}, and V_{BOOT} refer to any of the two capacitors, and Q_{GATE} refers to any of the two associated MOSFETs. C_{BOOT} must be correctly selected to ensure proper operation of the device: too large and time will be wasted charging the capacitor, resulting in a limit on the maximum duty cycle and PWM frequency; too small and there can be a large voltage drop at the time the charge is transferred from C_{BOOT} to the MOSFET gate.

To keep the voltage drop due to charge sharing small, the charge in the bootstrap capacitor (Q_{BOOT}) should be much larger than Q_{GATE}, the charge required by the gate:

$$Q_{BOOT} \gg Q_{GATE}$$

A factor of 20 is a reasonable value.

$$Q_{BOOT} = C_{BOOT} \times V_{BOOT} = Q_{GATE} \times 20$$

$$C_{BOOT} = \frac{Q_{GATE} \times 20}{V_{BOOT}}$$

where V_{BOOT} is the voltage across the bootstrap capacitor.

The voltage drop (ΔV) across the bootstrap capacitor as the MOSFET is being turned on can be approximated by:

$$\Delta V = \frac{Q_{GATE}}{C_{BOOT}}$$

So for a factor of 20, ΔV will be 5% of V_{BOOT}

The maximum voltage across the bootstrap capacitor under normal operating conditions is V_{REG} (max). However, in some circumstances, the voltage may transiently reach a maximum of 18 V, which is the clamp voltage of the Zener diode between the Cx terminal and the Sx terminal. In most applications, with a good ceramic capacitor, the working voltage can be limited to 16 V.

Bootstrap Charging

It is good practice to ensure the high-side bootstrap capacitor is completely charged before a high-side PWM cycle is requested. The time required to charge the capacitor (t_{CHARGE}), in µs, is approximated by:

$$t_{CHARGE} = \frac{C_{BOOT} \times \Delta V}{100}$$

where C_{BOOT} is the value of the bootstrap capacitor in nF and ΔV is the required voltage of the bootstrap capacitor. At power-up and when the drivers have been disabled for a long time, the bootstrap capacitor can be completely discharged. In this case, ΔV can be considered to be the full, high-side drive voltage (12 V); otherwise, ΔV is the amount of voltage dropped during the charge transfer, which should be 400 mV or less. The capacitor is charged whenever the Sx terminal is pulled low and current flows from the capacitor connected to the VREG terminal through the internal bootstrap diode circuit to C_{BOOT}.

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VREG Capacitor Selection

The internal reference (V_{REG}) supplies current for the low-side gate-drive circuits and the charging current for the bootstrap capacitors. When a low-side MOSFET is turned on, the gate-drive circuit will provide the high transient current to the gate that is necessary to turn the MOSFET on quickly. This current, which can be several hundred milliamperes, cannot be provided directly by the limited output of the VREG regulator, but must be supplied by an external capacitor (C_{REG}) connected between the VREG terminal and GND

The turn-on current for the high-side MOSFET is similar in value but is mainly supplied by the bootstrap capacitor. However, the bootstrap capacitor must then be recharged from C_{REG} through the VREG terminal. Unfortunately, the bootstrap recharge can occur a very short time after the low-side turn-on occurs. This means that the value of C_{REG} between VREG and GND should be high enough to minimize the transient voltage drop on VREG for the combination of a low-side MOSFET turn-on and a bootstrap capacitor recharge. For most applications, a minimum value of $20 \times C_{BOOT}$ is a reasonable. The maximum working voltage of C_{REG} will never exceed V_{REG}, so it can be as low as 15 V. However, it is recommended to use a capacitor with at least twice the maximum working voltage to reduce any voltage effects on the capacitance value. This capacitor should be placed as close as possible to the VREG terminal.

Supply Decoupling

Since this is a switching circuit, there will be current spikes from all supplies at the switching points. As with all such circuits, the power supply connections should be decoupled with a ceramic capacitor (typically 100 nF) between the supply terminal and ground. These capacitors should be connected as close as possible to the device supply terminal (V_{BB}) and the power ground terminal (GND).

Braking

The A3924 can be used to perform dynamic braking by either forcing all low-side MOSFETs on and all high-side MOSFETs off or, inversely, by forcing all low-side off and all high-side on. This will effectively short-circuit the back EMF of the motor, creating a braking torque. During braking, the load current (I_{BRAKE}) can be approximated by:

$$I_{BRAKE} = \frac{V_{bemf}}{R_L}$$

where V_{bemf} is the voltage generated by the motor and R_L is the resistance of the phase winding. Care must be taken during braking to ensure that the power MOSFETs' maximum ratings are not exceeded. Dynamic braking is equivalent to slow decay with synchronous rectification and all phases enabled.

The A3924 can also be used to perform regenerative braking. This is equivalent to using fast decay with synchronous rectification. Note that the supply must be capable of managing the reverse current, for example, by connecting a resistive load or dumping the current to a battery or capacitor.

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INPUT/OUTPUT STRUCTURES

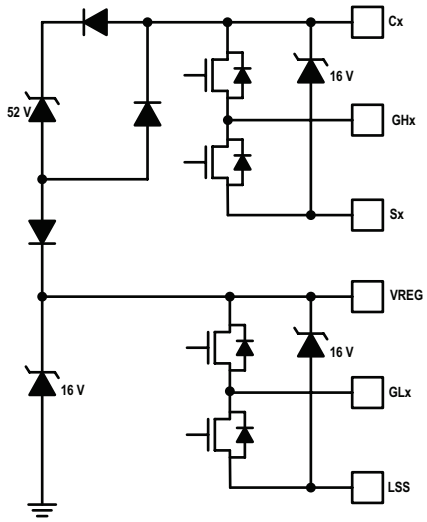

Figure 14A: Gate Drive Outputs

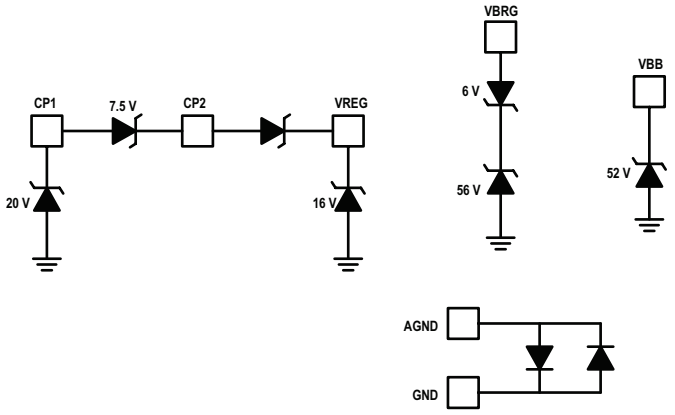

Figure 14B: Supplies

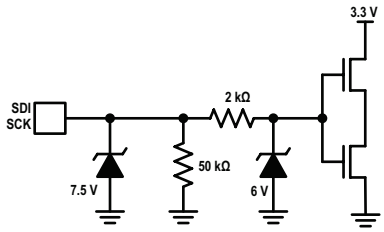

Figure 14C: SDI & SCK Inputs

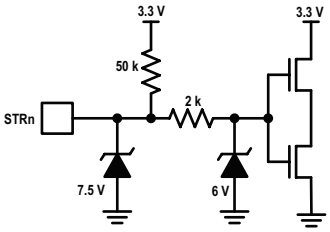

Figure 14D: STRn Input

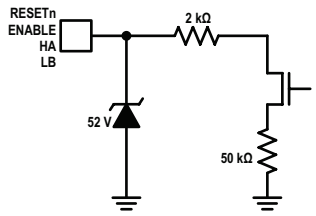

Figure 14E: RESETn, ENABLE, HA, & LB

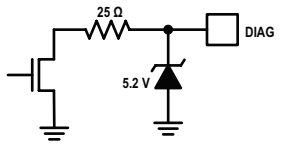

Figure 14F: DIAG Output

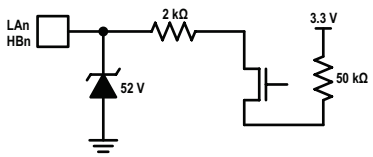

Figure 14G: LAn & HBn Inputs

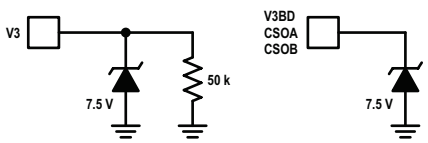

Figure 14H: V3 Input & V3BD, CSOA, & CSOB Outputs

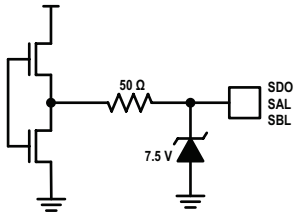

Figure 14I: SDO, SAL & SBL Outputs

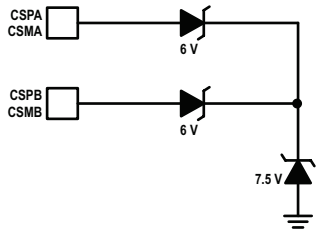

Figure 14J: CSPA, CSMA, CSPB, & CSMB Inputs

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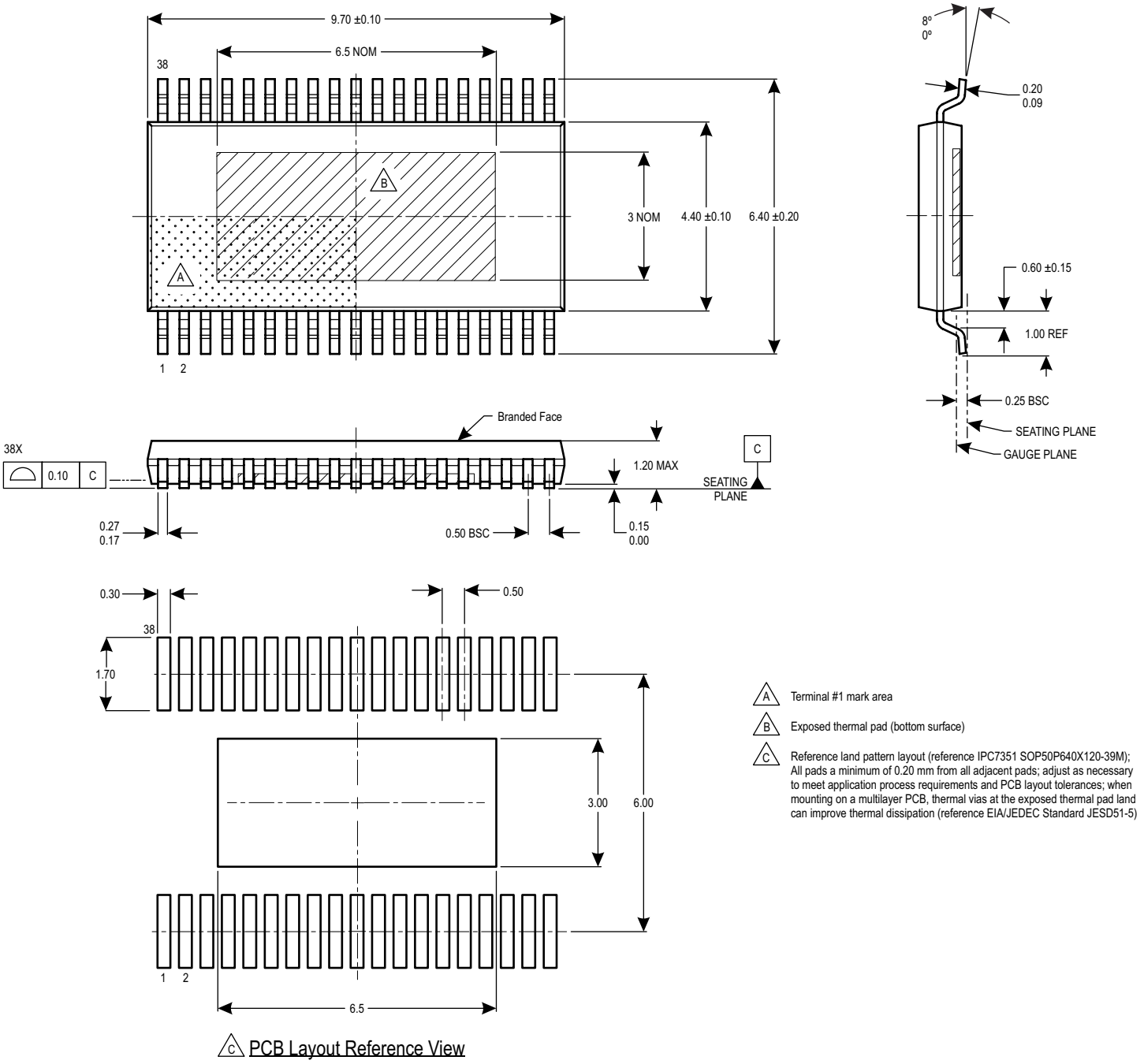
PACKAGE OUTLINE DRAWINGS

For Reference Only – Not for Tooling Use

(Reference JEDEC MO-153 BDT-1)
Dimensions in millimeters
NOT TO SCALE
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown



A Terminal #1 mark area

B Exposed thermal pad (bottom surface)

C Reference land pattern layout (reference IPC7351 SOP50P640X120-39M); All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

Figure 15: Package LV, 38-Pin eTSSOP with Exposed Pad

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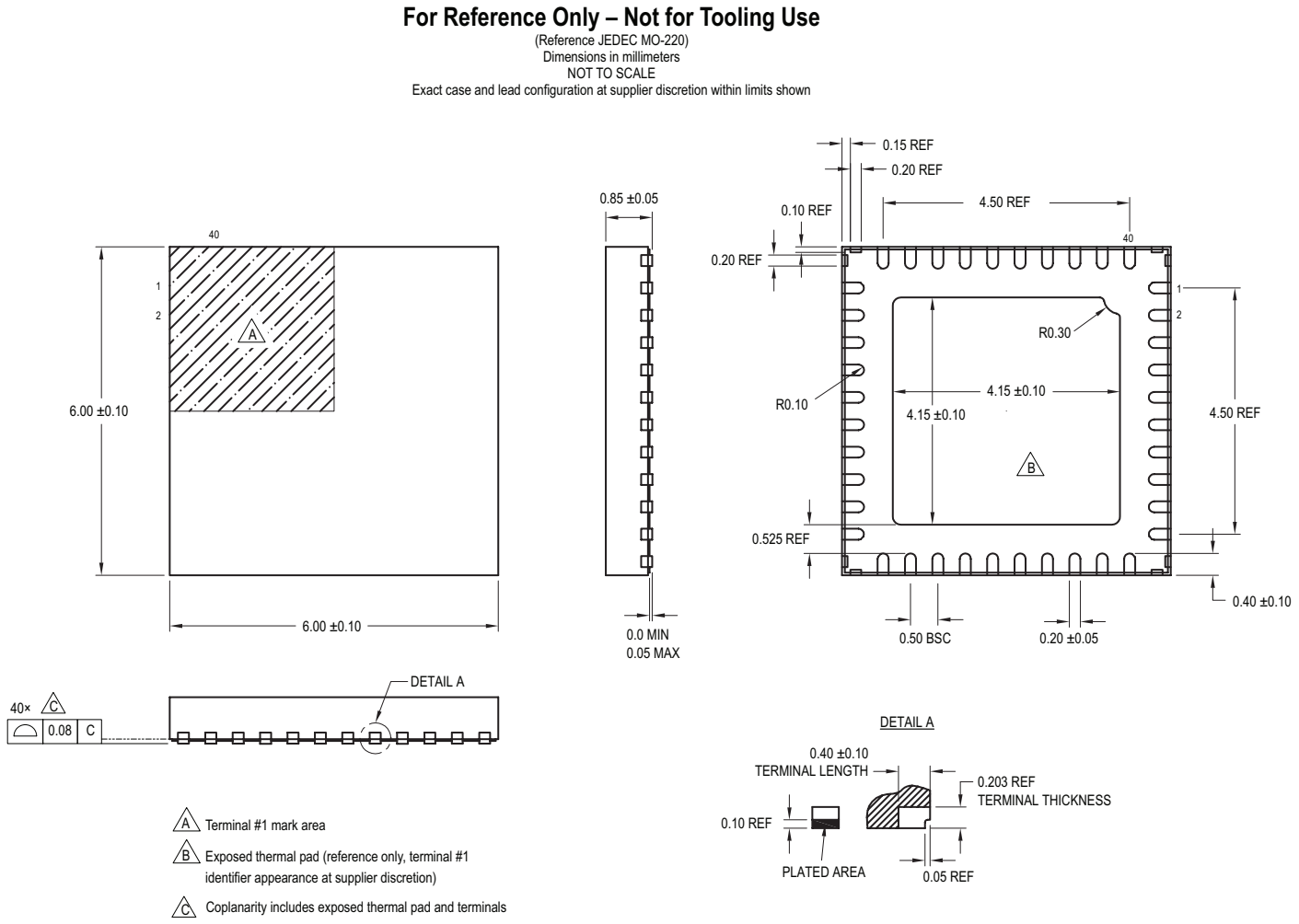

Figure 16: Package EV, Wettable Flank 40-Terminal eQFN with Exposed Pad

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Revision History

Number	Date	Description
–	March 8, 2016	Initial Release
1	February 1, 2017	Updated VBB Quiescent Current max value (page 6, 1st condition), Pull-down On-Resistance max values (page 7), VBRG Input Voltage min value (page 10), High-Side VDS Threshold conditions and values (page 10), Low-Side VDS Threshold Offset conditions and values (page 10)
2	March 29, 2017	Added EV-40 package option
3	February 27, 2018	Updated Table of Contents (page 3) and V_{REG} characteristic (page 8)
4	June 25, 2018	Updated Output Offset Error test condition (page 11); minor editorial updates
5	August 23, 2019	Minor editorial updates
6	November 30, 2021	Updated Sense Amplifier Output value, Bridge Low-Side Source Terminal value (page 4), Temperature Warning Threshold symbol (page 13), Off-State Open-Load Detection section (pages 27-28).
7	March 11, 2024	Part variant A3924KEVSR-J status changed to Last-Time Buy (page 2).

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