THE DATASHEET OF

A6270KLPTR-T-1

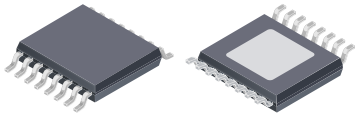
www.win-source.net 0086-755-83957316

High-Current, Two-Channel, Automotive LED Controller

FEATURES AND BENEFITS

- AEC-Q100 qualified
- 5.3 to 40 V supply; operates down to 5.1 V, when enabled
- LED current programmed independently with two external MOSFETs
- Flexible LED dimming options
  - □ Integrated PWM dimming set by resistors
  - □ External PWM dimming set by microcontroller
  - □ Analog voltage control for PWM dimming
  - □ Current slew rate limit during PWM dimming
- LED current derating for elevated V_{IN}
- LED current derating for elevated junction temperature
- Low regulation voltage for low power dissipation
- Extensive fault detection and protection
  - □ Drain short-to-ground detection
  - □ Drain short-to-VIN, open LED, V_{IN} undervoltage, and thermal protection
- Parallel IC operation for higher number of strings with good matching

PACKAGE:



16-pin TSSOP with exposed thermal pad (suffix LP)

Not to scale

DESCRIPTION

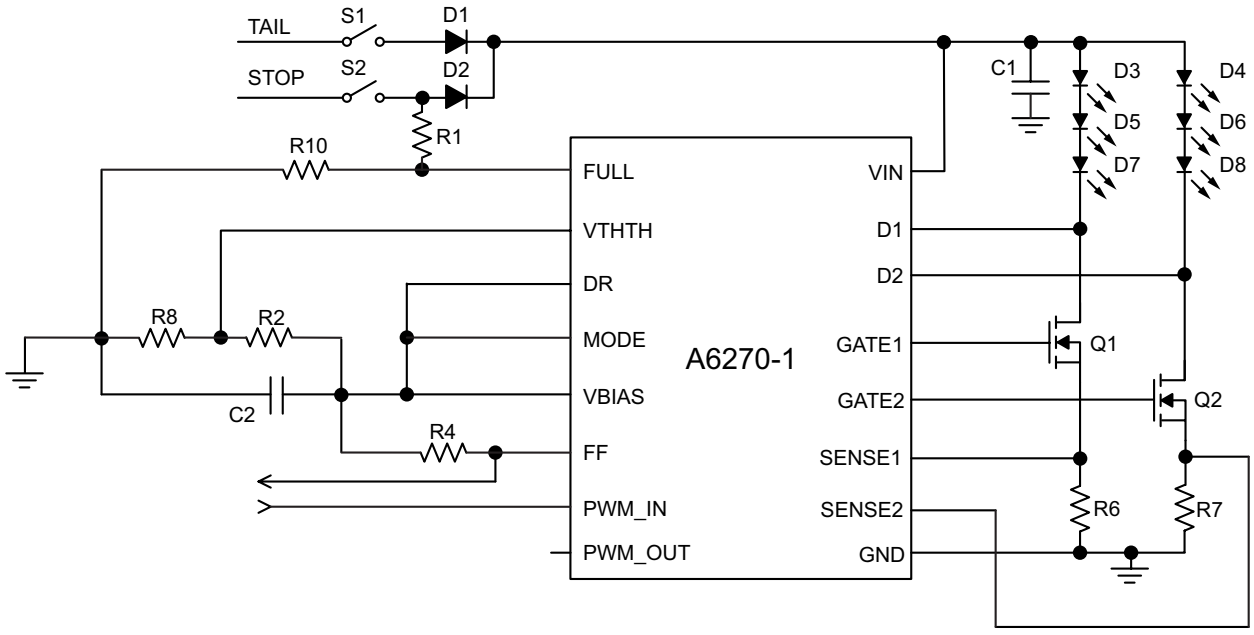
The A6270-1 is a linear, programmable current controller capable of accurately regulating LED current in two strings with external MOSFETs. The LED current can be switched between high current and low current for Stop/Tail or DRL/position applications. The two LED current levels from each output are set by two sense resistors. Current reference accuracy for each string current is better than ±4%.

Driving LEDs with constant current ensures safe operation with maximum possible light output. ICs can be connected in parallel in a master-slave arrangement for larger lighting applications.

Drain short-to-ground detection is provided for both external MOSFETs. The A6270-1 also offers MOSFET drain short-to-VIN and open LED fault protection. The MODE pin controls the action of the IC in case of a fault.

A temperature monitor is included to reduce the LED drive current if the chip temperature exceeds a thermal threshold.

An input voltage monitor is included to reduce LED current if V_{IN} rises above 17 V. The device package is a 16-pin TSSOP (LP), with exposed pad for enhanced thermal dissipation. The package is lead (Pb) free, with 100% matte-tin leadframe plating.



Typical Application Diagram

SELECTION GUIDE

Part Number	Packing*
A6270KLPTR-T-1	4000 pieces per reel

*Contact Allegro™ for additional packing options.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS*

Characteristic	Symbol	Notes	Rating	Unit
VIN, D1, D2 Pins	–		–0.3 to 42	V
DR Pin	–		–0.3 to V_{BIAS} + 0.7	V
FULL Pin	–	Through 10 kΩ resistor	–1 to 42	V
GATE1, GATE2 Pins	–		–0.3 to 10	V
All Other Pins	–		–0.3 to 7	V
Maximum Continuous Junction Temperature	T_J(max)		150	°C
Transient Junction Temperature	T_{TJ}		175	°C
Storage Temperature Range	T_{stg}		–55 to 150	°C

*With respect to GND.

THERMAL CHARACTERISTICS: May require derating at maximum conditions; see application information

Characteristic	Symbol	Test Conditions*	Value	Unit
Package Thermal Resistance (Junction to Ambient)	$R_{\theta JA}$	On 4-layer PCB based on JEDEC standard	34	°C/W
		On 2-layer PCB with 3.8 in.^{2} copper area each side	43	°C/W
Package Thermal Resistance (Junction to Pad)	$R_{\theta JP}$		2	°C/W

*Additional thermal information available on the Allegro website.

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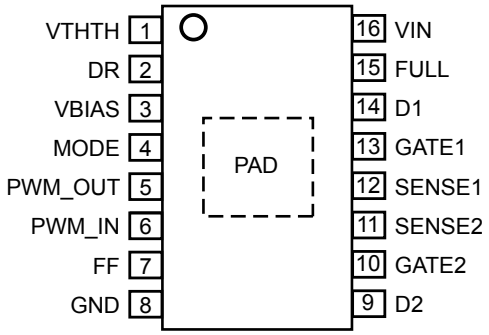
PINOUT DIAGRAM AND TERMINAL LIST TABLE



Package LP, 16-Pin TSSOP with Exposed Thermal Pad Pinout Diagram

Terminal List Table

Name	Number	Function
D1	14	Drain sensing for Channel 1 faults: drain short-to-VIN, and open LED or drain short-to-GND. If this channel is not used, connect the D1 pin to GND through 10 kΩ resistor.
D2	9	Drain sensing for Channel 2 faults: drain short-to-VIN, and open LED or drain short-to-GND. If this channel is not used, connect D2 pin to GND through 10 kΩ resistor.
DR	2	Connect to external DC voltage to adjust operating duty cycle in internal PWM mode only. In slave or external PWM mode, connect DR pin to VBIAS. When DR connected to VBIAS, PWM duty cycle is controlled by PWM_IN.
FF	7	Fault flag output. Also used as fault input when MODE is connected to VBIAS.
FULL	15	Full (Stop) mode current select 100% duty cycle operation. While FULL pin is high the DR pin, PWM_IN pin and external PWM information is overridden.
GATE1	13	Gate driver for external N-channel MOSFET1.
GATE2	10	Gate driver for external N-channel MOSFET2.
GND	8	Ground. Connect separate signal and power GND planes to this pin.
MODE	4	MODE pin decides the fault mode. Refer to Table 1 for details.
PAD	–	Exposed thermal pad. Connect to external ground pad for better thermal performance.
PWM_IN	6	In internal PWM mode (DR pin voltage < 3.7 V), PWM frequency is set by a resistor to GND. If DR pin connected to VBIAS, PWM frequency and duty cycle are determined by external signal.
PWM_OUT	5	PWM dimming frequency and duty cycle out. Leave PWM_OUT pin open if it is not used.
SENSE1	12	Current sense for Channel 1. Connect sense resistor to set peak current level for Channel 1.
SENSE2	11	Current sense for Channel 2. Connect sense resistor to set peak current level for Channel 2.
VBIAS	3	Internal bias supply. Connect to GND through a 0.1 µF capacitor.
VIN	16	Input supply.
VTHTH	1	Voltage at this pin sets the V_{IN} undervoltage fault detect threshold.

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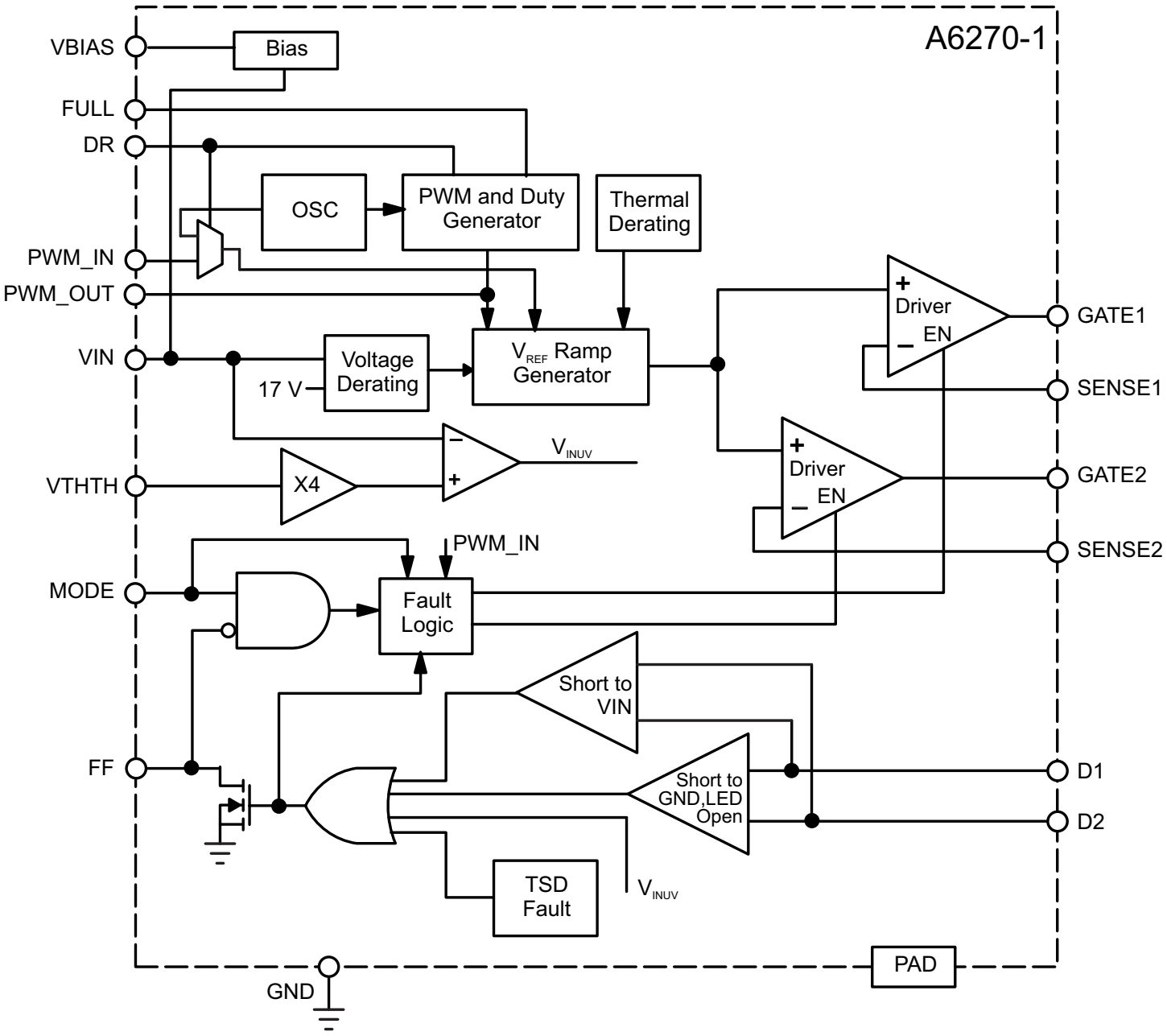

Functional Block Diagram

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ELECTRICAL CHARACTERISTICS: Valid at V_{IN} = 7 to 24 V, • indicates specifications across the full operating temperature range with $T_A = T_J$ = –40°C to 125°C, other specifications are at $T_A = T_J$ = 25°C, unless noted otherwise. Refer Figure A1 in application information section for typical application circuit.

Characteristics	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
INPUT SUPPLY							
Operating Input Voltage Range	V_{IN}		•	5.3	–	40	V
V_{IN} Operational Current	I_{INQ}	FULL = V_{IHF}	•	–	–	10	mA
Startup Time	t_{ON}	V_{IN} > 7 V, C_{VBIAS} = 0.1 µF, V_{REF} = 20 mV		–	100	–	µs
CURRENT REGULATION							
Reference Voltage on SENSE1 and SENSE2	V_{REF}	V_{IN} = 12 V	•	192	200	208	mV
		V_{IN} = 12 V, T_J = 125°C		194	200	206	mV
Maximum V_{IN} Derating for Reference Voltage	V_{REF1}	V_{IN} ≥ 24 V		–	50	–	%
Matching Between SENSE1 and SENSE2 Reference [1]	$ErrV_{REF}$	No V_{IN} derating		–	–	2	%
VBIAS Pin Voltage	V_{VBIAS}	I_{VBIAS} = 0 to 3 mA	•	5.15	5.3	5.45	V
VBIAS Undervoltage Release	$V_{VBIASUV}$	V_{IN} rising		–	4.5	–	V
VBIAS Undervoltage Lockout Hysteresis	$V_{VBIASHYS}$	IC disabled		–	0.2	–	V
GATE DRIVER							
GATE1 and GATE2 High-Level Output	V_{GATEH}	V_{IN} = 12 V, PWM_IN = high, V_{REF} = 150 mV, DR = VBIAS		6	–	9	V
GATE1 and GATE2 Low-Level Output	V_{GATEL}	PWM_IN = low		–	–	0.7	V
GATE Driver Dropout	V_{GATE_drop}	V_{IN} = 7 V, V_{REF} = 150 mV, measured as ($V_{IN} – V_{GATE}$)		–	–	1	V
Gate Pull-Up Current	I_{GPU}	V_{SENSE} = 180 mV, V_{GATE} = 0 V, V_{IN} = 7 V		–	–360	–	µA
Gate Pull-Down Current	I_{GPD}	V_{SENSE} = 220 mV, V_{GATE} = 7 V, V_{IN} = 7 V		–	360	–	µA
External FET Gate Capacitance Range	C_{GISS}	For stable operation		250	–	2000	pF
Propagation Delay	t_{pd}	Delay from PWM_IN to PWM_OUT pin, DR connected to VBIAS		–	2	–	µs
PWM Dimming Frequency	f_{PWM}	External R_{FPWM} = 30.9 kΩ, across PWM_IN to GND	•	180	200	220	Hz
PWM Duty Cycle	D_{PWM5}	V_{DR} driven by resistor divider from VBIAS, V_{VBIAS}/ V_{DR} = 29.7, PWM = 200 Hz		4.5	5	5.5	%
	D_{PWM90}	V_{DR} driven by resistor divider from VBIAS, V_{VBIAS}/ V_{DR} = 1.63, PWM = 200 Hz		88	90	92	%
Current Slew Time	t_{SR}	Rising or falling between 20% and 90% levels, for internal reference ramp		43	70	97	µs
Rise Time to Fall Time Matching [2]	t_{SRM}	Rising or falling between 20% and 90% levels, for internal reference ramp		–	20	–	µs
Rise Time and Fall Time Mismatch Between Two Strings [3, 4]	t_{SRMS}	Rise and fall time mismatch between 20% and 90% levels in two strings		–	–	2	%

Continued on the next page…

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ELECTRICAL CHARACTERISTICS (continued): Valid at V_{IN} = 7 to 24 V, • indicates specifications across the full operating temperature range with $T_A = T_J$ = –40°C to 125°C, other specifications are at $T_A = T_J$ = 25°C, unless noted otherwise. Refer Figure A1 in application information section for typical application circuit.

Characteristics	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
LOGIC PINS							
MODE, PWM_IN Pins Input Low Voltage	V_{IL}	Below V_{IL} level, input voltage considered as logic LOW	•	–	–	0.8	V
MODE, PWM_IN Pins Input High Voltage	V_{IH}	Above V_{IH} level, input voltage considered as logic HIGH	•	2	–	–	V
FF, PWM_OUT Pins Output Low Voltage	V_{OL}	I_{OL} = 1 mA	•	–	–	0.4	V
PWM_OUT Pin Output High Voltage	V_{OH}	I_{OH} = –1 mA	•	4	–	–	V
FULL Pin Input Low Voltage	V_{ILF}	Below V_{ILF} level, input voltage on FULL pin will disable FULL mode	•	0.85	–	1.15	V
FULL Pin Input High Voltage	V_{IHF}	Above V_{IHF} level, input voltage on FULL pin will enable FULL mode	•	1.06	–	1.44	V
MODE Pin Pull-Down Current	I_{lkg}	MODE connected to VBIAS		–	10	–	µA
PROTECTION							
Input Voltage Required to Derate V_{REF} by 10%	$V_{INth(L)}$			16.7	17.7	18.7	V
V_{IN} Derating Range ($V_{INth(H)}$ to $V_{INth(L)}$)	V_{INthd}	V_{REF} drops from 180 mV to 120 mV		–	2.16	–	V
VIN to Drain Short Detect Voltage	V_{SCV}	Measured as $V_{IN} – V_{Dx}$, GATEx = high	•	0.5	0.8	1.1	V
Open LED Fault Detect Voltage	V_{OLED}	Measured at Dx, GATEx = low	•	0.19	0.24	0.29	V
Input Voltage Undervoltage Fault Detect Level, V_{IN} Rising	V_{INUV}	V_{THTH} = 1.75 V		–	7	–	V
Input Voltage Undervoltage Hysteresis	$V_{INUVhys}$			–	262	–	mV
Thermal Monitor Activation Temperature[4]	T_{JM}	T_J with I_{SENSEx}, V_{REF} = 180 mV		–	T_{JF} – 21	–	°C
Thermal Monitor Low-Current Temperature[4]	T_{JL}	T_J with I_{SENSEx}, V_{REF} = 70 mV		–	T_{JF} – 7	–	°C
Overtemperature Shutdown[4]	T_{JF}	Temperature increasing		–	170	–	°C
Overtemperature Hysteresis[4]	T_{Jhys}	Recovery = $T_{JF} – T_{Jhys}$		–	30	–	°C

[1] Reference matching is defined as: $(V_{SENSE1} – V_{SENSE2}) / V_{SENSE(AVG)}$. Where $V_{SENSE(AVG)}$ is the average of V_{SENSE1} and V_{SENSE2}.
[2] Rise Time to Fall Time Matching is defined as the maximum difference between the rise time and the fall time of the same string.
[3] Rise Time to Fall Time Mismatch Between Two Strings is defined as the maximum ratio of the difference between either the rise time or the fall time to the average of the rise time or fall times between two strings.
[4] Ensured by design and characterization.

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FUNCTIONAL DESCRIPTION

Protection Functions

Various short-circuit faults handled by A6270-1 are shown in Figure 1.

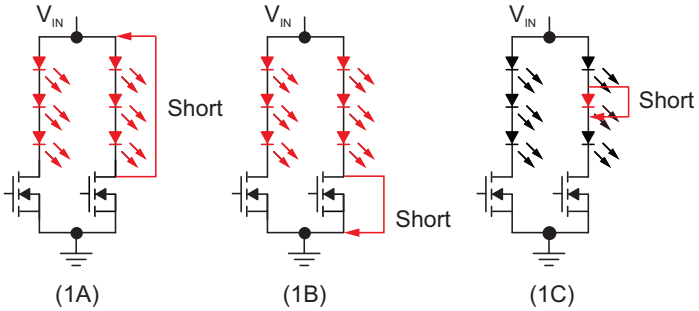

Figure 1: Short-Circuit Protection

For the fault description below, it is assumed (for a simpler explanation) that the fault is applied on D2 string, and D1 is assumed to be a healthy string. The IC will respond similarly, in case of a fault on D1.

DRAIN SHORT TO VIN (Figure 1a, Figure 2a, and Figure 2b)

This fault is detected when ($V_{IN} - V_{D2}$) < 0.8 V and both GATEs are asserted high and after completion of reference ramp. When detected, the FF flag remains low, independent of GATE status. Once the fault is detected, GATE2 is pulled high and GATE1 is pulled low. This keeps MOSFET2 on to detect removal of the fault for autorecovery. When the fault is removed, ($V_{IN} - V_{D2}$) > 0.8 V and the IC returns to normal operation. As GATE2 remains continuously high, Q2 will dissipate significant power. Current through Q2 is regulated to set level.

When MODE = VBIAS, GATE2 remains high with 100% duty cycle, irrespective of FULL or TAIL mode. GATE1, PWM_OUT and FF are pulled low once the fault is detected but not latched. The IC returns to normal operation (FF = HIGH, PWM_OUT and GATE1 active) when the fault removed. As the drain is shorted to VIN, current through LED2 string is zero and GATE1 is pulled low to keep LED1 current low. ICs connected in parallel turn off as FF and PWM_OUT are pulled low.

When MODE = LOW, both gates switch at 100% duty cycle (FULL mode) or desired PWM duty cycle (TAIL mode). PWM_OUT operates normally. Only the FF pin is pulled low continuously. The IC returns to normal operation (FF = HIGH) when the fault removed and GATE2 is asserted high. In this mode, the IC will operate normally, except FF pin is pulled low. The current in LED1 string and the current in slave-connected ICs will be normal. The current in LED2 string is zero as D2 is shorted to VIN. The FF pin does not affect operation of slave-connected ICs.

The symmetrical action applies if the fault is in string 1, i.e. ($V_{IN} - V_{D1}$) < 0.8 V.

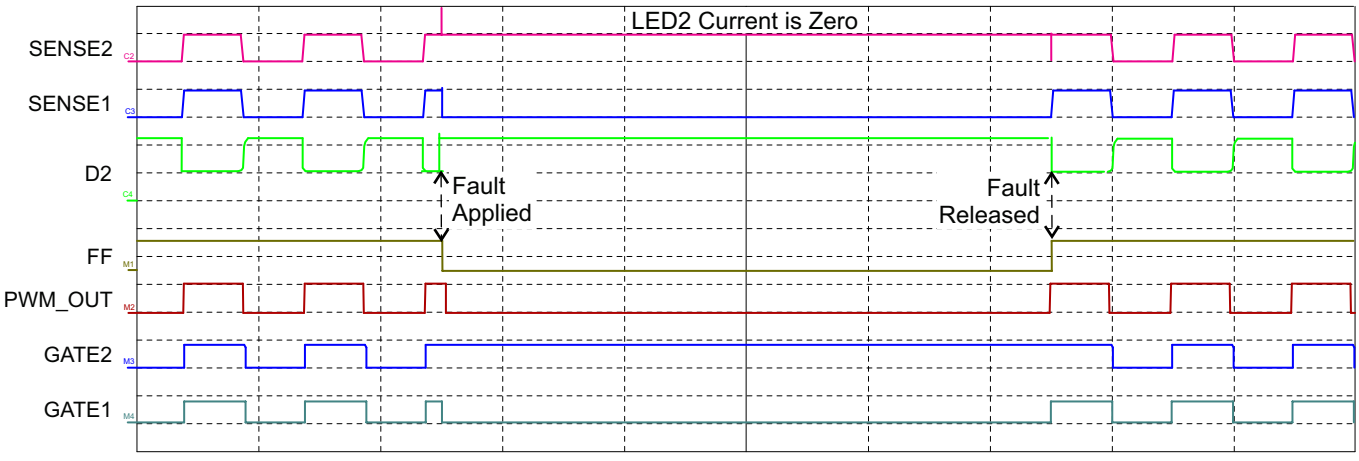

Figure 2a: Drain Short to VIN Fault on D2 with MODE = HIGH and PWM Dimming

C2-C3 200 mV/div and C4, M1-M4 5 V/div. Time 5 ms/div.

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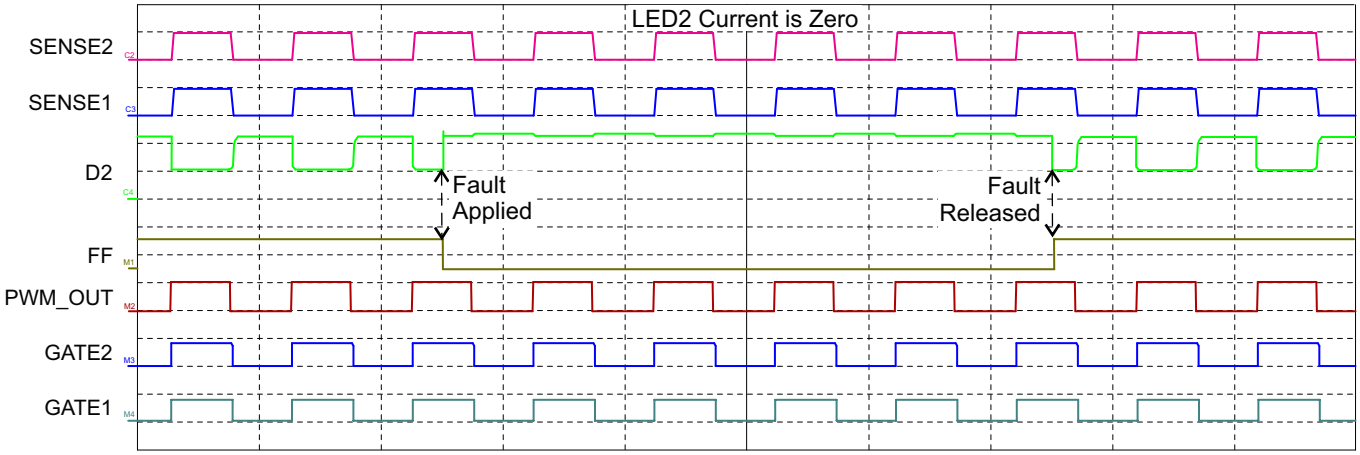

Figure 2b: Drain Short to VIN Fault on D2 with MODE = LOW and PWM Dimming
C2-C3 200 mV/div and C4, M1-M4 5 V/div. Time 5 ms/div.

OPEN LED (Figure 3, Figure 4a, and Figure 4b)

This fault is detected when $V_{D2} < 0.24$ V.

When MODE = VBIAS, GATE2 remains on with 100% duty cycle, irrespective of FULL or TAIL mode. GATE1, PWM_OUT and FF are pulled low once the fault is detected, but they are not latched. The IC pulls faulty GATE2 high. This keeps MOSFET2 on to detect removal of the fault for autorecovery. When the fault is removed, $V_{D2} > 0.24$ V and the IC returns to normal operation. (FF = HIGH, PWM_OUT, and both GATEs return to normal operation).

As the LED2 string is opened, current through LED2 string is zero and GATE1 is pulled low to keep LED1 current off. Slave-connected ICs turn off LED string current as FF is pulled low.

When MODE = LOW, both gates run at 100% duty cycle (FULL mode) or desired PWM duty cycle (TAIL mode). PWM_OUT operates normally. Only the FF pin is pulled low as long as $V_{D2} < 0.24$ V. In FULL mode, V_{D2} will always be lower than 0.24 V and the FF pin goes low. In TAIL mode, V_{D2} changes based on PWM state. During PWM on, $V_{D2} < 0.24$ V and FF goes low, whereas during PWM off period, V_{D2} is pulled high and FF goes high. The IC returns to normal operation (FF = HIGH) when the fault is removed. During this fault, the IC will operate normally, except the FF pin is pulled low. Current in LED1 and in slave-connected ICs will be normal. Current in LED2 string is zero as LED2 string is open. FF pin does not affect operation of parallel connected ICs.

The symmetrical action applies if the fault is in string 1, i.e. $V_{D1} < 0.24$ V.

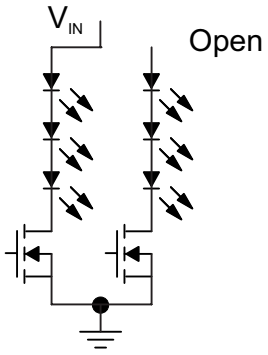

Figure 3: LED Open Protection

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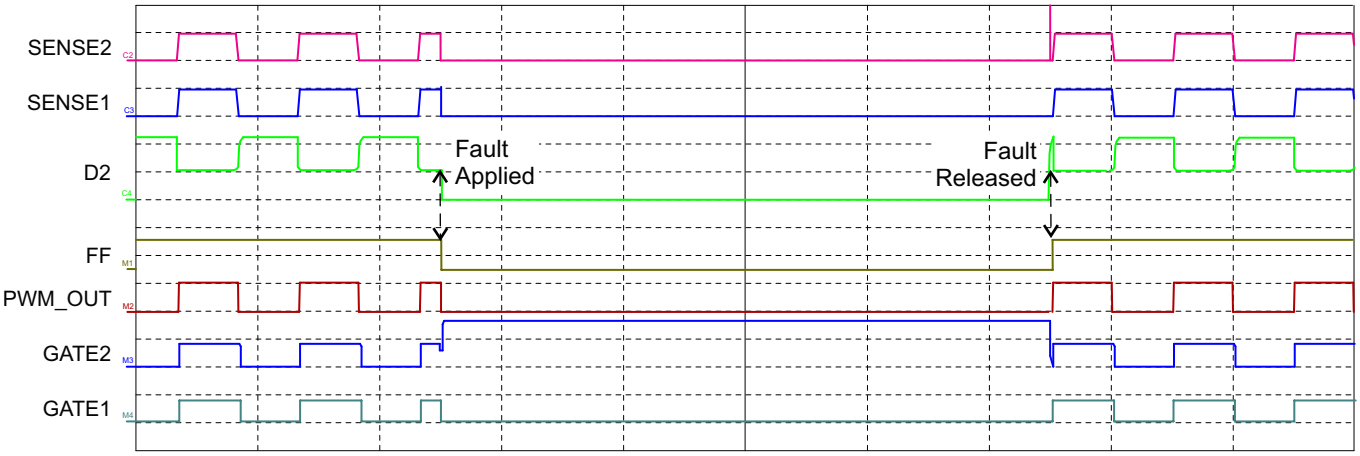

Figure 4a: Open LED Fault on D2 with MODE = HIGH and PWM Dimming
C2-C3 200 mV/div and C4, M1-M4 5 V/div. Time 5 ms/div.

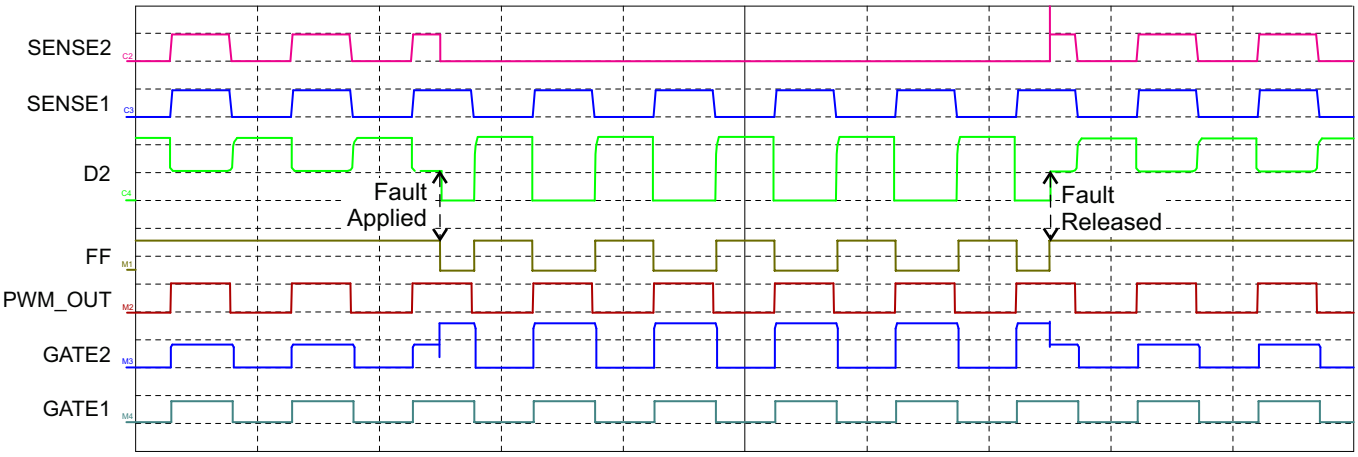

Figure 4b: Open LED Fault on D2 with MODE = LOW and PWM Dimming
C2-C3 200 mV/div and C4, M1-M4 5 V/div. Time 5 ms/div.

DRAIN SHORT TO GND (Figure 1b, Figure 5, and Figure 6)

This fault is detected when $V_{Dx} < 0.24$ V (same as open LED fault).

When MODE = VBIAS, GATE2 remains on with 100% duty cycle, irrespective of FULL or TAIL mode. GATE1, PWM_OUT and FF are pulled low once the fault is detected, but they are not latched. The IC pulls faulty GATE2 high. This keeps MOSFET2 on to detect removal of the fault for autorecovery. When the fault is removed, $V_{D2} > 0.24$ V and the IC returns to normal operation (FF = HIGH, PWM_OUT and both GATEs return to normal operation).

As the LED2 string is shorted to GND, a large current will flow through the LED2 string. GATE1 is pulled low to keep LED1 current off. Slave-connected ICs turn LED string current off as FF is pulled low.

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When MODE = LOW, both gates run at 100% duty cycle (FULL mode) or desired PWM duty cycle (TAIL mode). PWM_OUT operates normally. Only the FF pin is pulled low as long as $V_{D2} < 0.24$ V. The IC returns to normal operation (FF = HIGH) when the fault is removed. During this fault, the IC will operate normally except the FF pin is pulled low. The current in LED1 and in slave-connected ICs will be normal. As the LED2 string is shorted to GND, a large current will flow through LED2 string. The FF pin does not affect operation of slave-connected ICs.

The symmetrical action applies if the fault is in string 1, i.e. $V_{D1} < 0.24$ V.

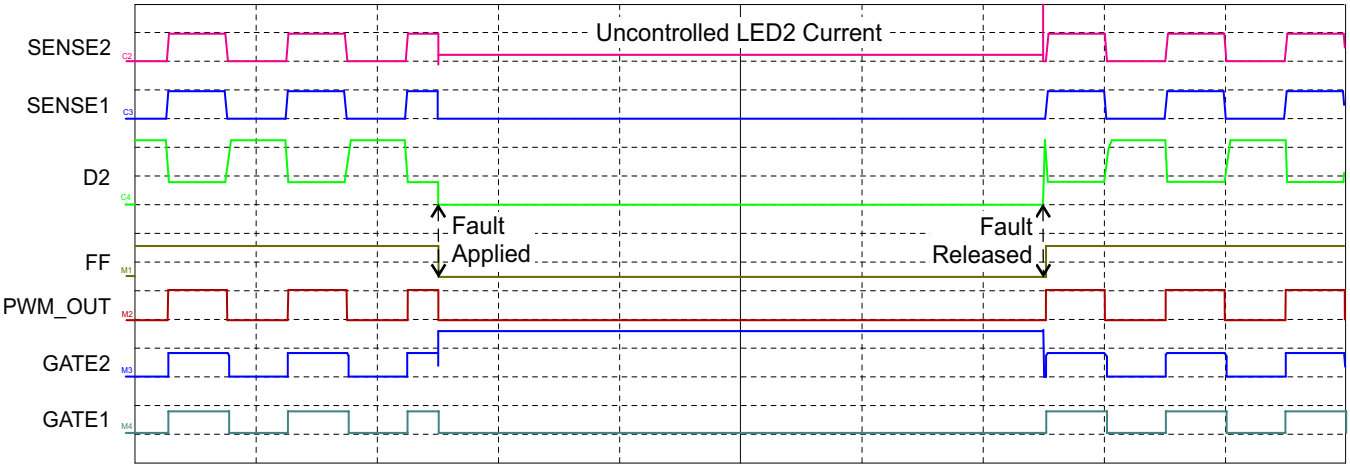

Figure 5: Drain Short to GND Fault on D2 with MODE = HIGH and PWM Dimming.
C2-C3 200 mV/div and C4, M1-M4 5 V/div. Time 5 ms/div.

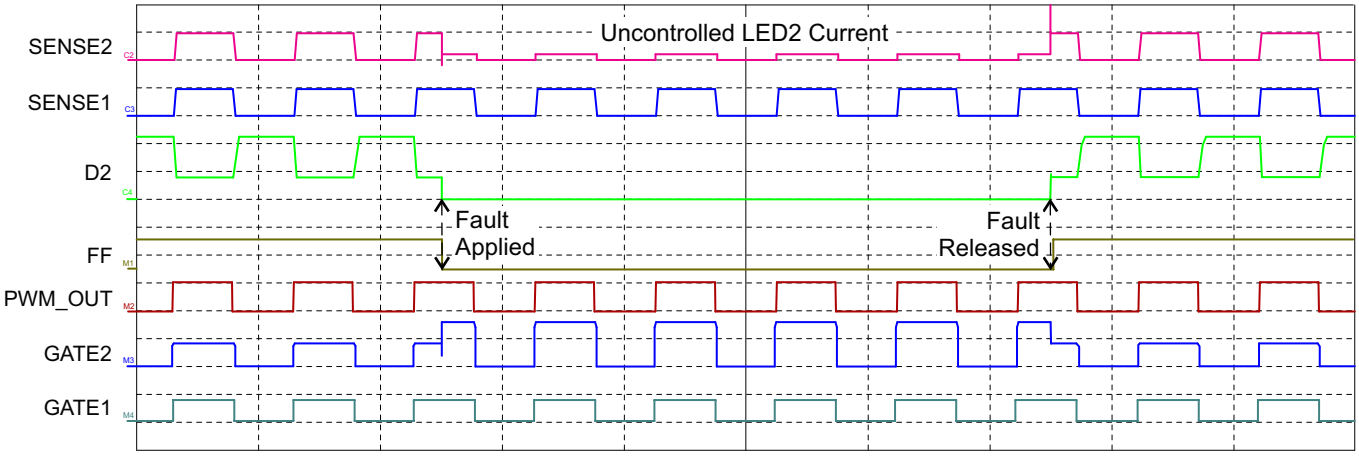

Figure 6: Drain Short to GND Fault on D2 with MODE = LOW and PWM Dimming.
C2-C3 200 mV/div and C4, M1-M4 5 V/div. Time 5 ms/div.

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SINGLE LED SHORT (Figure 1C)

In the case where a few LEDs are shorted, the IC continues to work normally.

INPUT UNDERVOLTAGE FAULT

Input undervoltage fault is detected when input voltage V_{IN} is below V_{INUV} as defined by voltage on the VTHTH pin. When the fault is detected, the FF pin is pulled low. If MODE = LOW, the IC works normally, and for MODE = HI, both channels are turned off and auto-restart when V_{IN} rises above V_{INUV}. Maximum voltage on V_{THTH} pin can be 3.6 V, which limits V_{INUV} level to 14.4 V.

V_{INUV} level is set as:

$$V_{INUV} = 4 \times V_{THTH} \quad (1)$$

$$V_{INUVhys} = 0.15 \times V_{THTH} \quad (2)$$

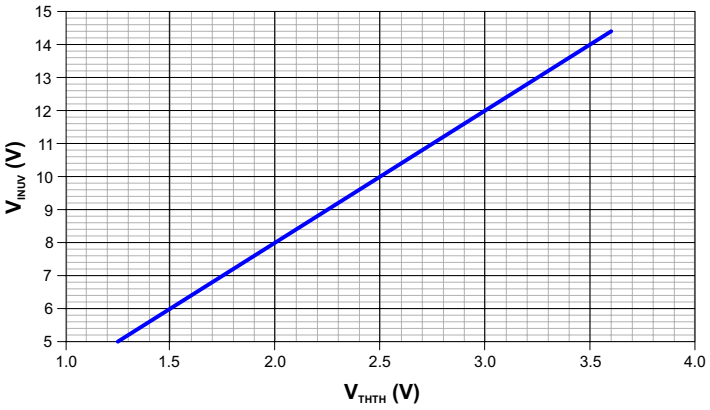

Figure 7: V_{THTH} Voltage versus Input Undervoltage Fault Threshold V_{INUV}

INPUT OVERVOLTAGE DERATING

This feature takes effect at higher V_{IN} levels, limiting power dissipation in the external MOSFETs. At higher input voltages, output current drops corresponding with increasing V_{IN}. Output current is controlled with peak current (see Figure 8). The V_{IN} derating threshold is fixed internally. The reference voltage drops to 90% at the $V_{INth(L)}$ = 17.7 V level and to 60% at $V_{INth(H)}$ = 19.9 V level. Reference level drops to 50% and stays at this level for higher input voltages.

THERMAL DERATING AND PROTECTION SHUTDOWN

This feature takes effect at higher temperatures, limiting power dissipation in the external MOSFETs. At higher temperatures, the reference voltage drops with increasing T_J, as shown in Figure 9. Thermal shutdown (TSD) completely disables the outputs under extreme overtemperature (>170°C) conditions, and FF goes low. The IC restarts when the temperature drops by 30°C.

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Internal Dimming Frequency and Duty Cycle

Dimming frequency can be set using the PWM_IN pin. This PWM frequency can be set in the range from 200 Hz to 1 kHz, either by using an external resistor, or by using an external clock signal, on the PWM_IN pin. The equation for frequency setting with the PWM_IN pin resistor is as follows:

$$f_{PWM} = 5400 / R_{FPWM} + 25 \quad (3)$$

where f_{PWM} is in Hz and R_{FPWM} is in kΩ. For example, with a 30.9 kΩ resistor, f_{PWM} = 200 Hz.

When frequency is set through an external resistor (for internal PWM), the voltage on the DR pin determines the operating duty cycle. For better accuracy, derive this voltage from VBIAS using a voltage divider. The PWM duty cycle depends on ratio of the DR and VBIAS pin voltages. The IC works with 100% duty cycle in Stop mode (FULL = HIGH). In Tail mode, the duty cycle can be programmed by controlling the analog voltage on the DR pin. The duty cycle can be changed from 5% to 90% (see Figure 10), as:

$$PWM\ (\%) = 148 \times V_{DR} / V_{VBIAS} \quad (4)$$

where V_{DR} and V_{VBIAS} are in volts.

If the DR pin is connected to VBIAS, an external clock pulse on the PWM_IN pin controls dimming frequency and duty cycle.

For master-slave operation, connect the PWM_OUT pin of the master IC to the PWM_IN pin of the slave ICs.

The PWM_OUT signal is identical to the internal gate state. The slave will operate with same PWM frequency and duty cycle as the master.

LED CURRENT SETTING

LED peak current (100%) level can be set independently for each channel by selecting a proper resistor value from the SENSEx pin to GND, as follows:

$$LED\ Peak\ Current = 200 / R_{SENSE} \quad (5)$$

where LED peak current is in mA and R_{SENSE} is in Ω.

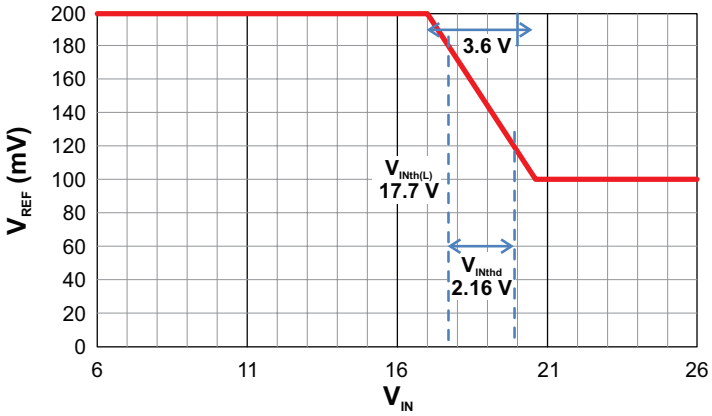

Figure 8: Output Current Foldback Based on V_{IN}

V_{REF} drops to the 90% level when V_{IN} exceeds $V_{INth(L)}$, which is 17.7 V

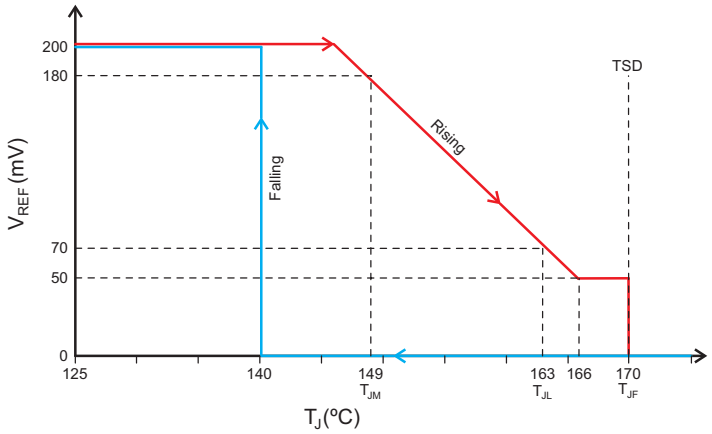

Figure 9: Output Current Foldback Based on Rising T_J

Output current changed by DC current control; when temperature exceeds 170°C (typ) the gates turn off due to TSD function, and turns on again at 140°C (30°C (typ) hysteresis)

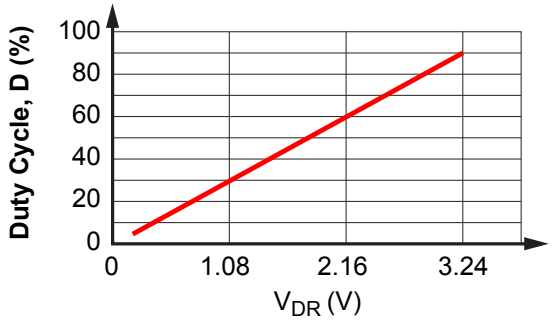

Figure 10: Relationship of External Voltage Input on DR Pin and Dimming Duty Cycle

V_{DR} can be varied from 0 to 3.6 V.

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Table 1: Fault Operation and Derating

	FF	MODE = VBIAS		MODE = Low	
		PWM_OUT	Operation	PWM_OUT	Operation
Drain Shorted to VIN	Low	Low	Detected when (V_{IN} –V_{Dx}) < 0.8 V. The faulty string remains on with 100% duty cycle irrespective of FULL or TAIL mode. Other string, PWM_OUT, and FF pulled low once fault detected but not latched. Faulty MOSFET drop full VIN voltage. IC recovers to normal operation when fault removed.	Normal	Detected when (V_{IN} –V_{Dx}) < 0.8 V. IC operates normally except FF pin pulled low. Faulty MOSFET drop full VIN voltage when enabled. FF pin goes high when fault removed.
	The fault is detected when both GATEs are asserted high and after completion of reference ramp. When detected, the fault remains active independent of GATE status.				
Open LED	Low	Low	Detected when V_{Dx} < 0.24 V. The faulty string remains on with 100% duty cycle irrespective of FULL or TAIL mode. Other GATEx is turned off. IC recovers to normal operation when fault removed.	Normal	Detected when V_{Dx} < 0.24 V. IC operates normally except FF pin pulled low. FF pin goes high when fault removed.
Drain Shorted to GND	Low	Low	Detected when V_{Dx} < 0.24 V. The faulty string remains on with 100% duty cycle irrespective of FULL or TAIL mode. Other GATEx is turned off. IC recovers to normal operation when fault removed. LEDs in faulty string may damage due to excessive LED current.	Normal	Detected when V_{Dx} < 0.24 V. IC operates normally except FF pin pulled low. LEDs in faulty string may damage due to excessive LED current. FF pin goes high when fault removed.
Thermal Derating	Normal	Normal	LED current derates based on junction temperature.	Same operation as MODE = VBIAS	
V_{IN} Derating	Normal	Normal	LED current derates based on supply voltage.	Same operation as MODE = VBIAS	
TSD	Low	Low	LEDs turn off when T_J exceeds 170°C and autorecover when T_J drops below 140°C.	Normal	LEDs turn off when T_J exceeds 170°C but PWM_OUT is normal. Autorecover when T_J drops below 140°C.
V_{IN} Undervoltage	Low	Low	LEDs turn off when V_{IN} < V_{INUV} – $V_{INUVhys}$ and auto-restart when V_{IN} rises above V_{INUV}.	Normal	IC operates normally, but FF set low.

Table 2: Simplified Fault Table

Description	Detection Condition	FULL	MODE = HIGH				MODE = LOW			
			FF	$G_{AFFECTED}$	G_{NORMAL}	PWM_OUT	FF	$G_{AFFECTED}$	G_{NORMAL}	PWM_OUT
Drain Shorted to VIN [1]	$V_{IN} – V_{Dx}$ < typ 0.8 V min = 0.5 V max = 1.1 V	HIGH	LOW	HIGH	LOW	LOW	LOW	HIGH	HIGH	HIGH
		LOW	LOW	HIGH	LOW	LOW	LOW	PWM	PWM	PWM
Open LED fault	V_{Dx} < typ 0.24 V min = 0.19 V max = 0.29 V	HIGH	LOW	HIGH	LOW	LOW	LOW	HIGH	HIGH	HIGH
		LOW	LOW	HIGH	LOW	LOW	$\overline{PWM}$	PWM	PWM	PWM
Drain Shorted to GND	V_{Dx} < typ 0.24 V min = 0.19 V max = 0.29 V	HIGH	LOW	HIGH	LOW	LOW	LOW	HIGH	HIGH	HIGH
		LOW	LOW	HIGH	LOW	LOW	LOW	PWM	PWM	PWM
V_{IN} Undervoltage	V_{IN} < (4 × V_{THTH} – 0.15 × V_{THTH})	X	LOW	LOW	LOW	LOW	LOW	Normal	Normal	Normal
Thermal Shutdown	T_J > 170°C	X	LOW	LOW	LOW	LOW	LOW	LOW	LOW	Normal

X = Don't Care

[1] Detected after completion of ramp time.

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APPLICATION INFORMATION

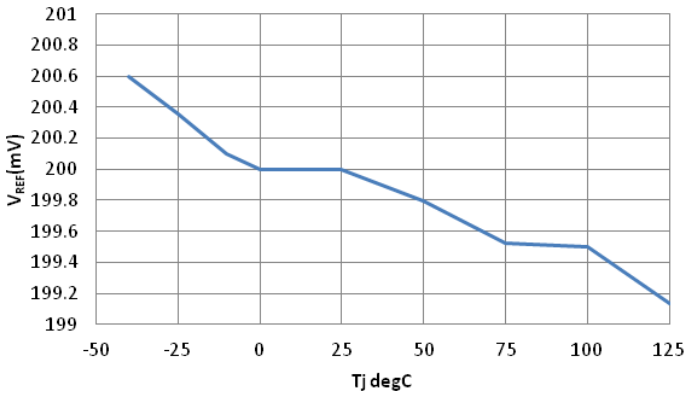

Figure 12: Temperature vs. V_{REF}

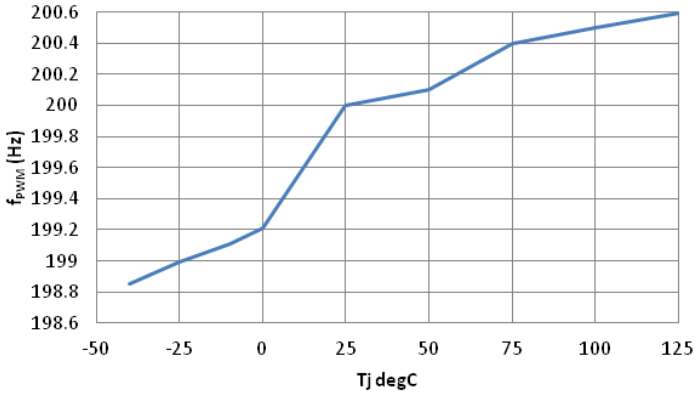

Figure 13: Temperature vs. f_{PWM} (R_{FPWM} = 30.9 kΩ)

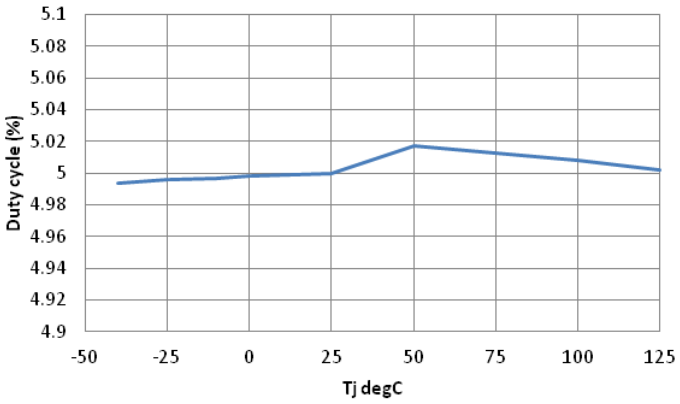

Figure 14: Temperature vs. Duty Cycle (V_{VBIAS}/V_{DR} = 29.7)

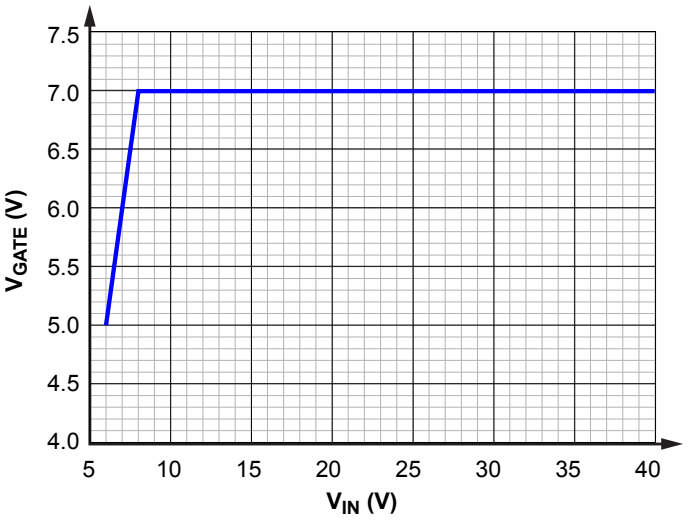

Figure 11: GATE Voltage vs. V_{IN}

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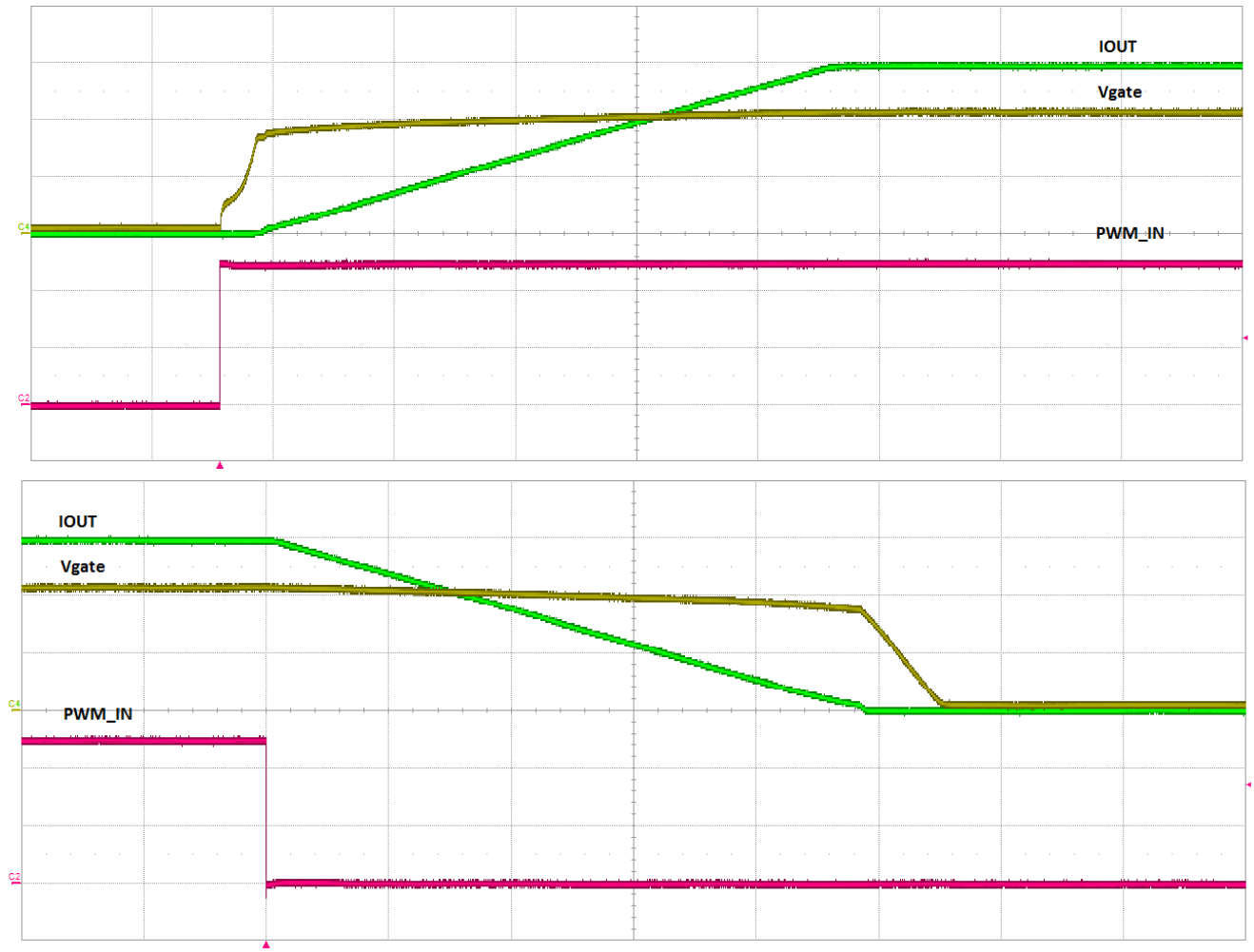

Figure 15: Rise Time and Fall Time During PWM Dimming.
I_{OUT} (Total LED Current) (200 mA/div), PWM_IN and V_{GATE} (2 V/div), Time (20 µs/div)

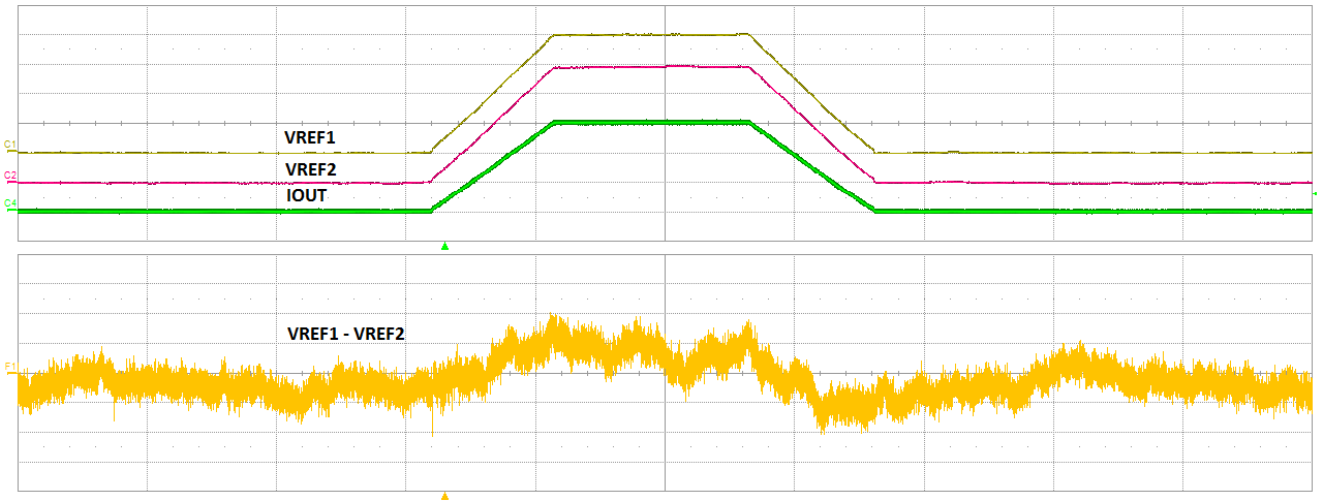

Figure 16: Reference Matching During PWM Dimming
V_{REF1}, V_{REF2} (50 mV/div), I_{OUT} (Total LED Current)(200 mA/div), V_{REF1}–V_{REF2} (2 mV/div), Time (100 µs/div).

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Modes of Operation

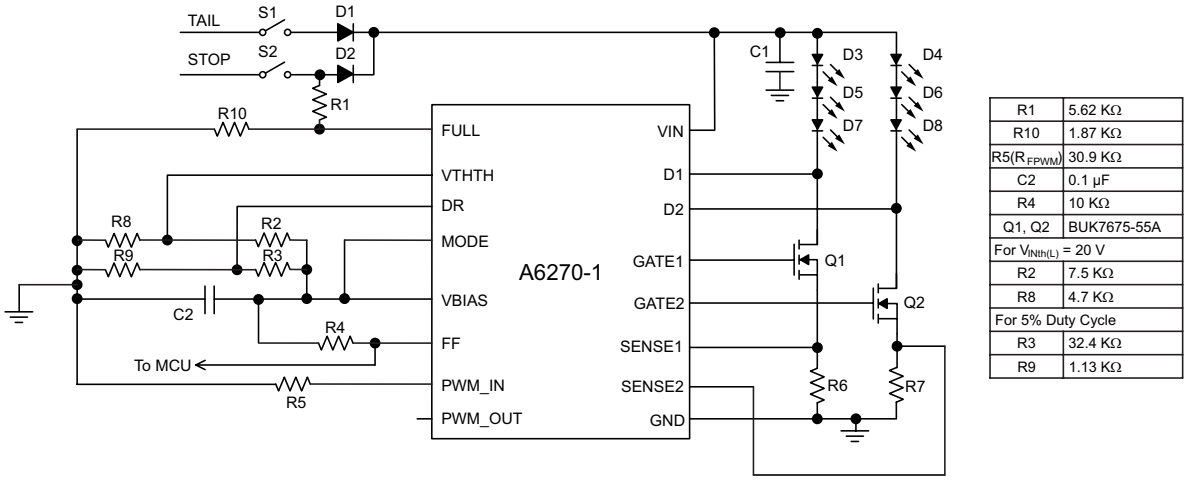
The IC can operate in one of the following modes:

A. Single IC, internal PWM mode
B. Single IC, external PWM mode
C. Multiple ICs, master-slave arrangement
D. Multiple ICs, in parallel mode

These are each described in the remainder of this section.

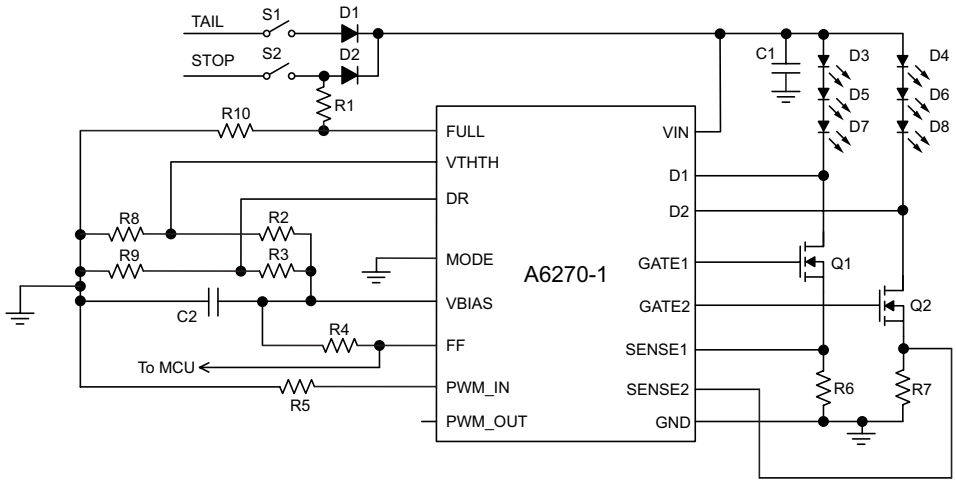
A. SINGLE IC, INTERNAL PWM MODE

In TAIL mode, the IC generates its PWM frequency based on a resistor connected from the PWM_IN pin to GND, and the duty cycle is controlled by voltage at the DR pin (which can be generated by a resistor divider, or driven by an external DC signal). In Full (Stop) mode, the duty cycle is always 100%. Overtemperature or input overvoltage conditions derate LED current by controlling peak current in both Stop and Tail modes.



R1	5.62 KΩ
R10	1.87 KΩ
R5(R_{FPWM})	30.9 KΩ
C2	0.1 µF
R4	10 KΩ
Q1, Q2	BUK7675-55A
For $V_{INth(L)}$ = 20 V	
R2	7.5 KΩ
R8	4.7 KΩ
For 5% Duty Cycle	
R3	32.4 KΩ
R9	1.13 KΩ

Typical Application Circuit A1: Single IC Operation with Internal Reference to DR and MODE Pulled High.



Typical Application Circuit A2: Single IC Operation with Internal Reference to DR and MODE Shorted to GND.

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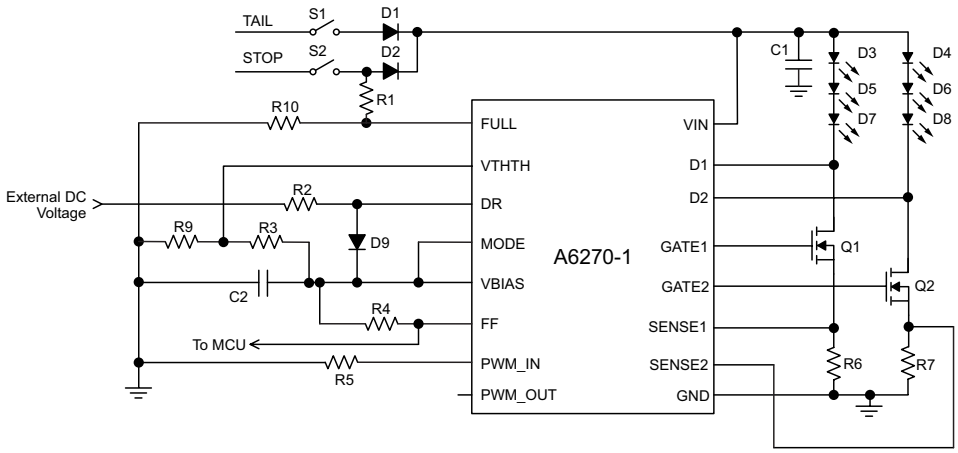
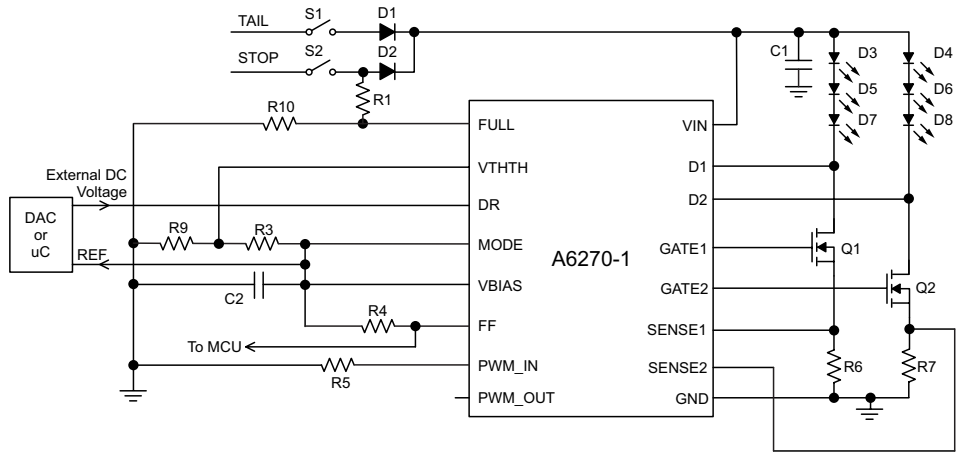


Typical Application Circuit A3a: Single IC Operation with External Analog Reference to DR and MODE Pulled High

External DC voltage can be applied on DR pin to control PWM dimming. Voltage on DR pin should be $0 < V_{DR} < 3.6$ V for duty cycle control. Voltage on DR pin must be lower than V_{VBIAS} under all conditions. Optional R2 – D9 clamp used to ensure DR pin voltage limited to V_{VBIAS}.



Typical Application Circuit A3b: Using DAC to Microcontroller to Control PWM Duty Cycle

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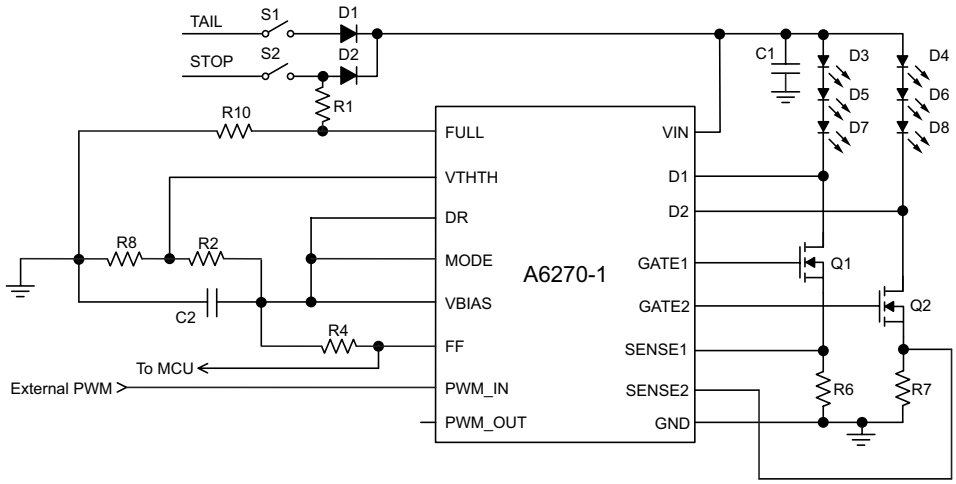
B. SINGLE IC, EXTERNAL PWM MODE

When the DR pin is connected to VBIAS , in Tail mode, the IC disables internal PWM generation and replicates the frequency and duty cycle of the signal at the PWM_IN pin onto GATEx. In Full mode, the duty cycle is always 100%. Overtemperature or input overvoltage conditions derate LED current by controlling peak current in both Stop and Tail modes. Voltage on the VTHTH pin sets the V_{IN} undervoltage fault detect threshold.



Typical Application Circuit B1: Single IC Operation with External PWM to PWM_IN Pin and MODE Pulled High.
For the above configuration, DR pin voltage is always connected to the VBIAS pin.

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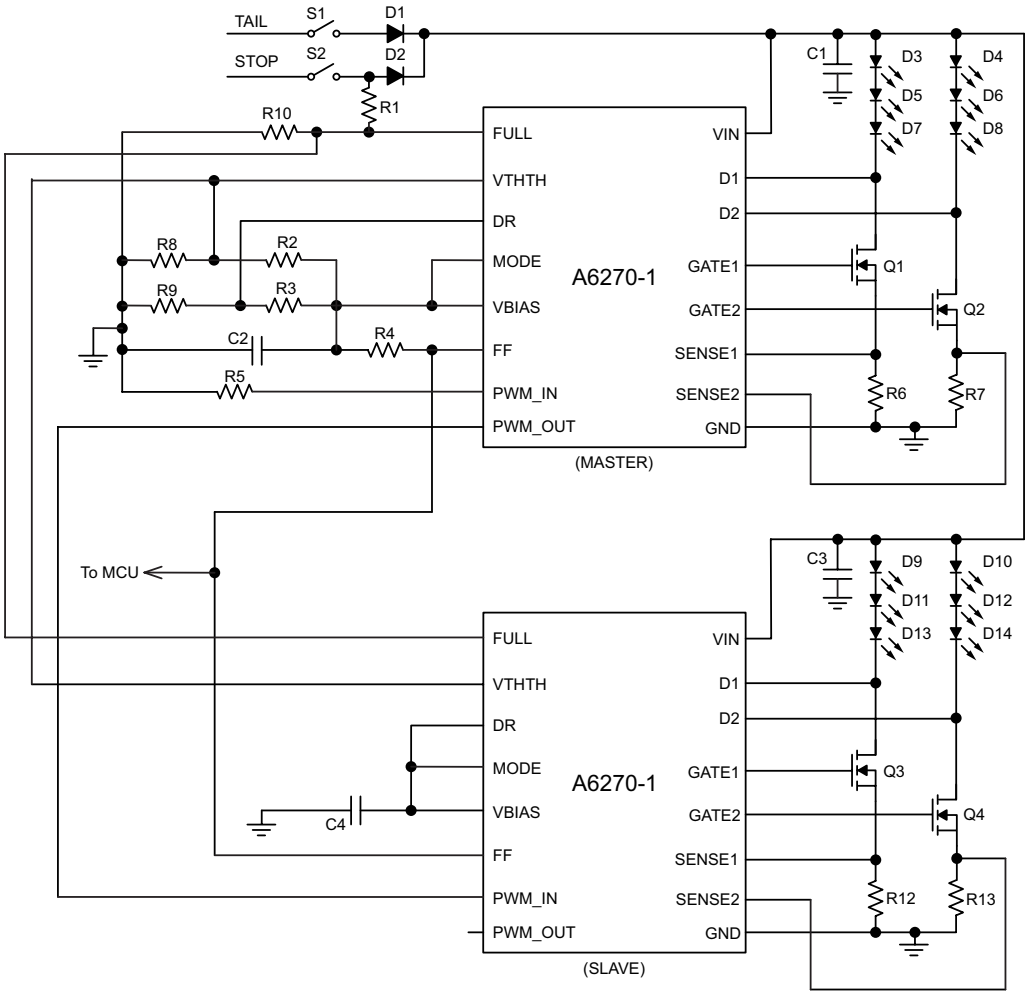
C. MULTIPLE IC, MASTER-SLAVE ARRANGEMENT

The master IC is configured as a single IC in Internal PWM mode. In TAIL mode, a resistor on the PWM_IN pin determines the PWM frequency, and the duty cycle is controlled by voltage on the DR pin. In Full mode, duty cycle is always 100%. Over-temperature or input overvoltage conditions derate LED current by controlling peak current in both Stop and Tail modes. Voltage on the VTHTH pin sets the V_{IN} undervoltage fault detect threshold.

Operating PWM frequency and duty cycle output is provided on the PWM_OUT pin. Connect this pin to the PWM_IN pin of the slave ICs.

Each slave IC is configured in Single IC, External PWM mode.

Master and slaves derate LED current independently, based on VIN pin voltage and junction temperature of the respective IC. Refer to Table 1 for operation under various faults.



Typical Application Circuit C1: Master-Slave Operation with Internal Reference to DR on Master and MODE Pulled High

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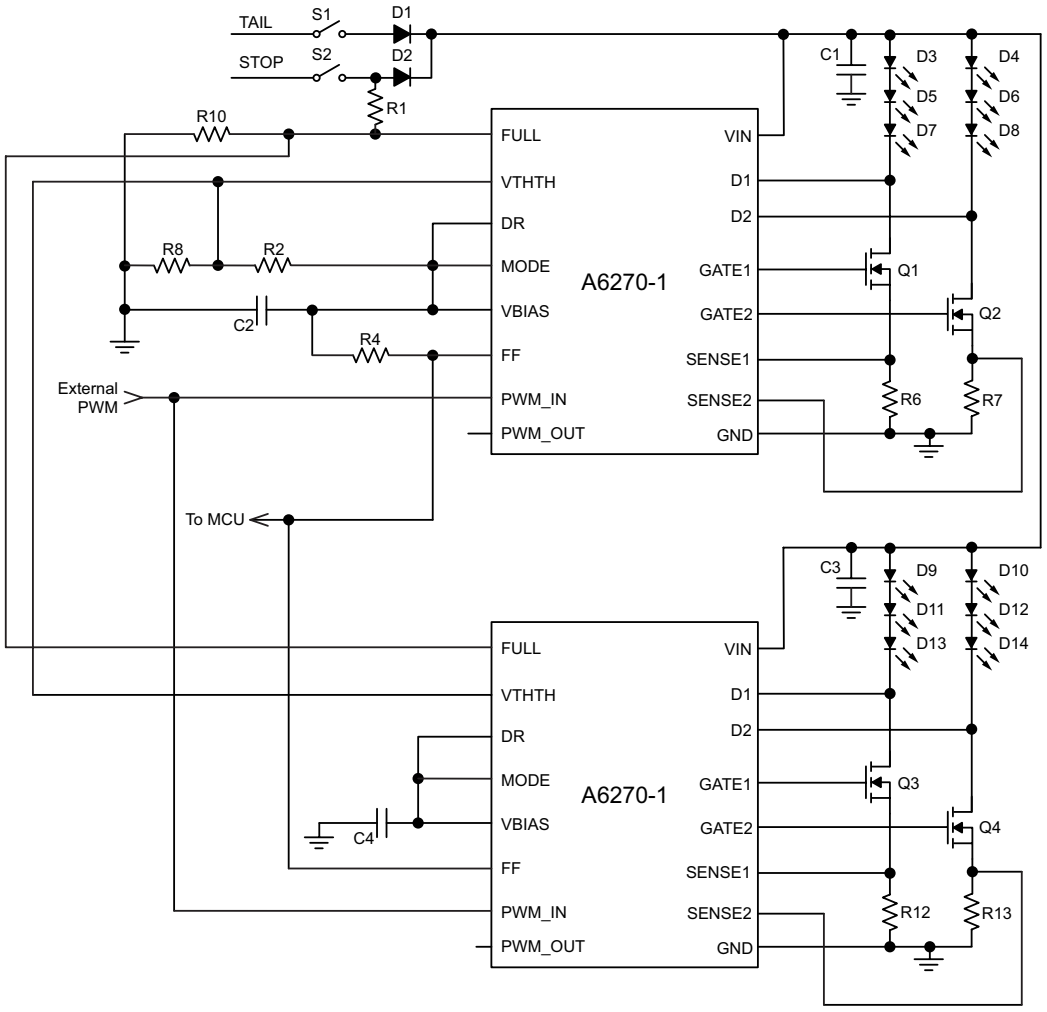
D. MULTIPLE ICS, IN PARALLEL MODE

All the ICs are configured for external PWM mode. PWM input from the MCU controls frequency and duty cycle in Tail mode. In Stop mode, duty cycle is always 100%.

Each IC derates LED current independently, based on VIN pin voltage and junction temperature of the respective IC.



Typical Application Circuit D1: Parallel Operation with External PWM and MODE Pulled High

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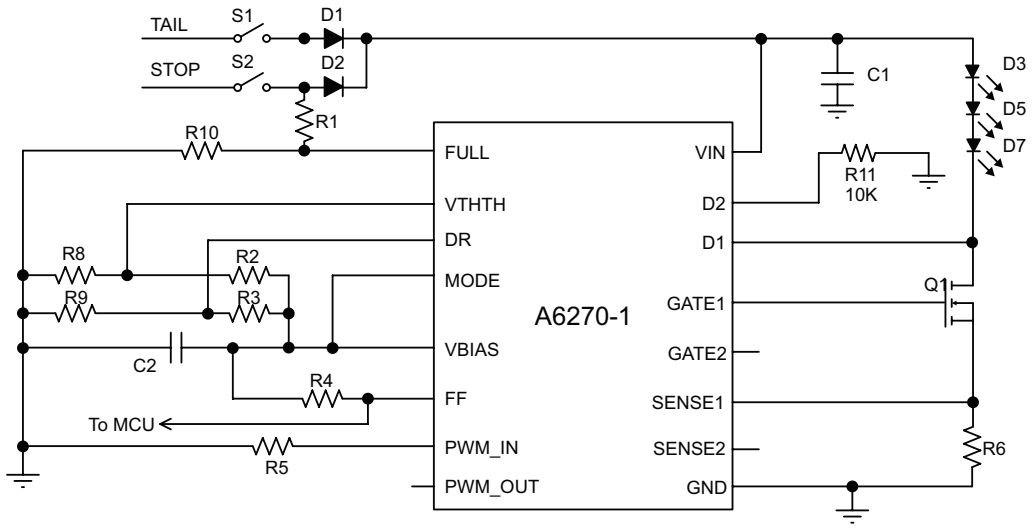
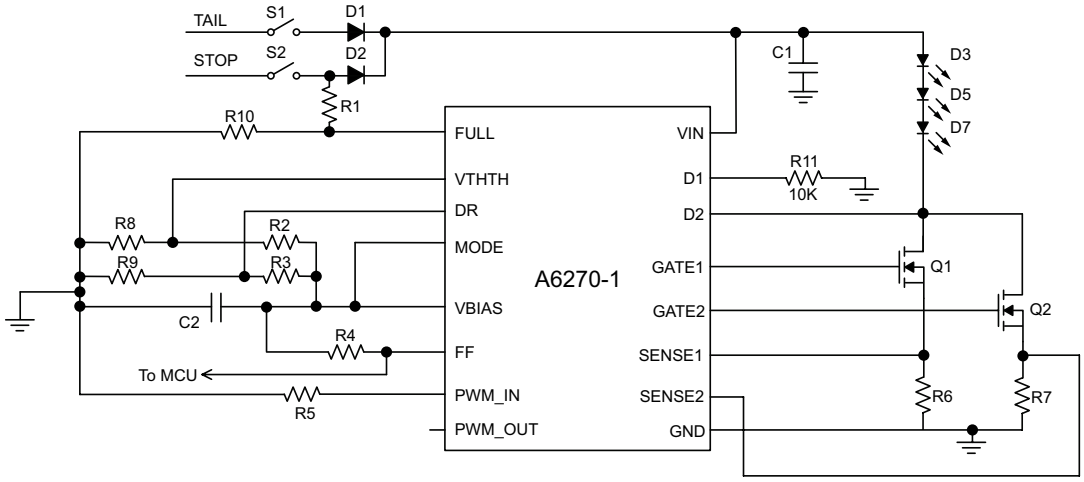


Typical Application Circuit E1: Single LED String Driven by a MOSFET (MODE = HIGH).

Connect unused Dx pin to GND through 10 kΩ resistor.

Keep unused GATEx and SENSEx pins open.



Typical Application Circuit F1: Single LED String Driven by Two MOSFETs for Higher Current Applications (MODE = HIGH).

Drains of Q1 and Q2 can be connected together for driving single high current LED string. To avoid interaction of fault sensing on D1 and D2, connect one of Dx pin to GND through 10 kΩ resistor.

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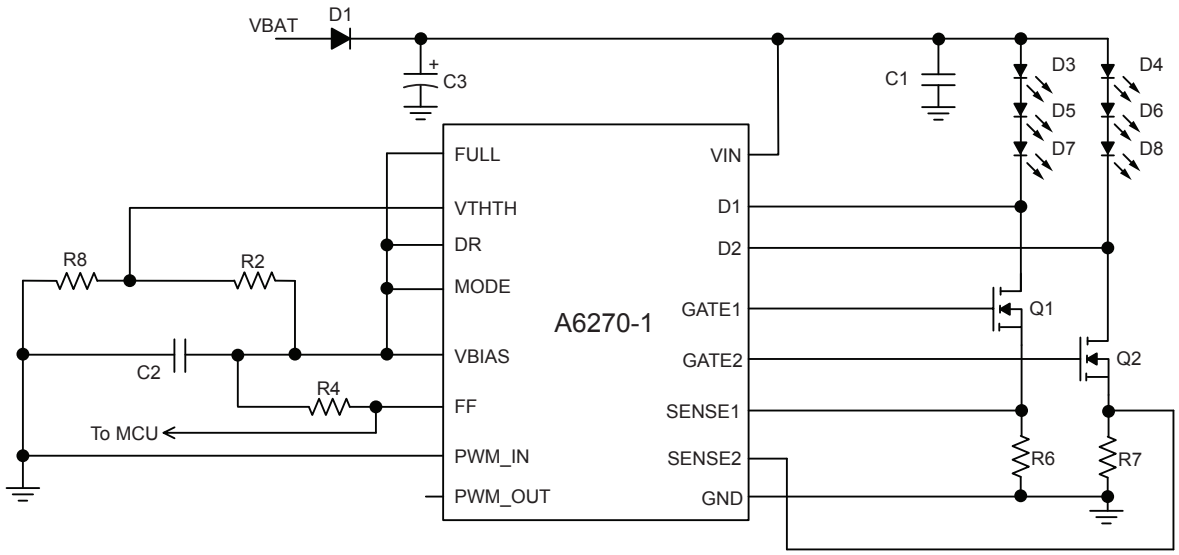

Typical Application Circuit G1: Application Circuit for driving LEDs always with 100% duty cycle

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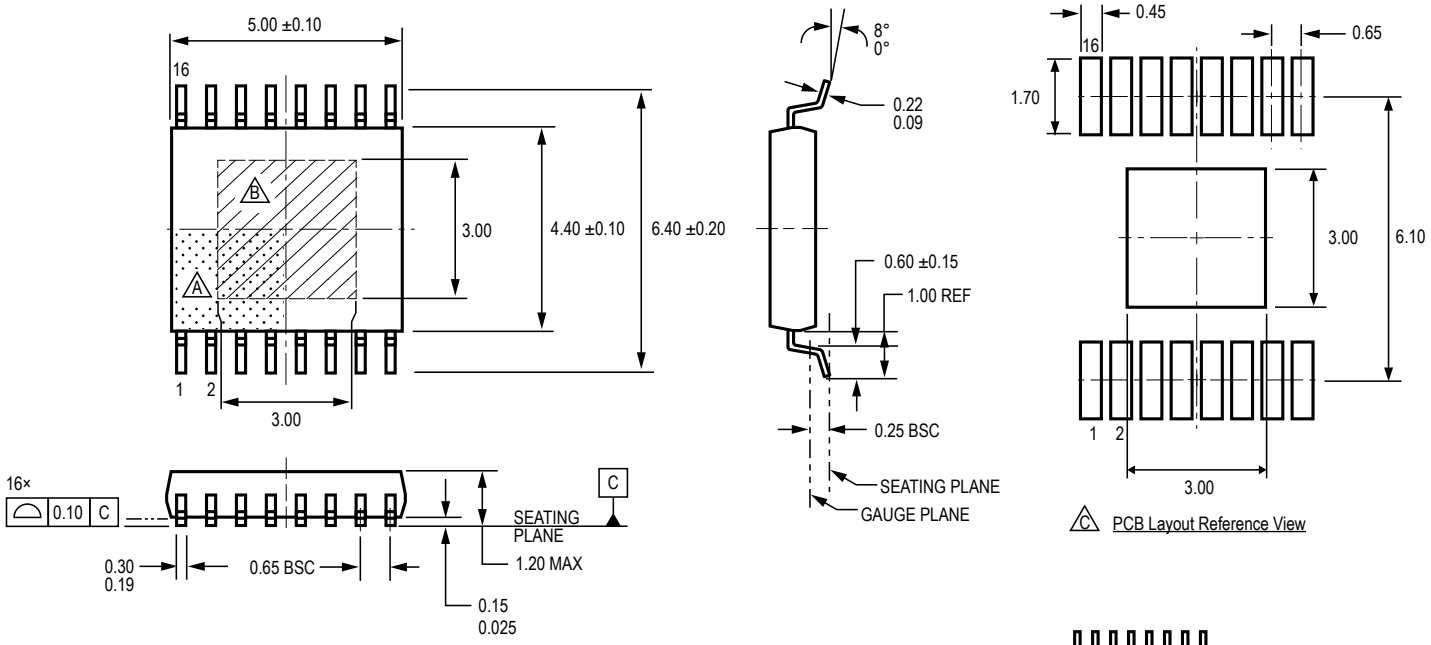
PACKAGE OUTLINE DRAWING

For Reference Only – Not for Tooling Use

(Reference JEDEC MO-153 ABT; Allegro DWG-0000379, Rev. 3)
Dimensions in millimeters – NOT TO SCALE
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown



A Terminal #1 mark area

B Exposed thermal pad (bottom surface)

C Reference land pattern layout (reference IPC7351 SOP65P640X110-17M); All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

D Branding scale and appearance at supplier discretion

D Standard Branding Reference View

Line 1, 2 = 7 characters
Line 3 = 5 characters

Line 1: Part Number
Line 2: Logo A, 4 digit Date Code
Line 3: Characters 5, 6, 7, 8 of Assembly Lot Number

Figure 17: Package LP, 16-Pin TSSOP with Exposed Thermal Pad

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Revision History

Number	Date	Description
–	September 24, 2015	Initial Release
1	April 28, 2016	Updated Functional Description and added Simplified Fault Table
2	May 31, 2016	Updated Functional Description (page 10)
3	August 22, 2016	Updated Simplified Fault Table and Typical Application Circuit G1
4	March 12, 2019	Minor editorial updates
5	March 18, 2020	Minor editorial updates
6	March 11, 2022	Updated package drawing (page 23)

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